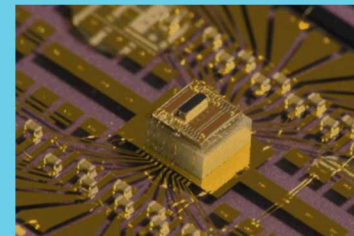
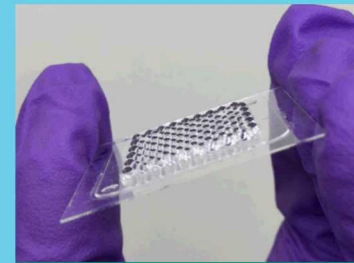
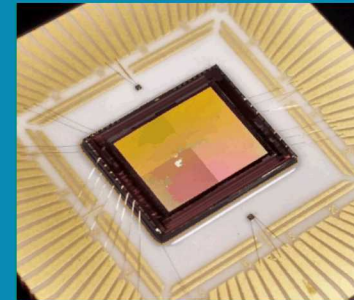


Heterogeneous Integration (HI) of III-V Semiconductors for Imaging and High-Speed Communication



ECS2019 10/15/2019

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Senior Member of Technical Staff

Sandia National Labs



This work was supported in part by the Laboratory Directed Research and Development program at Sandia National Laboratories. Sandia National Laboratories is a multitechnology laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA-0003525. This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

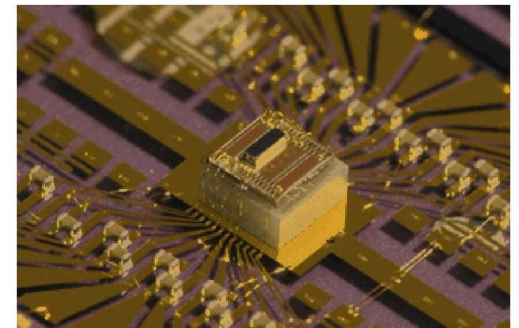
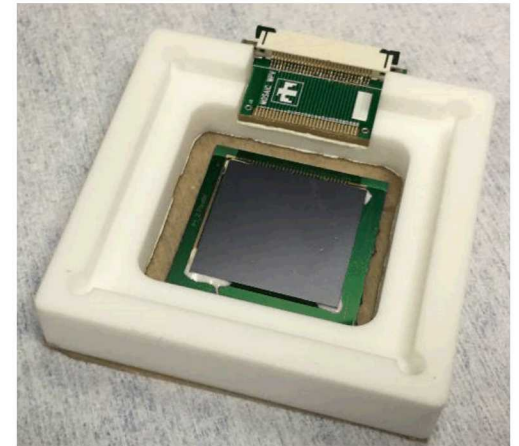
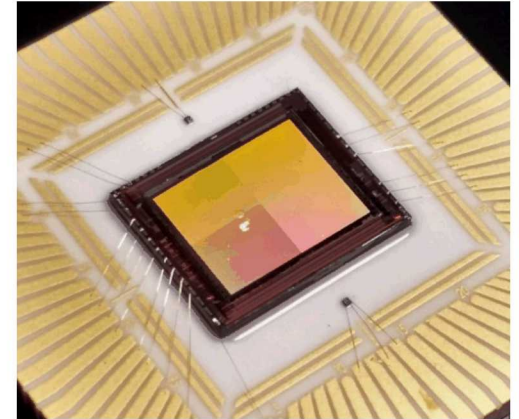
Outline

Overview of III-V HI Capabilities at Sandia

Applications of III-V HI

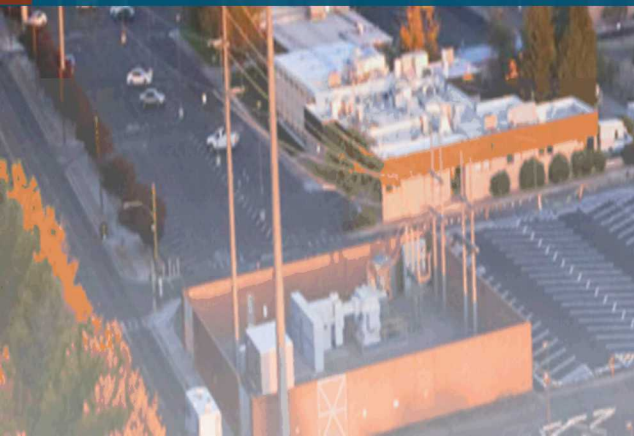
- Application 1: Focal Plane Arrays from IR to x-rays
- Application 2: Concentrating Solar Cells
- Application 3: High-Speed Communication

Conclusion





Overview of III-V HI at Sandia



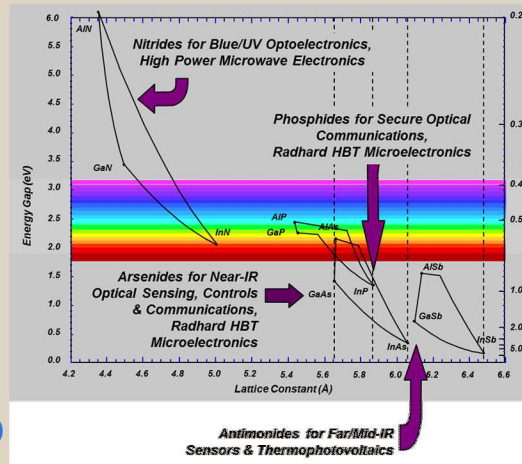
Compound Semiconductors and Heterogeneous Integration

Microfabrication

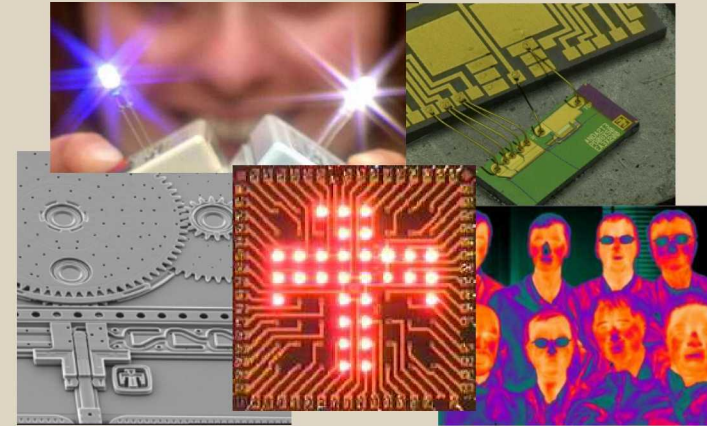


MESA SiFab: 11,900 ft² Class I
 MESA MicroFab: 14,230 ft² Class 10/100
 CINT NanoFab: 9,000 ft² Class 100

III-V semiconductor growth



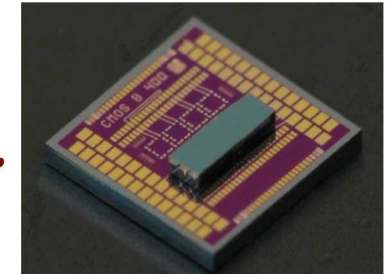
Photonics expertise



Heterogeneous integration: rationale

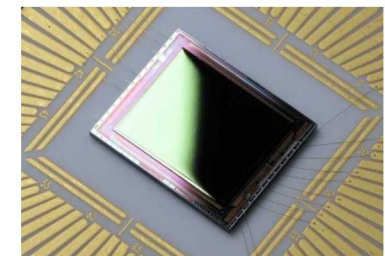
- **SWAP-C:** size, weight, and power; cost
- **performance:** combine technologies, improve interconnect
- **diverse functionality:** optical, RF, MEMS, analog, chem, bio
- **agility & turn time:** prototyping and low-volume
- **trust:** secure microsystems

low volume,
high value



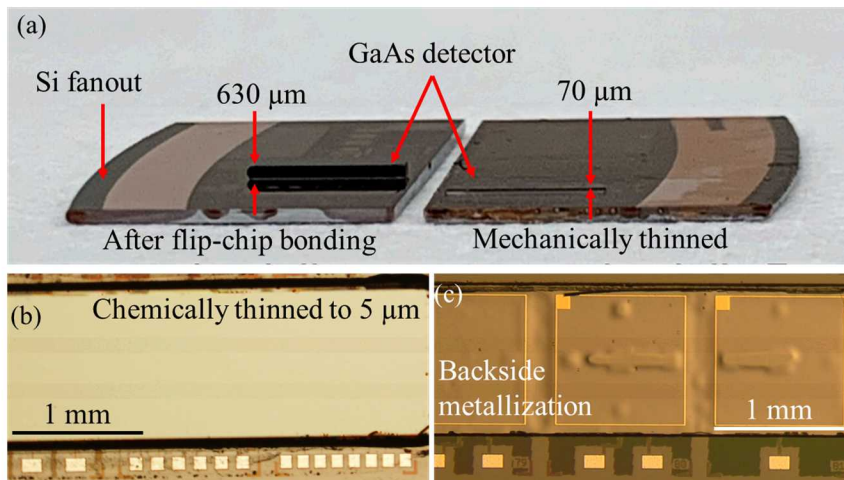
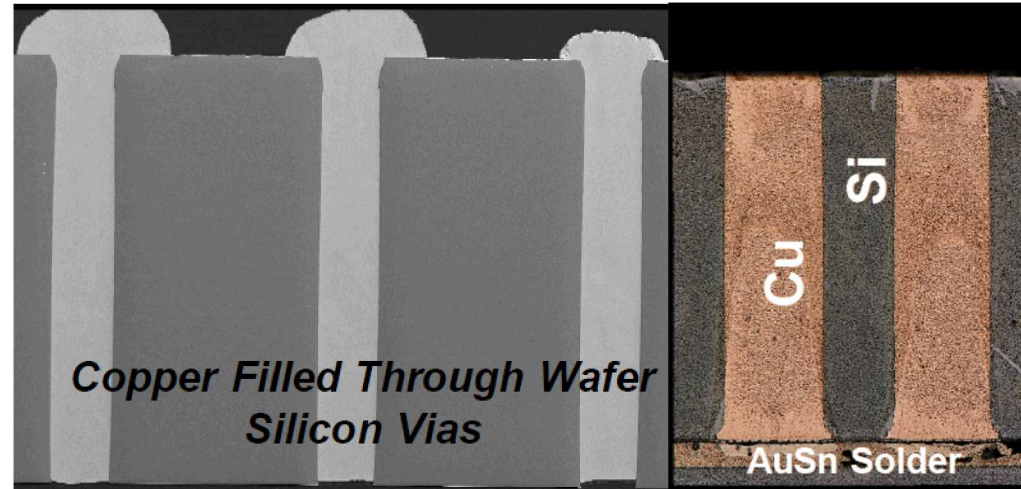
Approaches to integration

- in-package
 - die-to-die: micro bump, flip-chip, micro-optics, etc.
 - wafer-level: interconnect bonding (3D DBI)
 - wafer-level: epitaxy bonding (dielectric interfaces)
 - monolithic integration
- R&D** →
- Production** →



HI capabilities overview

- In-house back-end processing:
 - In bump deposition and reflow
 - Solder ball jetting
 - Metal plating
 - Through-substrate vias
- Integration capabilities:
 - Flip-chip bonding
 - Wafer bonding
 - Post-bond substrate removal
 - Automated dense wire bonding
 - 3D printed enclosures and supports



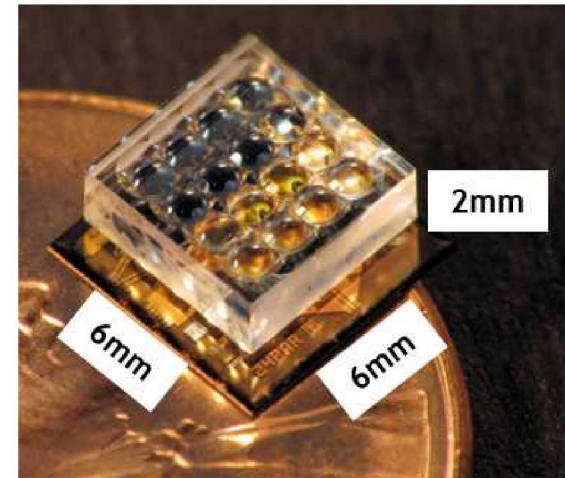
Post-bond thinning and processing



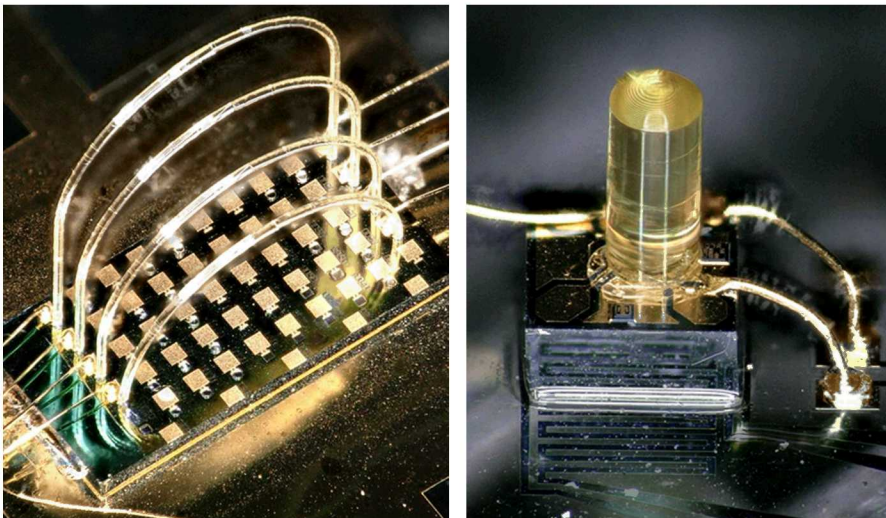
Semi-automated flip-chip bonder

HI capabilities overview

- Optical HI:
 - Diamond turning for microlenses
 - 3D printed optics
- Device testing:
 - DC and pulsed optical and x-ray sources
 - Extreme environmental and mechanical testing



Custom microlens array on
GaAs transceiver



3D printed micro-optic interconnects and lenses

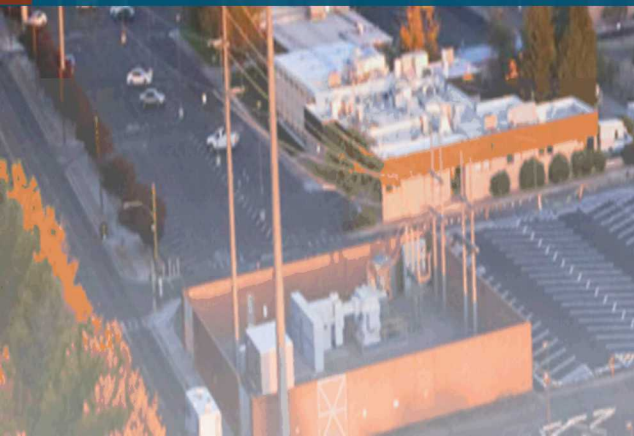


3D printed fiber holder and
collimating lens



Applications of III-V HI:

I: Focal plane arrays from IR to x-rays

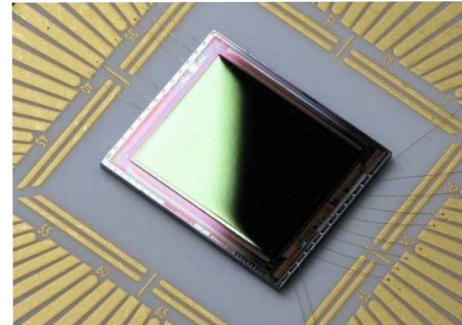


MWIR/LWIR focal plane imager

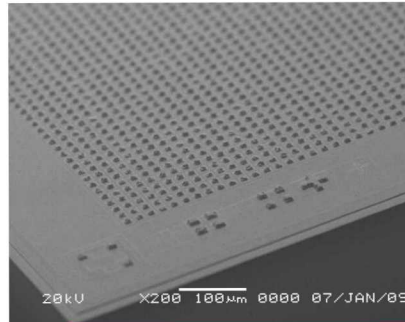
- nBn detectors for IR focal plane arrays
 - III-V detector material for IR imaging
 - Performance becoming competitive to MCT
 - Potential to scale to large arrays



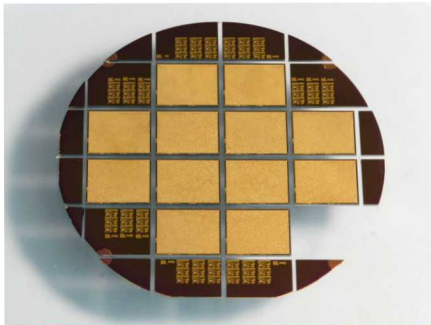
MWIR still frame,
160K



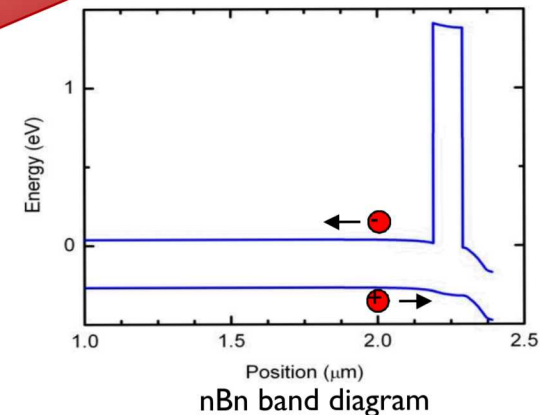
hybridized nBn FPA
prototype



nBn array with
indium bumps



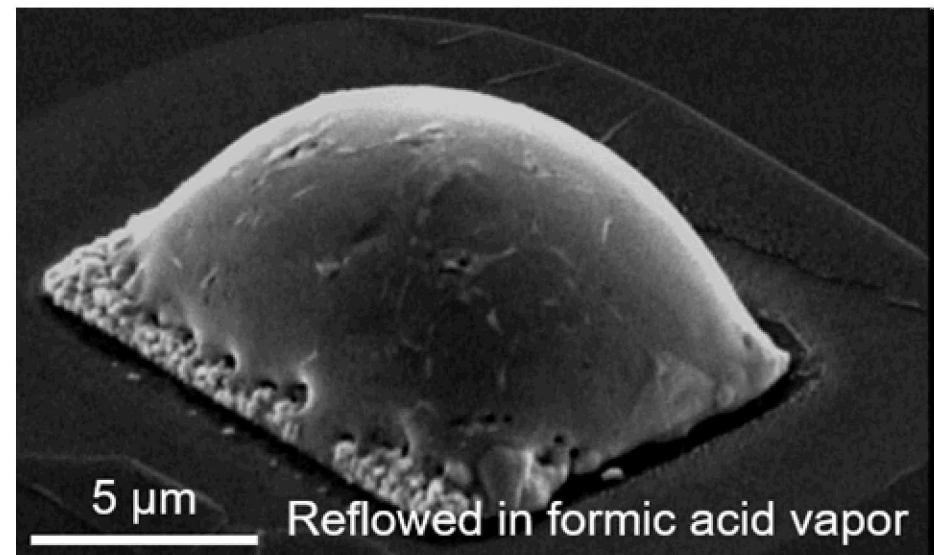
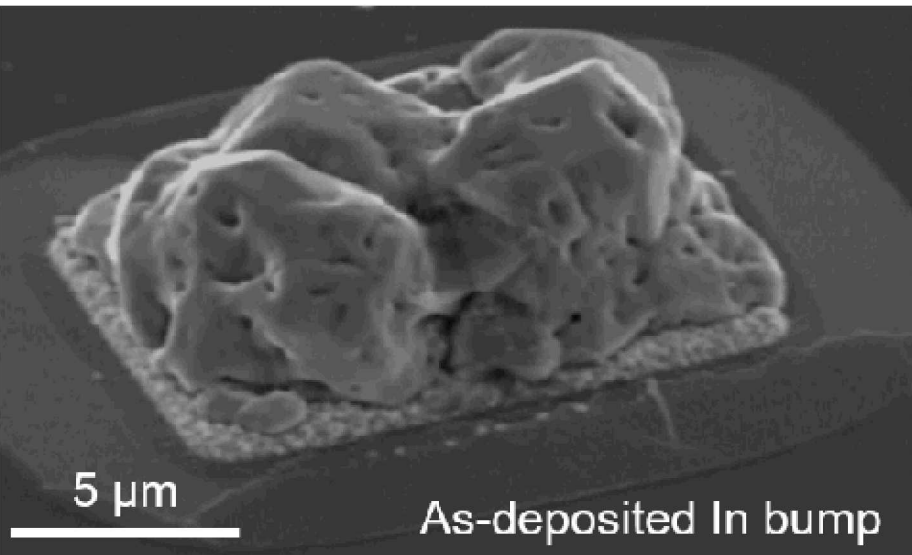
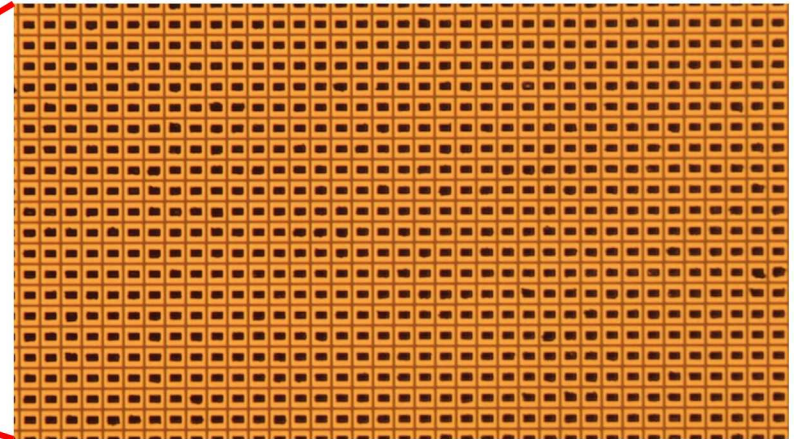
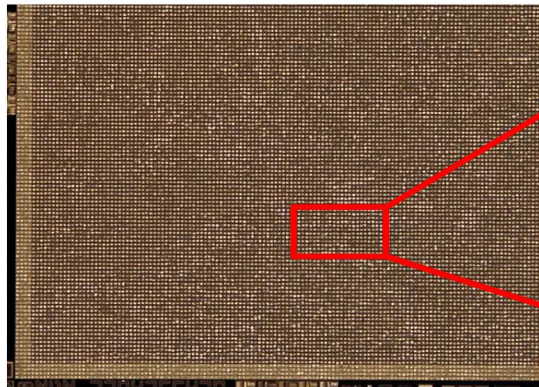
GaSb detector
epitaxy



- In-house development of nBn detector technology includes growth, fabrication, integration, and device/system testing
- Requires hybridization of large (≤ 1 MP) GaSb detectors to CMOS ROICs

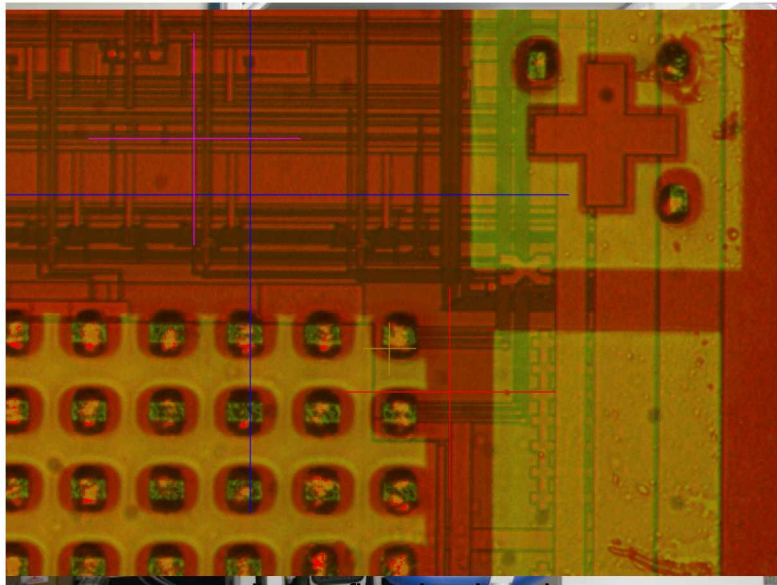
Focal plane array integration

- ROIC hybridization after back-end fabrication & detector testing
 - solder dam, underbump metallization
 - indium solder bumps (electroplating or evaporation)
 - singulation
 - flip-chip bonding with in-situ reflow



Focal plane array integration

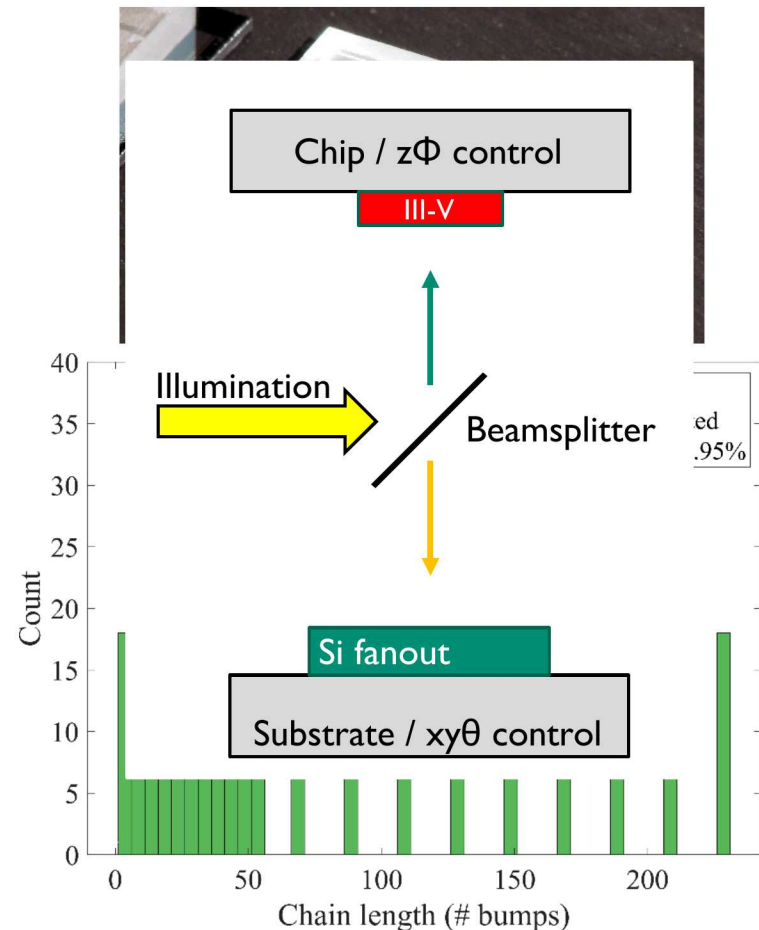
- ROIC hybridization after back-end fabrication & detector testing
 - solder dam, underbump metallization
 - indium solder bumps (electroplating or evaporation)
 - singulation
 - flip-chip bonding with in-situ reflow



view during flip-chip bonding
semi-automated flip-chip bonder

Capabilities:

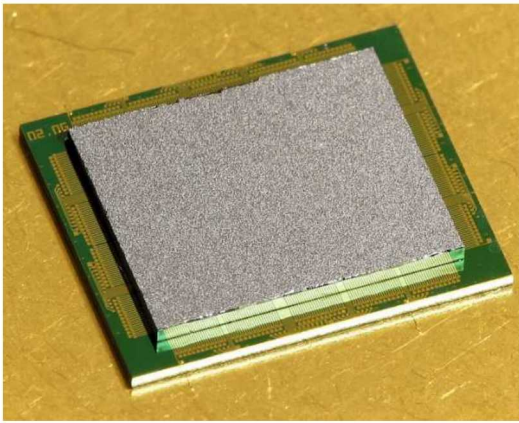
- +/- 1 micron xyz accuracy, excellent planarity
- 400x imaging, alignments at >450C
- thermocompression bonding up to 100 kg
- flip-chip, die attach, UV-curing, fiber alignment, replication
- “dry flux” vapor removes oxides to improve bonds



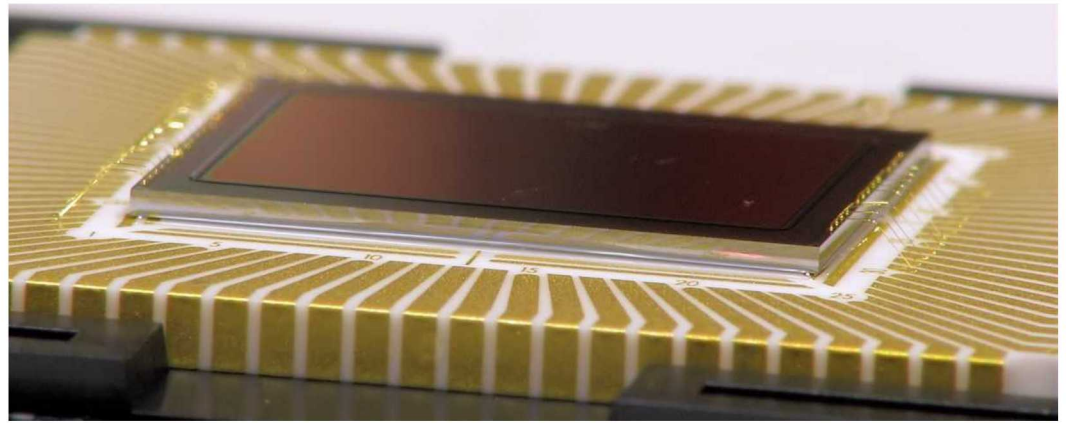
Daisy chain test vehicle showing yield >99%
Average bump-to-bump resistance: 3.35 Ω

Focal plane array integration

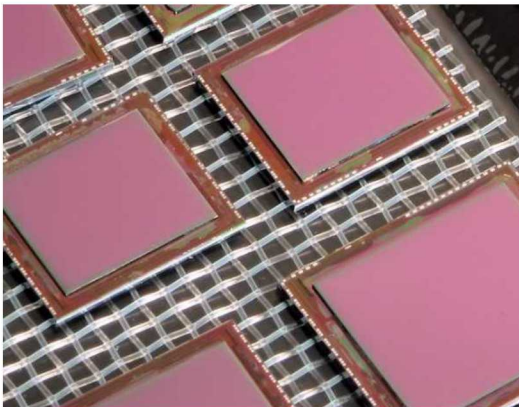
- Post flip-chip processes
 - epoxy underfill
 - backside grinding & polishing
 - precision optical coatings
 - packaging and testing



Full thickness hybridized chips



FPA packaged for cryogenic testing



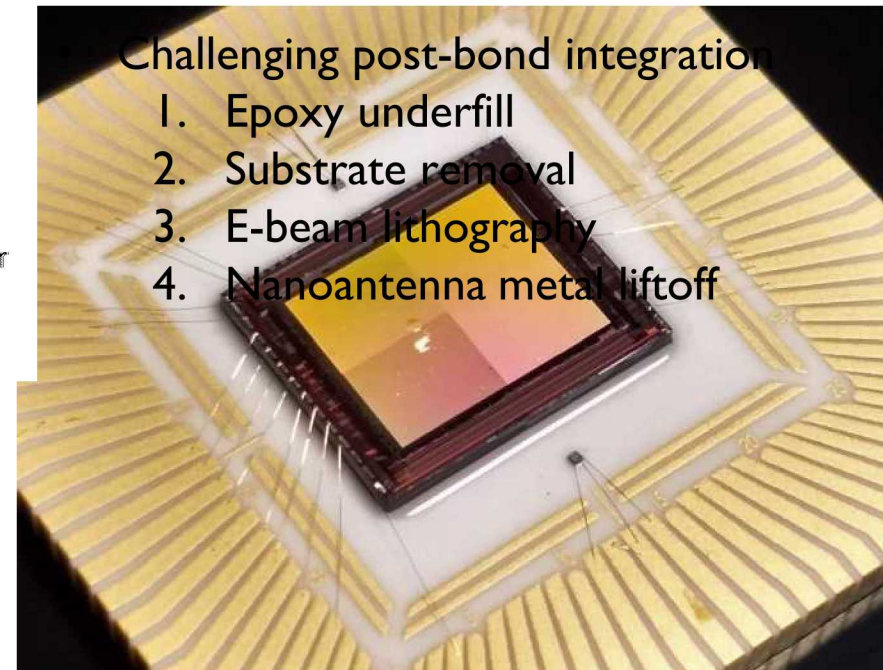
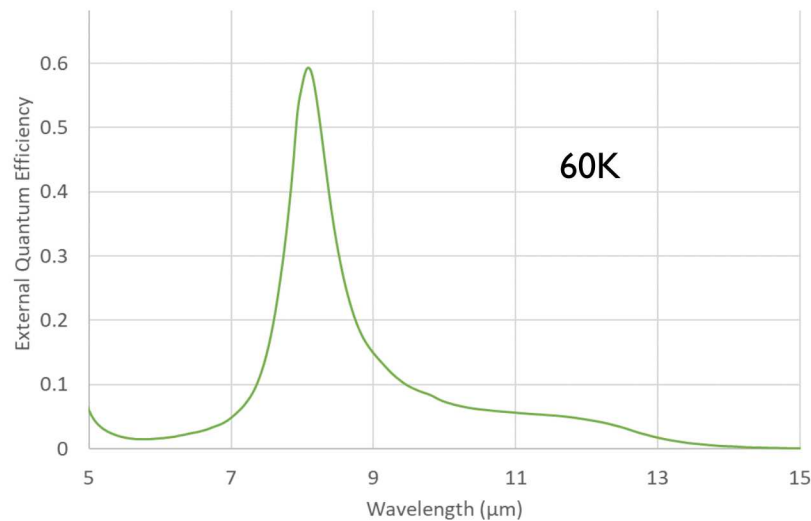
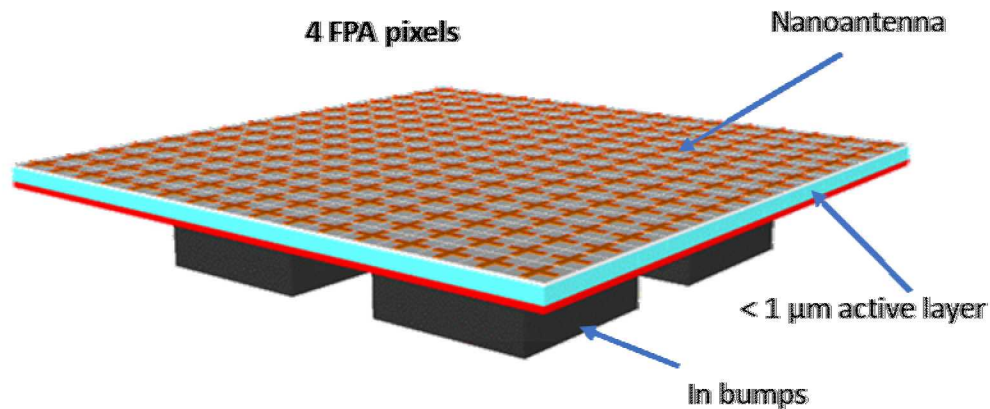
FPAs after thinning and AR coat



MWIR imaging with nBn sensor

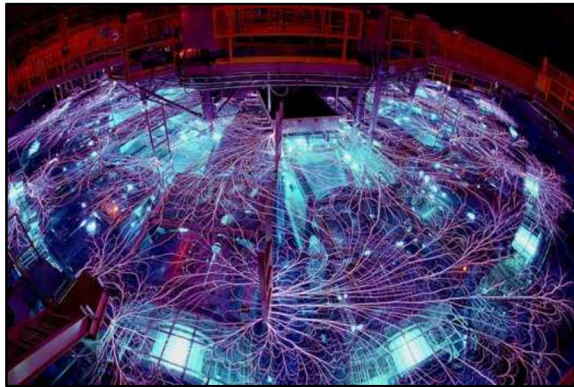
Longwave IR FPA with nanoantennas

- Resonant nanoantennas to boost quantum efficiency
 - Sub-wavelength metal antennas patterned on illumination-side after bonding and thinning
 - Resonant design allow reduced detector thickness for lower dark current while maintaining $QE > 50\%$

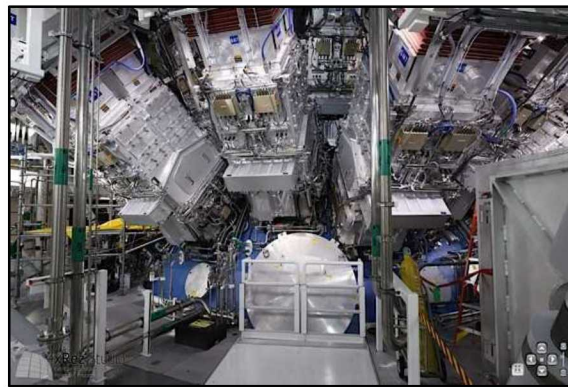


Packaged nanoantenna enabled FPA
Each quadrant has a different nanoantenna design for peak performance at different wavelengths

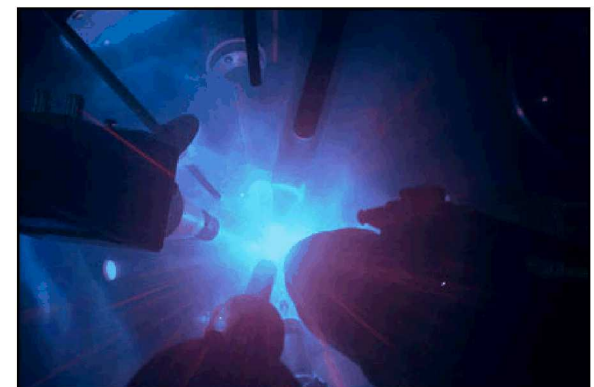
Ultrafast x-ray imager (UXI) program



Z-Machine

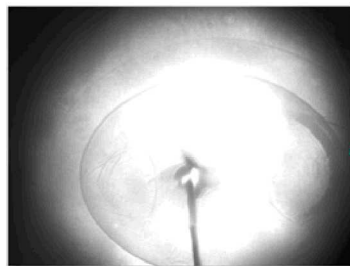


National Ignition Facility



Omega

- 2D, nanosecond gated imaging diagnostic for inertial confinement fusion research
 - Fast frame-rate reduces motion blur and provide temporal information
 - Cameras fielded in fusion facilities around the US
 - Current cameras use Si detectors; improved sensitivity possible with III-V detectors



Integrated image



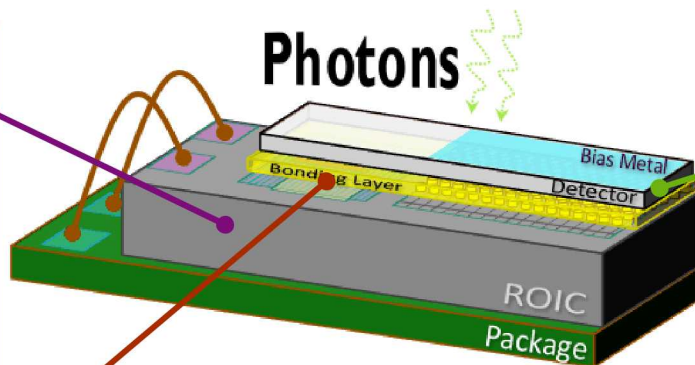
Gated image show
nanosecond evolution
of ICF physics

Ultrafast x-ray imager (UXI) program

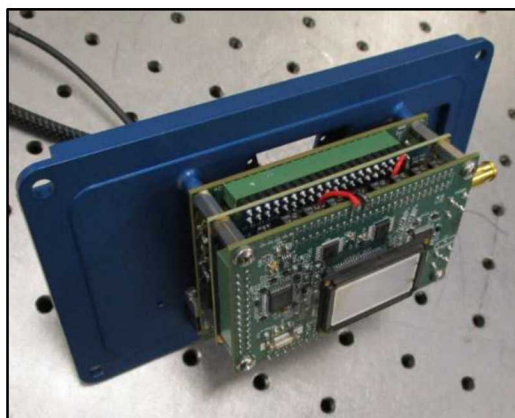
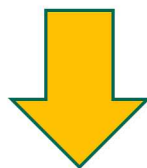
Readout Integrated Circuit (ROIC)



- Fabricated in SNL's 6" 350nm CMOS
- 1-2ns min shutter, 2-8 frames
- 1024x512 array of 25 μ m x 25 μ m pixels
- Adjustable shutter timing

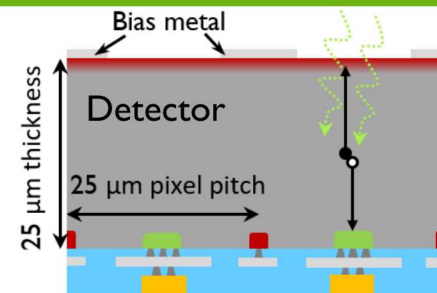


Hybrid CMOS Sensor



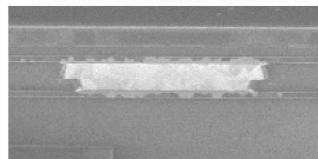
UXI Camera System Development for Application-Specific Needs

Detector Array



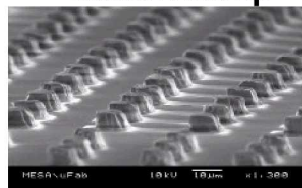
Integration

Direct Bond Interconnect (DBI)

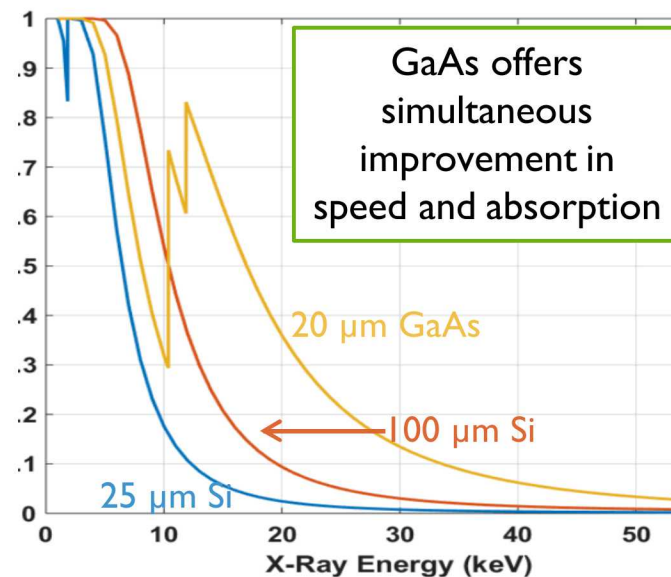


- Wafer-to-wafer bond

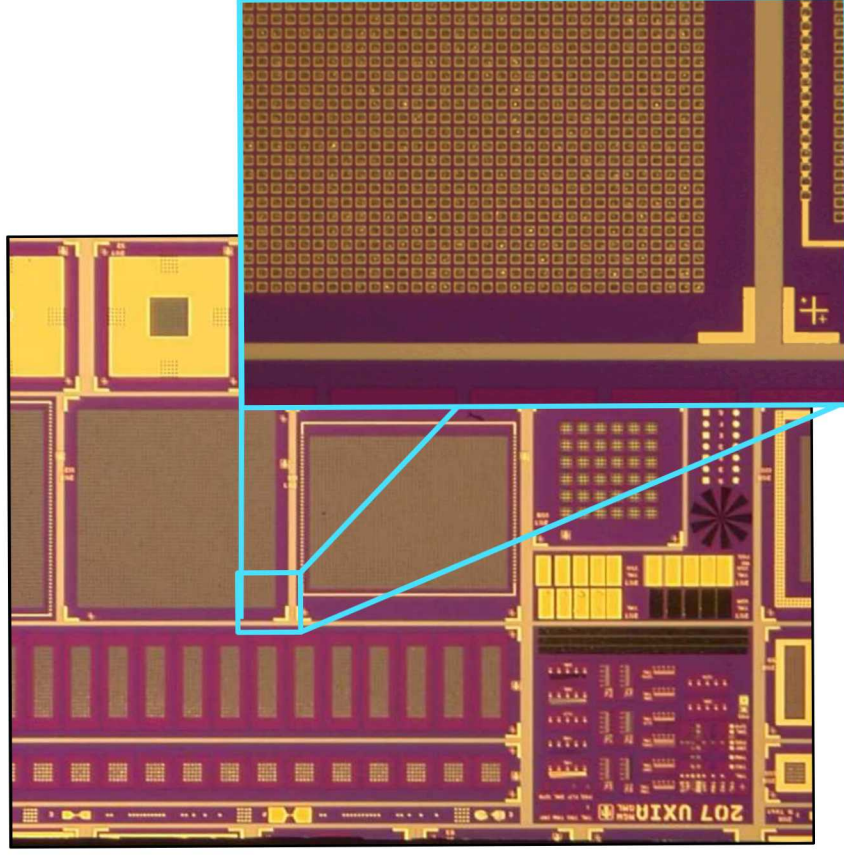
Indium bump



- Die level processing

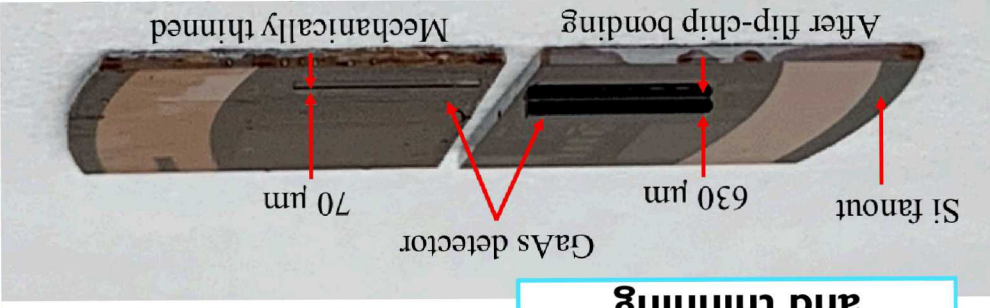
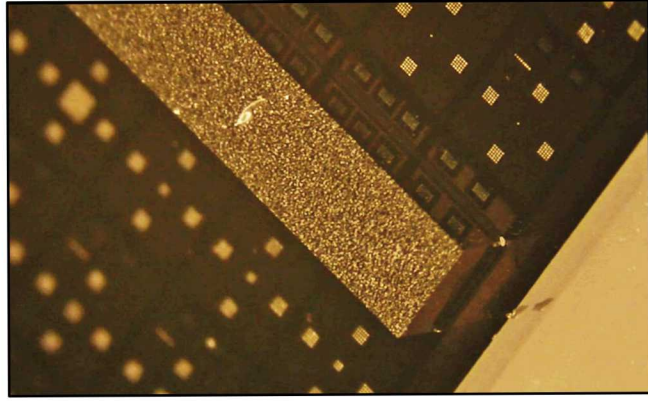
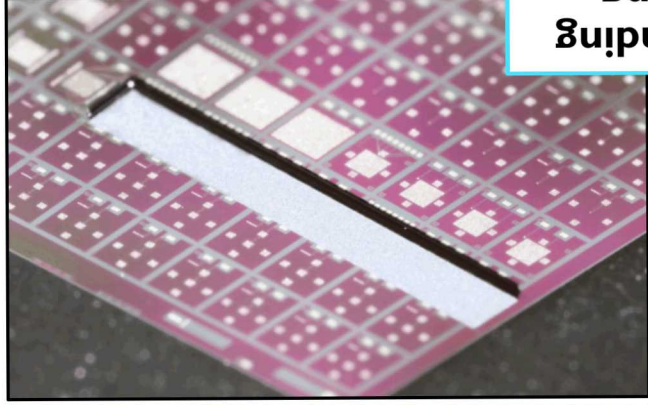


- Recent work on H1 of pixelated GaAs arrays for UXI
- Adopt techniques from IR FPAs to a new application
- First bonded test arrays complete
- 0.5 Mpix Icarus/Daedalus arrays available next year



GaAs test arrays with 25 μm pixel pitch

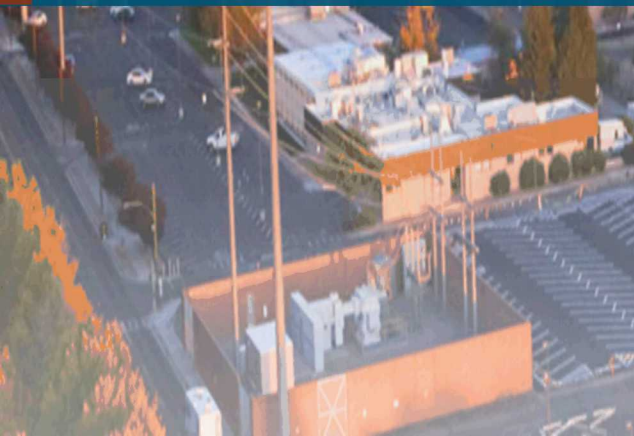
Flip-chip bonding and thinning



Q. Looker, et al. IFSA (2019).

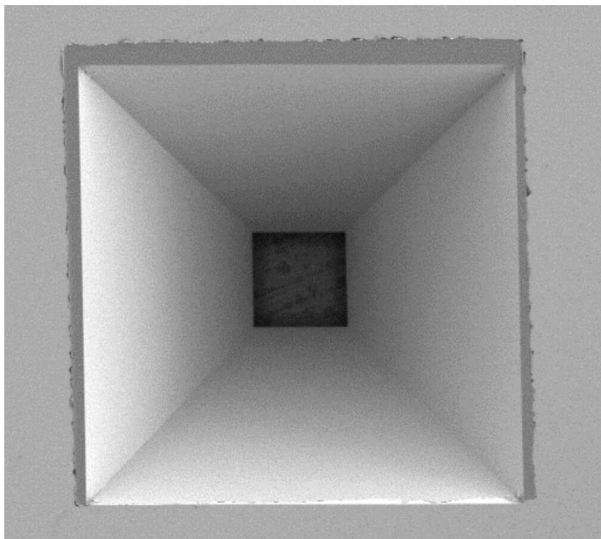
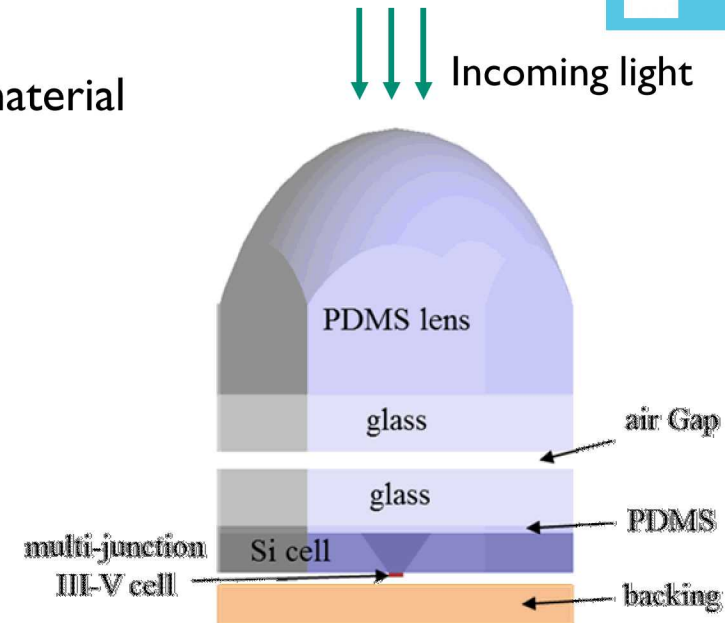


Applications of III-V HI: 2: Concentrating solar cells

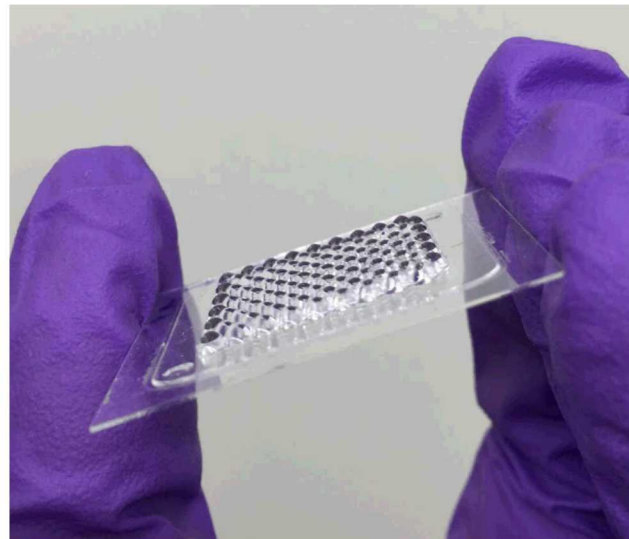


Concentrating microphotovoltaics for reduced cost solar

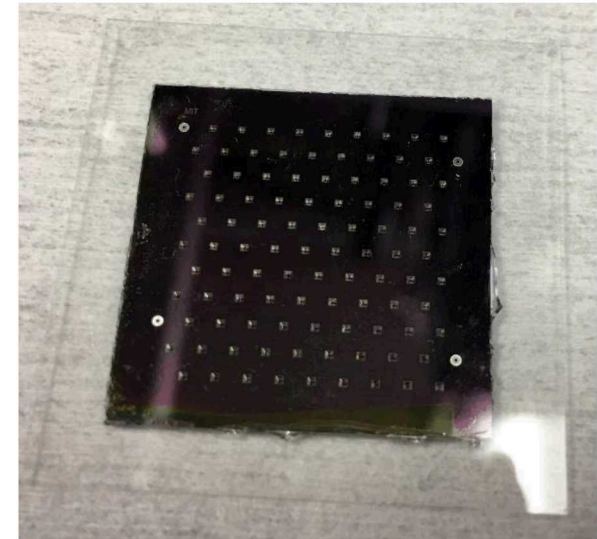
- HI used to maximize usage of high-cost III-V epitaxial material
 - Molded lenses and microfabricated reflector focus incoming light onto high efficiency III-V solar cell
 - III-V active area 100x smaller than cell area
 - Diffuse light absorbed in Si substrate for improved capture efficiency
 - Collaborative effort between MIT and Sandia



KOH-etched Si reflector groove



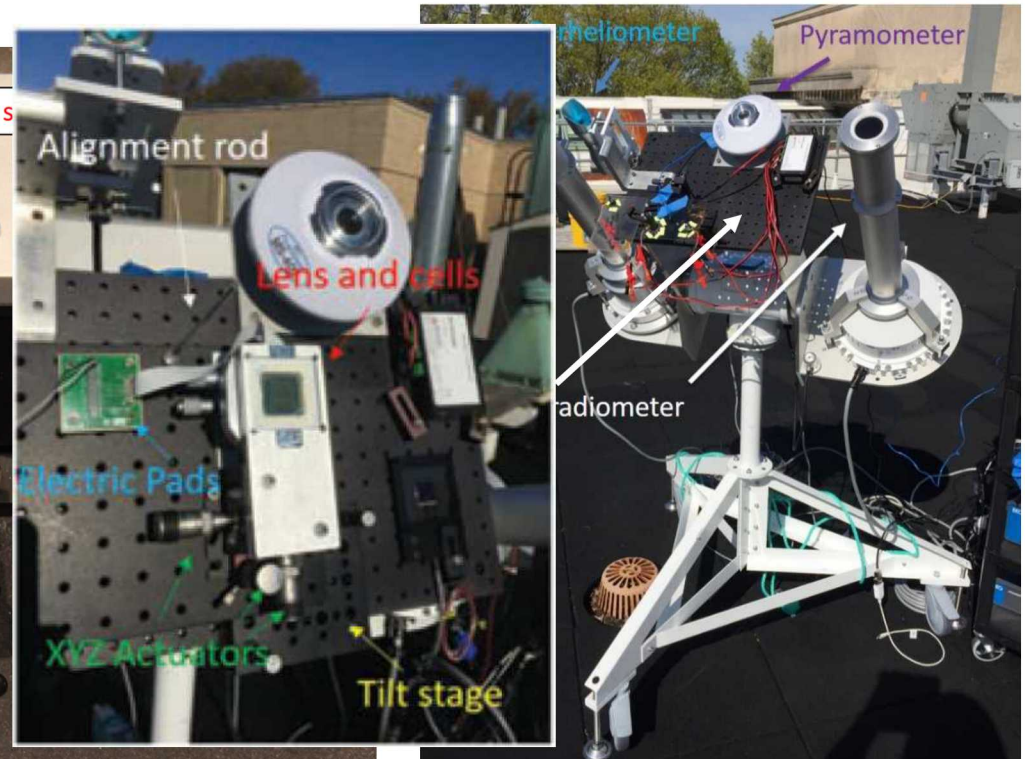
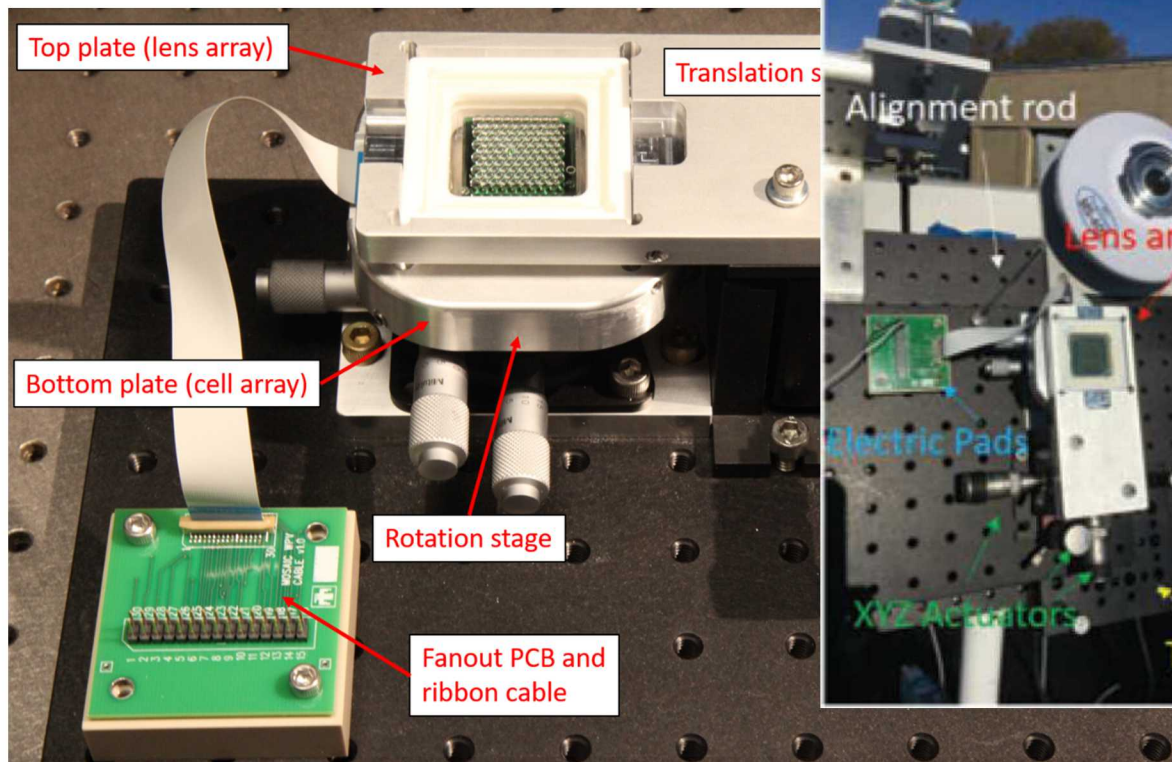
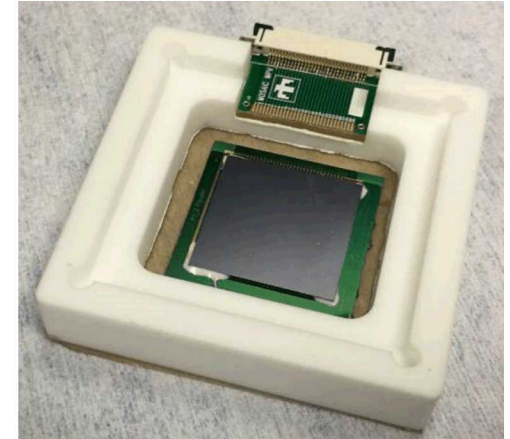
Molded PDMS lens array



III-V cell array flip-chip bonded to Si fanout and coverglass

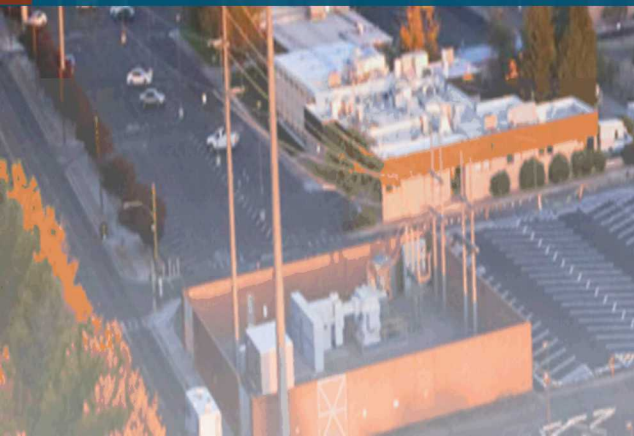
Concentrating microphotovoltaics for reduced cost solar

- Packaging and testing
 - Custom Macor frames machined to hold III-V/Si cell assembly and lens arrays
 - As proof-of-concept, manual alignment of lens array used to demonstrate concentration of incident light ($\sim 30\times$)
 - Assembly tested on calibrated solar measurement system at MIT



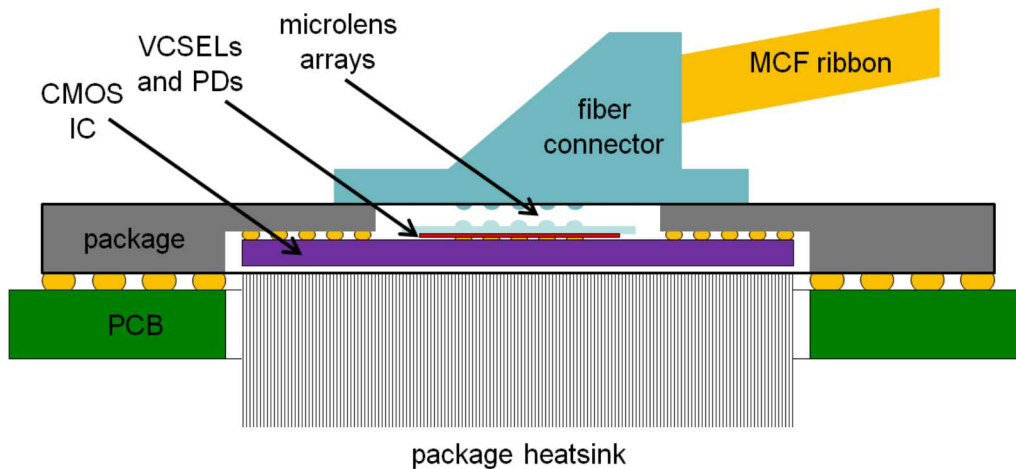


Applications of III-V HI: 3: High-speed communication

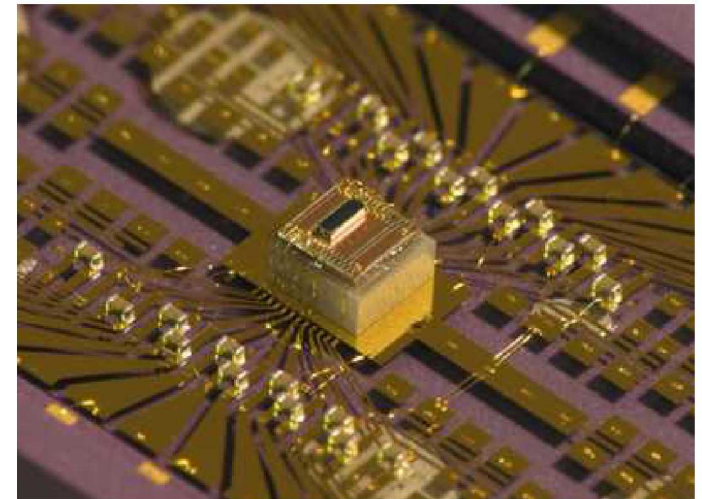


High-density photonic interconnects: overview

- Dense integration of photonics and CMOS for advanced interconnect technologies
 - III-V vertical-cavity surface-emitting lasers (VCSEL) and photodiodes (PDs) for high-speed optics and Si CMOS for low-power computing
 - Hybrid integration for very high density and low electrical parasitics
 - Targets low energy (pJ/bit) and high density (Tbps/mm²) into a multi-core fiber (MCF)
- Development of circuits, photonics, optics and integration techniques
 - Transmit/receive circuits in 32-nm and 45-nm CMOS
 - Combines VCSEL and photodiode arrays, micro-optics, custom fiber



Multichannel interconnect concept

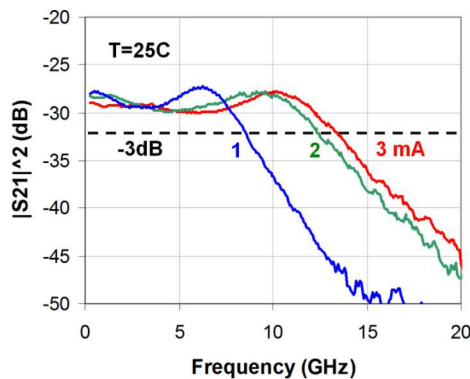
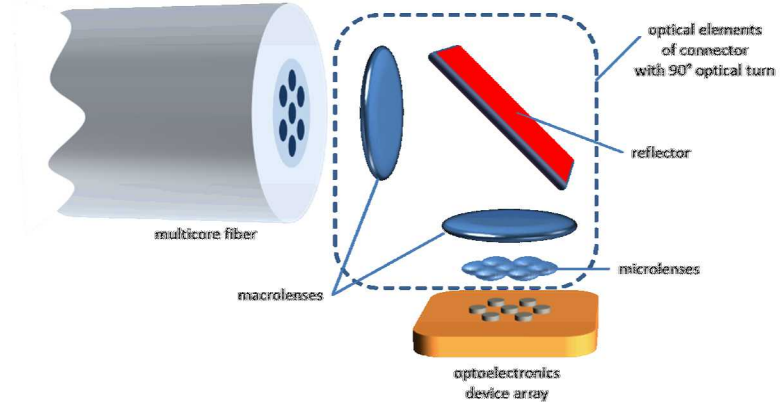
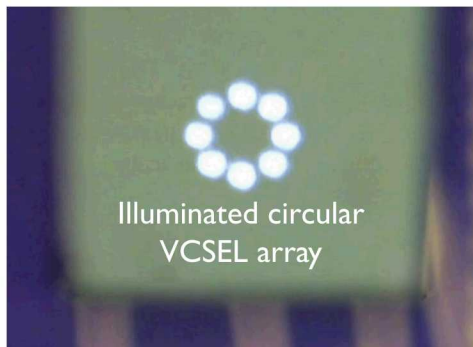


Packaged CMOS/VCSEL assembly

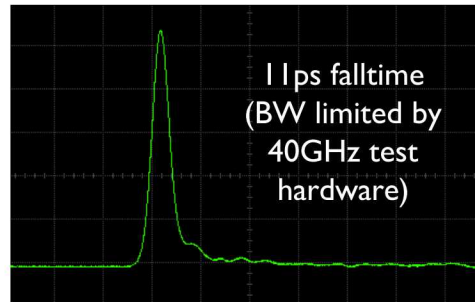
High-density photonic interconnects: components and HI

21

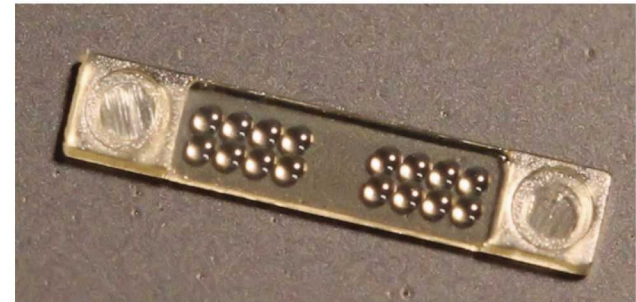
- Development of high-density optoelectronics arrays
 - Low-power VCSELs designed for high BW at low drive current
 - Photodiodes >40Gb/s with very low capacitance through flip-chip integration
- Micro-optics designed for coupling to multicore fibers



VCSEL performance



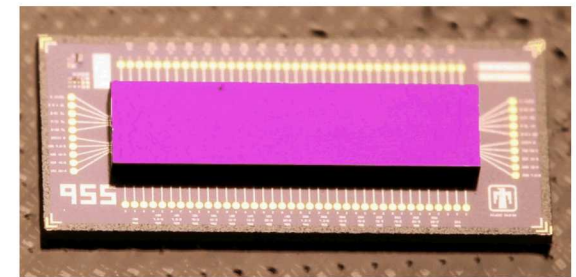
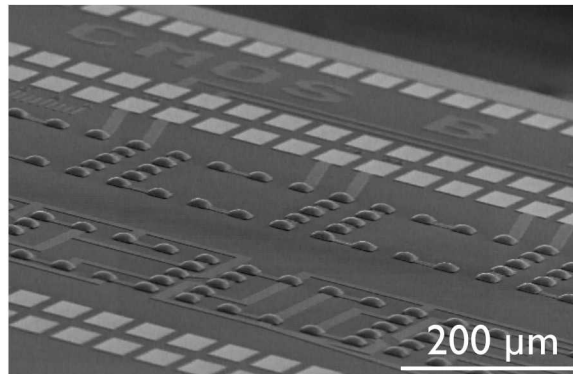
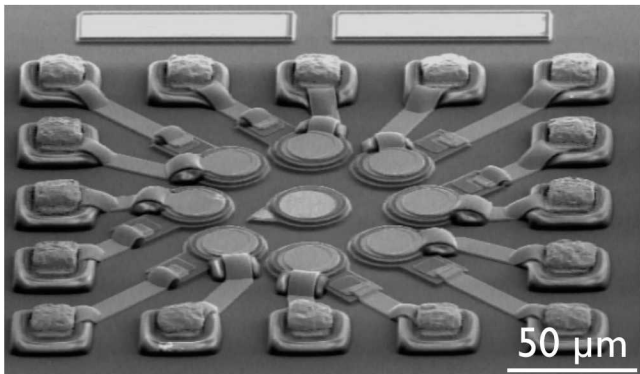
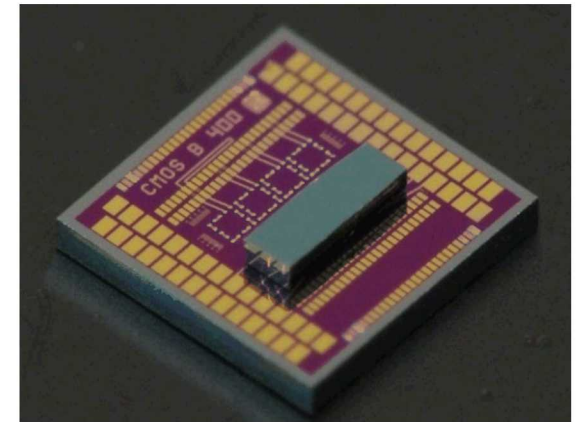
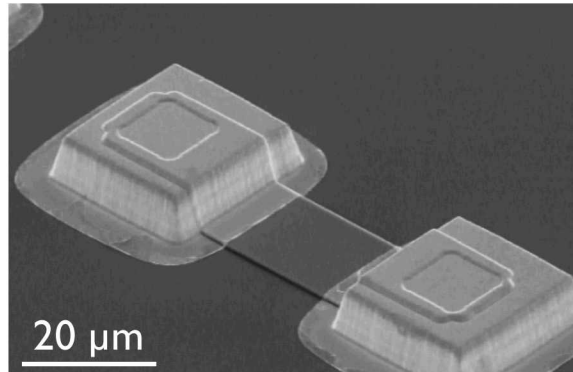
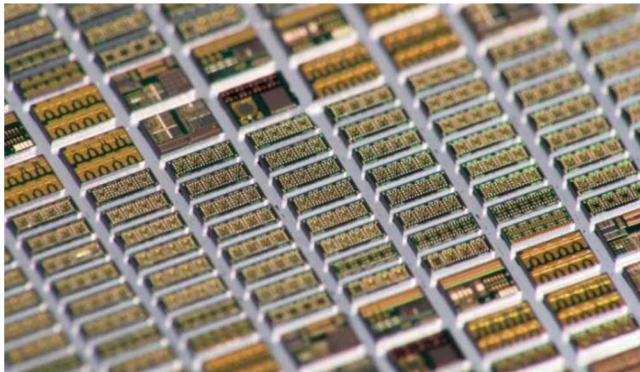
Photodiode performance



Micro-optics and multicore fibers

High-density photonic interconnects: components and HI

- III-V processes combined into photonics fabrication
 - AuSn bumps, 100 μ m substrate thinning, AR coating, scribe and break
- CMOS processed at die level: plated under-bump metal and bumps
- Flip-chip integration



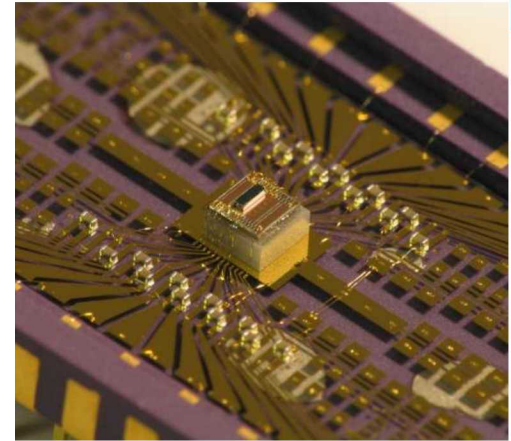
VCSEL and PD arrays
on GaAs and InP

CMOS IC prior to flip-chip
50 μ m bump pitch

CMOS IC with III-V
optoelectronics

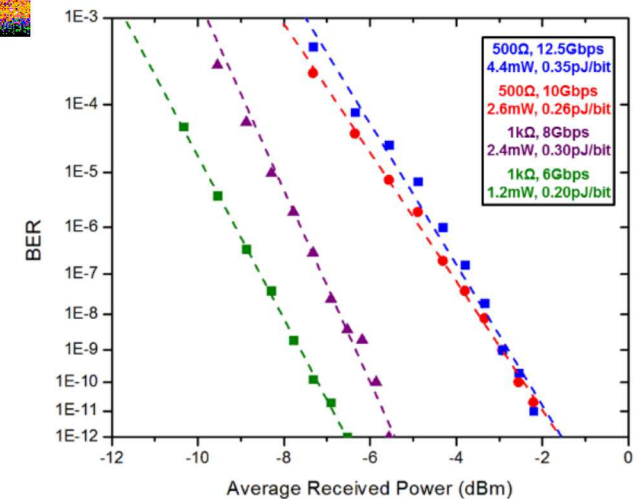
High-density photonic interconnects: testing

- Hybridized parts packaged for high-speed opto-electronic testing
 - DC wirebonding, RF probing
 - Active fiber alignment
- Single channel links demonstrated using 45-nm CMOS: 10+ Gbps at 1.7 pJ/bit

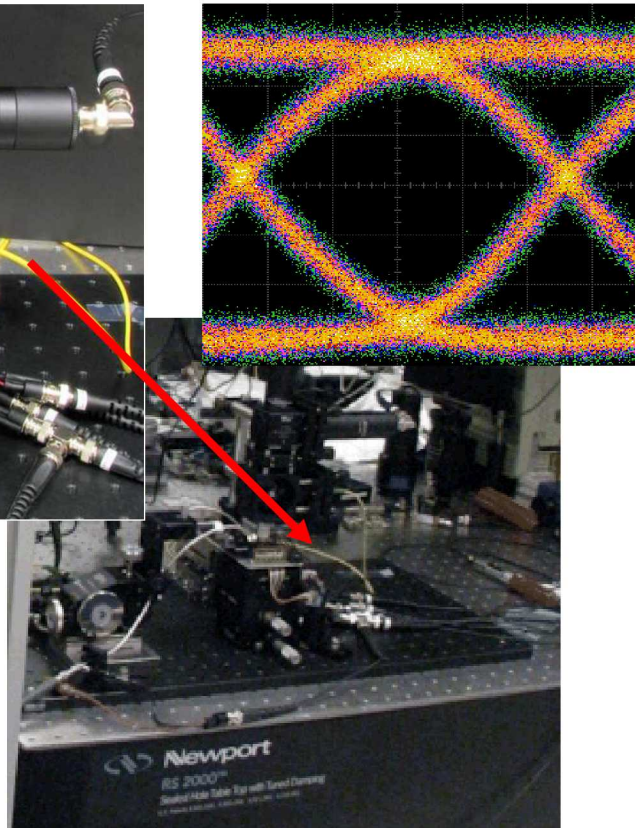
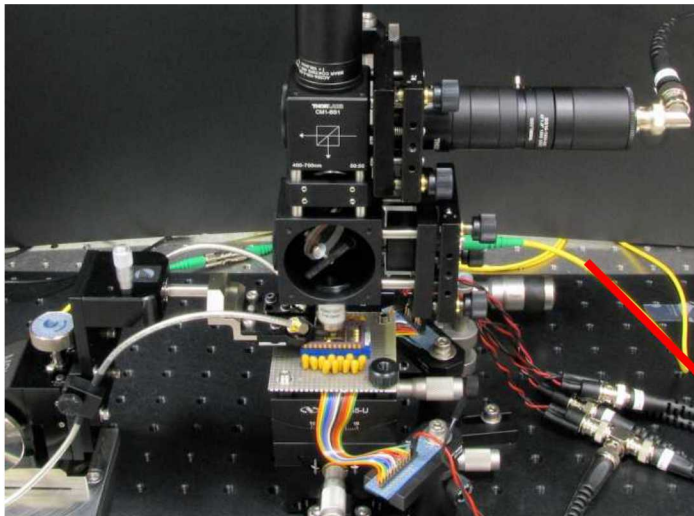


Packaged CMOS/III-V photonics

System link testing

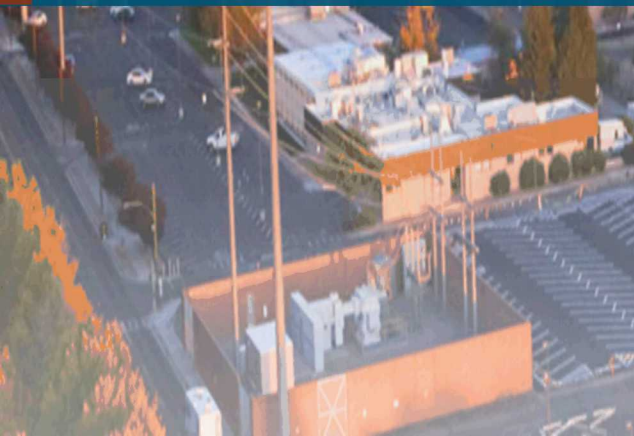


Lab-to-lab link demonstration





Conclusion



Conclusion

- Heterogeneous integration of compound semiconductors with silicon electronics enables new devices, improved performance, and compact form factors

Heterogeneous integration: rationale

- **SWAP-C:** size, weight, and power; cost
- **performance:** combine technologies, improve interconnect
- **diverse functionality:** optical, RF, MEMS, analog, chem, bio
- **agility & turn time:** prototyping and low-volume
- **trust:** secure microsystems

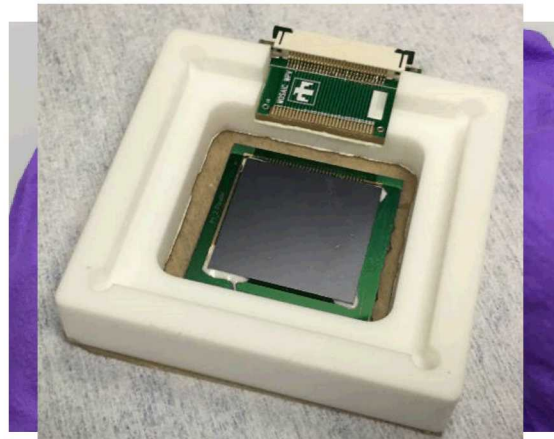
low volume,
high value

Approaches to integration

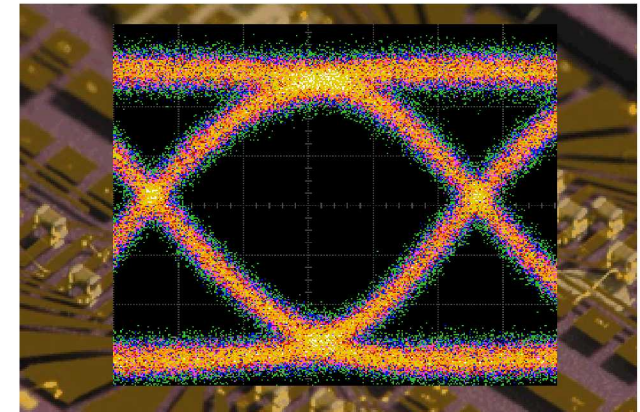
- R&D** → – die-to-die: micro bump, flip-chip, micro-optics, etc.
- Production** → – wafer-level: interconnect bonding (3D DBI)



Focal Plane Arrays
from IR to x-rays



Concentrating Solar Cells



High-Speed Communication

Acknowledgements

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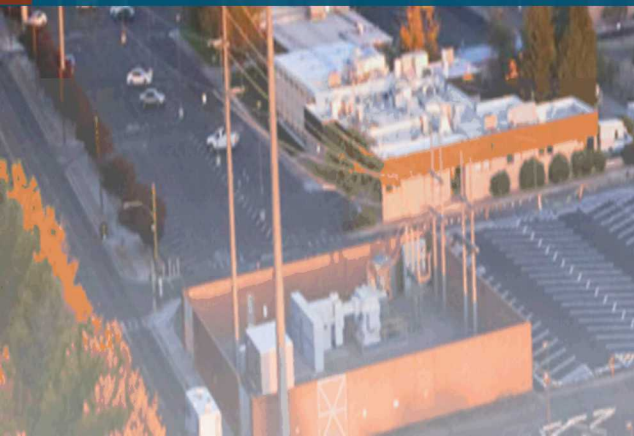
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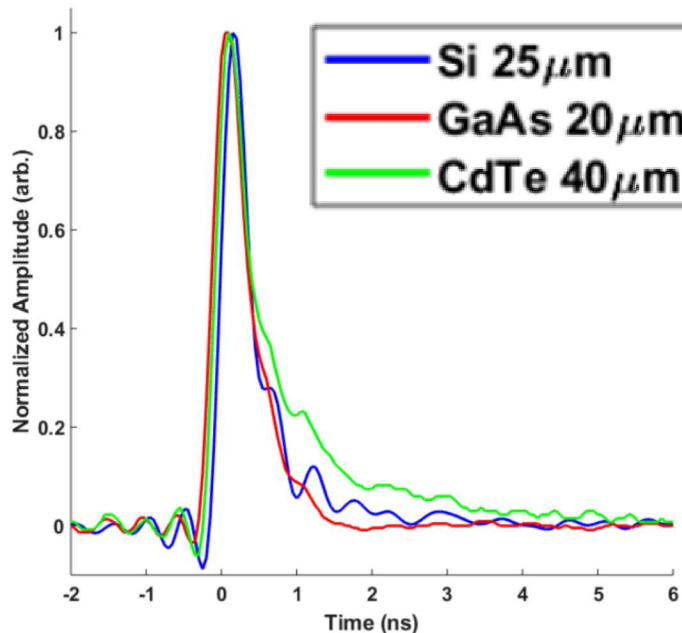
Backup slides



Other x-ray detector materials

Periodic table showing elements grouped by color. Elements highlighted in red boxes include Si (Group 14, Period 3), Ga (Group 13, Period 4), As (Group 15, Period 4), Cd (Group 12, Period 5), Te (Group 16, Period 5), and I (Group 17, Period 5). Arrows point from these elements to the table on the right.

Material Investigated	Notes
Si	Mature fabrication, low Z
GaAs	Demonstrated fast detectors
CdTe	Demonstrated fast detectors
CZT	Cannot obtain small detectors
GaN	Background doping too high
AlSb	Leakage current too high



Detector pulse shapes
obtained with
Advanced Photon
Source white beam

Diamond turning and lens molding

■ PDMS optics

- eighth order aspheric curves
 - targeting >90% optical efficiency at III-V
- cast onto 300 μ m thick Schott AF32 glass

■ Aluminum mold fabrication

- optical surfaces micro-machined & diamond milled
- lenses & glass edges aligned mechanically
- trapping bubbles challenges mold filling

■ Assembled into machined Macor frame

- bottom: optic array, facing inward
- top: 3mm thick Schott BK-7 cover glass, provides protection

