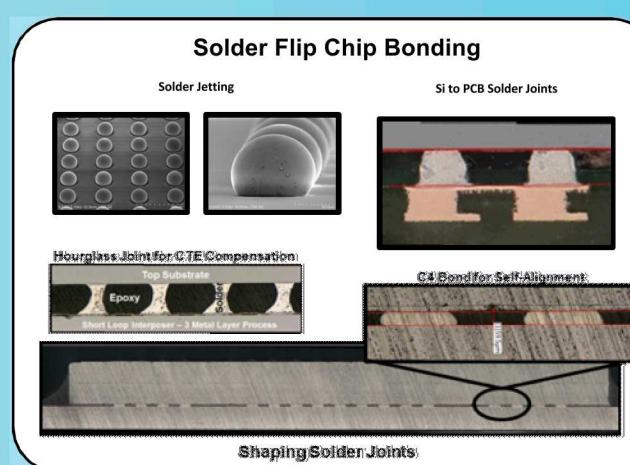
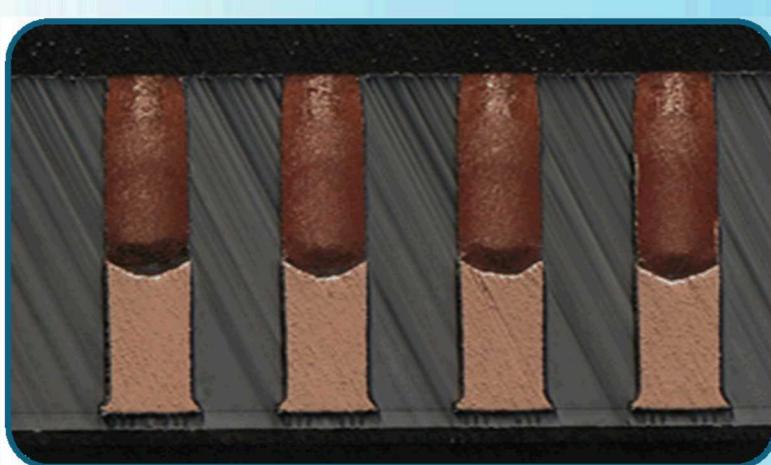




This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

SAND2019-9803C

Utilizing Electroplating for High Aspect Ratio Mesoscale Fabrication – Filling, Forming, and Coating



Andrew E. Hollowell - aehollo@sandia.gov

505 263 1095

  
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How to Apply - sandia.gov/careers

Advanced Search & Job Agent/email notification



We are hiring! Looking for entry level staff interested in microelectronics fabrication and post fab processes for 2.5D/3D integration!

NATIONAL PRIORITIES



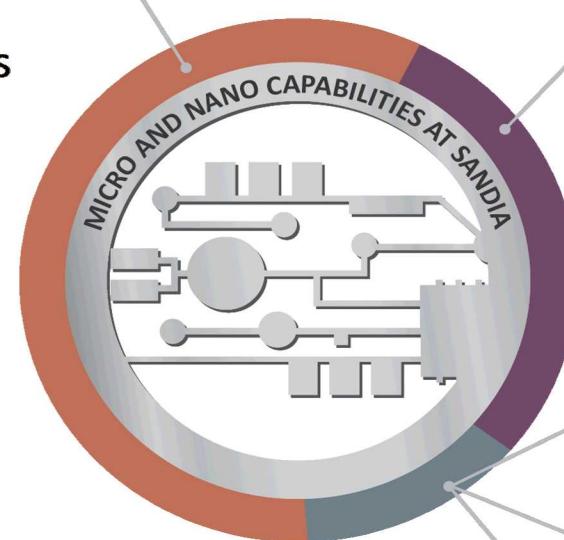
Unique Facilities Differentiate Sandia's Micro/Nano R&D



MESA

MICROSYSTEMS
ENGINEERING SCIENCES
AND APPLICATIONS

- Only source for custom strategic rad-hard microelectronics
- Largest government-owned foundry
- FFRDC with the broadest and deepest micro and nano expertise [derived R&D-product delivery work mix]



CDC

COUNTERFEIT
DETECTION CENTER



CINT

CENTER FOR INTEGRATED
NANOTECHNOLOGIES



IBL

ION BEAM LABORATORY



ACRR

ANNULAR CORE
RESEARCH REACTOR



What is MESA?



- Microsystems Engineering Sciences Applications (MESA) is a \$462M FFRDC-based development and production facility for any microsystem component or technology that cannot or should not be obtained commercially.
- MESA Develops and Delivers:
 - Strategic radiation-hardened custom integrated circuits (ICs)
 - Digital/Analog/Mixed-Signal/RF ICs
 - Trusted Products and Designs
 - 5-Level MEMS
 - III-V Compound Semiconductors
 - Optoelectronic/Photonic Devices
 - High-speed/RF Electronics
 - Heterogeneous Integration
 - Failure Analysis/Reliability Physics
 - Advanced Packaging
 - Specialized Sensors



MESA bridges science to systems, providing an environment where multidisciplinary teams create ***microsystems-enabled*** solutions to our nation's most challenging problems.

Sandia's MESA Fabs

Silicon Fab

- Over 13,000 ft² of Class 1 Clean Room
- Rad Hard CMOS Microelectronics
- MEMS
- Si Photonics, Optical Waveguides
- Ion Traps



Micro-Fab

- 15,000 ft² of Class 10/100 Clean Room
- Compound Semiconductors
- Vertical Cavity Lasers, Modulators
- RF Electronics & Photonics
- Post Silicon Wafer Processing
- 3D Integration



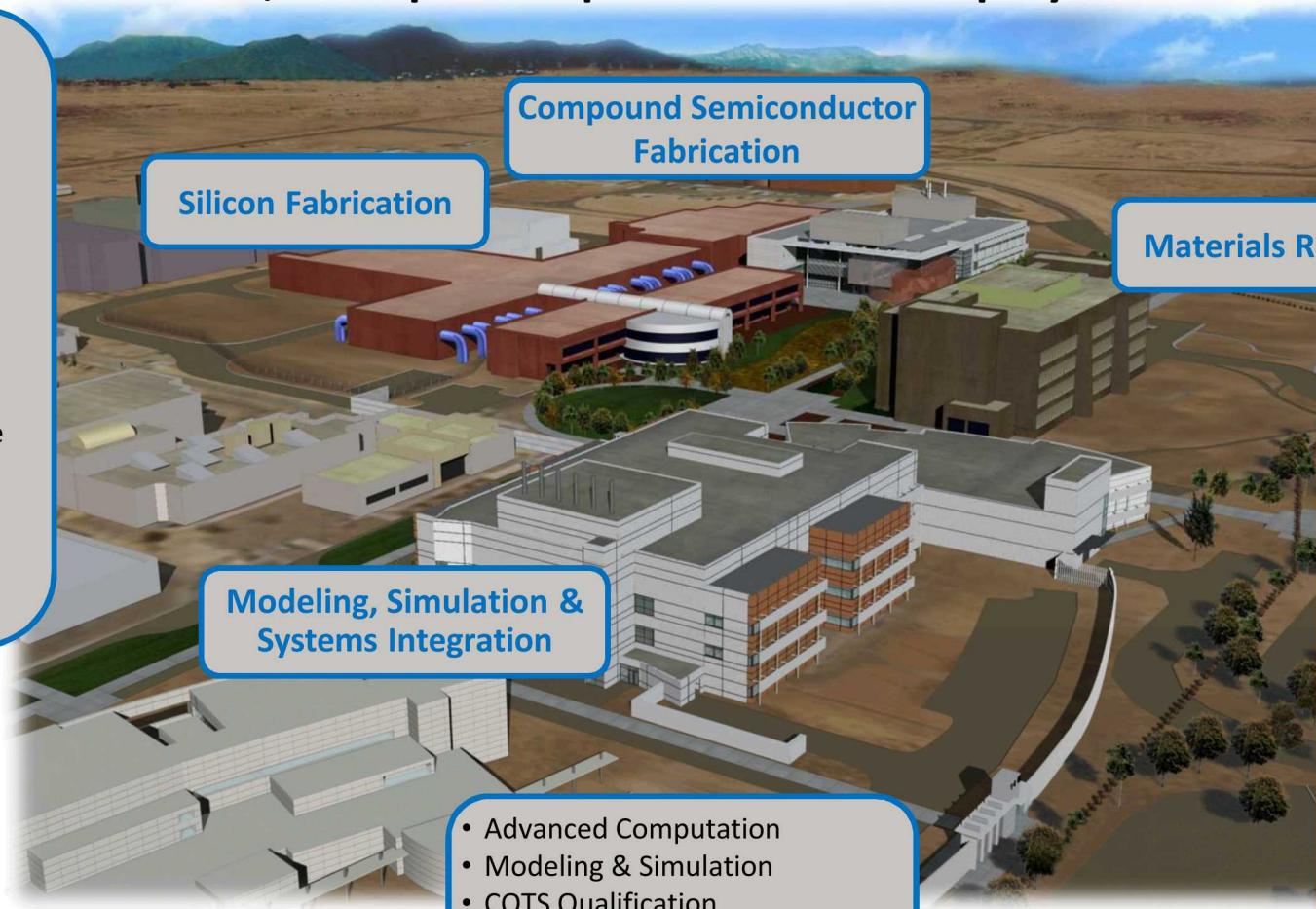
Micro Labs

Microsystems and Engineering Sciences Applications (MESA)



400,000 Sq-ft Complex with >650 Employees

- Trusted Digital, Analog, Mixed Signal & RF Integrated Circuits Design & Fabrication
- Custom IC Design
 - Secure microcontrollers
 - Analog/Digital/RF
 - IBM Trusted Foundry
 - Tamper Resistant
- Micromachining
- RAD Effects and Assurance
- Failure Analysis, Reliability Physics
- Test & Validation
- 3-D Integration Features

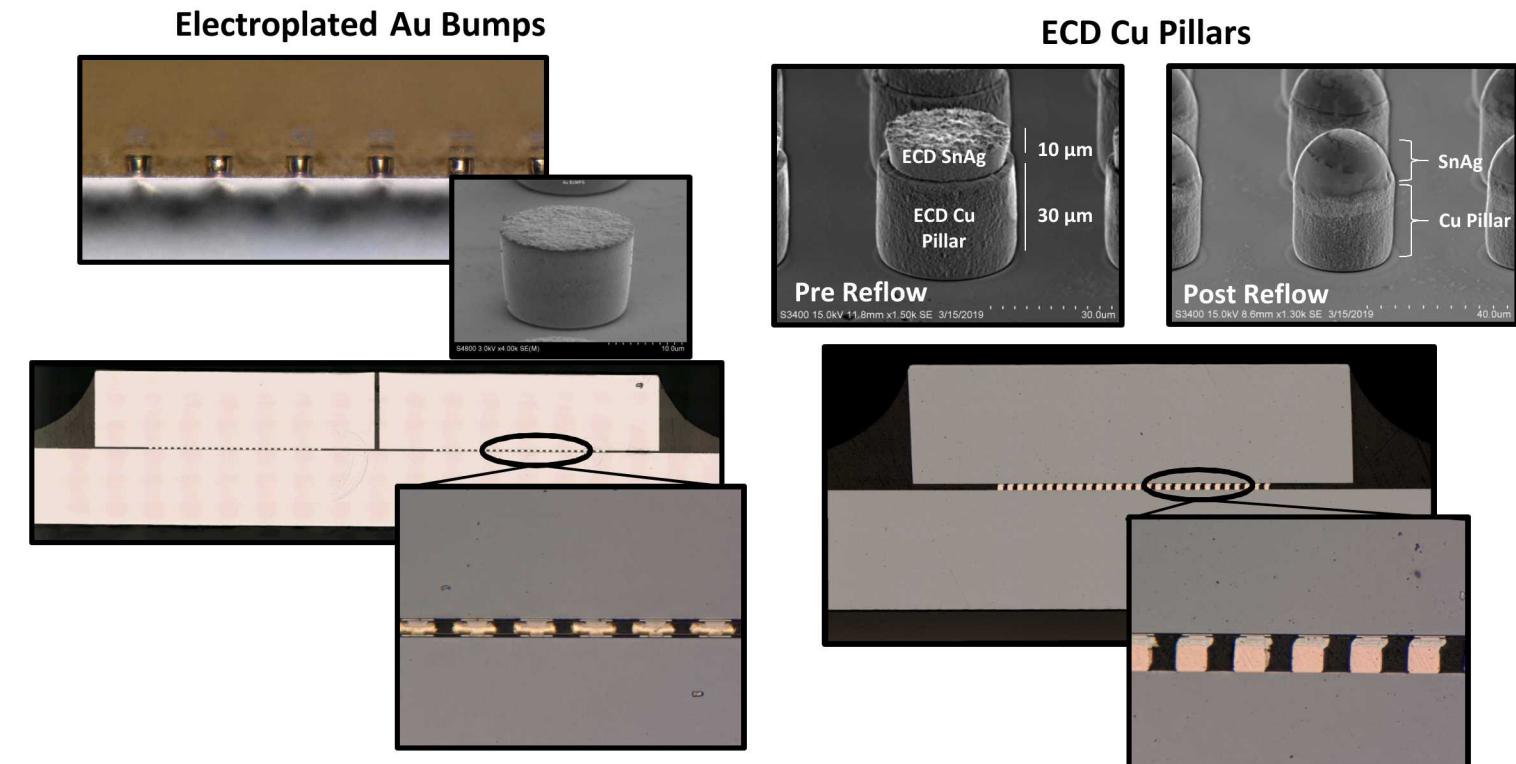
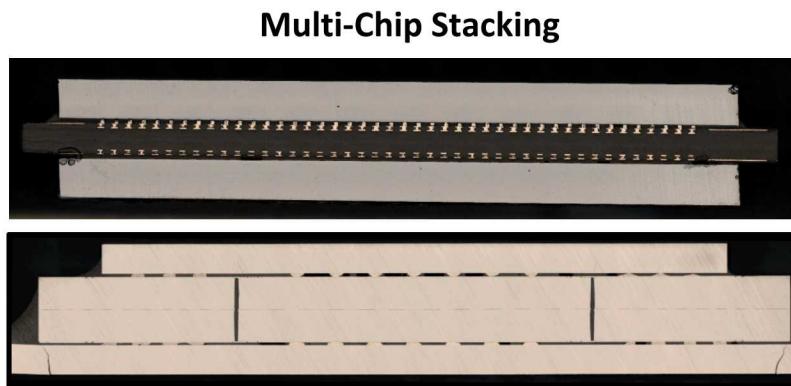
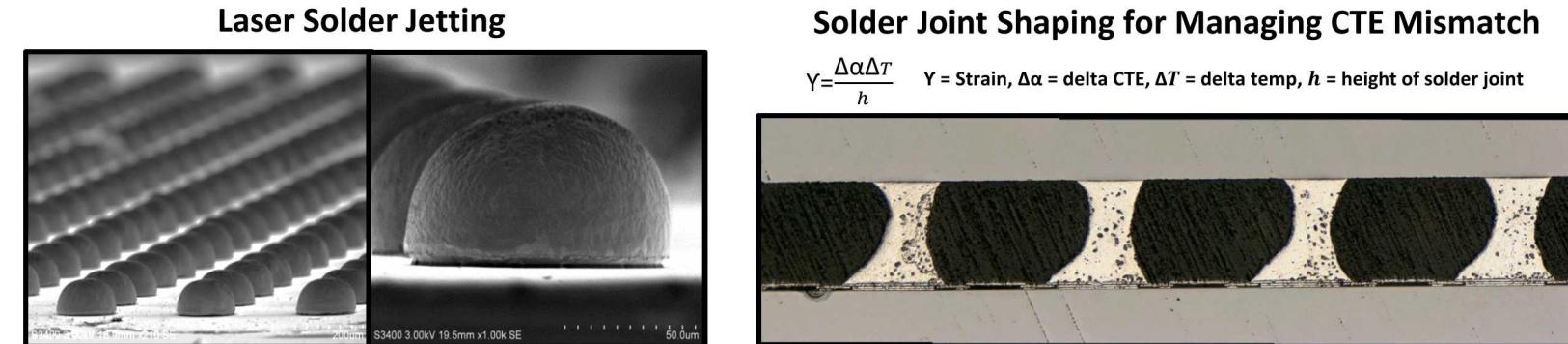


- Advanced Computation
- Modeling & Simulation
- COTS Qualification
- Advanced Packaging
- Custom Electronic Components
- System Design & Test

- Compound Semiconductor Epitaxial Growth
- Photonics, Optoelectronics
- MEMS, VCSELs
- Specialized Sensors
- Materials Science
- Nanotechnology, Chem/Bio
- Mixed-Technology Integration & Processing
- III-V Semiconductor Devices
 - Neutron-Immune HBT
 - Rad-hard Optical Links
 - Solid-State RF Devices

Flip Chip Bonding – Solder Jetting, Cu Pillars, Au and In Bumps

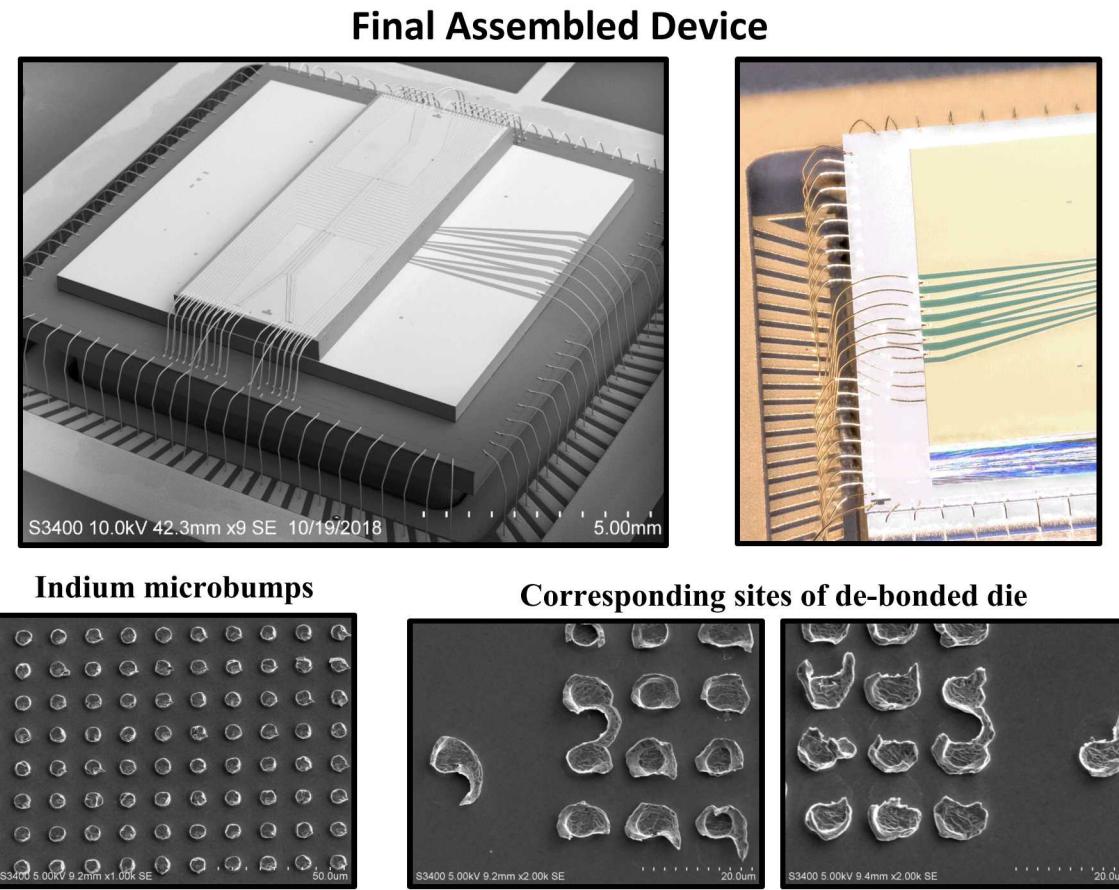
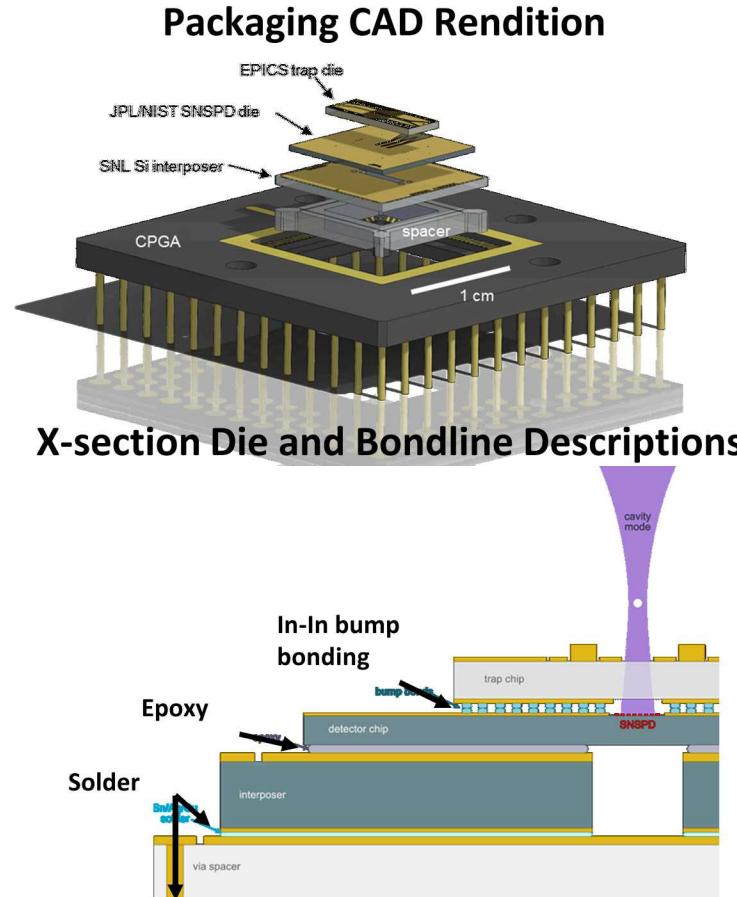
- Highly flexible R&D level solder bump deposition and rework
- D2D and D2W reflow attachment
- C4 flip chip
- Solder joint shaping
- Au thermocompression bonding
- Indium bump bonding
- Cu pillars



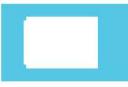
EPICS (Extreme Performance Ion Trap-Cavity System)

Heterogeneous Integration Approach

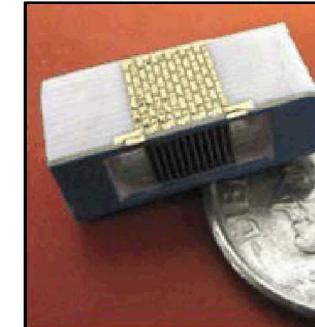
- Collaboration between SNL/JPL/NIST/Duke Univ.
- Combine SNSPD (superconducting nanowire single photo detector) with an optical cavity and microfabricated ion trap for enhanced ion detection
- Solder, epoxy, and indium bonds used to connect these 5 components with 4 different wirebond profiles for full connectivity



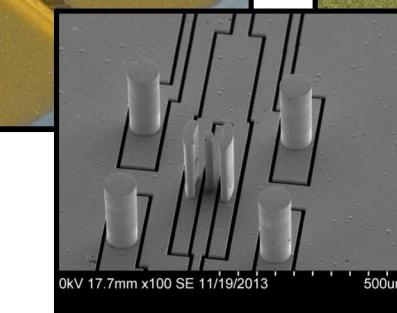
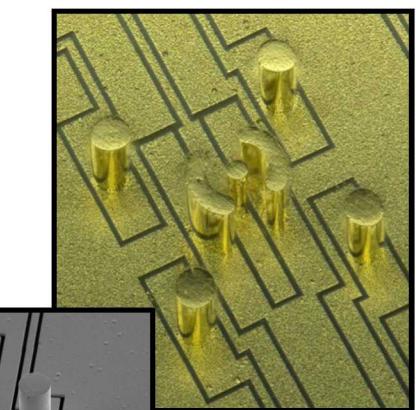
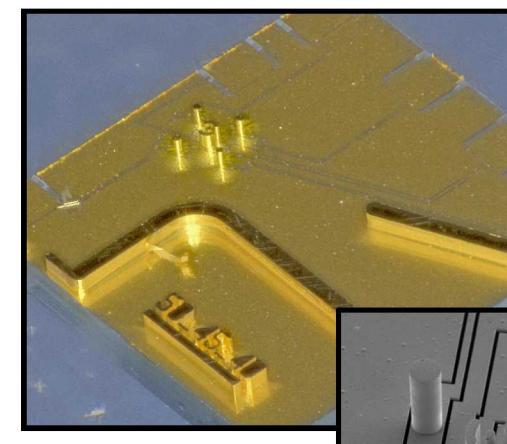
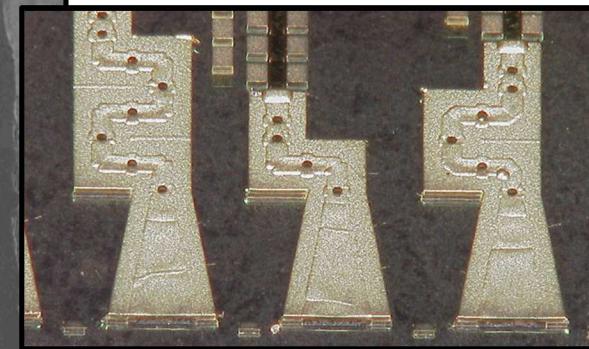
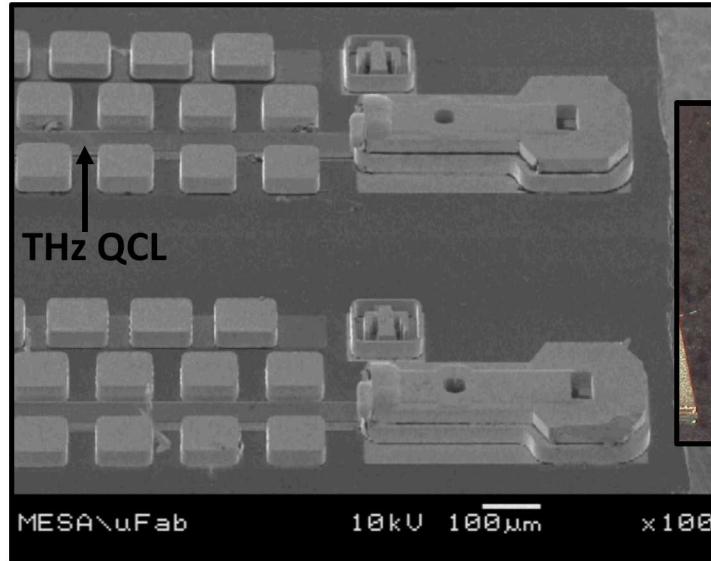
Electroplating Applications



Masking achieved through unique fixturing and controlled polymer deposition

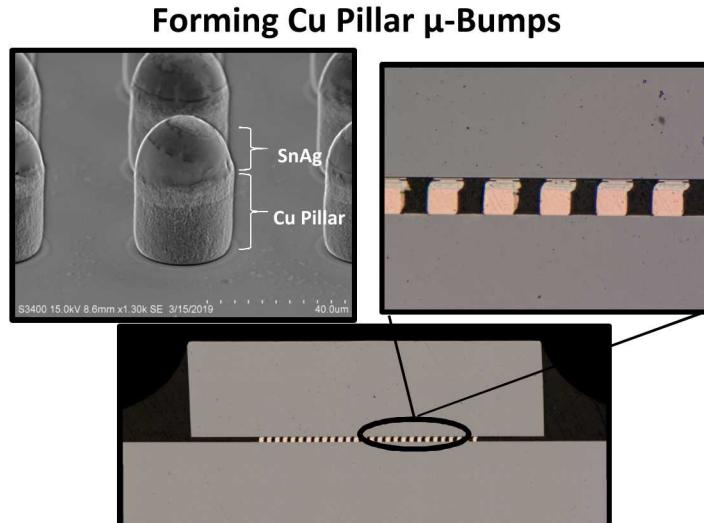


3-D Integrated Gold THz Waveguides

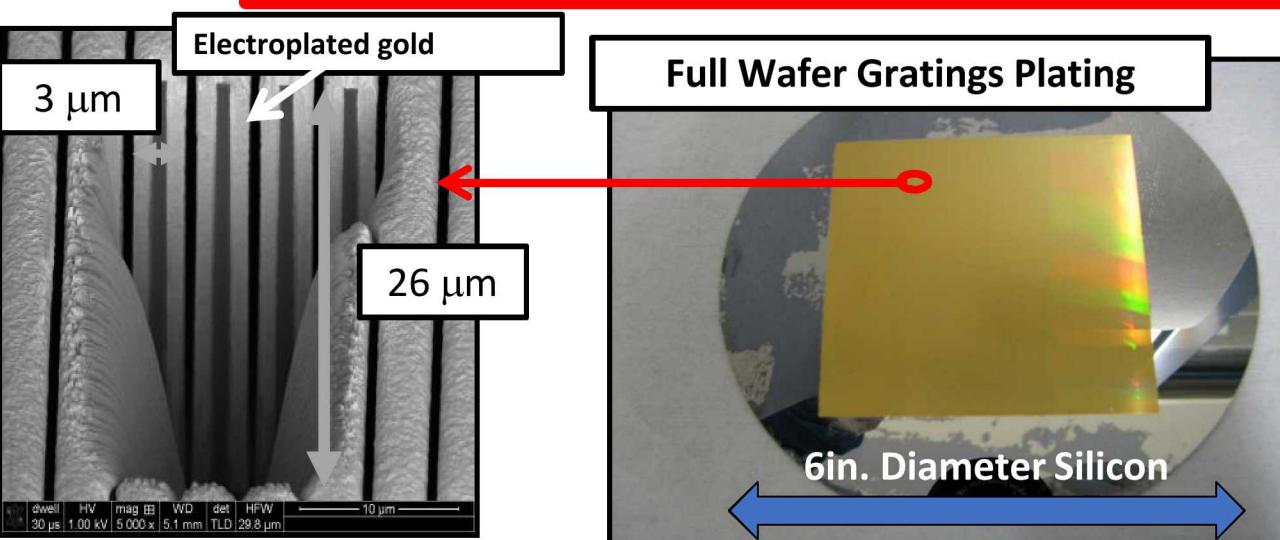
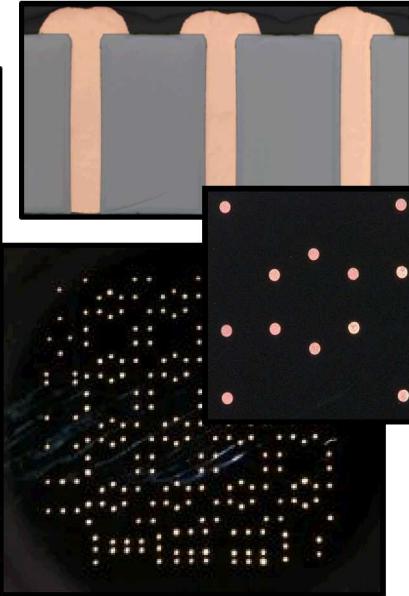
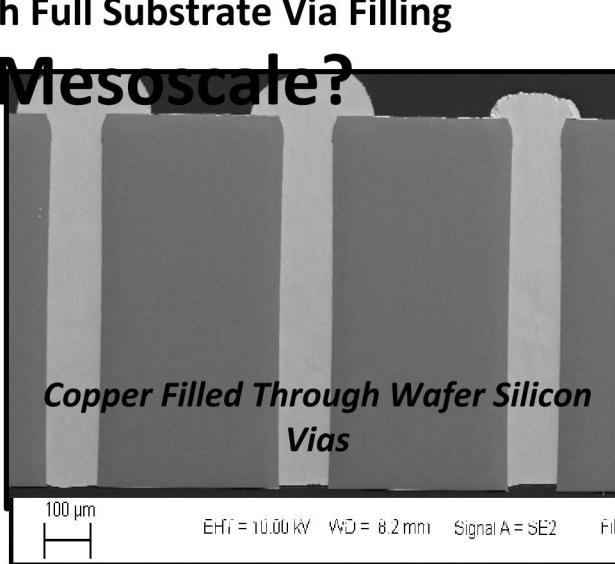


Electroformed 3D Au Stylus Ion Trap

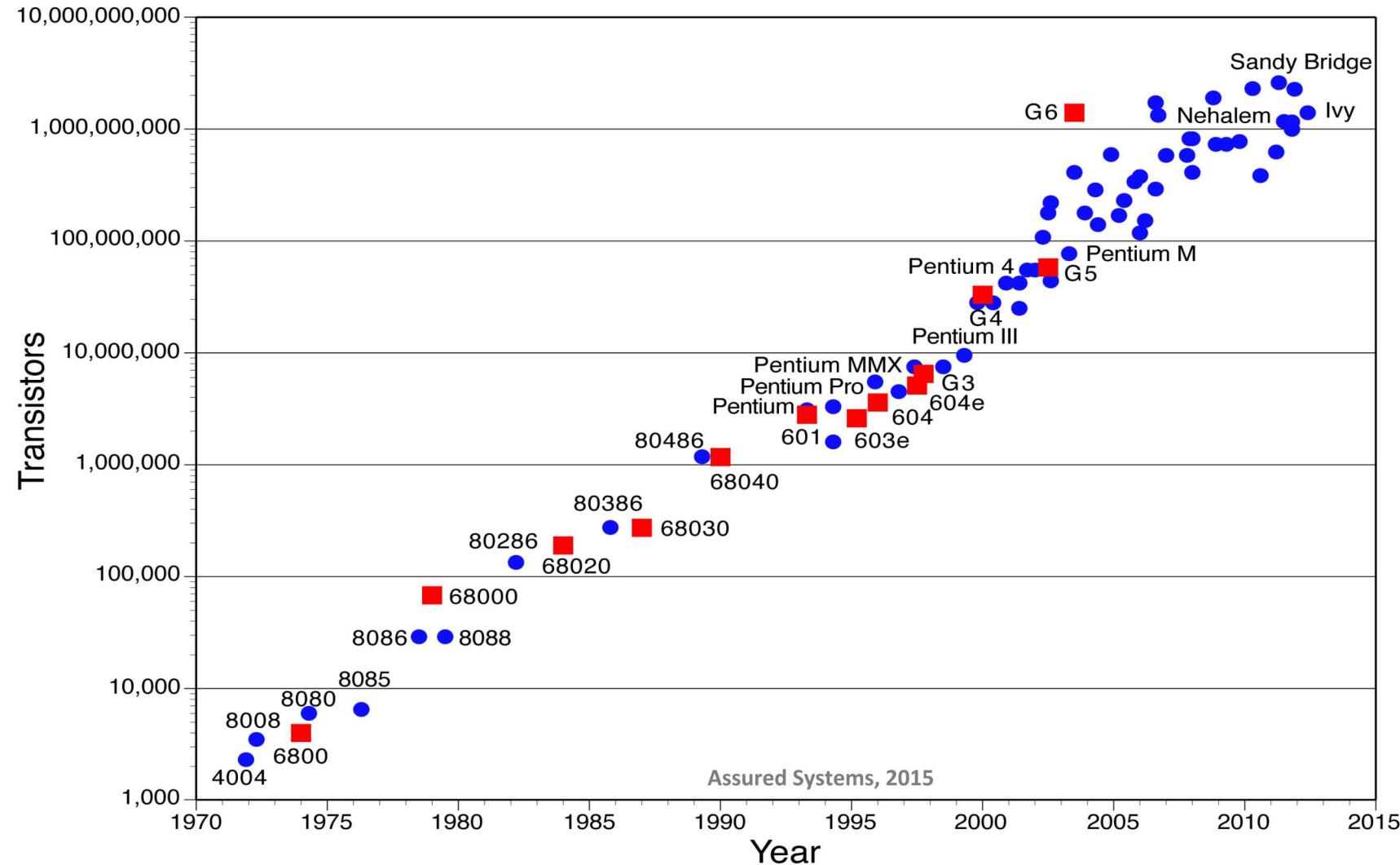
Mesoscale Fabrication: Forming, Filling, and Coating



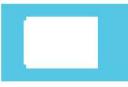
Through Full Substrate Via Filling
What is Mesoscale?



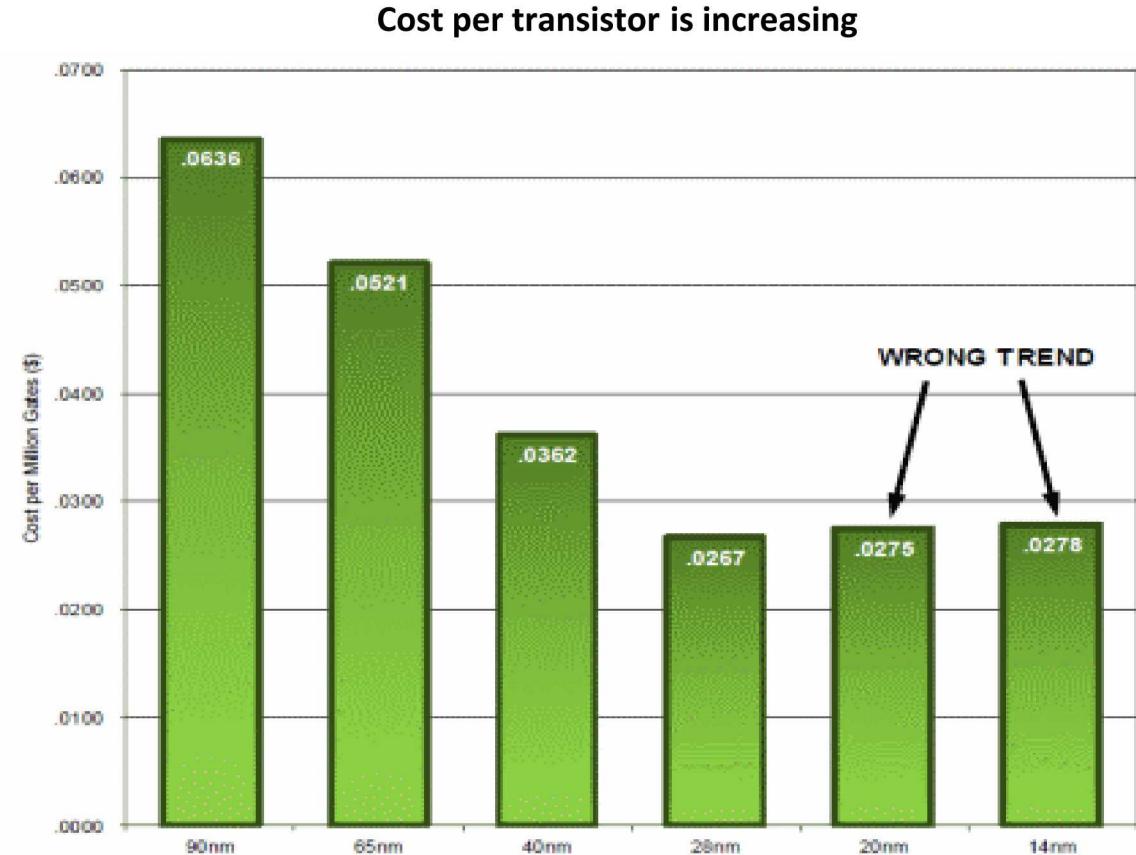
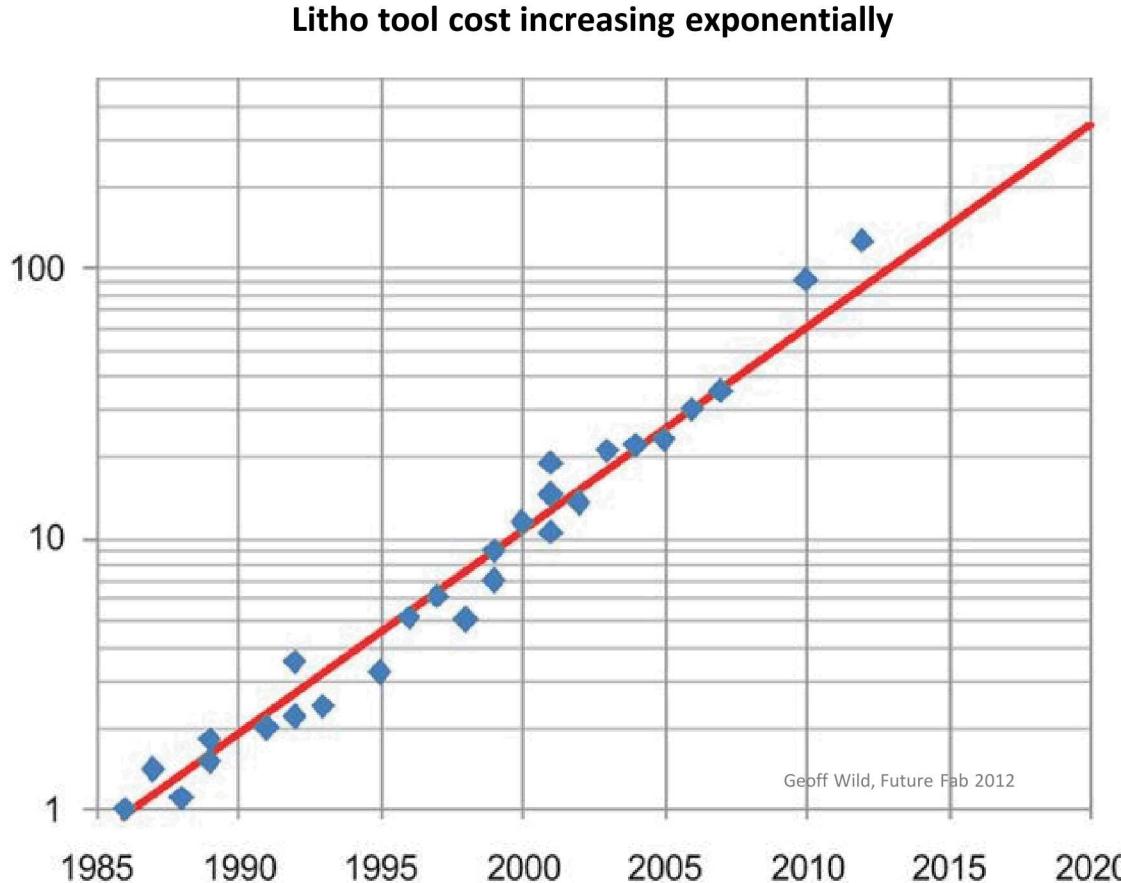
Moore's Law: Approaching 0 nm!



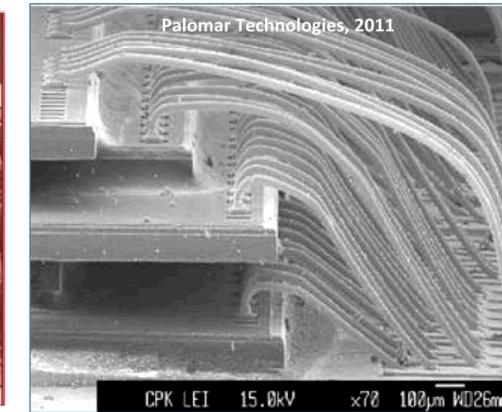
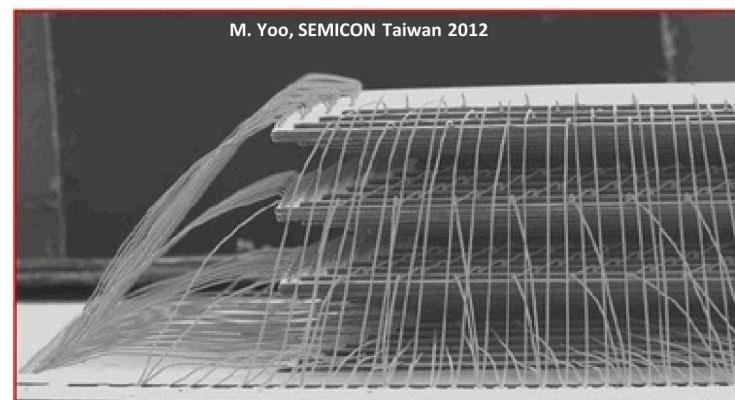
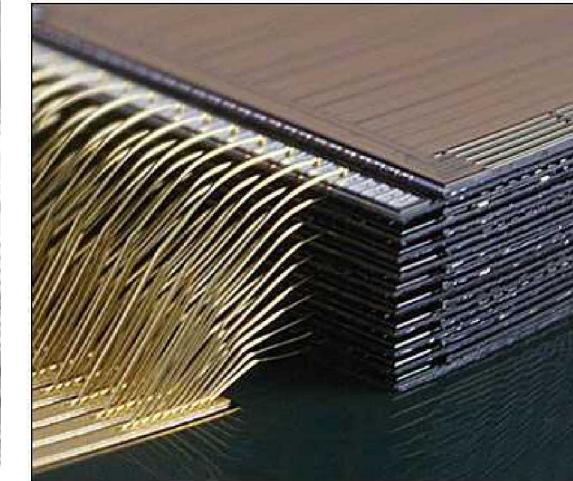
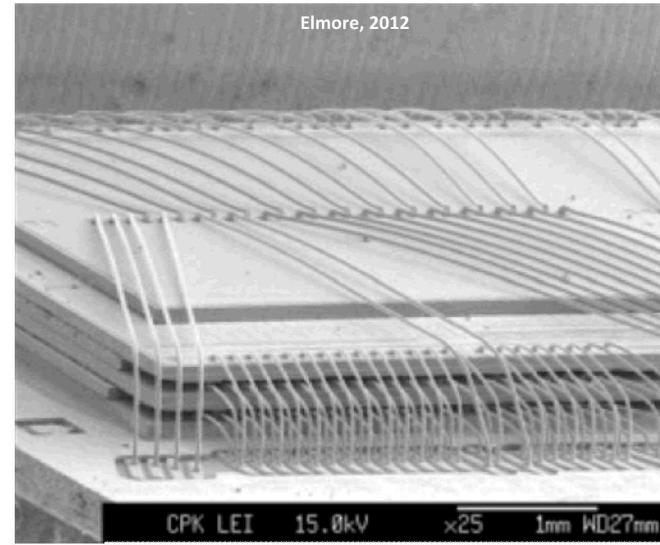
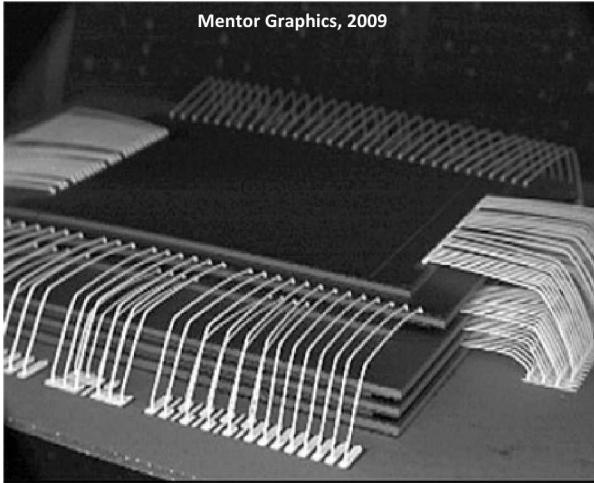
Moore's Law: Not so Fast...



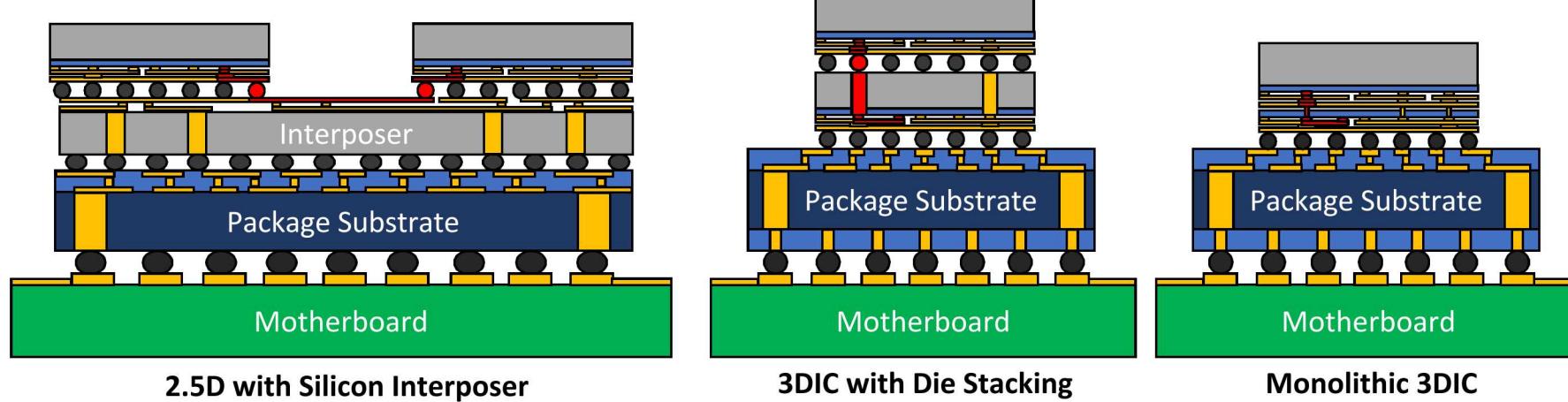
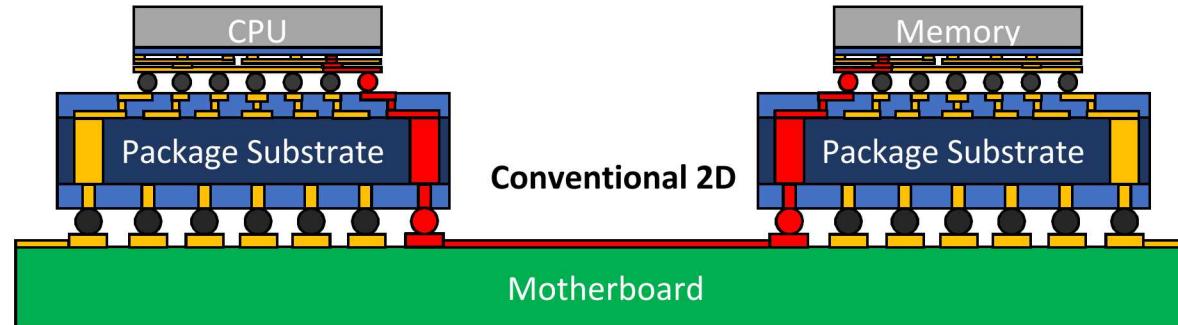
Lithography Tool Cost (\$1M)



Chip Stacking → Increased Performance Per Volume



3D Integration Landscape



Through Substrate Vias (TSVs) for MEMS Devices

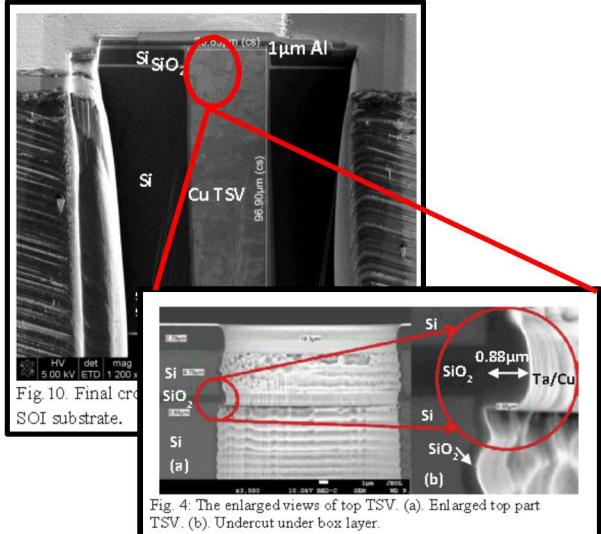


Cu TSVs vs Doped Si TSVs

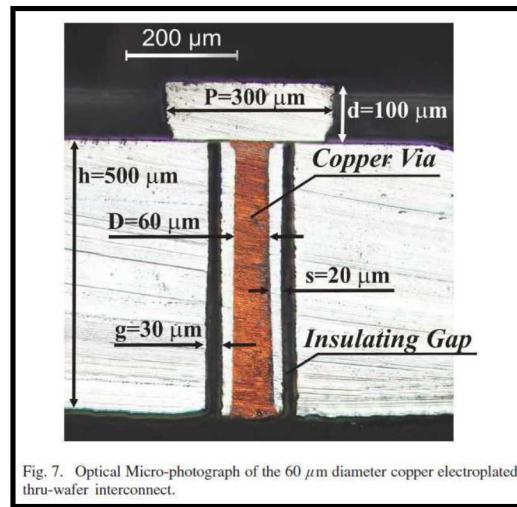
Material	Doped Si	Copper
Resistance single TSV	40Ω	$0.8 \text{ m}\Omega$
Thermal conductivity	$150 \frac{\text{W}}{\text{m}\cdot\text{K}}$	$400 \frac{\text{W}}{\text{m}\cdot\text{K}}$

MEMS TSVs Integration with SOI Substrates

TSV-First¹



TSV-Last²



Benefits of TSVs

- Increase I/O per area
- Improved thermal sinking
- Reduced electrical parasitics
- Simplified design and assembly

Sandia's TSV Requirements

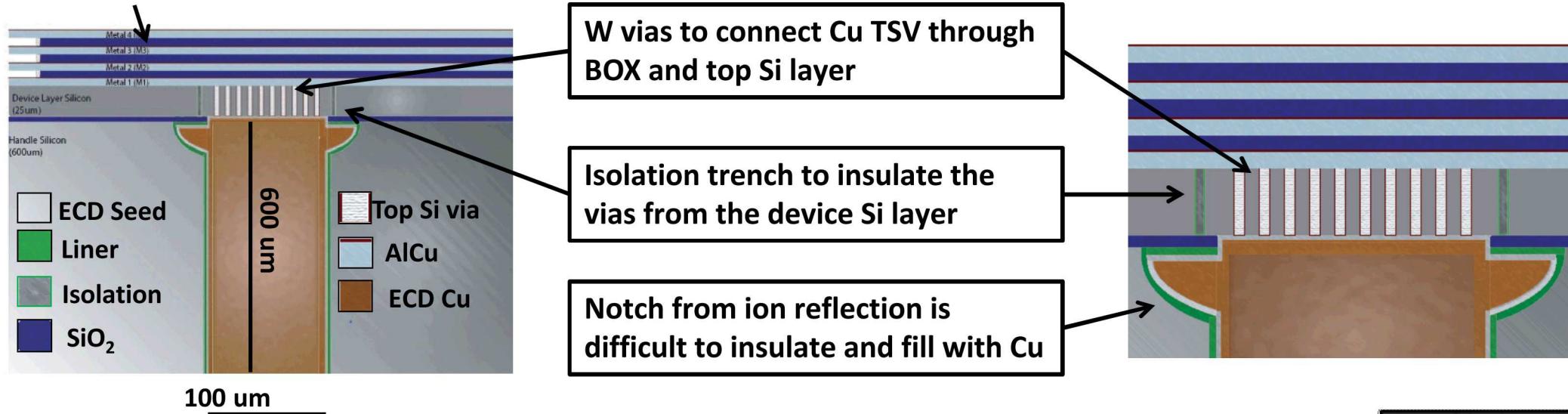
- Via-Last TSVs
- Full Thickness Si Wafers
 - Maintain radius of curvature
 - Maintain large mass for accelerometers
- Void free fill

1. G-K. Lau et. al "Process Integration and Challenges of Through Silicon Via (TSV) on Silicon-On-Insulator (SOI) Substrate for 3D Heterogeneous Applications." 17th Electron. Packaging Tech. Conf., (2015).

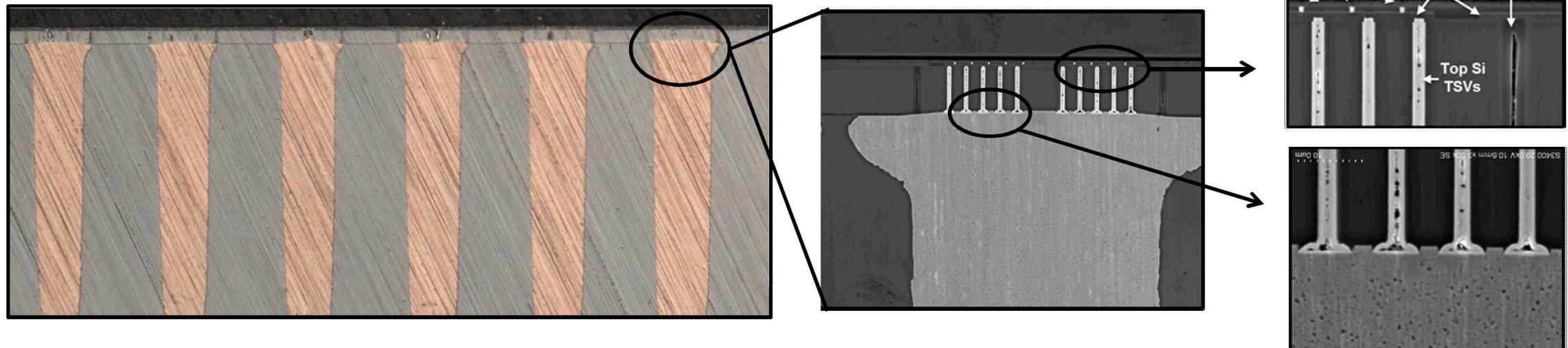
2. A. Efimovskaya, et. al "Double-Sided Process for MEMS SOI Sensors with Deep Vertical Thru-Wafer Interconnects." Journal of Microelectromechanical Systems, Vol. 27, No. 2, April 2018

Hybrid W Via First, Cu Via Last Approach for SOI Substrates

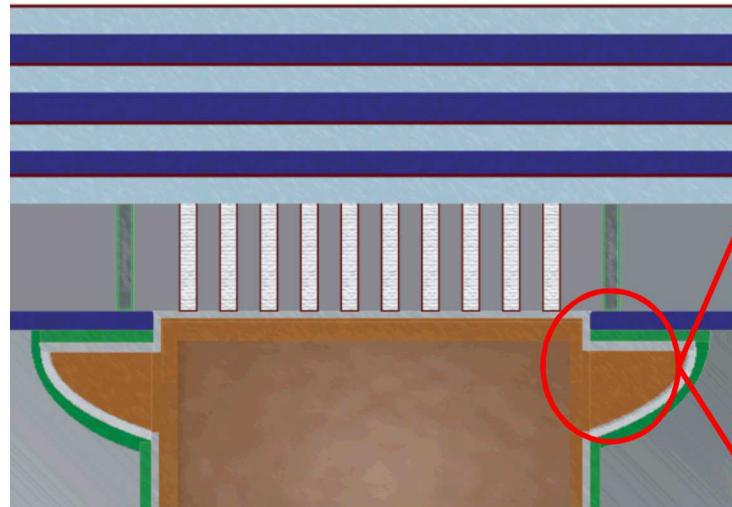
Multi-layer routing (SUMMiT-V or BEOL CMOS)



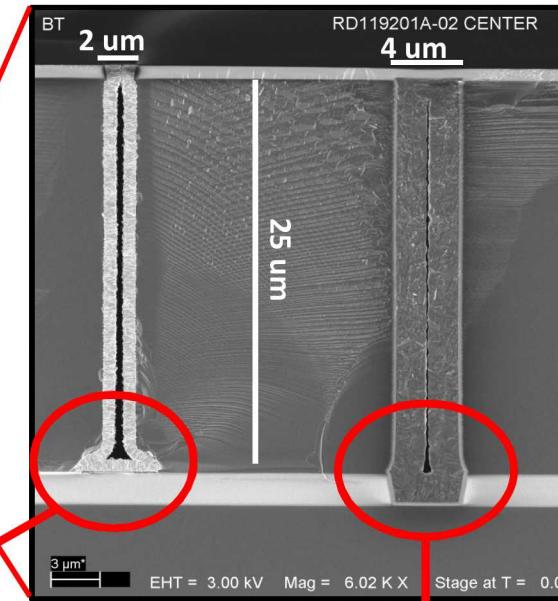
Superfilled Cu TSVs plated from a conformal ALD Pt seed



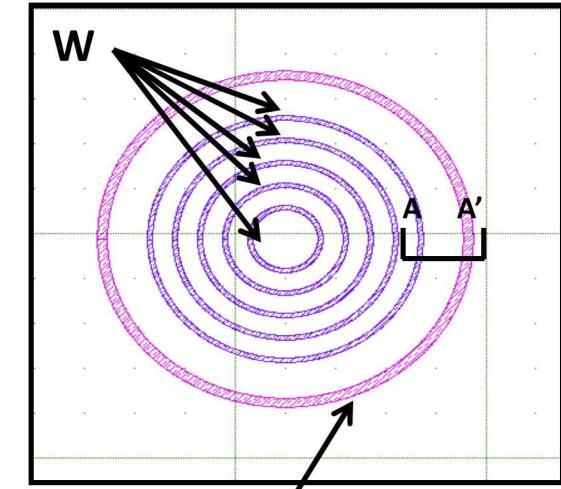
Conduction and Isolation Across the Device Layer Si



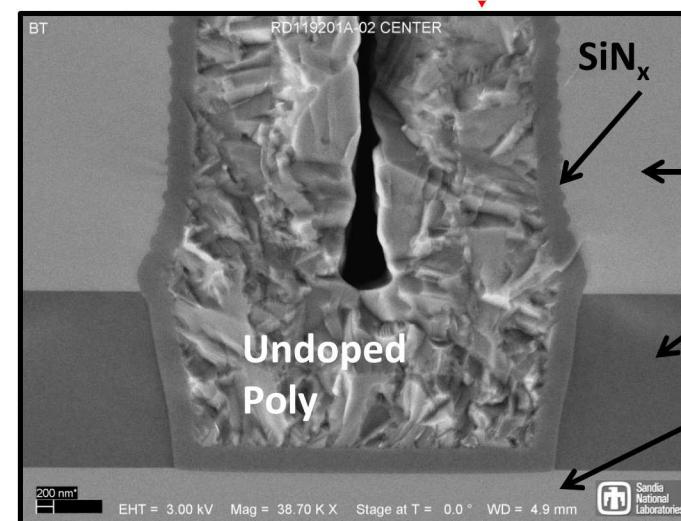
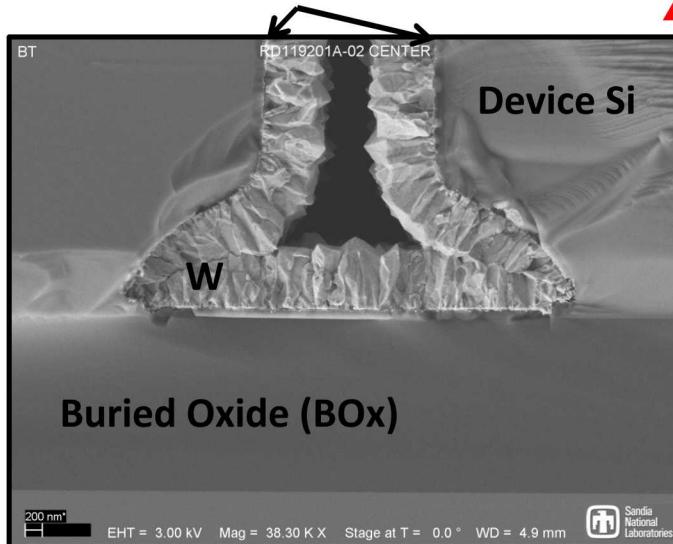
Cross section A-A'



Device Si Layout

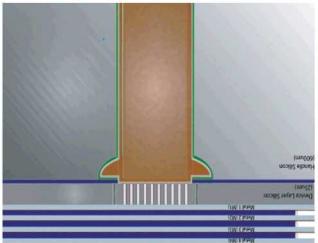


Degenerately doped Poly Si



Isolation Trench

TSV Insulating Liner



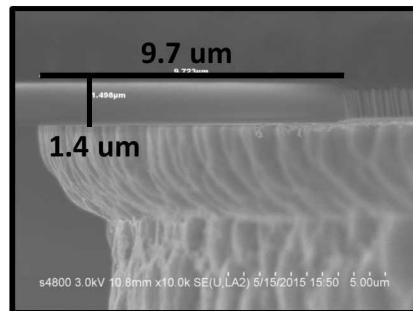
Insulating Liner Constraints

- Must be conformal
- Temperature can't exceed 450C
- Sufficient breakdown voltage

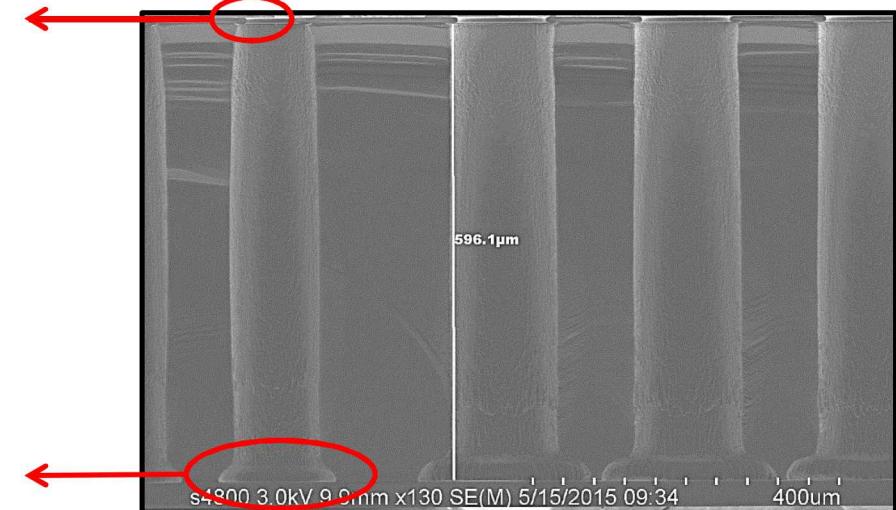
Liner Options

- ~~Sputter deposited insulator (SiO_2 , Al_2O_3 , etc.)~~
- **Low Temp Oxide (LTO)**
- ~~ALD Al_2O_3~~

Substantial hardmask undercut

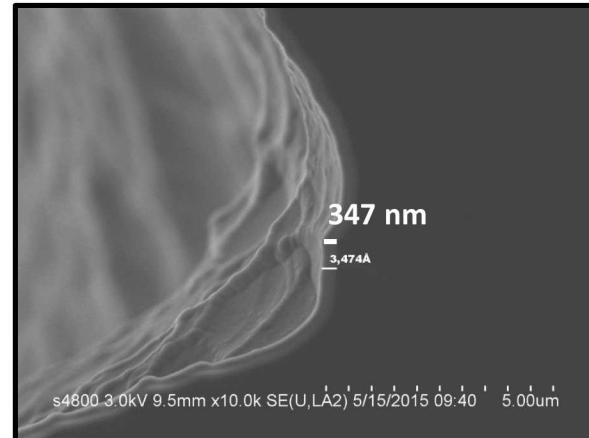
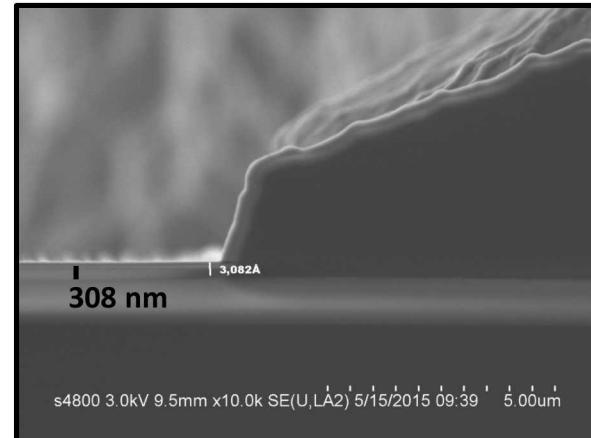
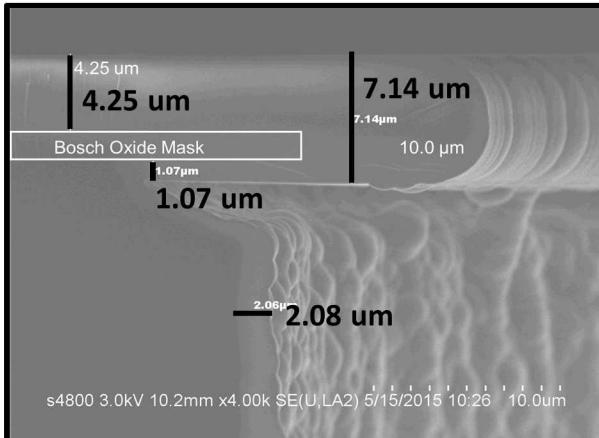


TSV Etch Cross Section



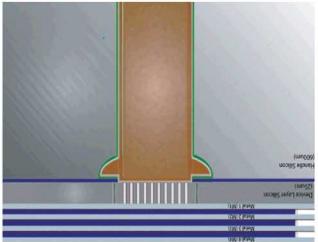
Using the BOX as an etch stop results in notching

Low Temperature Oxide Cross Section



- LTO does conform around the hardmask undercut
- Uniformity is not optimum: 4.25μm deposition on top surface and 300nm deposition at the bottom of the TSV

TSV Insulating Liner



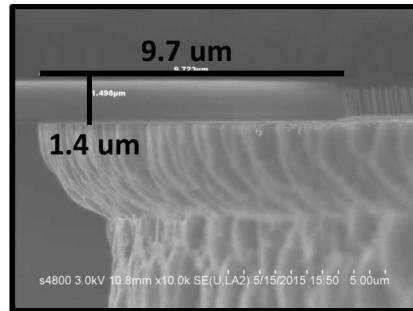
Insulating Liner Constraints

- Must be conformal
- Temperature can't exceed 450C
- Sufficient breakdown voltage

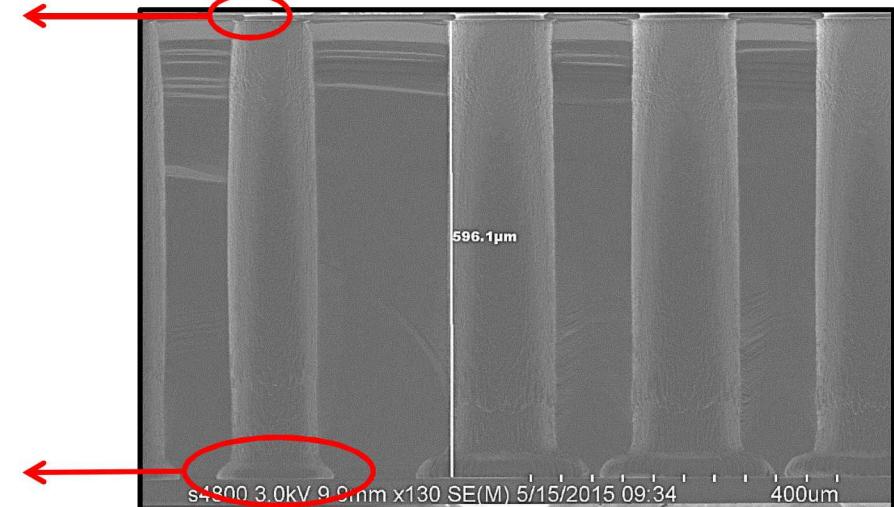
Liner Options

- ~~Sputter deposited insulator (SiO_2 , Al_2O_3 , etc.)~~
- ~~Low Temp Oxide (LTO)~~
- **ALD Al_2O_3**

Substantial hardmask undercut

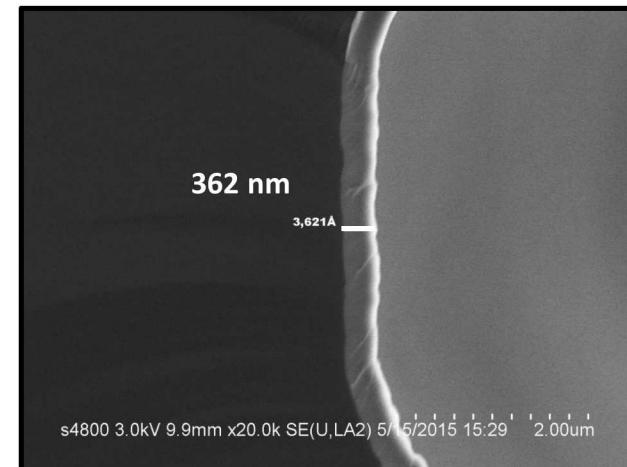
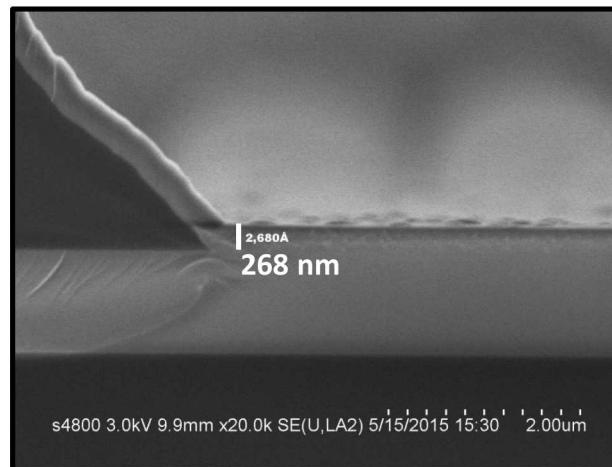
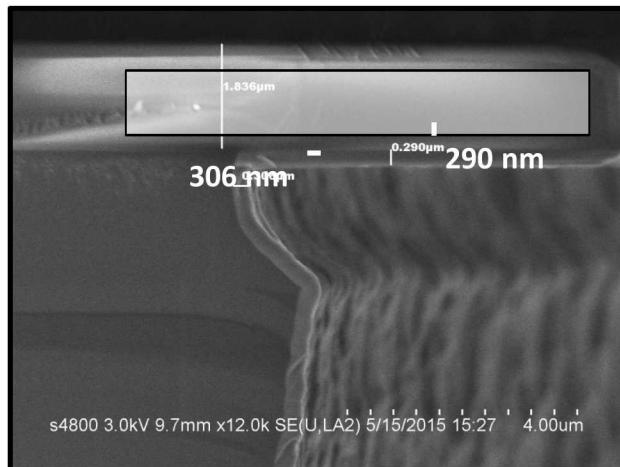


TSV Etch Cross Section



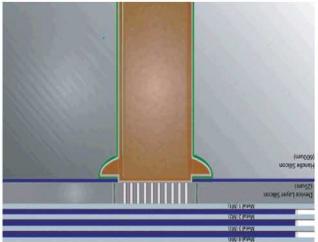
Using the BOX as an etch stop results in notching

Atomic Layer Deposition Al_2O_3 Cross Section



- ALD Al_2O_3 conforms around hardmask undercut and is extremely uniform between the top and bottom of the TSV

TSV Insulating Liner



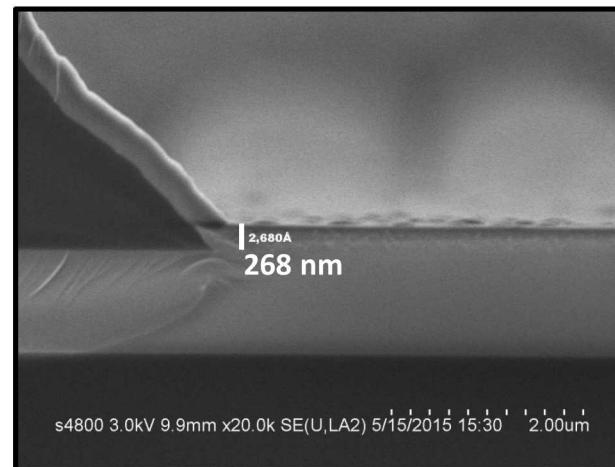
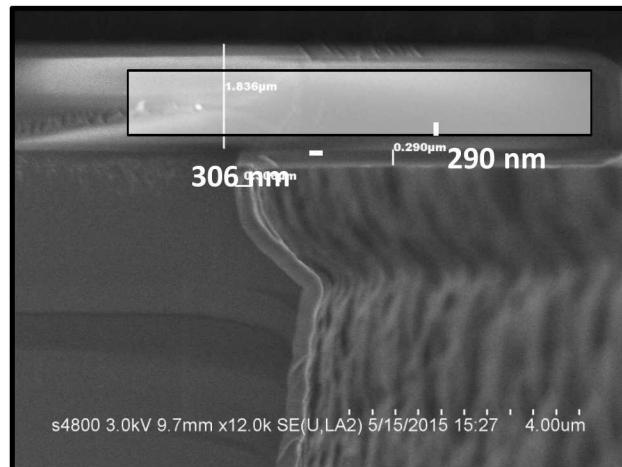
Insulating Liner Constraints

- Must be conformal
- Temperature can't exceed 450C
- Sufficient breakdown voltage

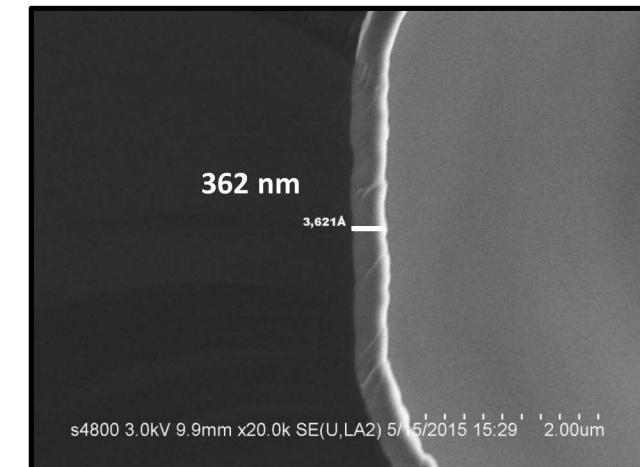
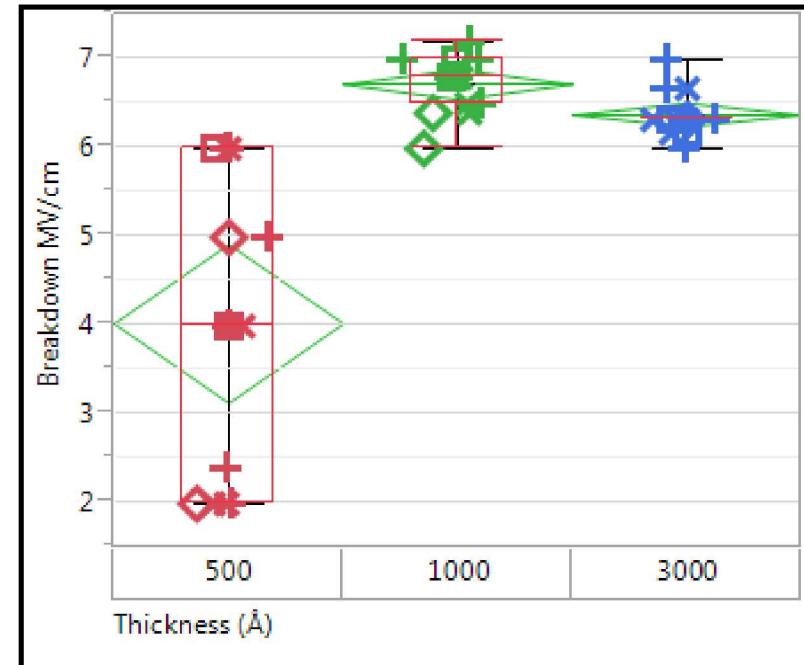
Liner Options

- ~~Sputter deposited insulator (SiO_2 , Al_2O_3 , etc.)~~
- ~~Low Temp Oxide (LTO)~~
- **ALD Al_2O_3**

Atomic Layer Deposition Al_2O_3 Cross Section



Dielectric Breakdown Voltage of Al_2O_3

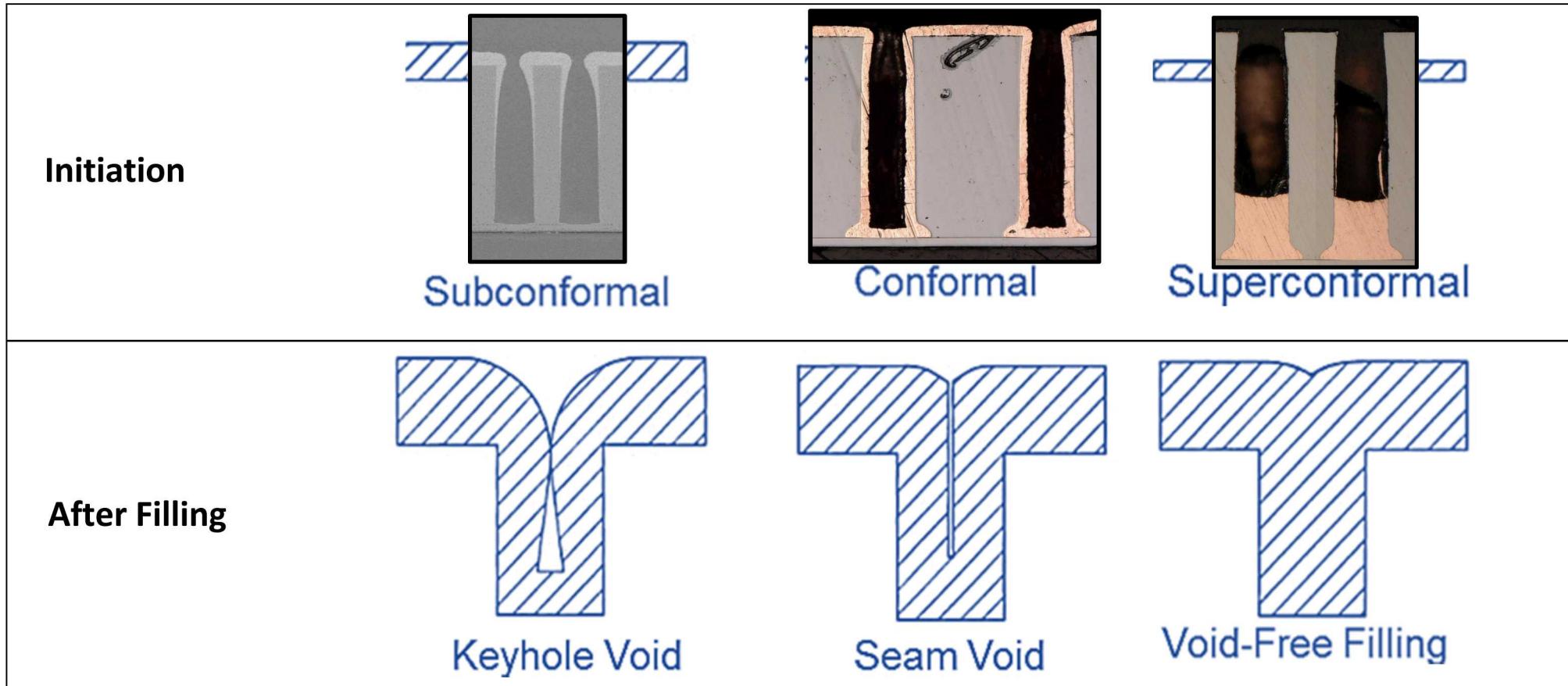


- ALD Al_2O_3 conforms around hardmask undercut and is extremely uniform between the top and bottom of the TSV

Electroplating Fill Profiles



- Additive free ECD leads to **subconformal fill**
- Pulsed plating regime can establish a **conformal fill profile**
- Additives enable **superconformal void-free filling**



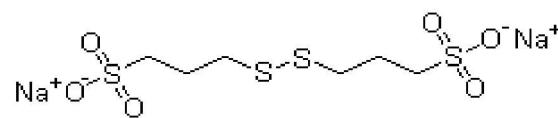
Acid Sulfate Electrodeposition Additives



Common Additives Used In Printed Circuit Board Plating

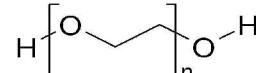
Accelerator

bis-(sodium sulfopropyl)-disulfide (SPS)



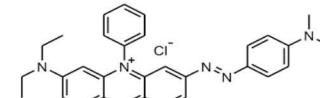
Suppressor

Polyethylene Glycol (PEG)



Leveler

Janus Green B (JGB)



HCl, KCl
Or
NaCl



- **Accelerator** – Surfactant molecule that adsorbs on the surface and, by coverage increase with area loss, preferentially increases plating rate in concave regions
- **Leveler** - Disables accelerator to reduce overburden thickness; grain refiner
- **Suppressor** - Large chain polymer, typically PEG, (1k-20k mW) whose gradient of concentration yields an associated gradient in deposition rate (slower higher in via)

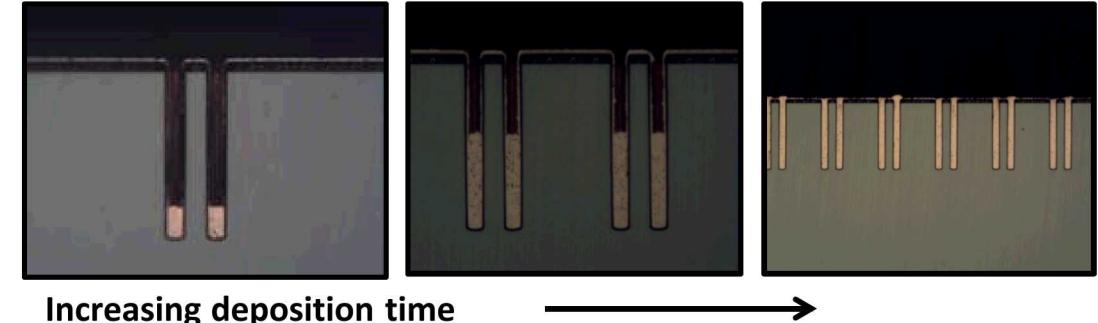
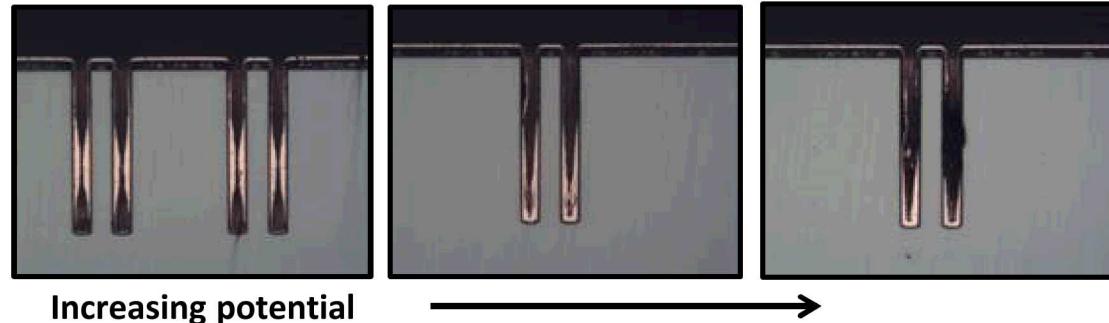
1. All 3 additives carried over from PCB plating development
2. Only the suppressor is needed to achieve void free TSV filling

S-NDR Electrolyte for Void Free Superfilling



NIST Bottom up filling in IBM 56 μm deep TSVs^{1,2}

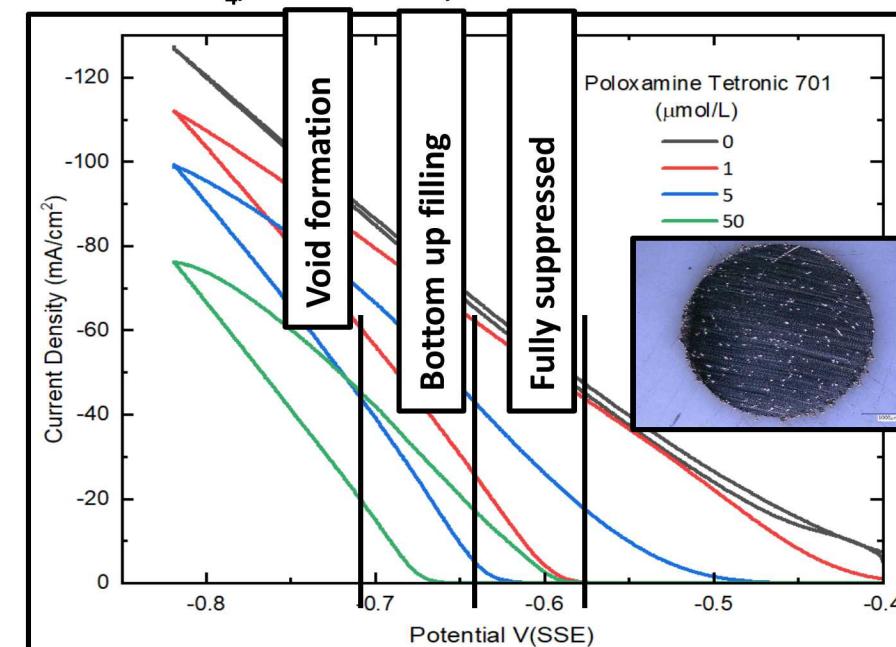
At a given suppressor concentration increasing applied potential pushes deposition down the TSV



1. Journal of the Electrochemical Society, 159 (4) D208-D216 (2012)
2. Journal of the Electrochemical Society, 159 (10) D570-D576 (2012)

Superfilled Bottom Up Plating

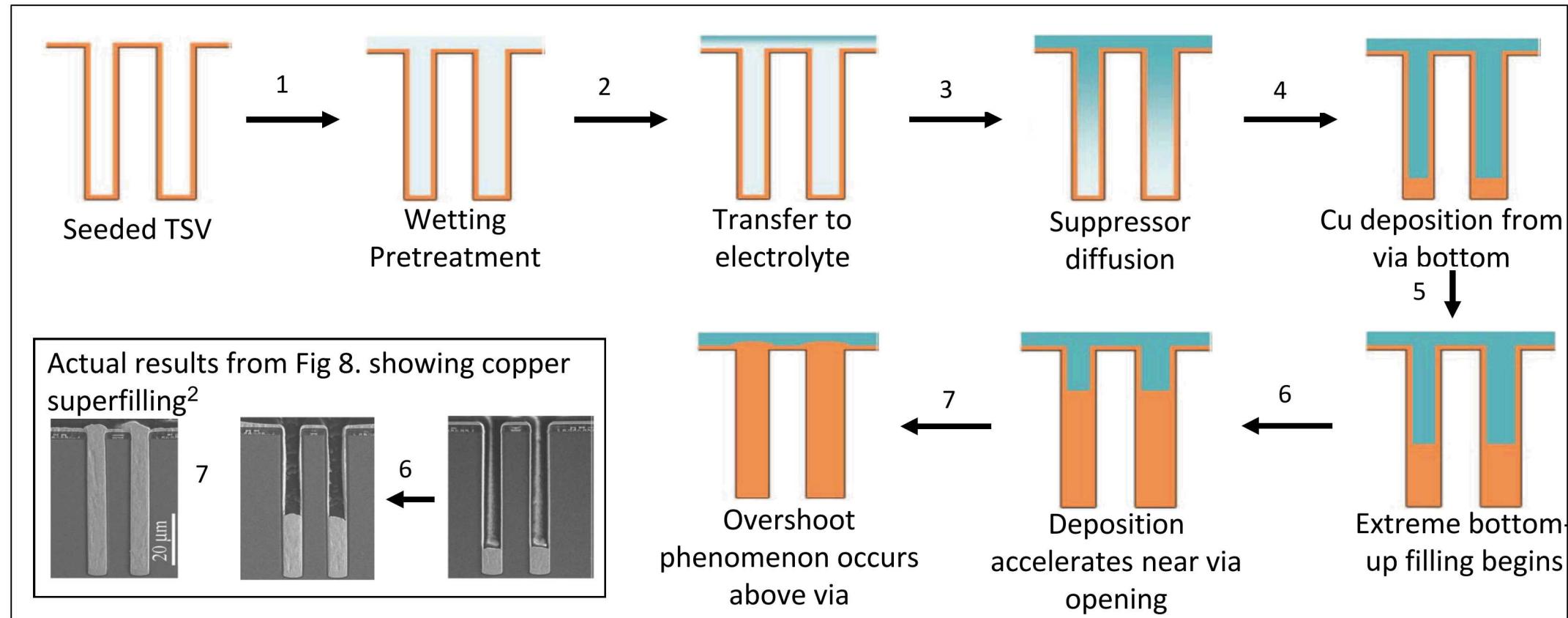
- **Void free filling**
- **Reasonable deposition times**
- **Complex balance b/t applied bias and electrolyte composition**
- **Geometry dependent plating conditions**



Theory: Bottom Up Fill

S-Shaped Negative Differential Resistance (S-NDR) Approach¹⁰

- Single suppressor additive system
- Bottom-up growth mode even with conformal seed metal

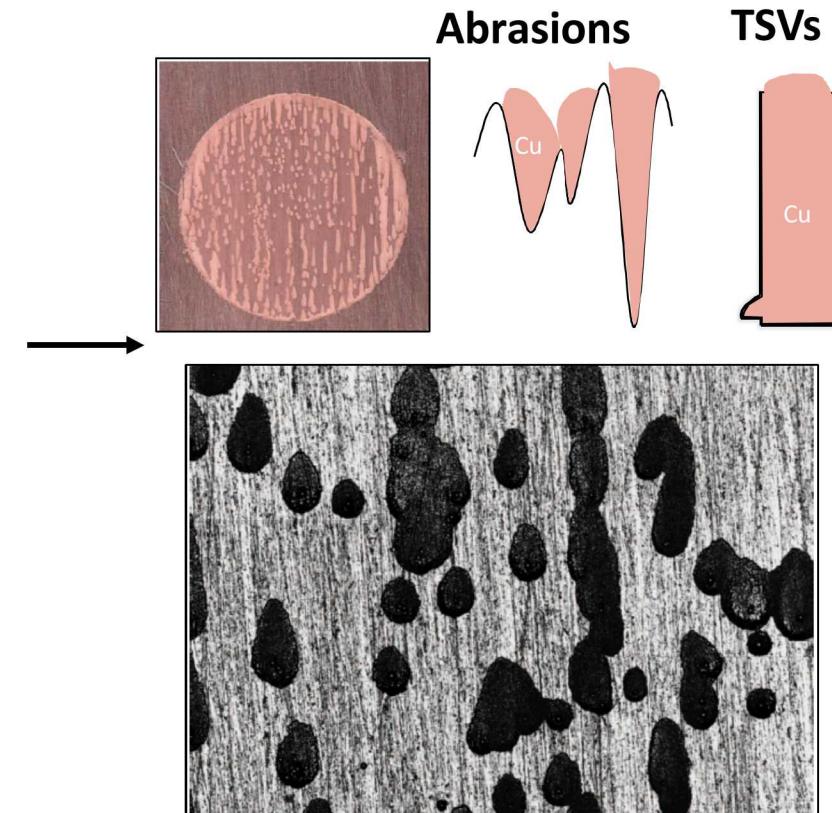
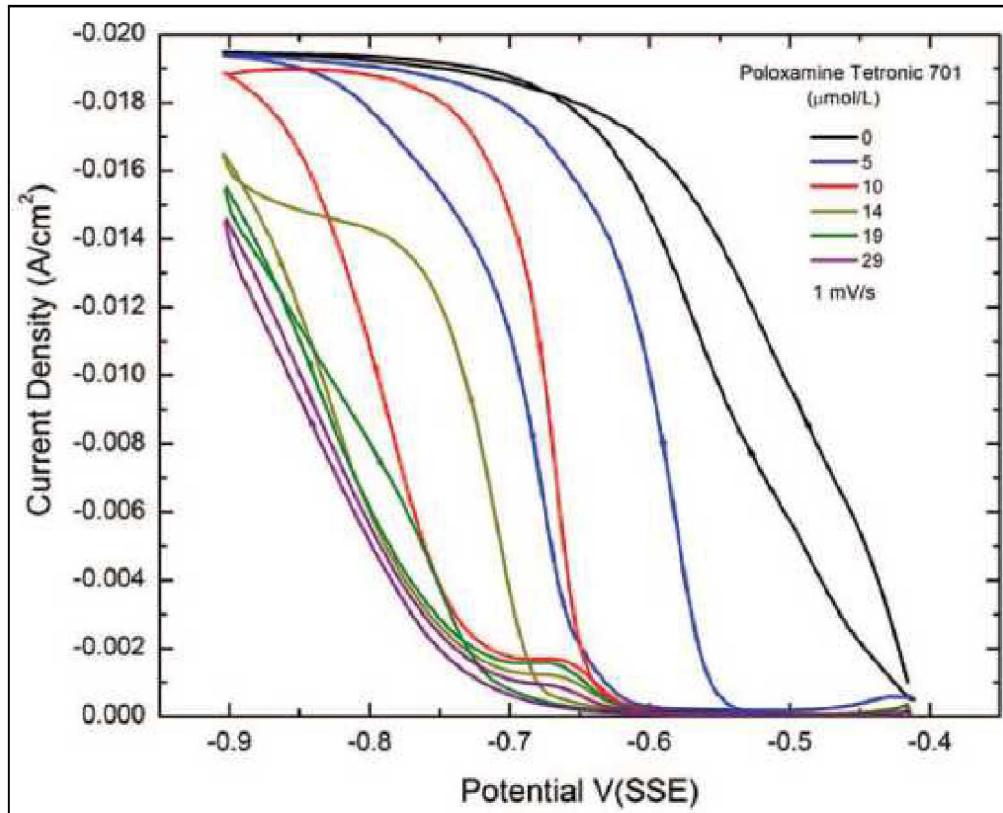
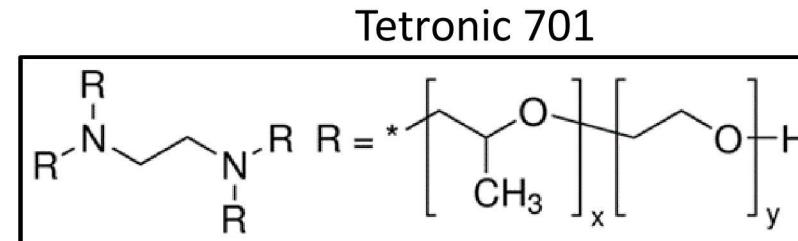


¹⁰ Moffat, T. P., and D. Josell. "Extreme bottom-up superfilling of through-silicon-vias by damascene processing: suppressor disruption, positive feedback and turing patterns." *Journal of The Electrochemical Society* 159.4 (2012): D208-D216.

Characteristics of an Electrolyte Capable of Achieving a Bottom-Up Void Free Fill



- Suppressor organics lead to hysteresis in CV curve
- Chemistries that exhibit this hysteresis cause ‘Turing Patterns’ on planar electrodes

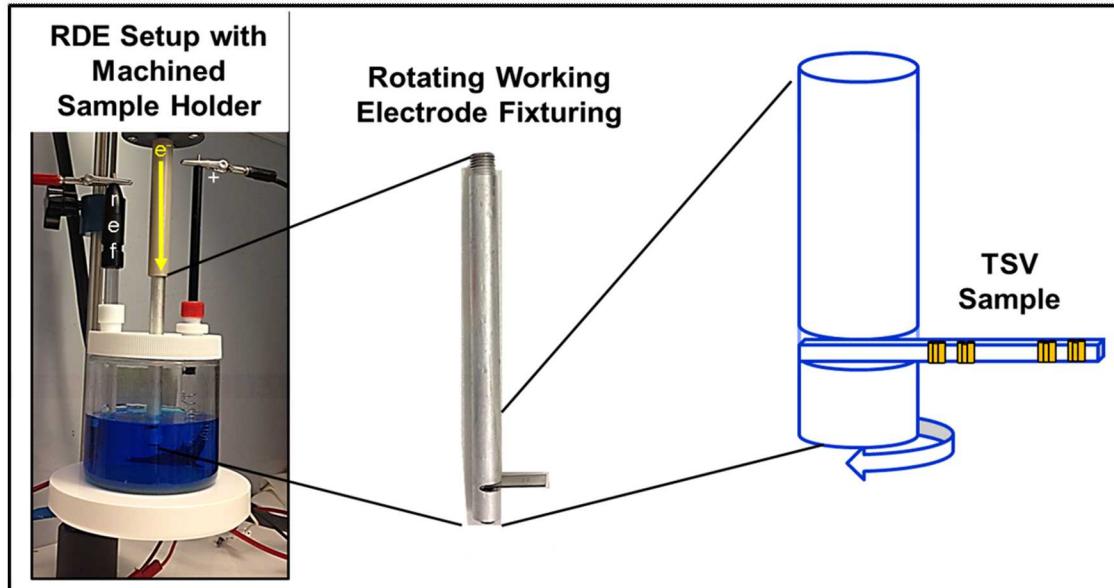


Presence of hysteresis and turing patterns is indicative of a chemistry capable of achieving a bottom up filled void free TSV

TSV Filling Experiments

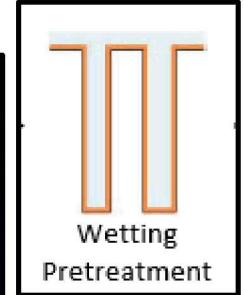
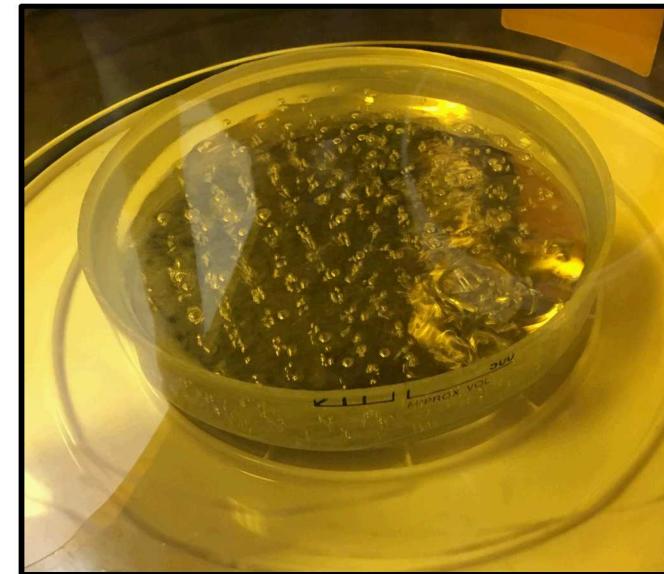


Experimental Apparatus



- Hg/Hg₂SO₄ reference electrode
- Pt anode
- Al sample holder with rotating disk electrode (RDE) to control rpm
- Sample RPM can be correlated to fluid flow and solution replenishment within the TSVs

TSV Pre-wet



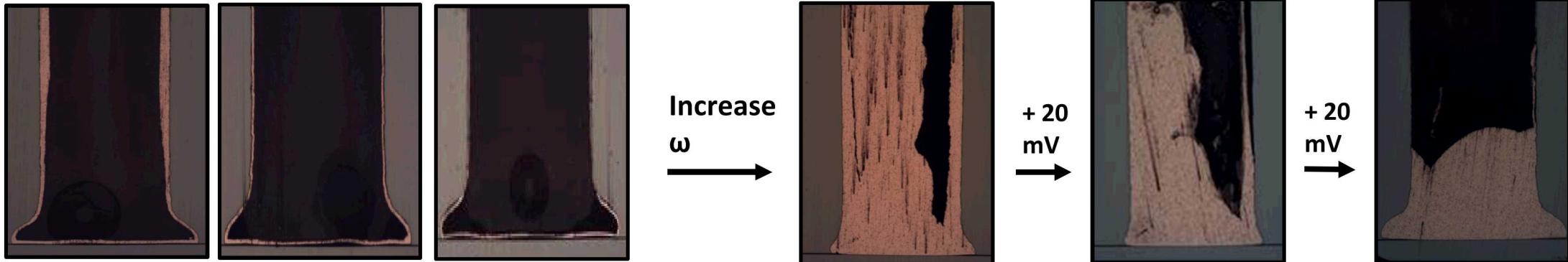
- TSV samples submersed in cooled IPA
- Rough pump vacuum chamber to evacuate all air from the TSVs
- TSV sample remains submersed in IPA until transferred directly to the plating electrolyte

TSV Filling Experiments

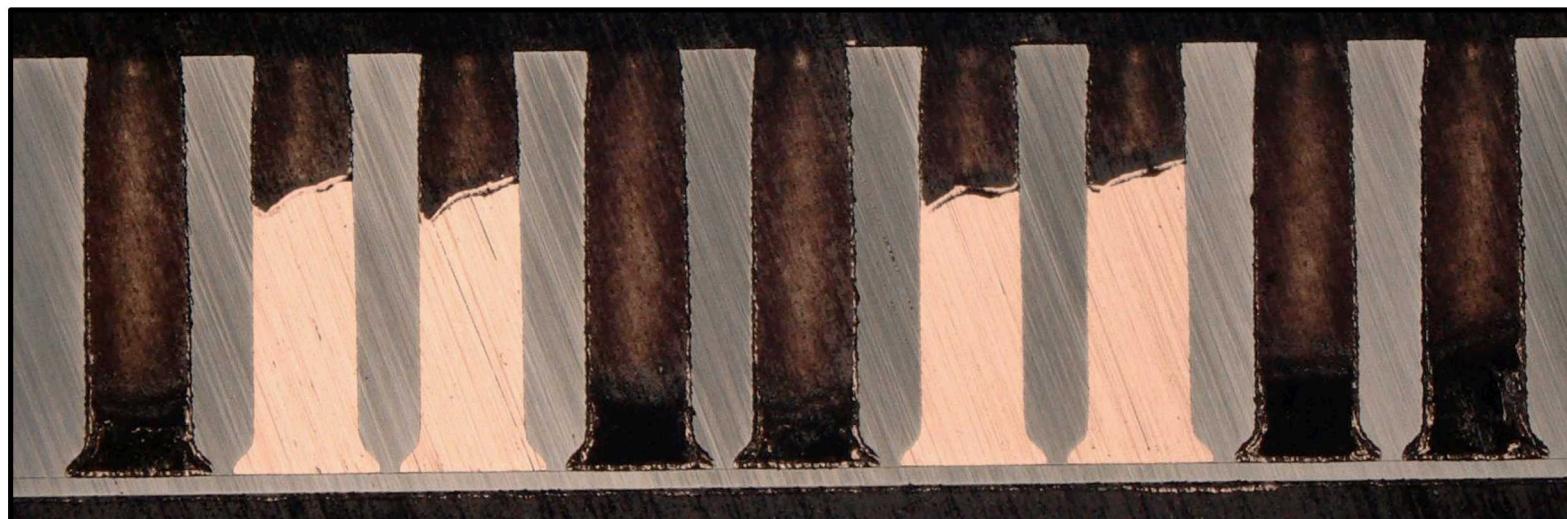


Applied potential, electrolyte fluid flow, and suppressor concentration effect filling

→
Apply higher bias, constant rotation rate (ω)



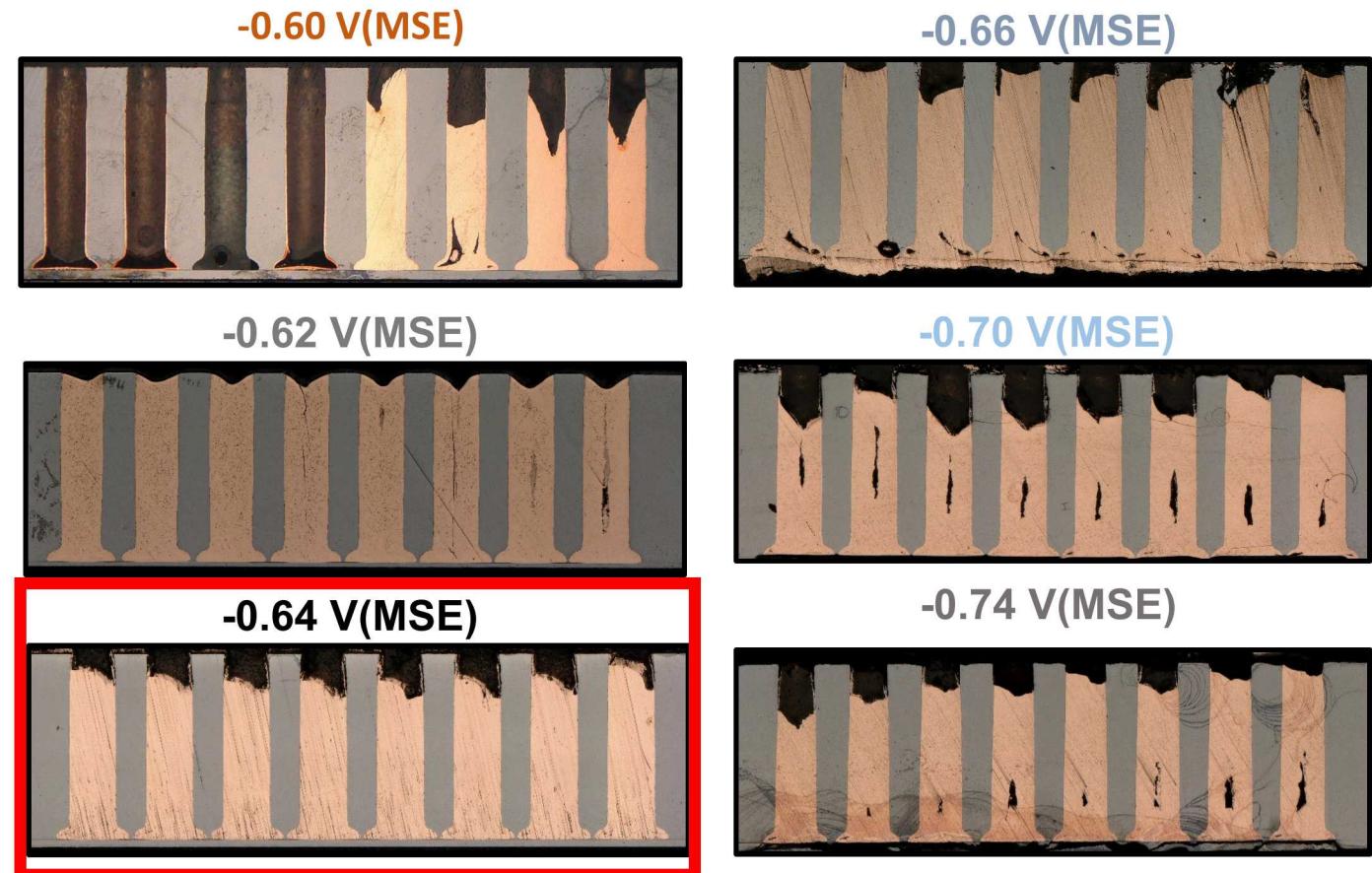
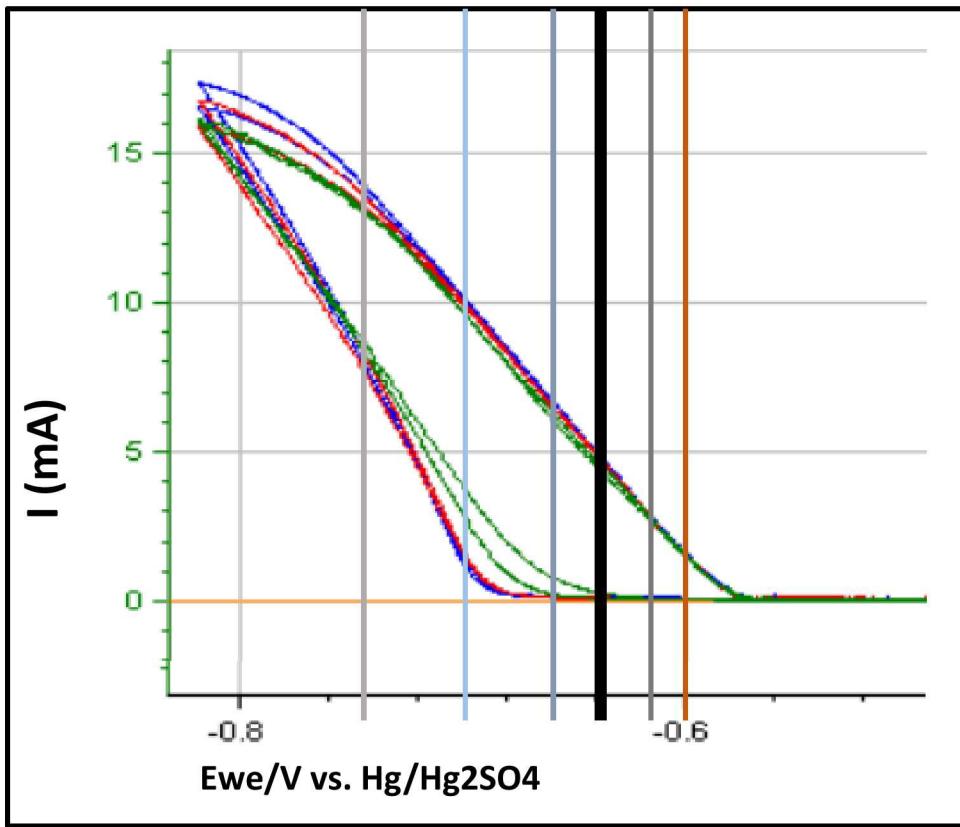
400 rpm, -0.6 V vs RE, 50 μ M Suppressor, 1.25 M CuSO_4 , 0.25 M MSA



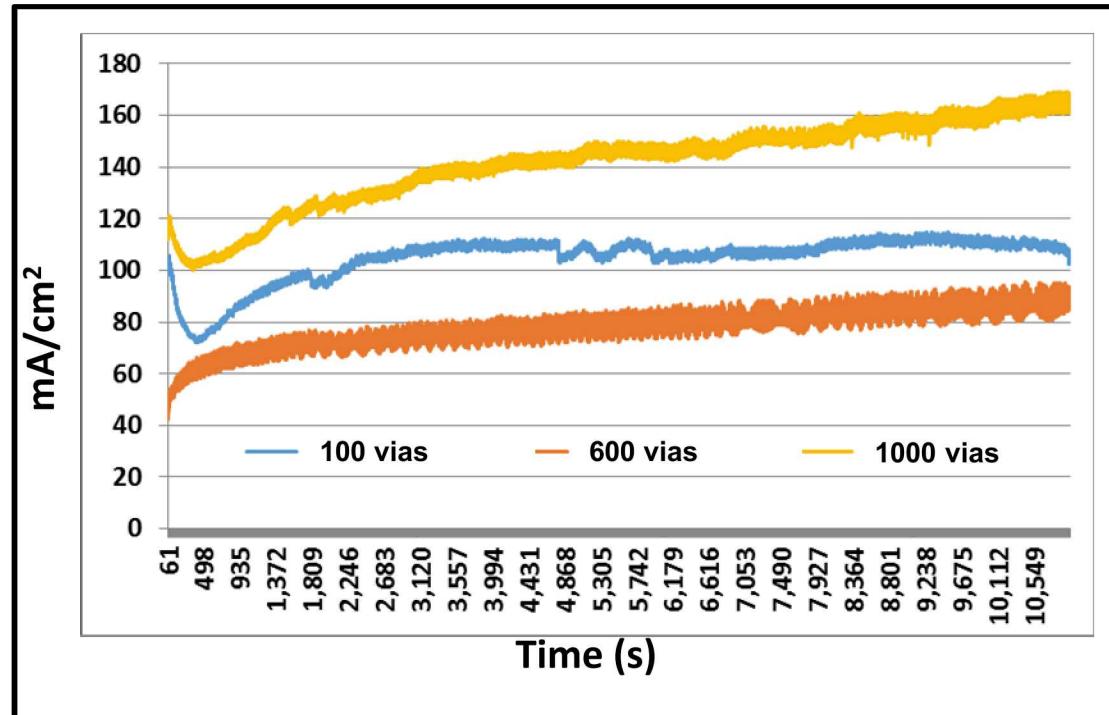
Phase 1: Potentiostatic TSV Filling



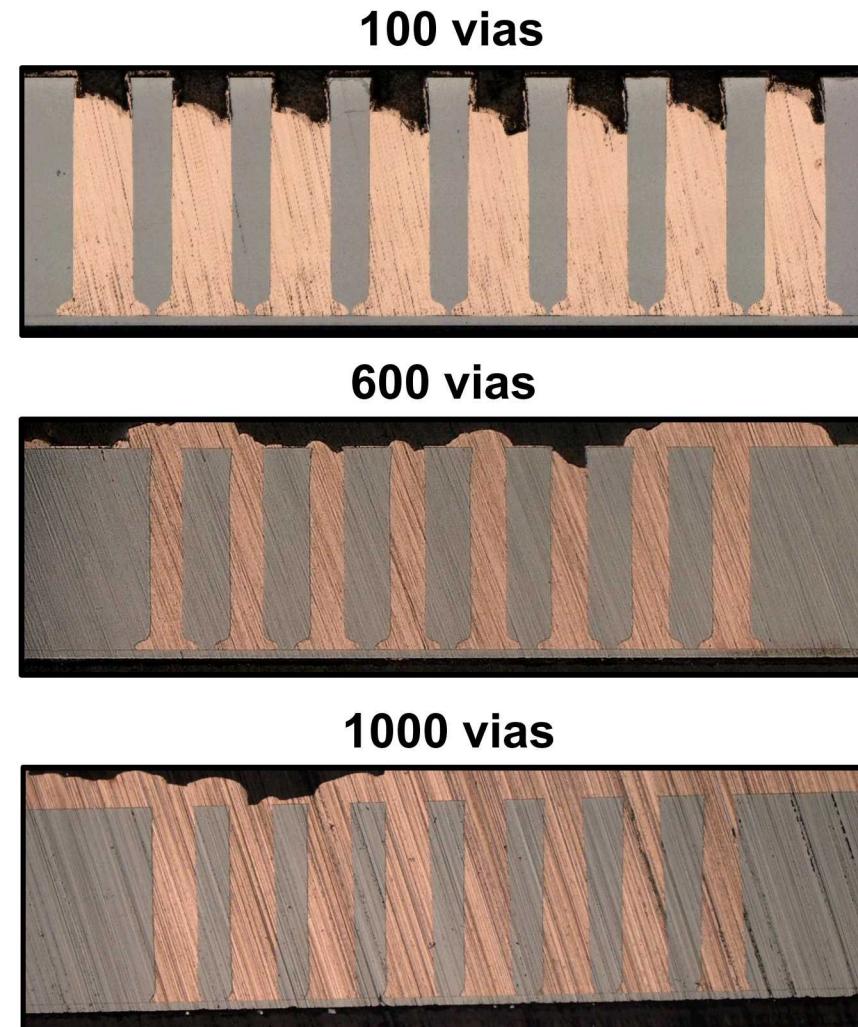
- Reference electrode use to finely tune applied potential
- Filling results are highly sensitive to applied voltage
- ~20mV window to obtain void free filling



Determining a Range of Current Densities to Investigate



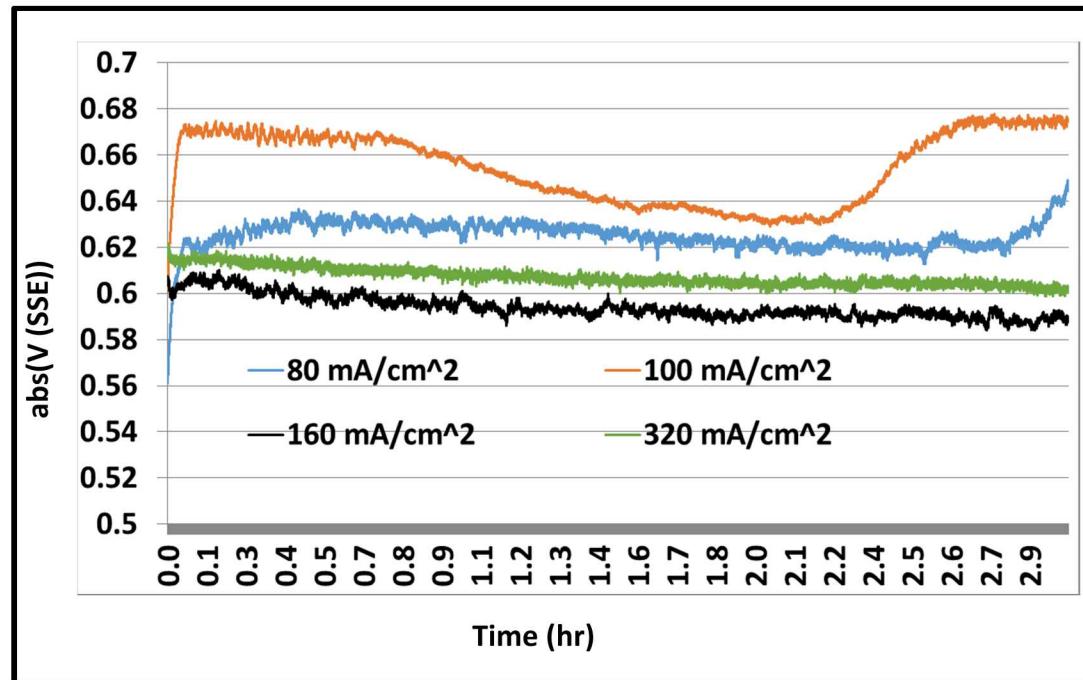
-0.64 V(SSE), 400 rpm, 50 μ M TET701



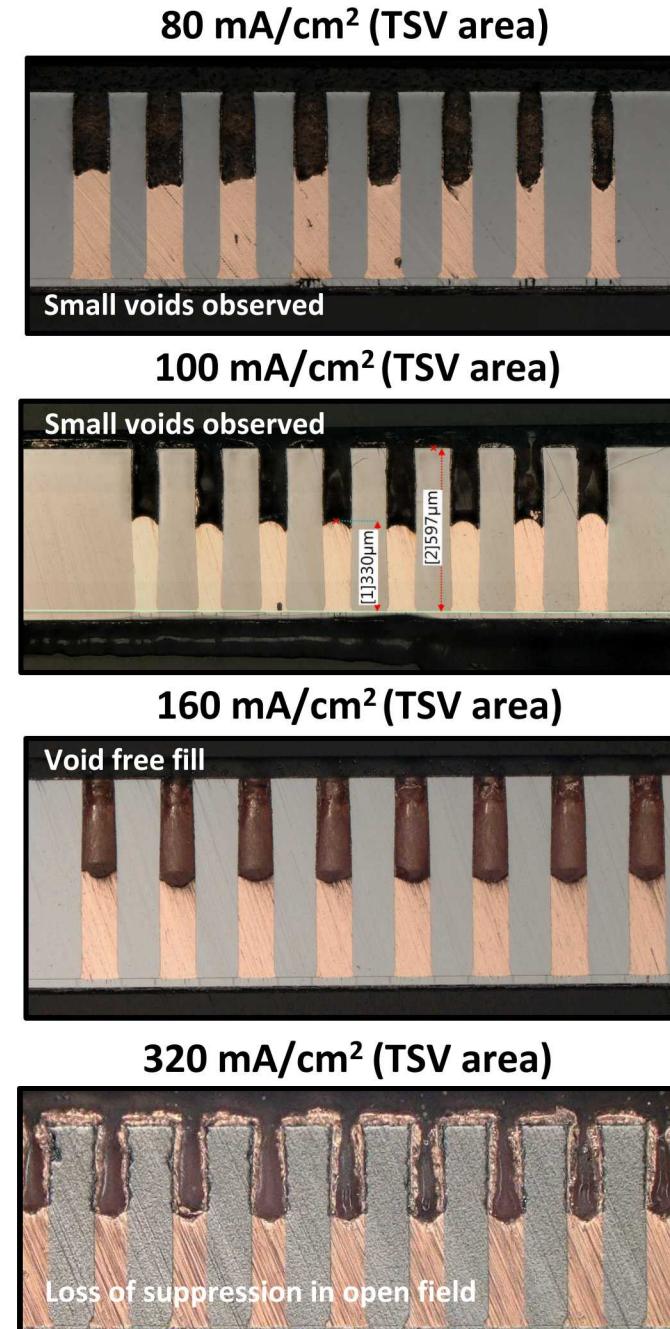
- Resultant current does not scale consistently with increasing area
- Data used to establish a range of current densities to investigate

Galvanostatic TSV Filling

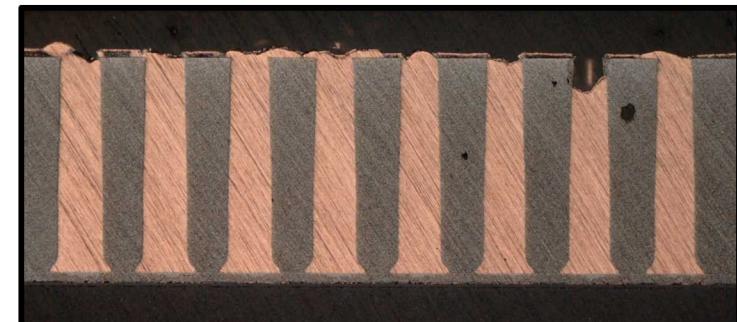
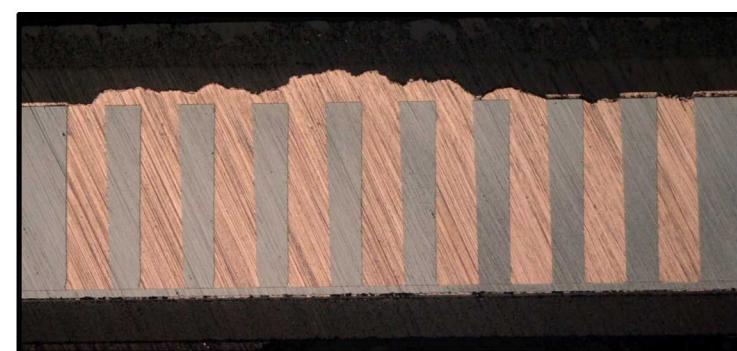
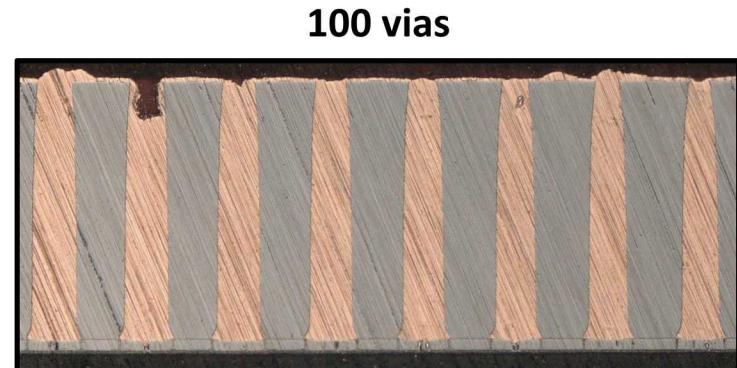
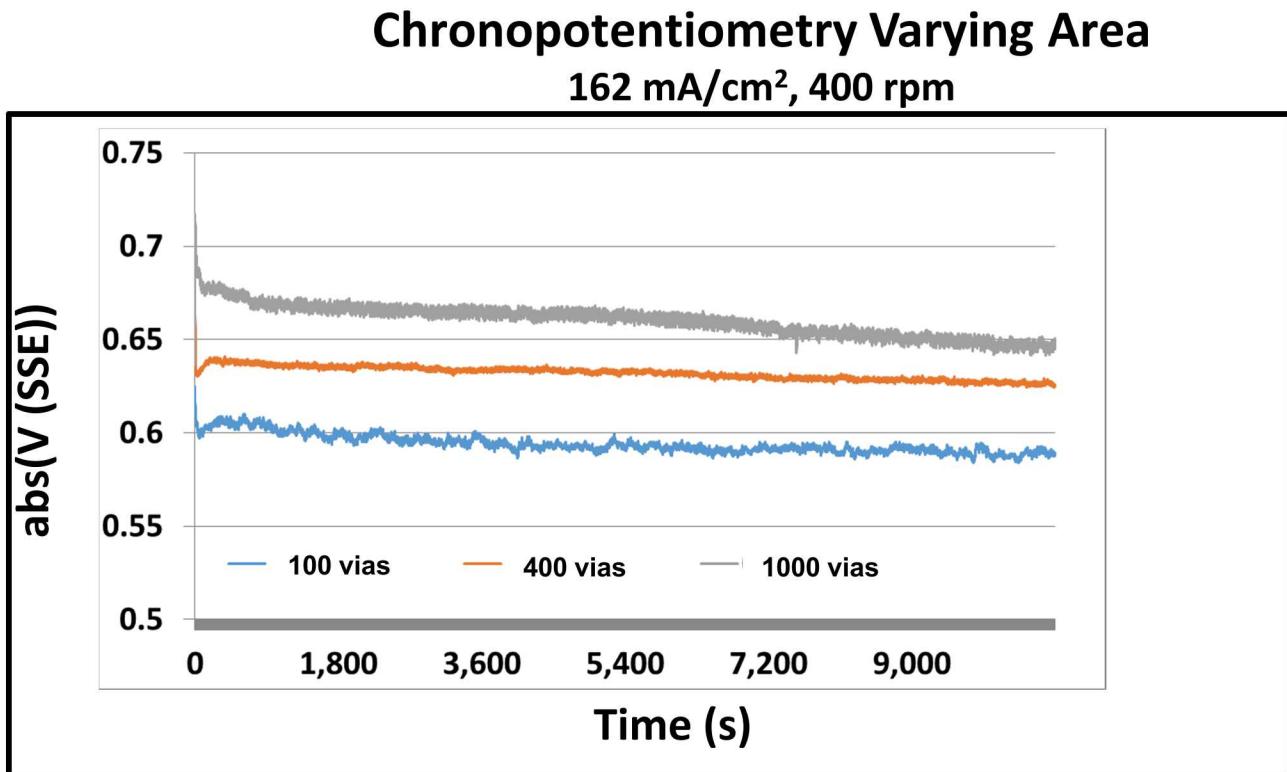
Chronopotentiometry at Various Current Densities



- Potential varies to accommodate applied current
- Electroactive vs total conducting surface
- Voltage does not scale consistently with increased current
- Galvanostatic plating dynamically adjusts for changes in suppressor breakdown



Scaling Current Controlled Deposition

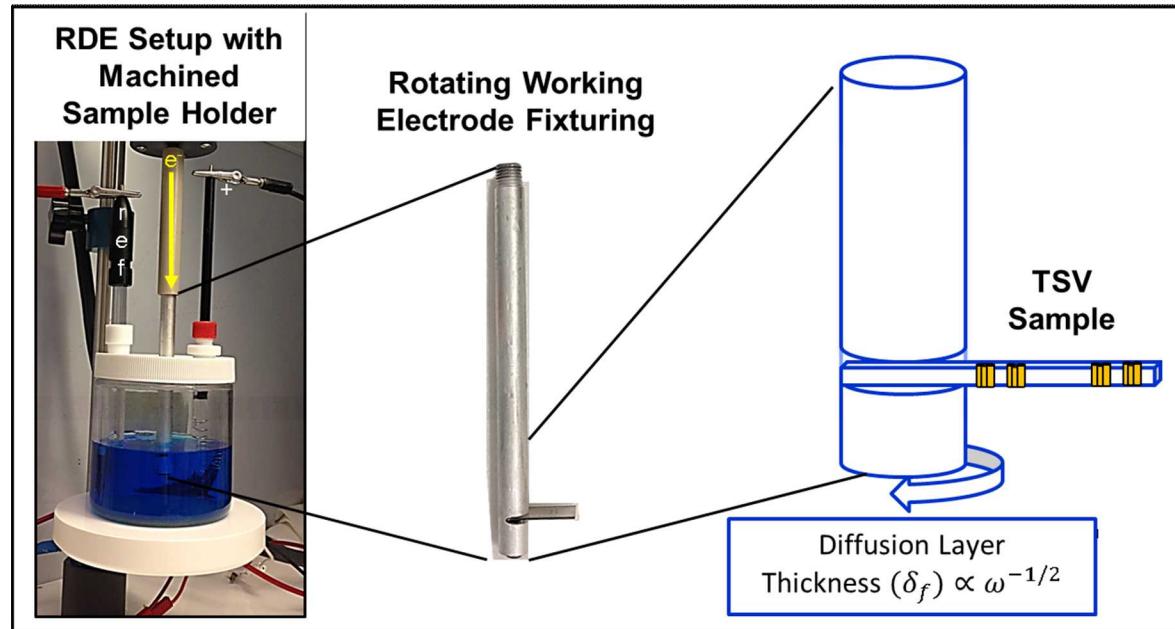


- Void free galvanostatic filling in a variety of sample sizes demonstrated
- Ongoing work focused on scaling this from die level filling to full wafer TSV filling

Scaling Current Controlled Deposition

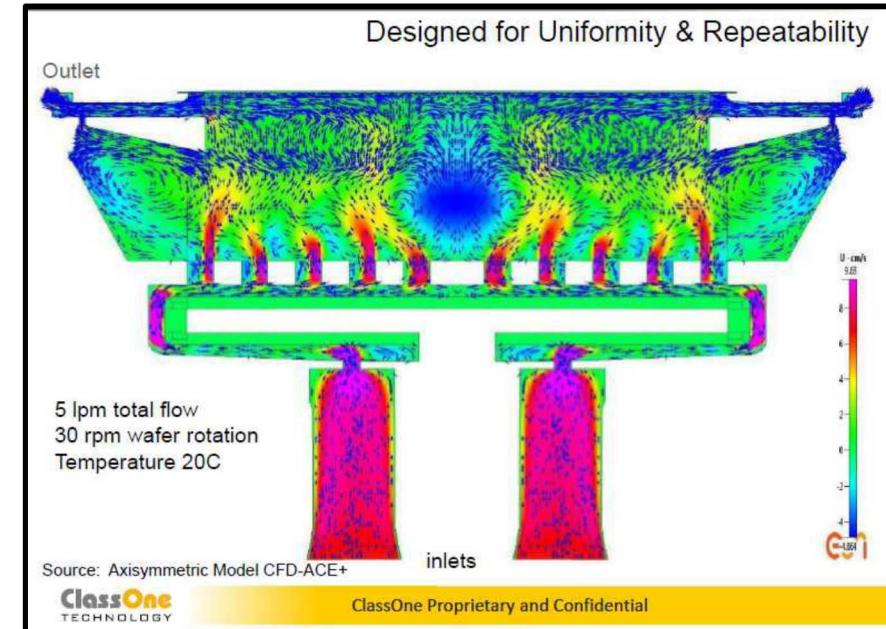


Die Level Fluid Dynamics Control



- Sample rotated in stagnant solution
- Change in RPM changes fluid replenishment in the TSVs

Production Tool Fluid Dynamics Control

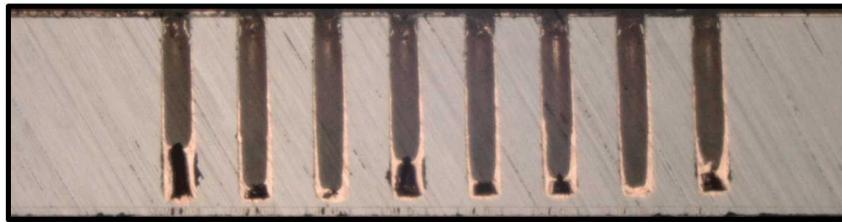


- Full wafer rotation
- Fountain style solution replenishment
- Baffled showerhead for controlling uniformity

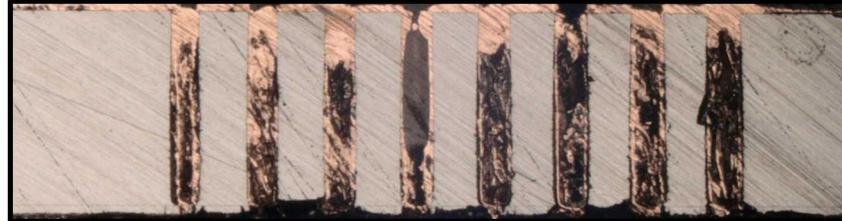
Solution Replenishment Modeling



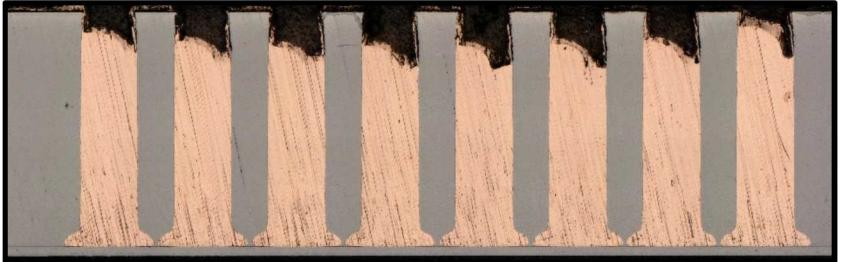
50 RPM



200 RPM

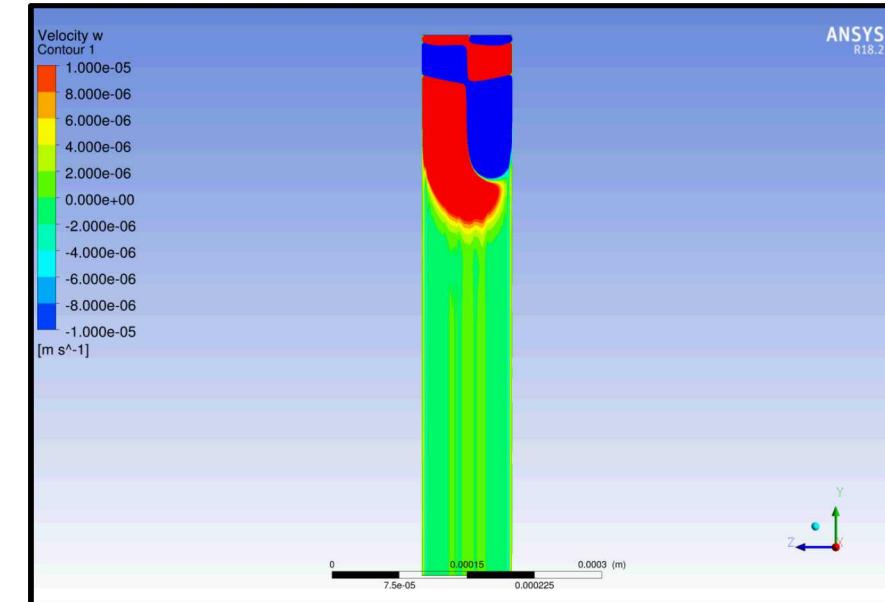


400 RPM



Solution replenishment across a 150 mm is radially dependent on the position of the vias

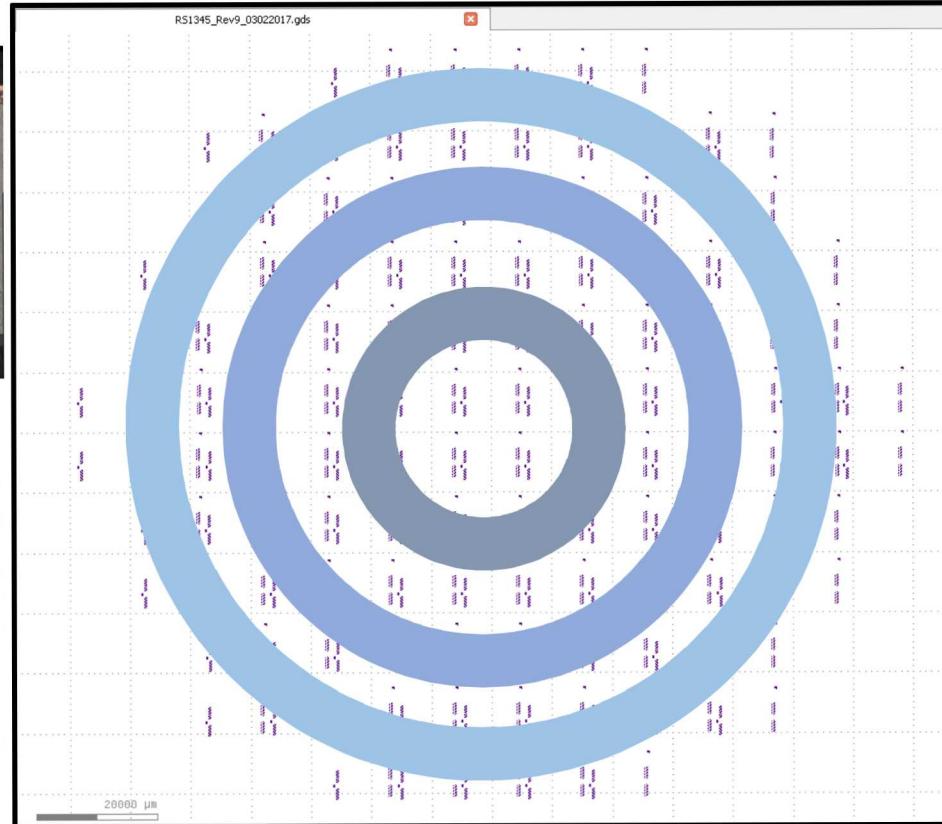
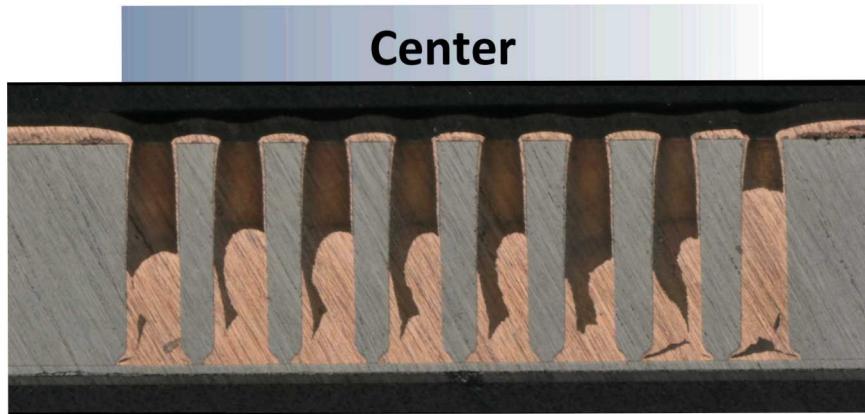
400 RPM CFD Model



- **Ansys fluid dynamics modelling**
- **There is almost no flow about halfway down the channel**
- **Asymmetry noticed during filling experiments**

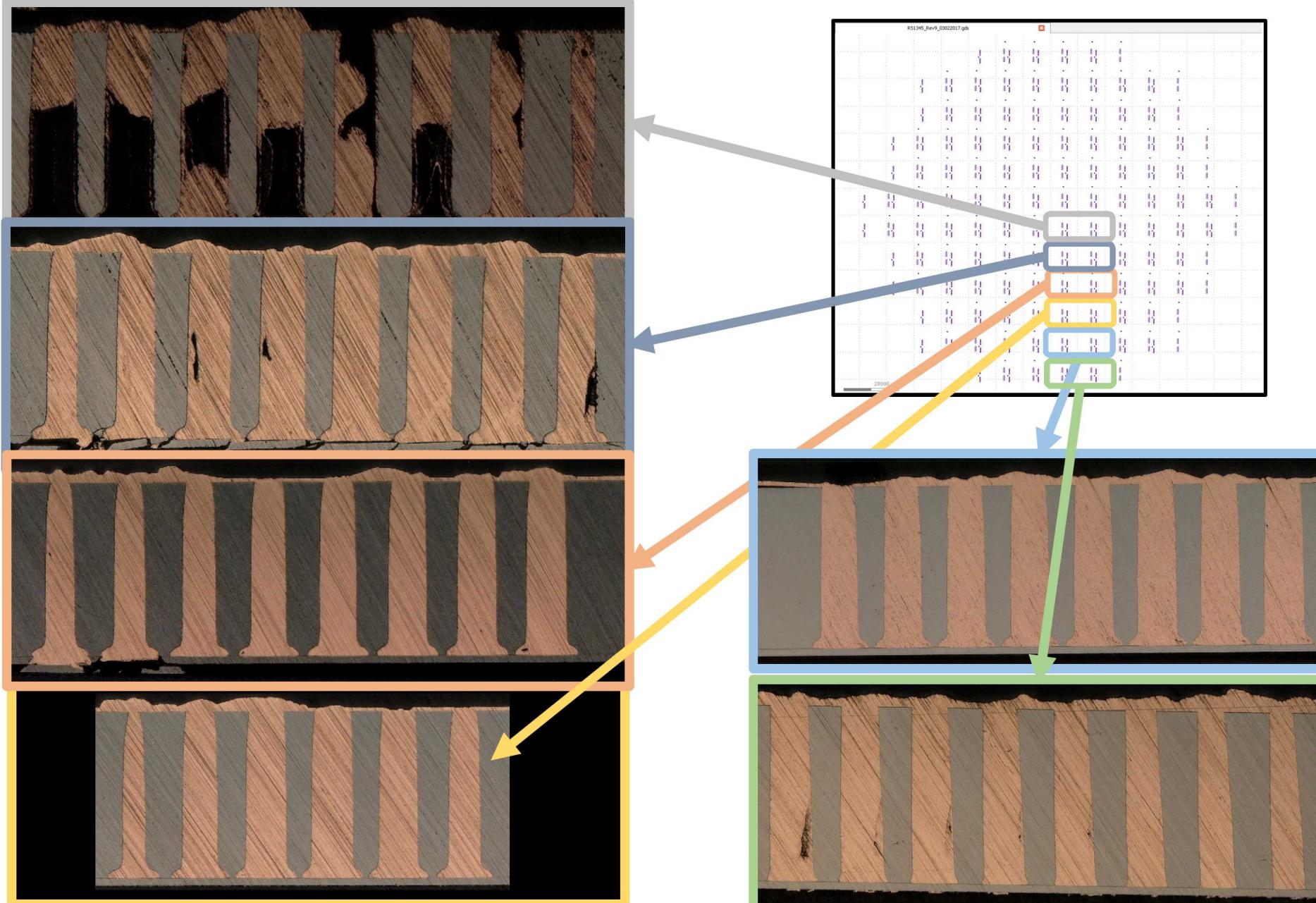
Filling result are highly dependent on fluid dynamics and solution replenishment

Increased Current Density: Void Free Filling



Void free filling except center wafer
Investigating :
Fluid flow
Center current density

Full Thickness Deposition Across 150 mm Wafer

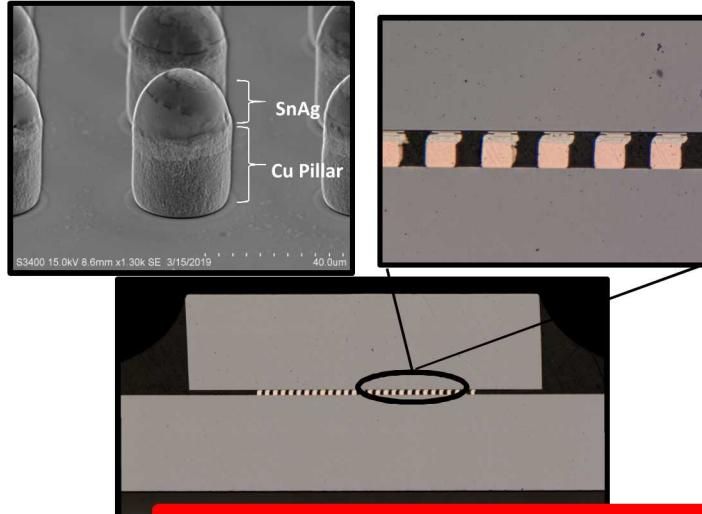




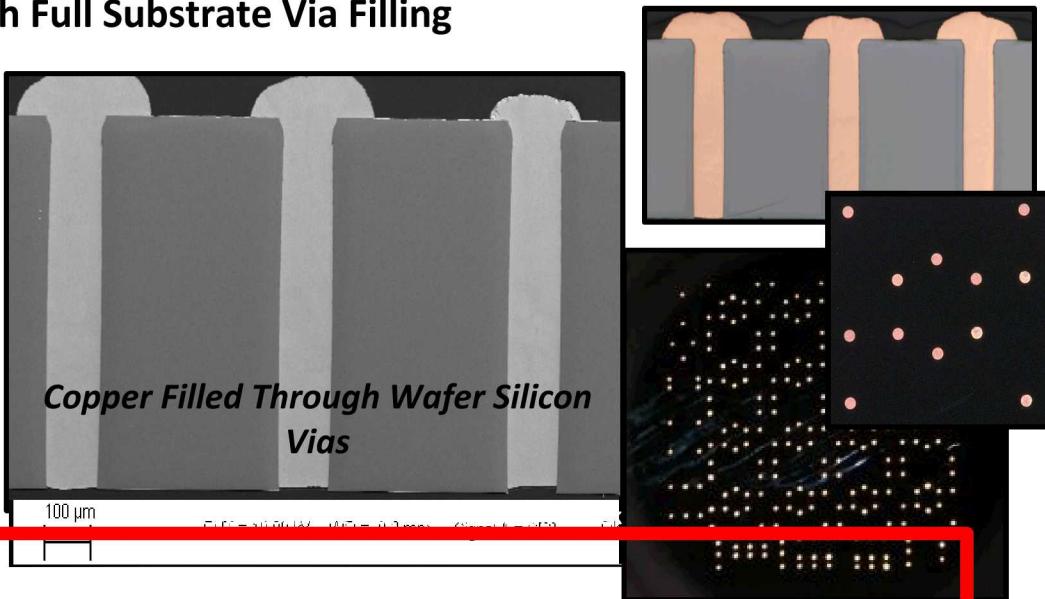
- 1. Perform scaling experiments towards full wafer plating**
- 2. Investigate different diameter TSVs**
- 3. Post plating integration**
 - **CMP development**
 - **Cu Pumping**
 - **Flip chip bonding**
- 4. Chemistry lifetime experiments**
 - **Suppressor precipitation onto Cu anode**
 - **Suppressor depletion vs A-min**

Mesoscale Fabrication – Forming, Filling, and Coating

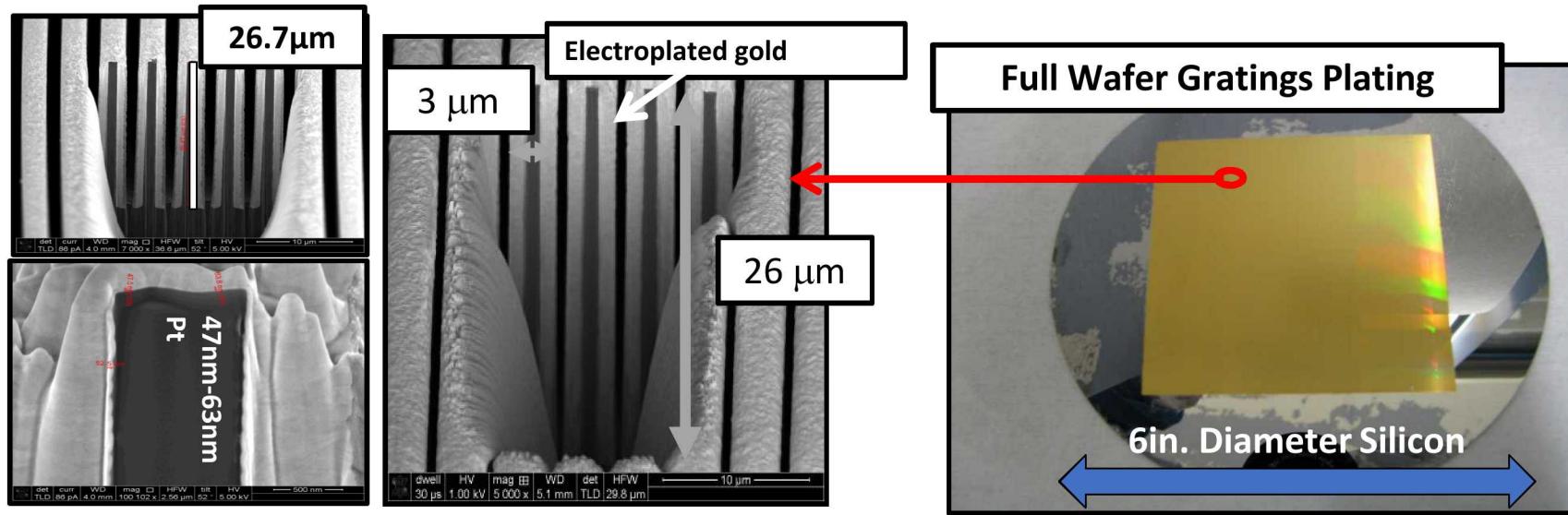
Forming Cu Pillar μ -Bumps



Through Full Substrate Via Filling



Precision Electro-coating



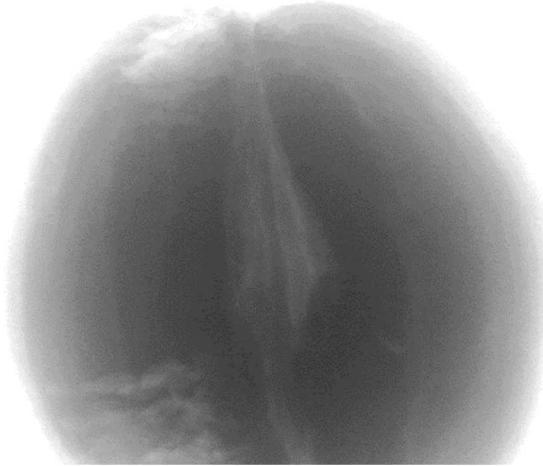
Conventional X-ray vs XPCI



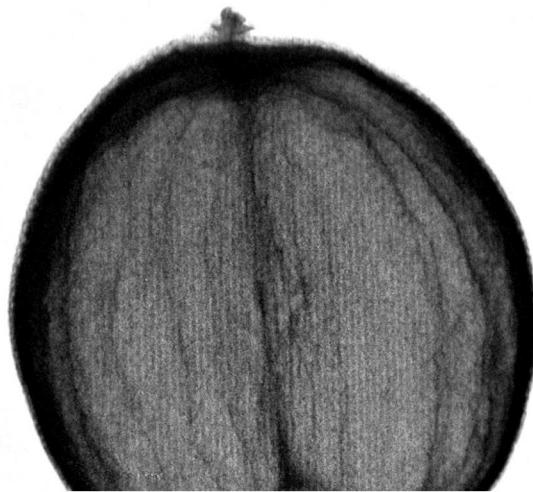
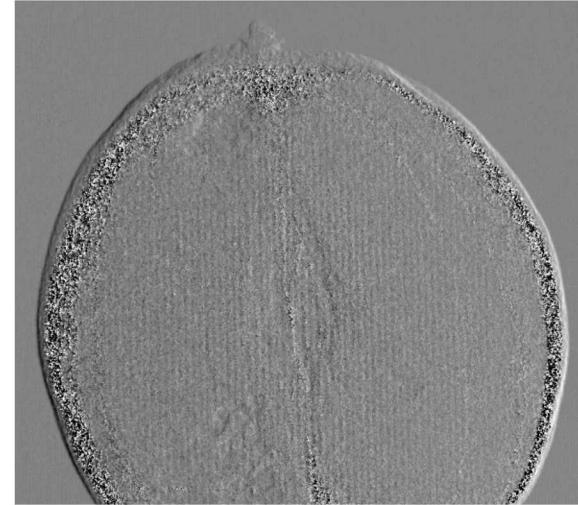
Orange



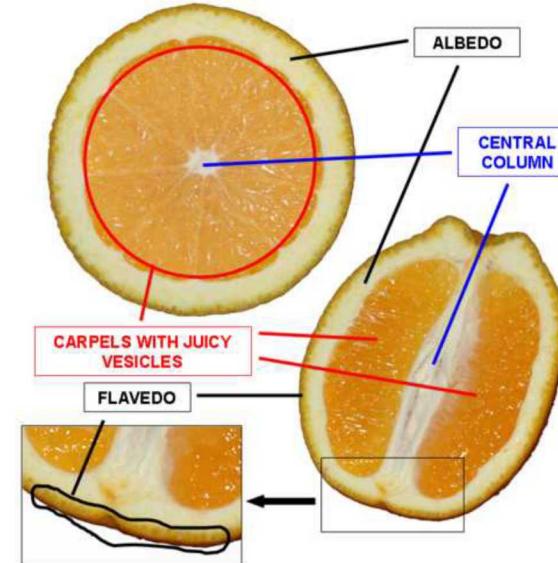
Absorption



Phase contrast



Dark field



Chicken Wing



Absorption



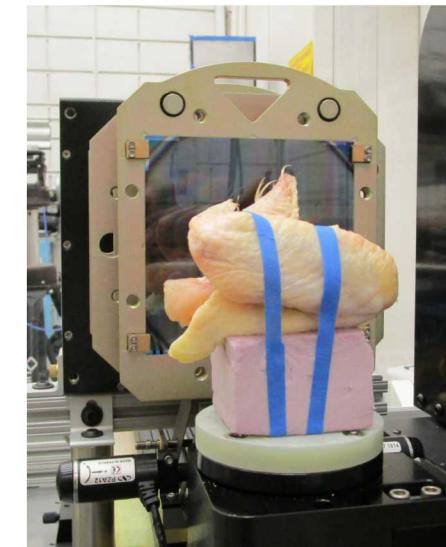
Phase contrast



Dark field



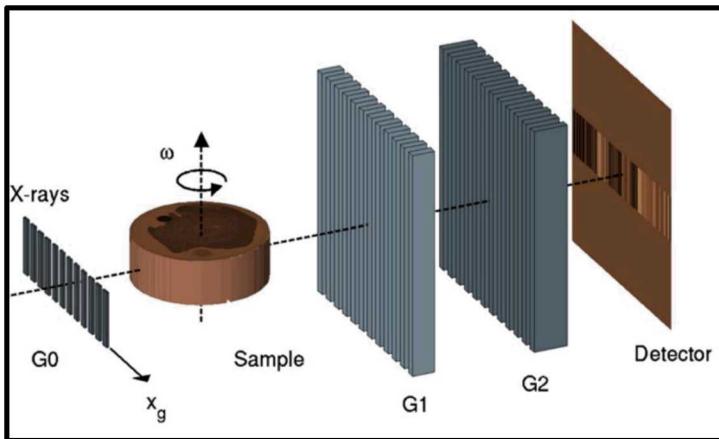
Combined



X-Ray Phase Contrast Imaging (XPCI)



Method	working principles	setup scheme	measured phase quantity	PROS	CONS	
Crystal interferometer	beam splitting and recombining crystals (Si)		phase ϕ	<ul style="list-style-type: none"> • highest phase sensitivity 	<ul style="list-style-type: none"> • mechanical instability • monochromatic (synchrotron) • limited FOV (crystals) • low efficiency 	
Analyzer based interferometer	bragg reflection		phase gradient $\nabla\phi$	<ul style="list-style-type: none"> • high phase sensitivity 	<ul style="list-style-type: none"> • monochromatic (synchrotron) • low efficiency 	
Grating based interferometer	grating interference		phase gradient $\nabla\phi$	<ul style="list-style-type: none"> • good phase sensitivity • polychromatic • large FOV • high efficiency 	<ul style="list-style-type: none"> • requires gratings 	
Propagation based interferometer	Free space Fresnel propagation		Laplace of phase $\Delta\phi$	<ul style="list-style-type: none"> • simple design • polychromatic 	<ul style="list-style-type: none"> • requires high-res detector • low phase sensitivity • low efficiency 	



Talbot-Lau Interferometer

G0 – Source Absorption Grating

Creates an array of individually coherent but mutually incoherent sources

G1 – Phase Grating

Creates zero and π phase shifts to form an interference pattern at G2 plane

G2 – Analyzer Absorption Grating

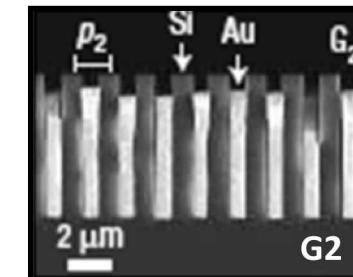
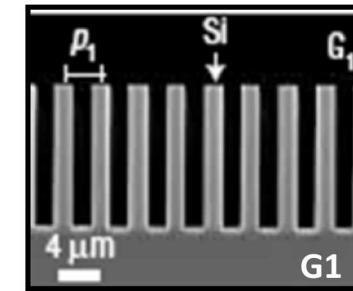
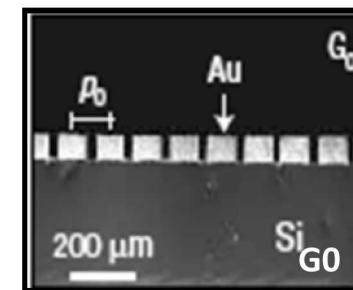
Modulate the interference signal on detector (local fringe position \rightarrow single intensity variation recorded by detector)

$$n = (1 - \delta) + i \cdot \beta$$

$\beta \rightarrow$ Absorption $\delta \rightarrow$ Phase

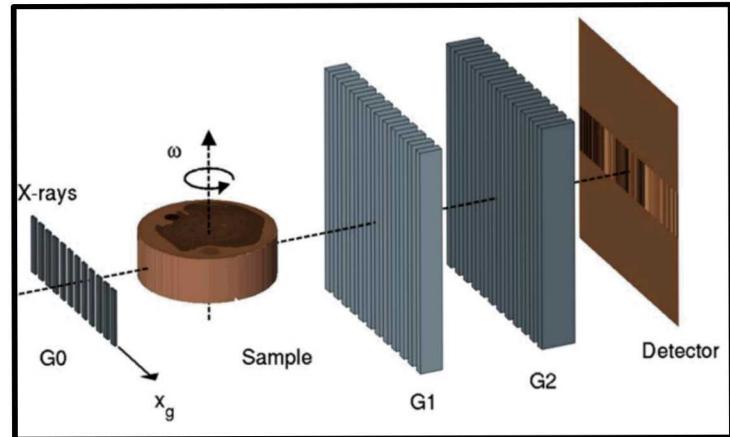
$$\delta/\beta \approx 10^3$$

Phase imaging is $\sim 10^3$ times higher sensitivity than absorption imaging



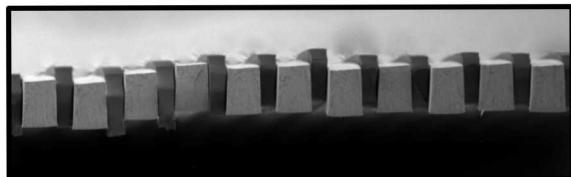
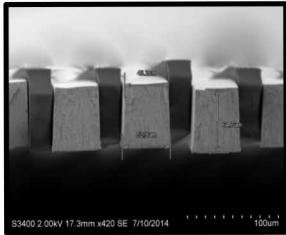
Sandia's Three Grating XPCI System

28 keV System

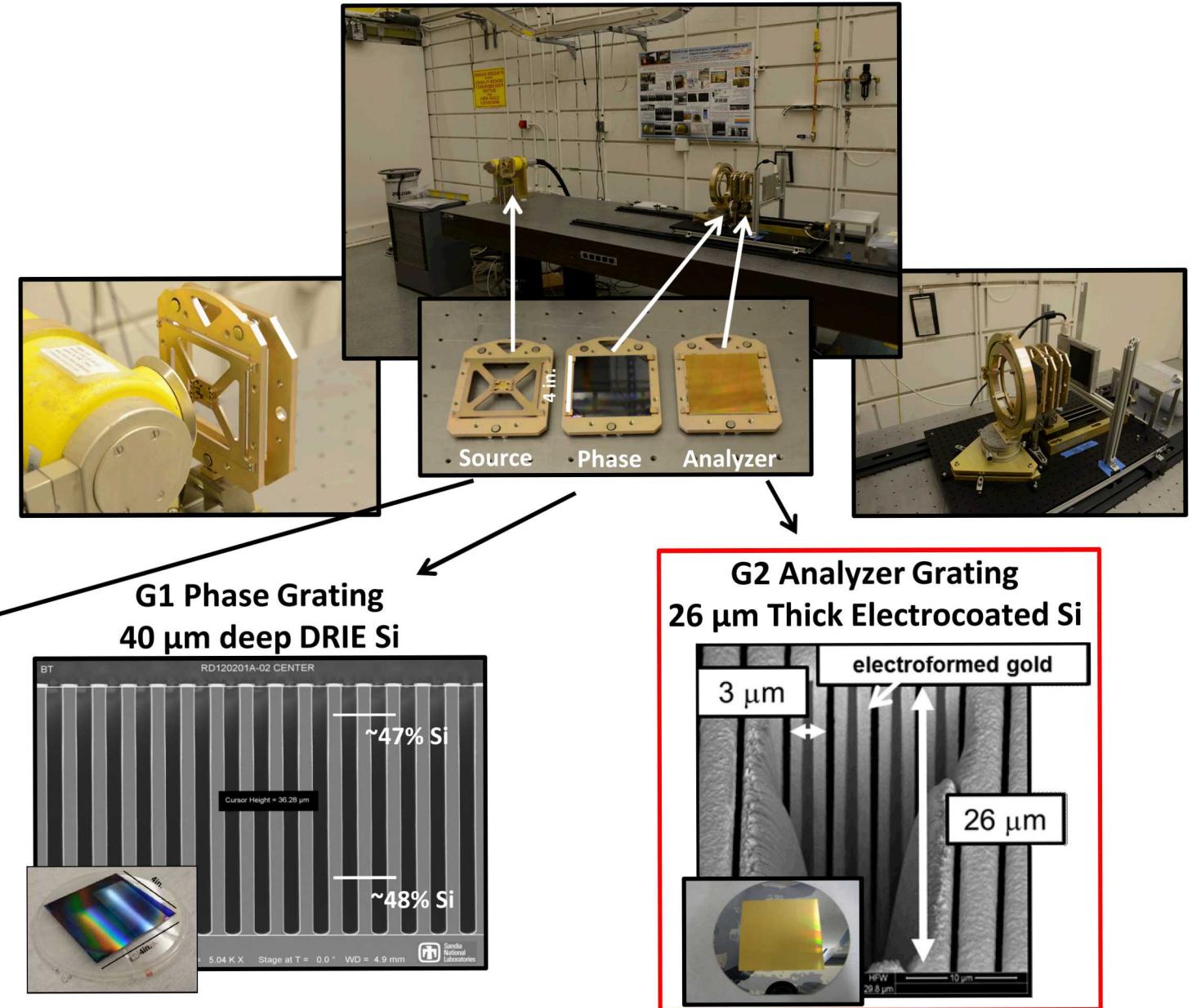


Talbot-Lau Interferometer

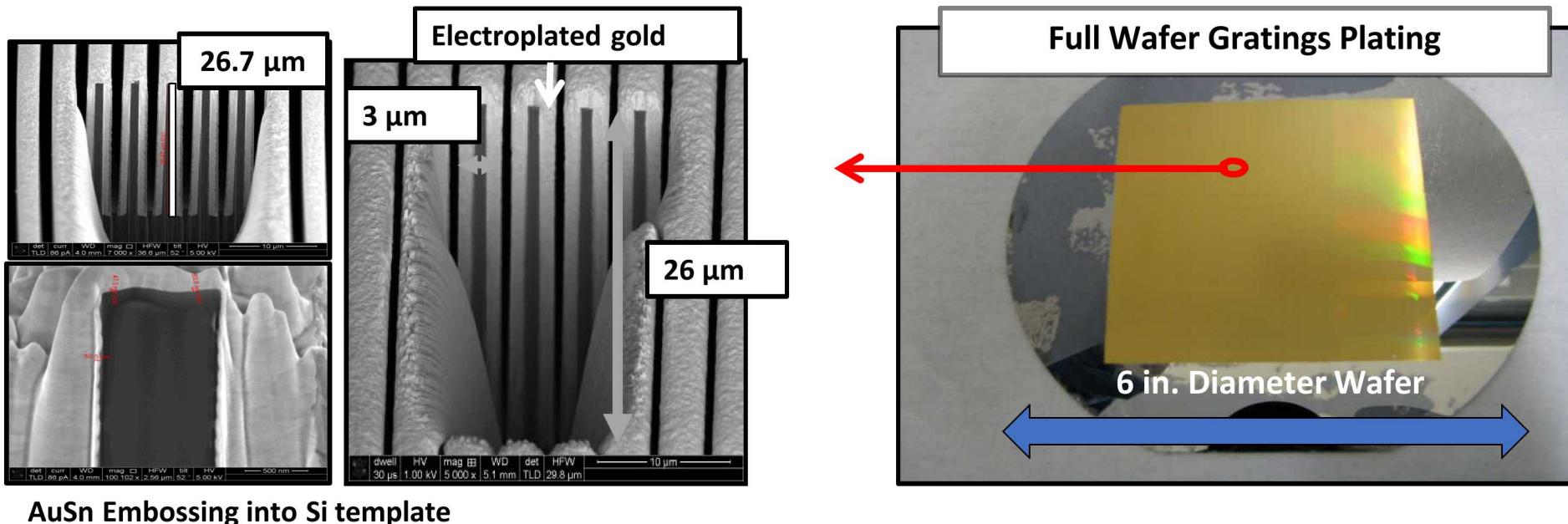
G0 Source Grating
65 μm Thick Au



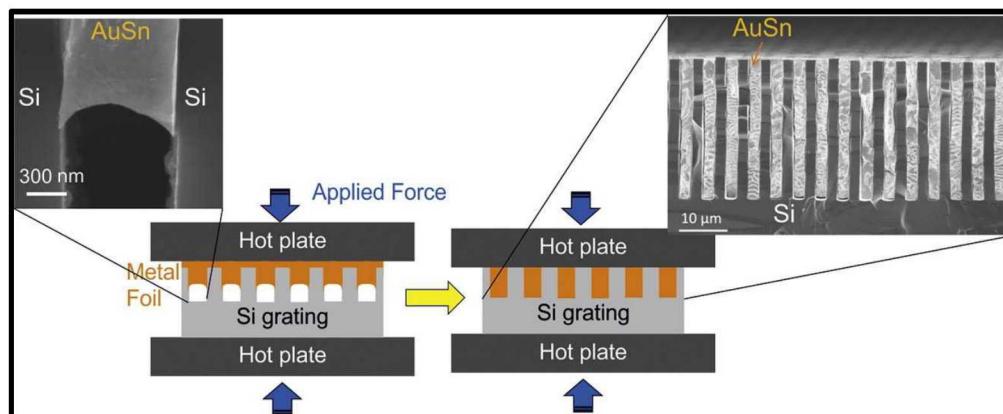
Delamination result of cross-section



Precision Electro-coated Si Gratings



AuSn Embossing into Si template



L. Romano et. al. Microelectronic Engineering 176(2017) 6-10

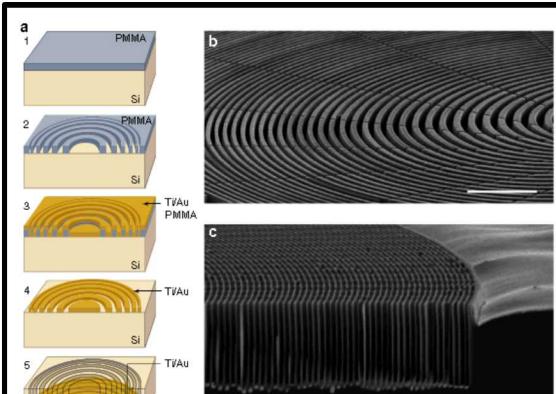
- **Cost effective material**
- **Less sensitive filling mechanism than electro-coating**
- **High uniformity is feasible with full wafer bonding tools**

Increasing the aspect ratio of our Si template will allow less expensive gratings to be fabricated at current x-ray energies or alternatively allow higher energy XPCI systems with the ECD Au approach

Alternative Etch/Molding Techniques for Increasing Aspect Ratio

Metal Assisted Chemical Etching (MACE)

C. Chang et. al., 10.1038/nocmms5243



LIGA Fabricated Gratings

T. Schroter et. al., J. Micro/Nanolith. MEMS MOEMS 16(1), 013501 (2017)

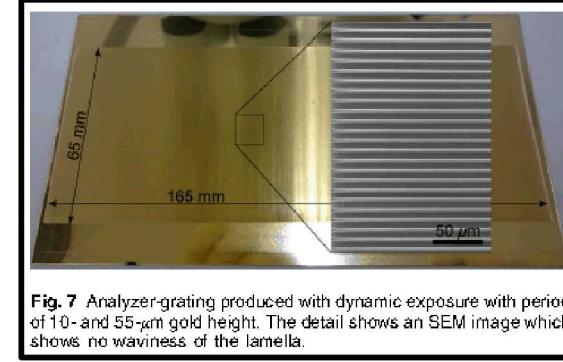
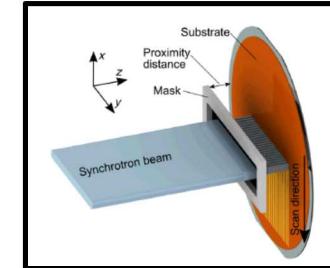
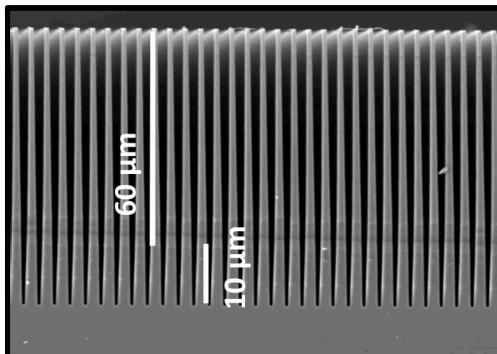


Fig. 7 Analyzer-grating produced with dynamic exposure with period of 10- and 55-μm gold height. The detail shows an SEM image which shows no waviness of the lamella.

In order to achieve higher energy XPCI systems we need to investigate alternative molding techniques or determine a way to accurately align multiple gratings

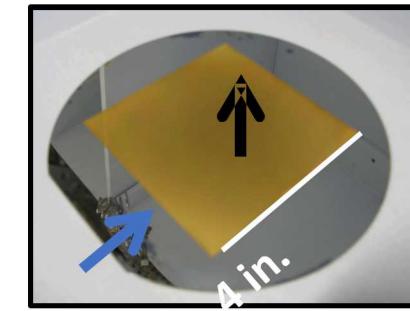
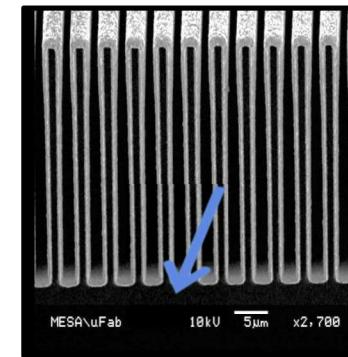
Deep Reactive Ion Etching



- 30:1 aspect ratios for etched features
- 60:1 aspect ratios for remaining features
- Very large field of view

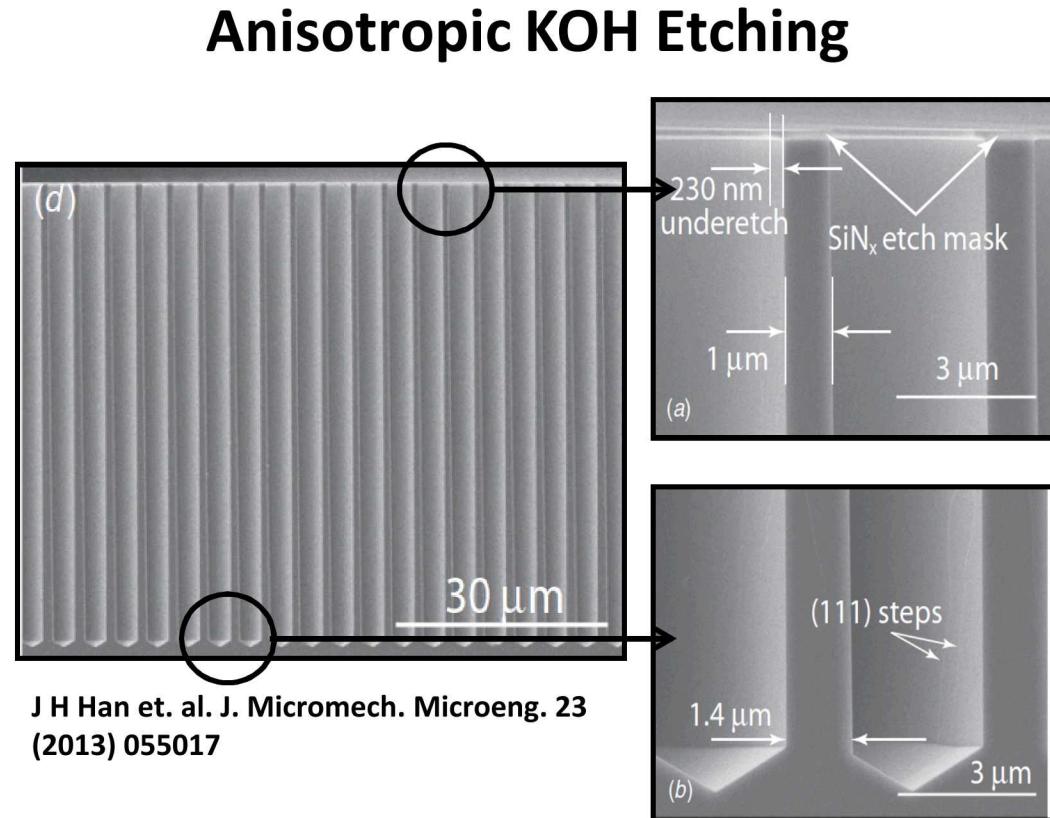
Standard x-ray k-vector

Alternative x-ray k-vector



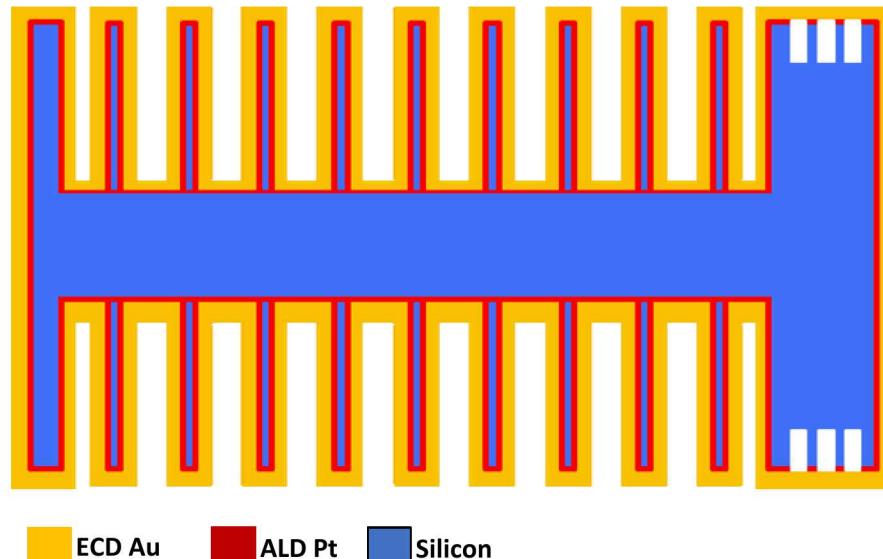
- Effective aspect ratio increases to 100,000:1
- Decreases field of view from 10 cm x 10 cm down to 50 μm x 10 cm

Increase Effective Aspect Ratio of Gratings



- 600:1 etch selectivity b/t [110] and [111] planes
- Very large field of view

Front to Backside Alignment

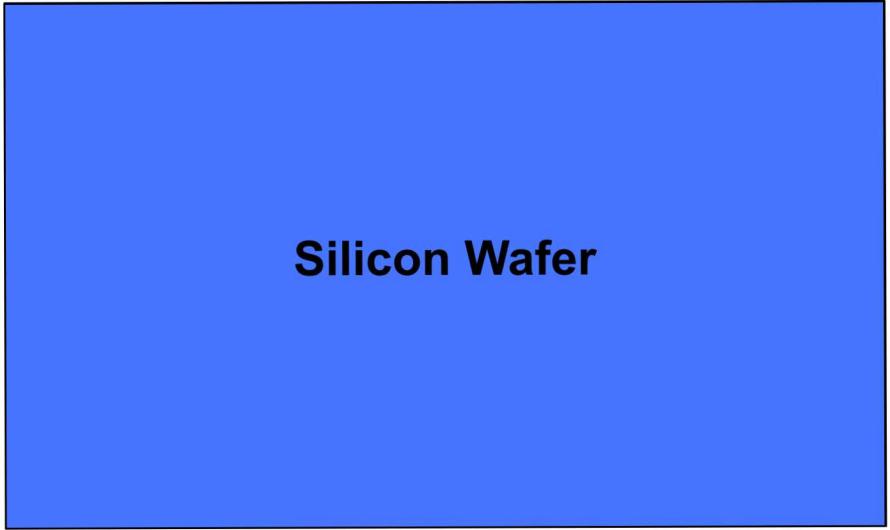


- Creates an effective aspect ratio that is twice that of whichever molding techniques is used

Front to Backside Aligned Gratings



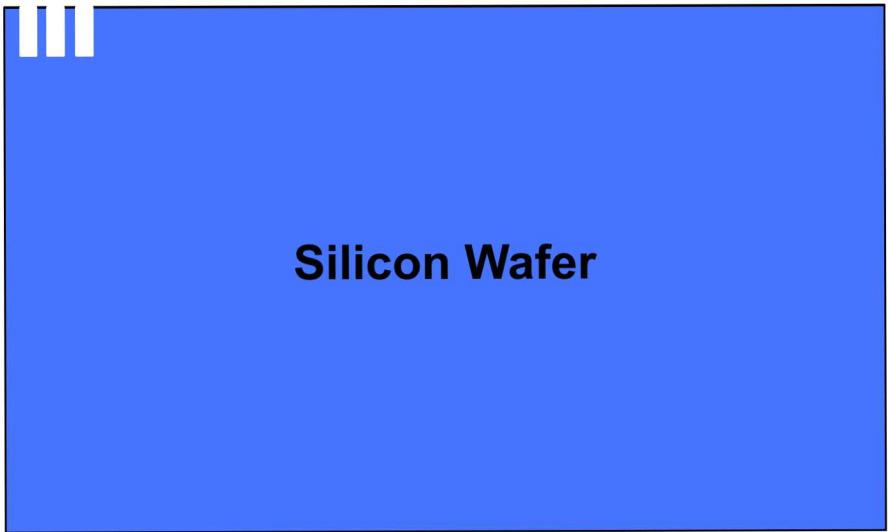
■ Silicon ■ ALD Pt ■ ECD Au



Front to Backside Aligned Gratings



■ Silicon ■ ALD Pt ■ ECD Au

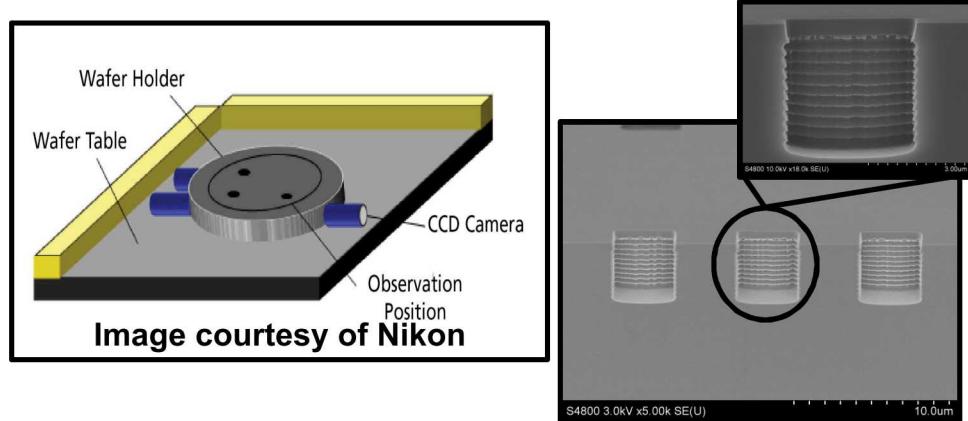


Front to Backside Aligned Gratings

■ Silicon ■ ALD Pt ■ ECD Au



Nikon Backside Field Image Alignment (BS-FIA)

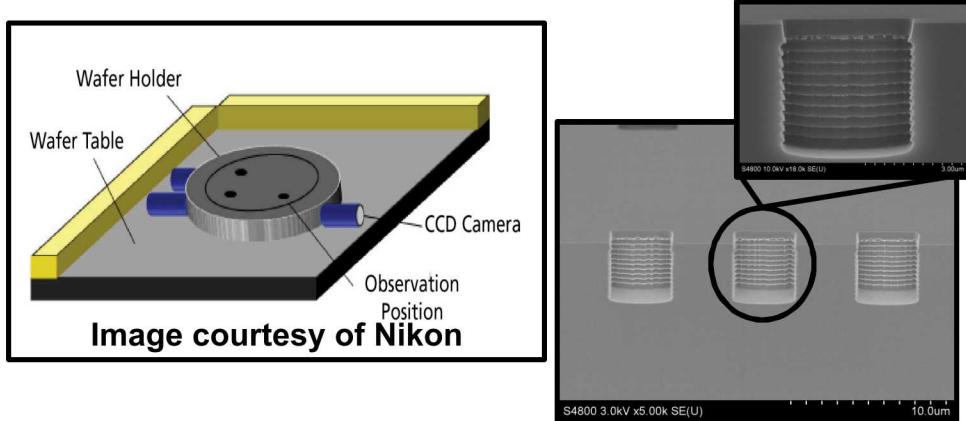


Front to Backside Aligned Gratings

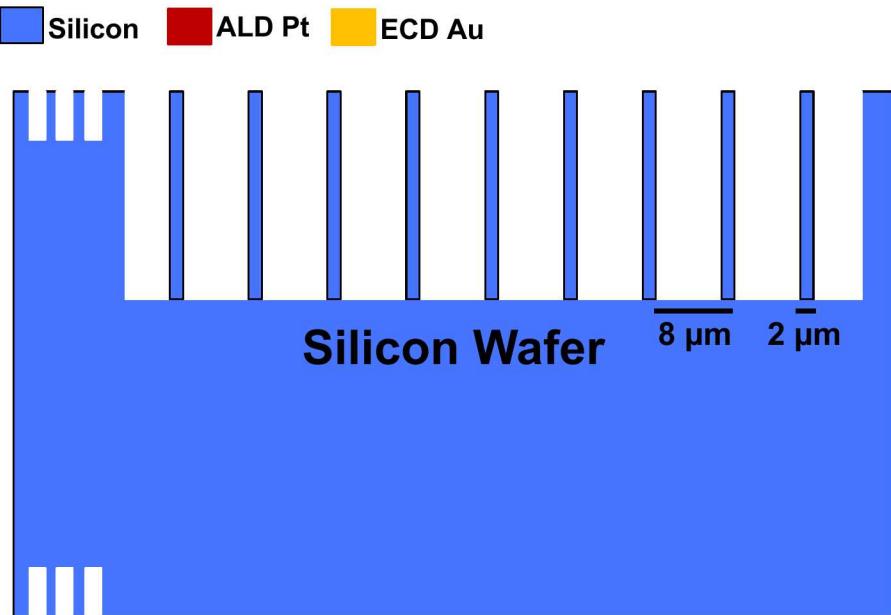
■ Silicon ■ ALD Pt ■ ECD Au



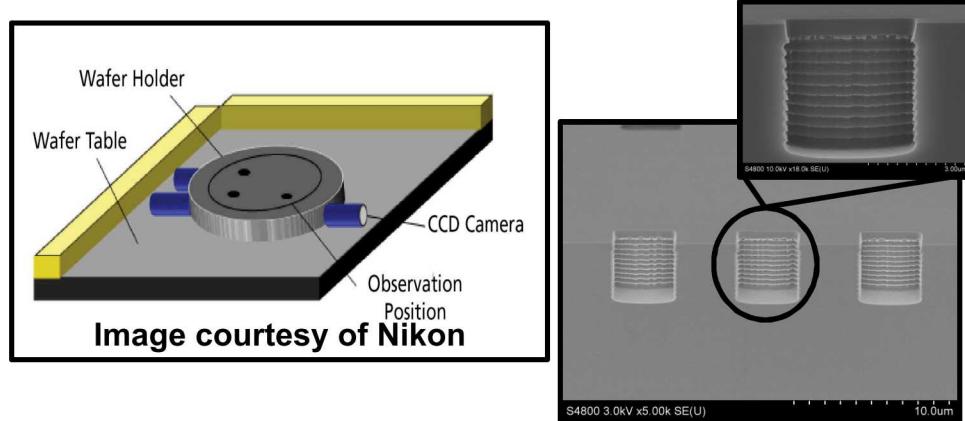
Nikon Backside Field Image Alignment (BS-FIA)



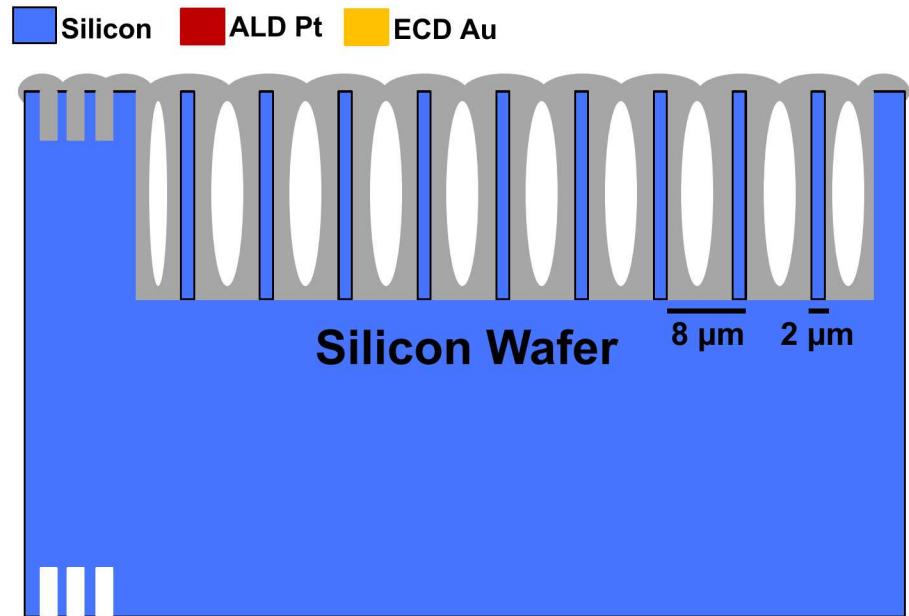
Front to Backside Aligned Gratings



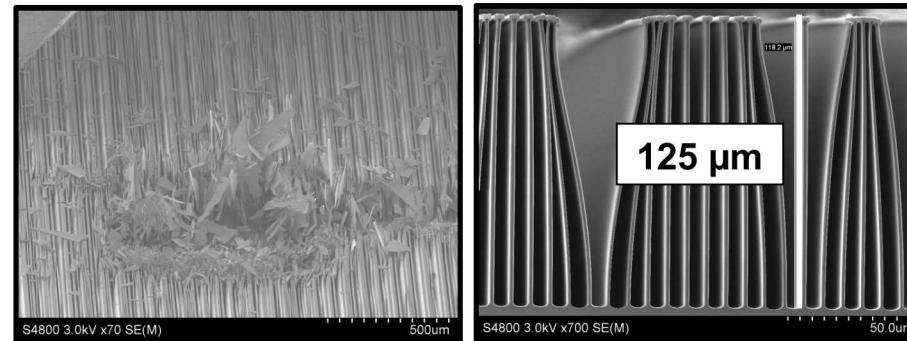
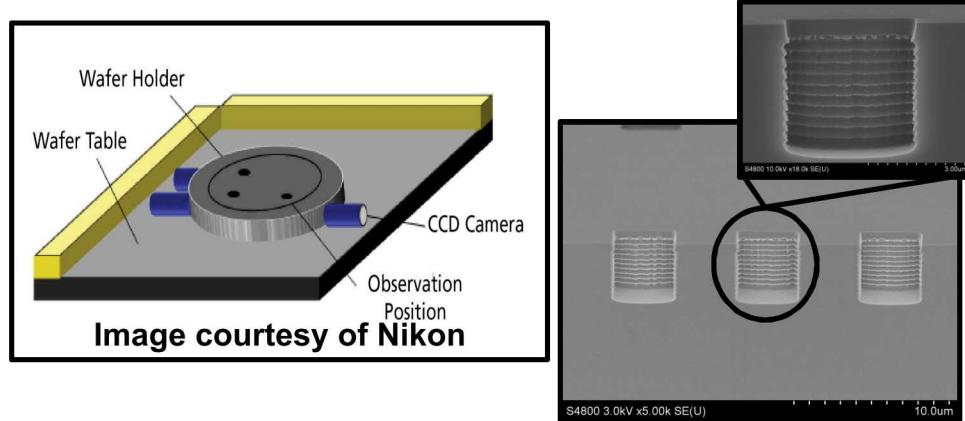
Nikon Backside Field Image Alignment (BS-FIA)



Front to Backside Aligned Gratings



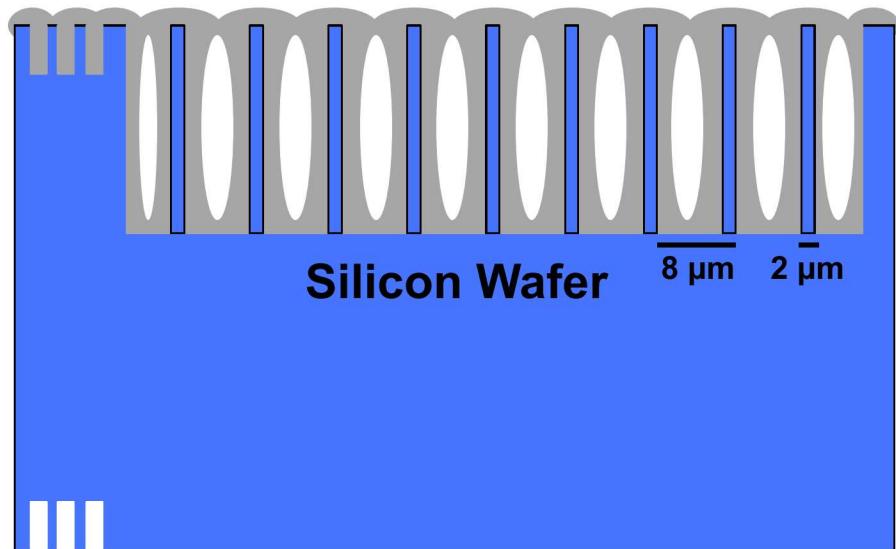
Nikon Backside Field Image Alignment (BS-FIA)



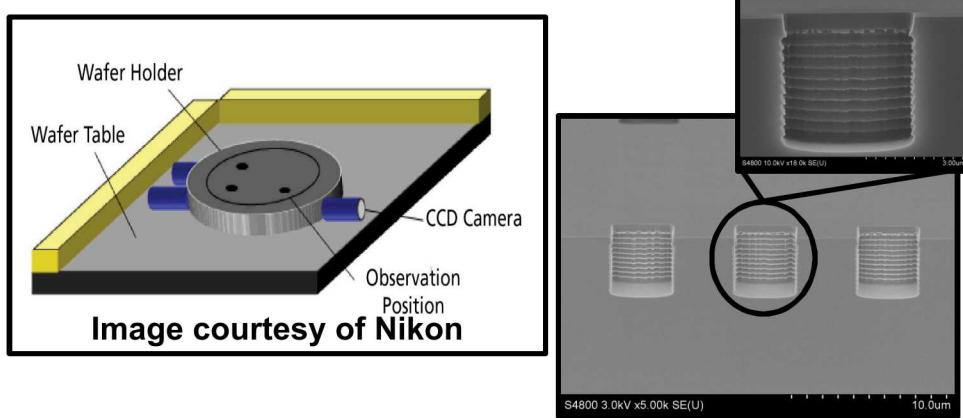
- **High aspect ratio Si features (> 60:1) are fragile**
- **Compressive stress from oxide deposition**
- **Surface tension forces**

Front to Backside Aligned Gratings

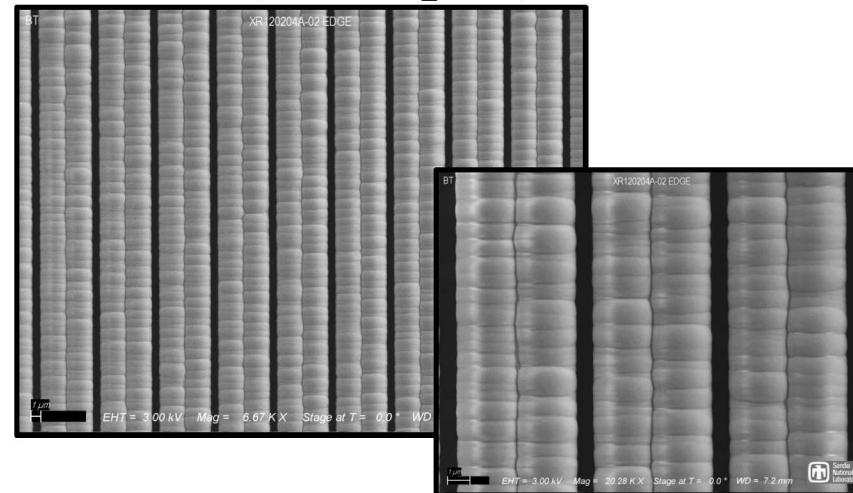
■ Silicon ■ ALD Pt ■ ECD Au



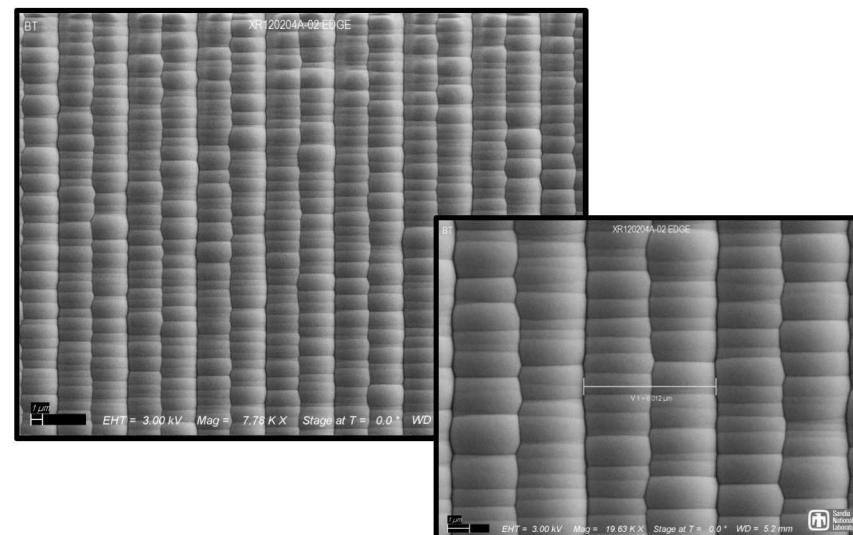
Nikon Backside Field Image Alignment (BS-FIA)



3 μm SiO₂ Deposition

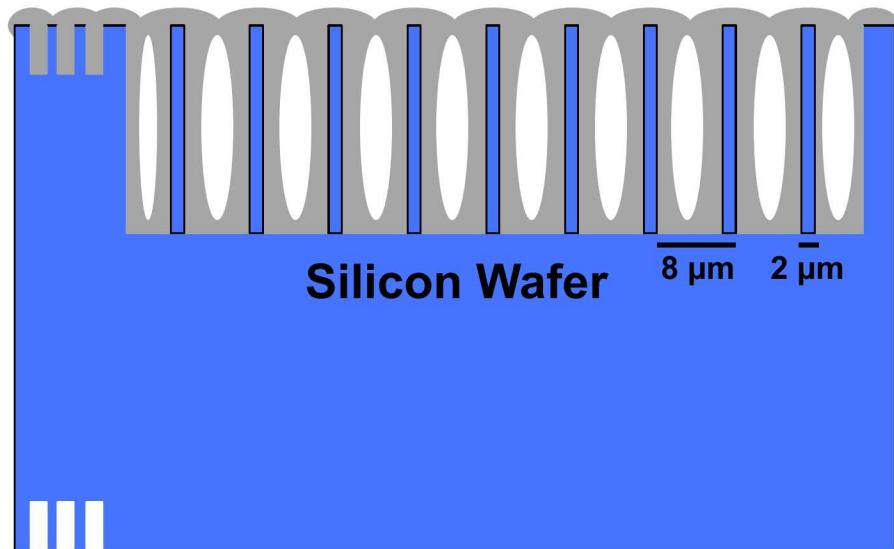


5 μm SiO₂ Deposition

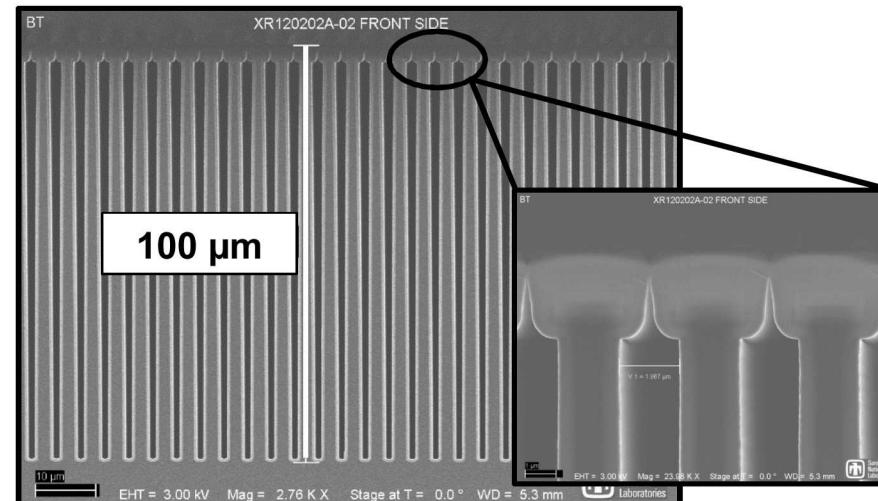


Front to Backside Aligned Gratings

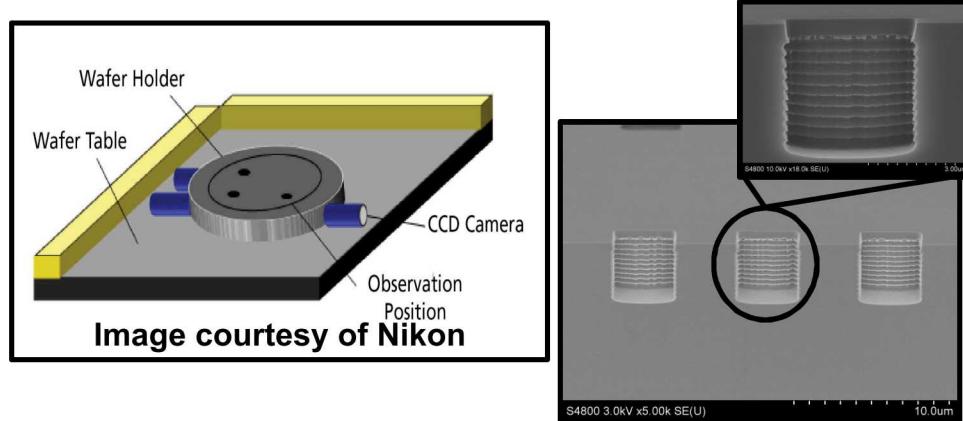
■ Silicon ■ ALD Pt ■ ECD Au



Oxide Coated Front Side Gratings

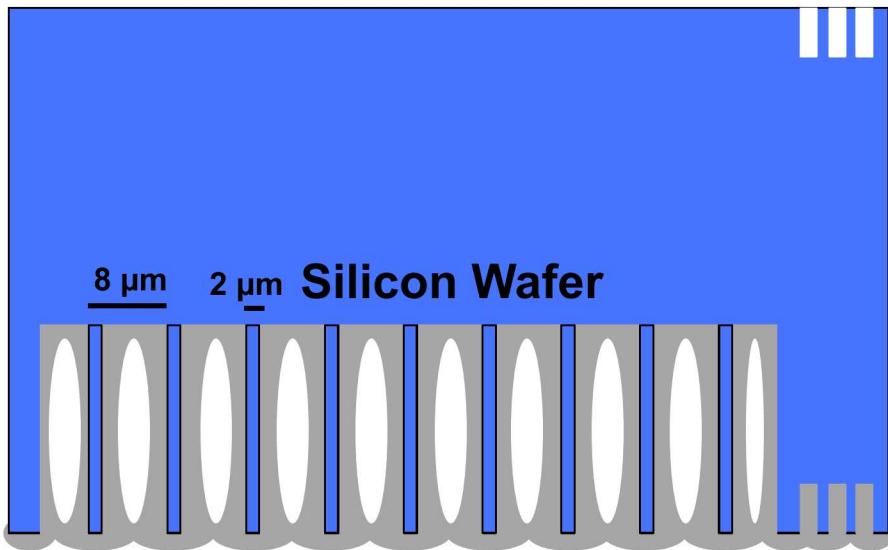


Nikon Backside Field Image Alignment (BS-FIA)

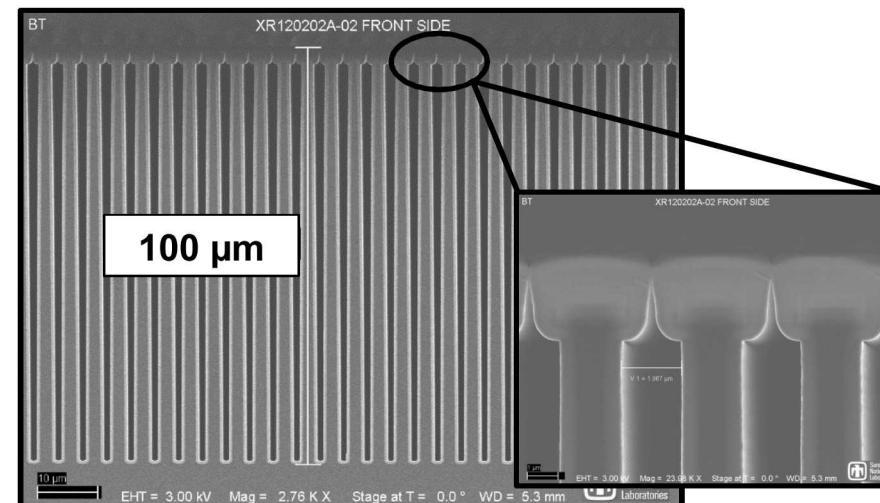


Front to Backside Aligned Gratings

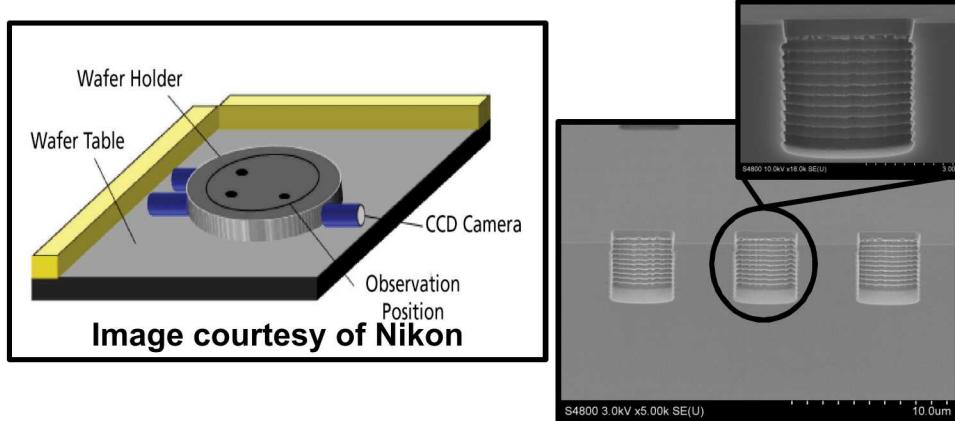
■ Silicon ■ ALD Pt ■ ECD Au



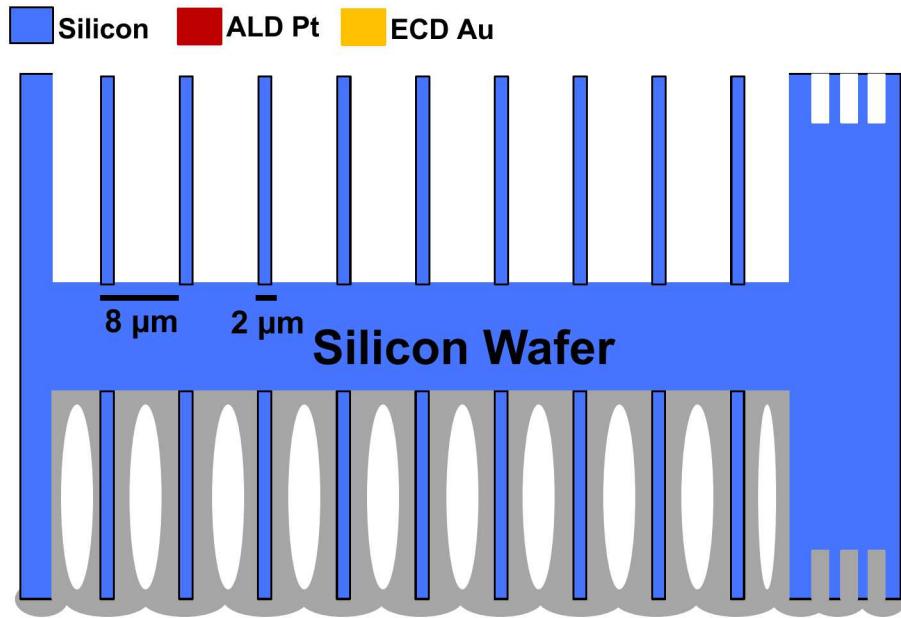
Oxide Coated Front Side Gratings



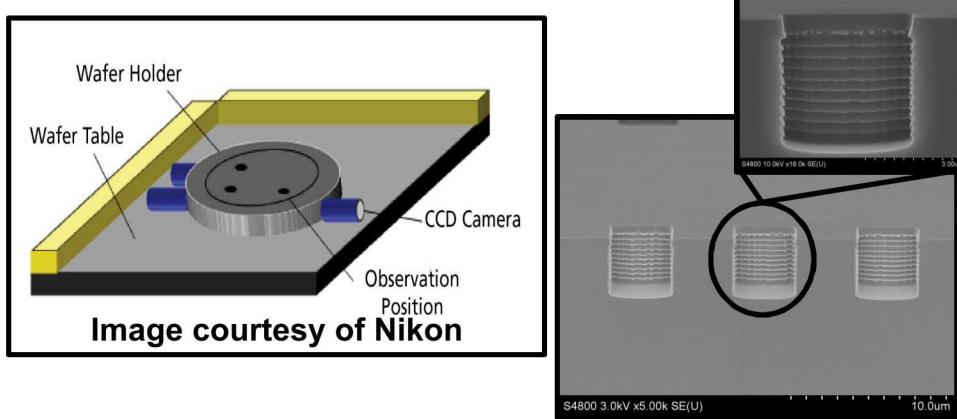
Nikon Backside Field Image Alignment (BS-FIA)



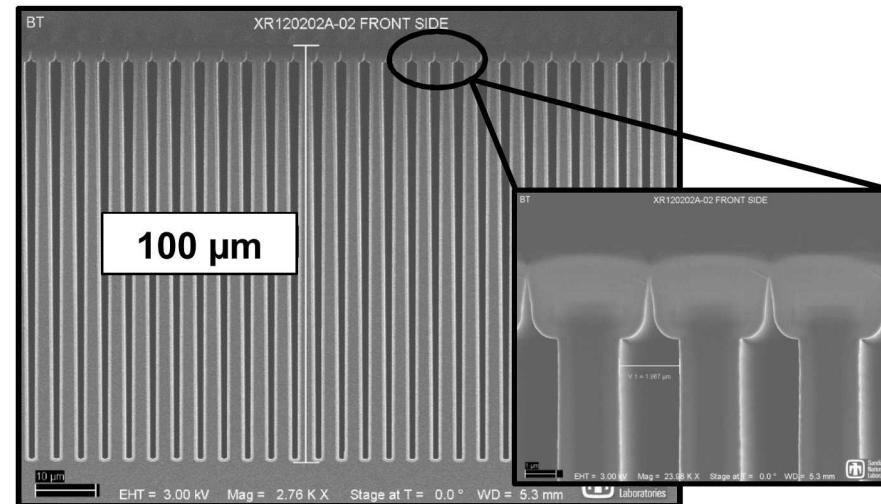
Front to Backside Aligned Gratings



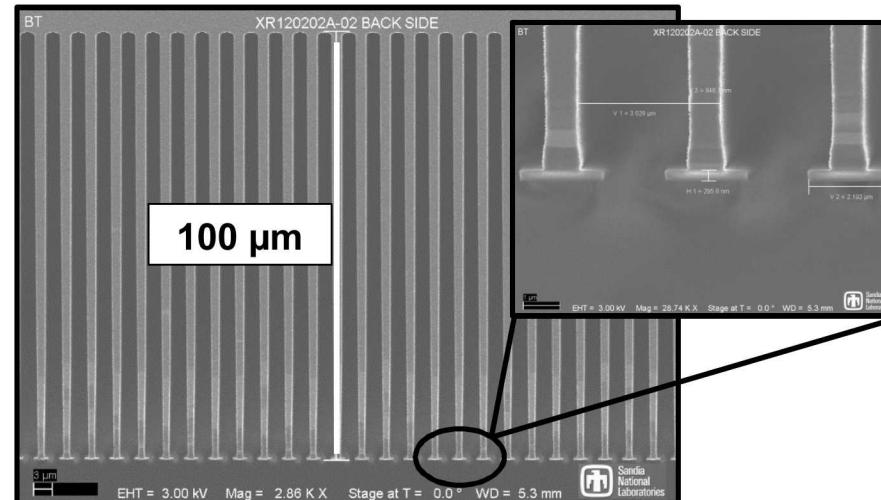
Nikon Backside Field Image Alignment (BS-FIA)



Oxide Coated Front Side Gratings

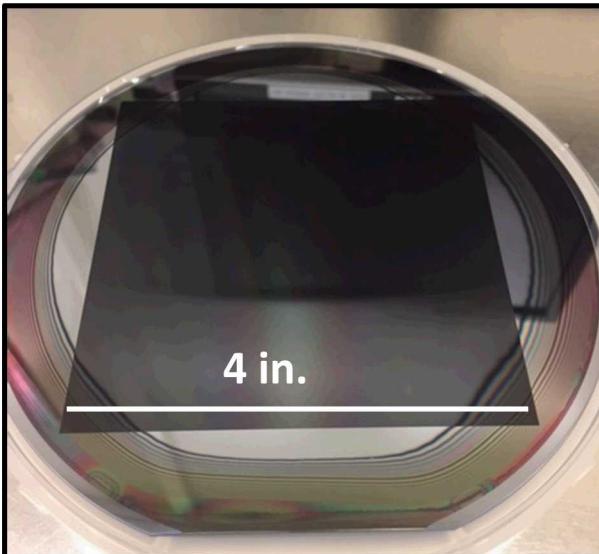


Backside Gratings

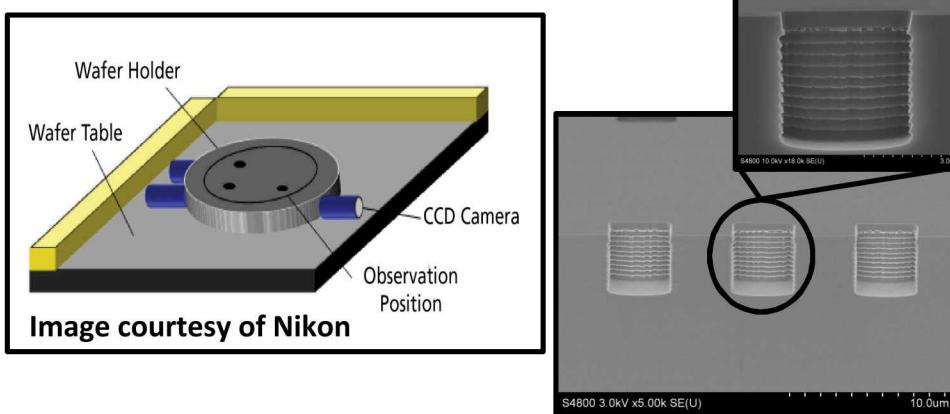


Front to Backside Aligned Gratings

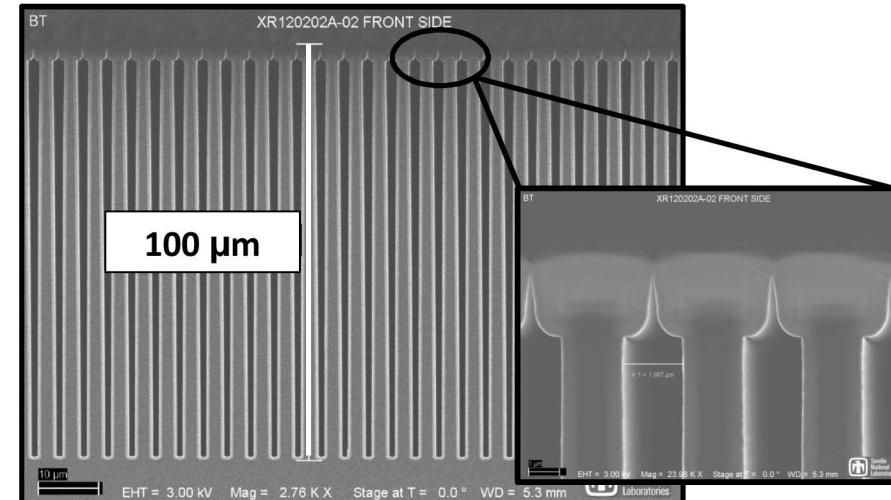
Large Fields of View Possible



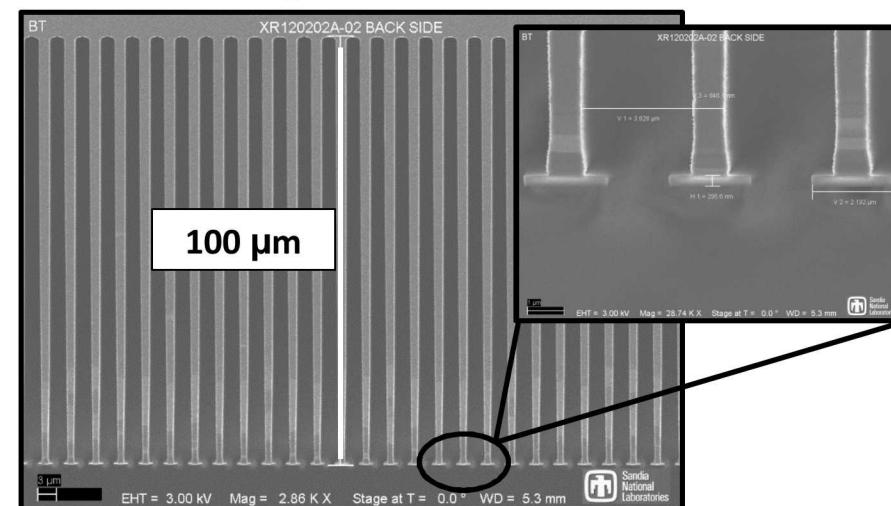
Nikon Backside Field Image Alignment (BS-FIA)



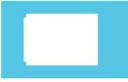
Oxide Coated Front Side Gratings



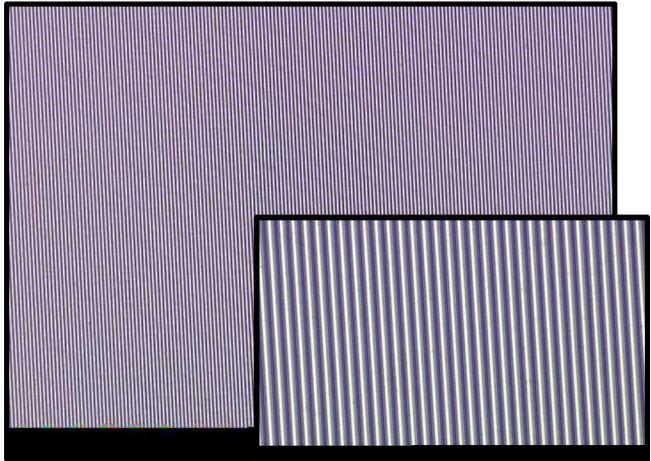
Backside Gratings



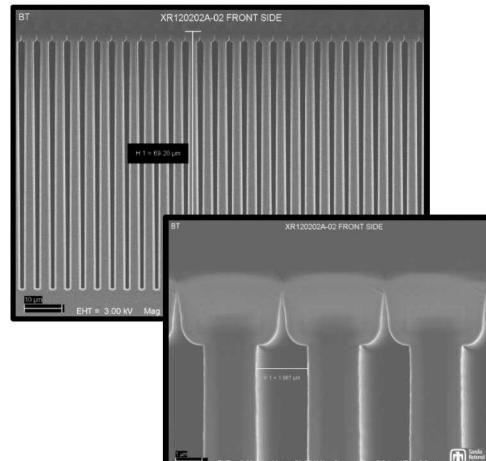
Front to Backside Aligned Gratings



Before Oxide Removal

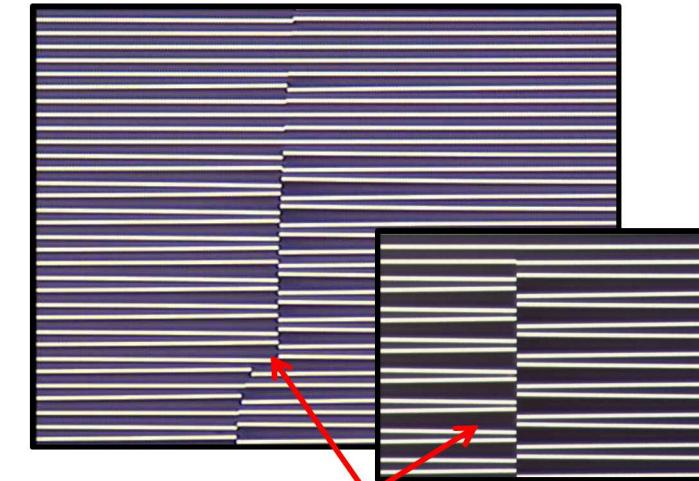


Top down optical Image



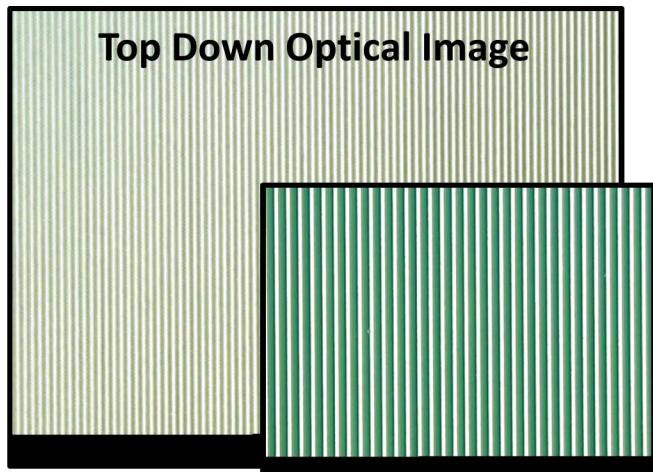
Cross-section SEM

Buffer Oxide Etch (BOE) with IPA Dry

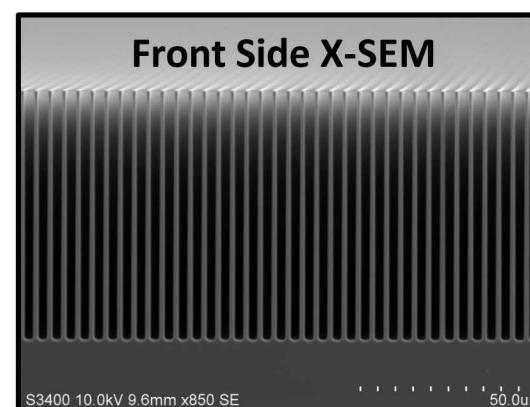


Surface tension induced breakage

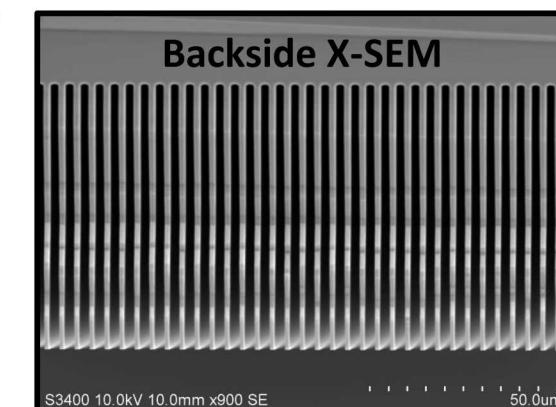
BOE with Critical Point Dryer



Top Down Optical Image



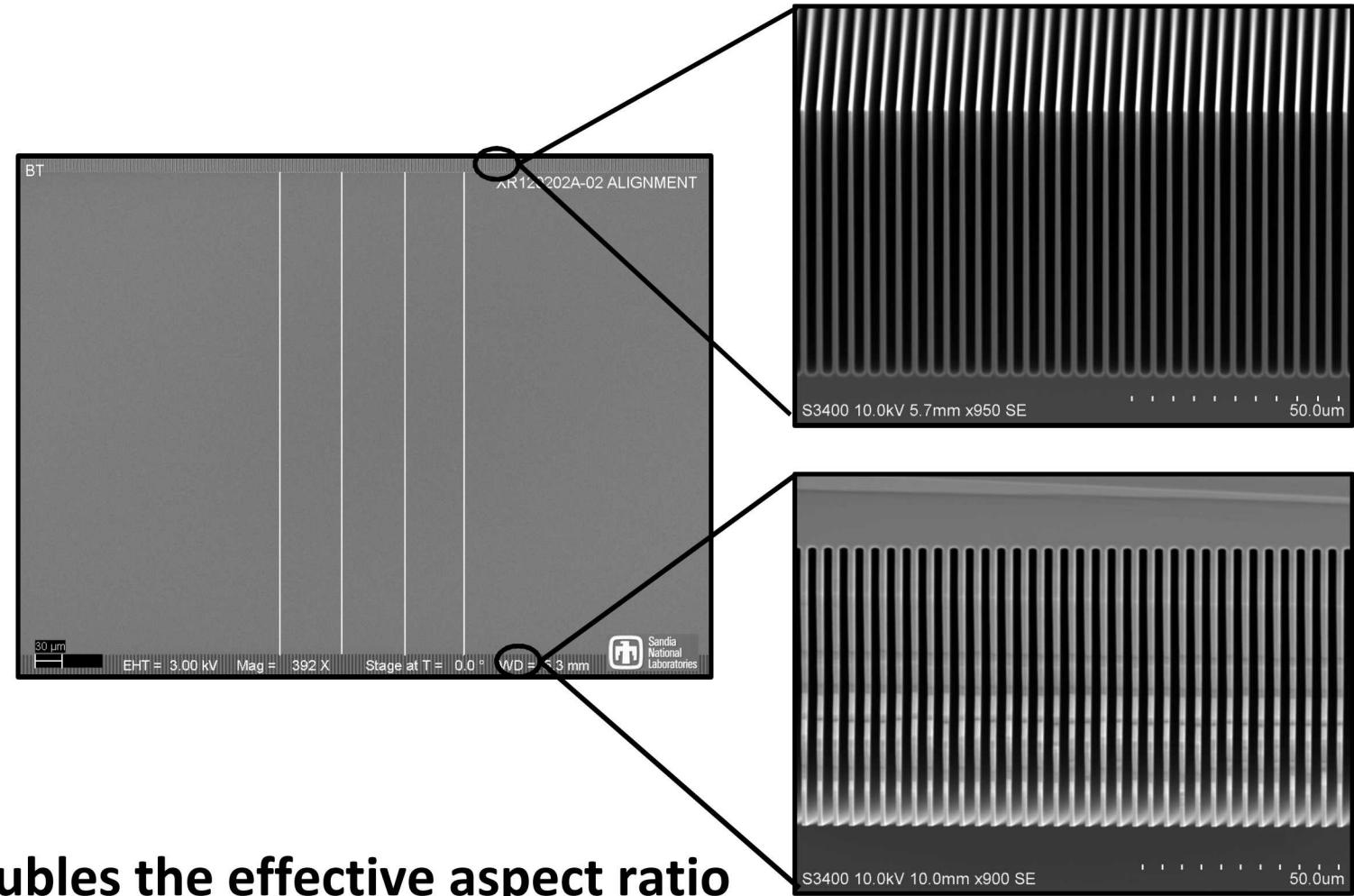
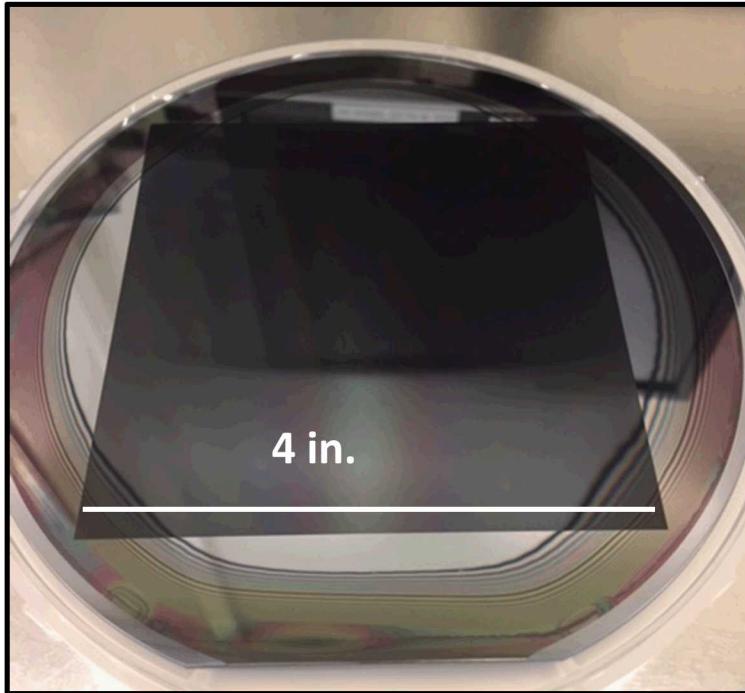
Front Side X-SEM



Backside X-SEM

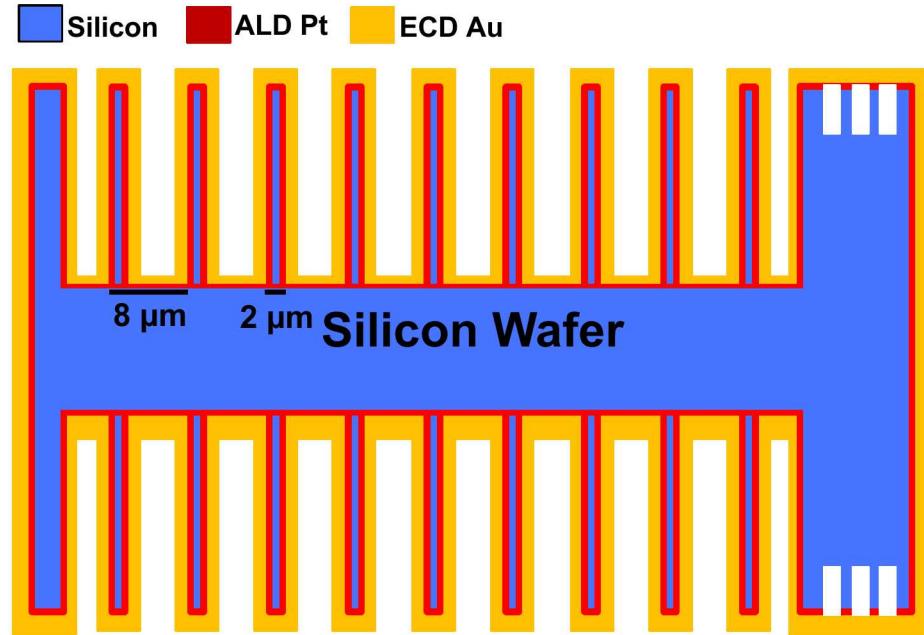
Critical point dryer eliminates surface tension
protecting the Si grating

Released Si Grating Results

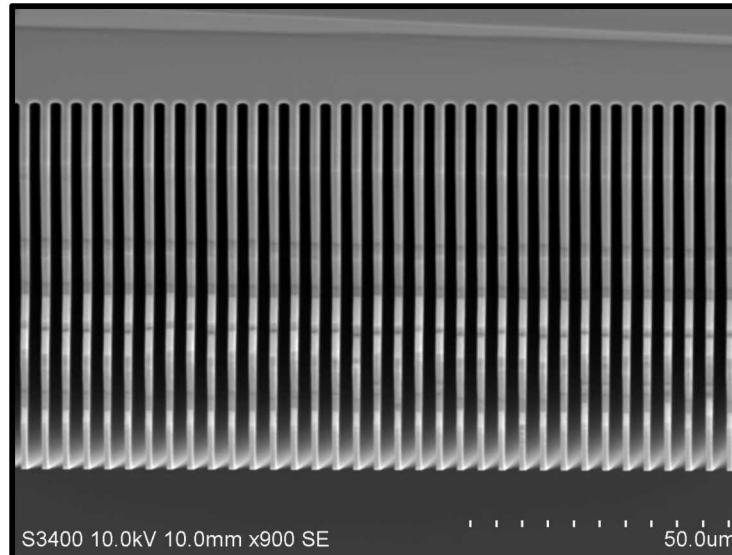
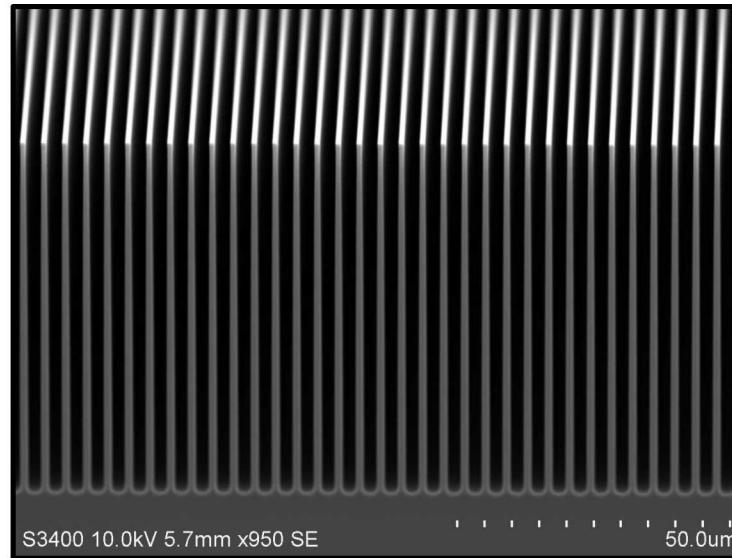


- **Front-to-back alignment doubles the effective aspect ratio**
- **Cost effective material can be used to fill this template at current x-ray energies**
- **Large area fields of view possible**

Released Si Grating Results



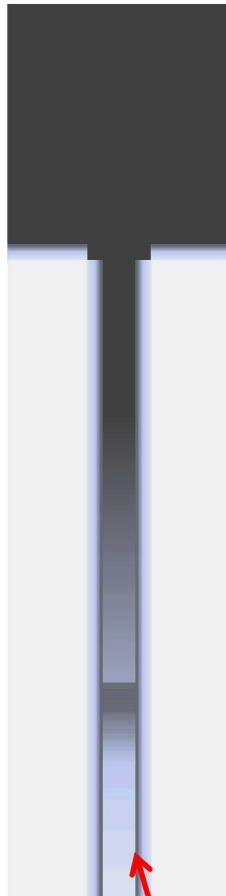
- Coat Si template with ALD Pt
- Precision electrodeposition of Au to complete grating fabrication



Challenges in Precision Electro-Coating



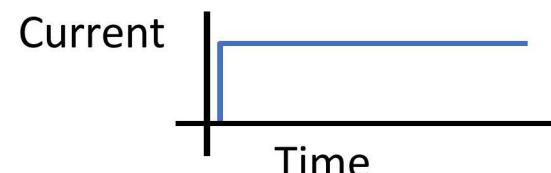
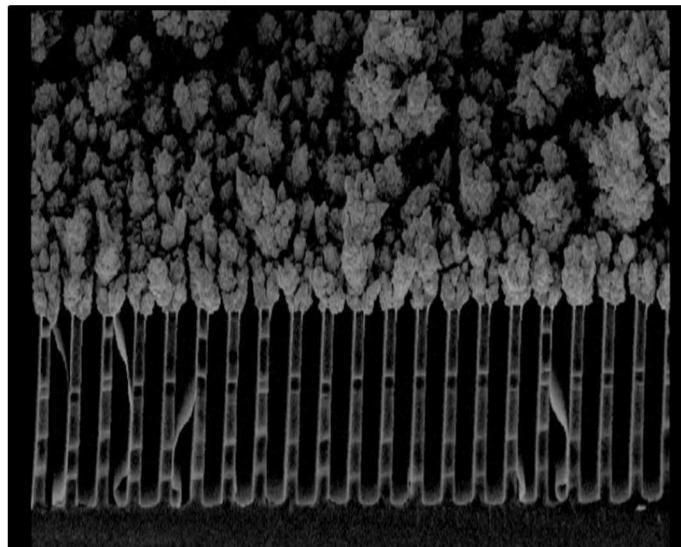
■ Max (bulk) Ion Concentration



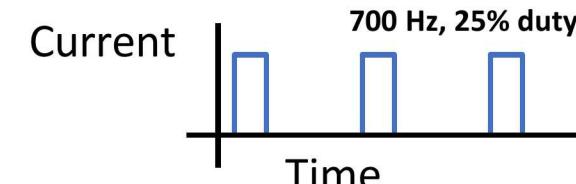
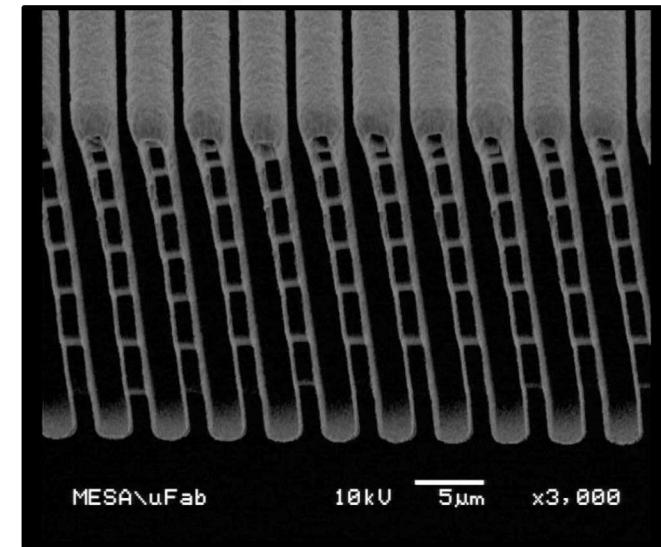
Severely depleted region

- Diffusion limitations are compounded with ionic depletion due to reduction in solution replenishment
- Conventional applied bias leads to non-uniform plating

DC Plating



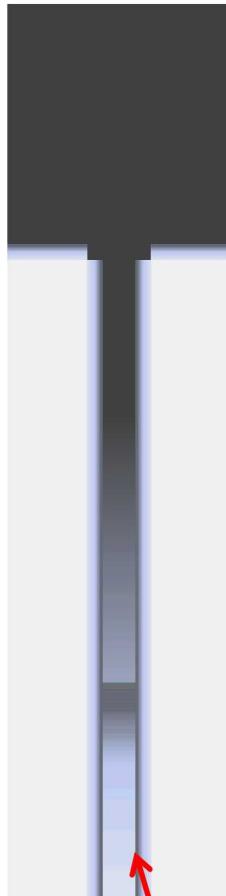
AC Plating



Challenges in Precision Electro-Coating



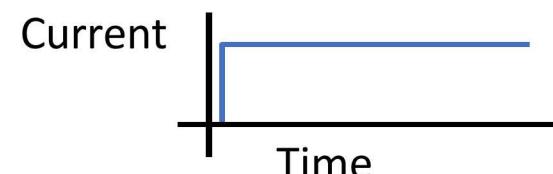
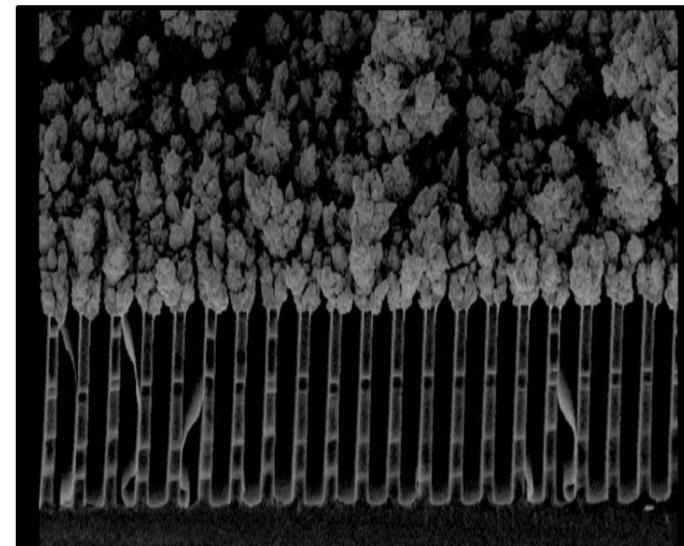
Max (bulk) Ion Concentration



Modifications to Improve Plating

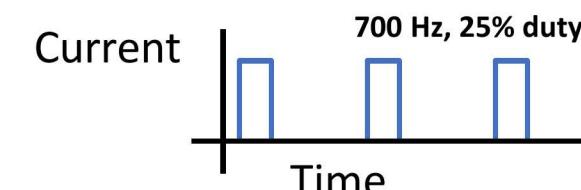
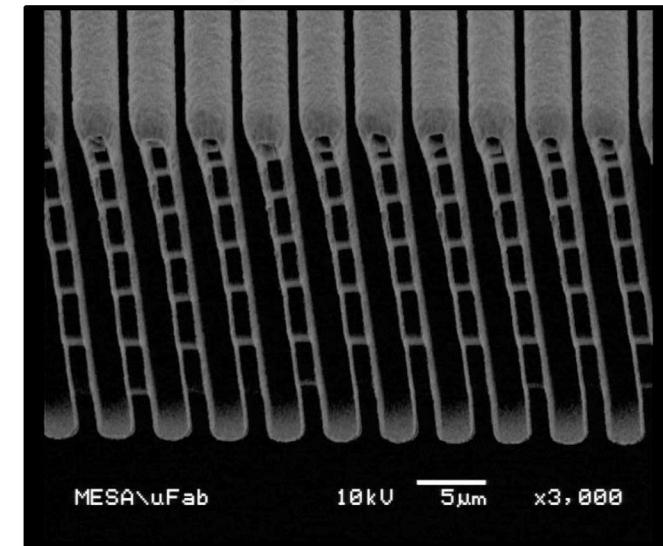
- Incorporate more time for ionic replenishment
- Equilibrate concentrations around plating surfaces
- Increase period of time between deposition pulses

DC Plating



Severely depleted region

AC Plating



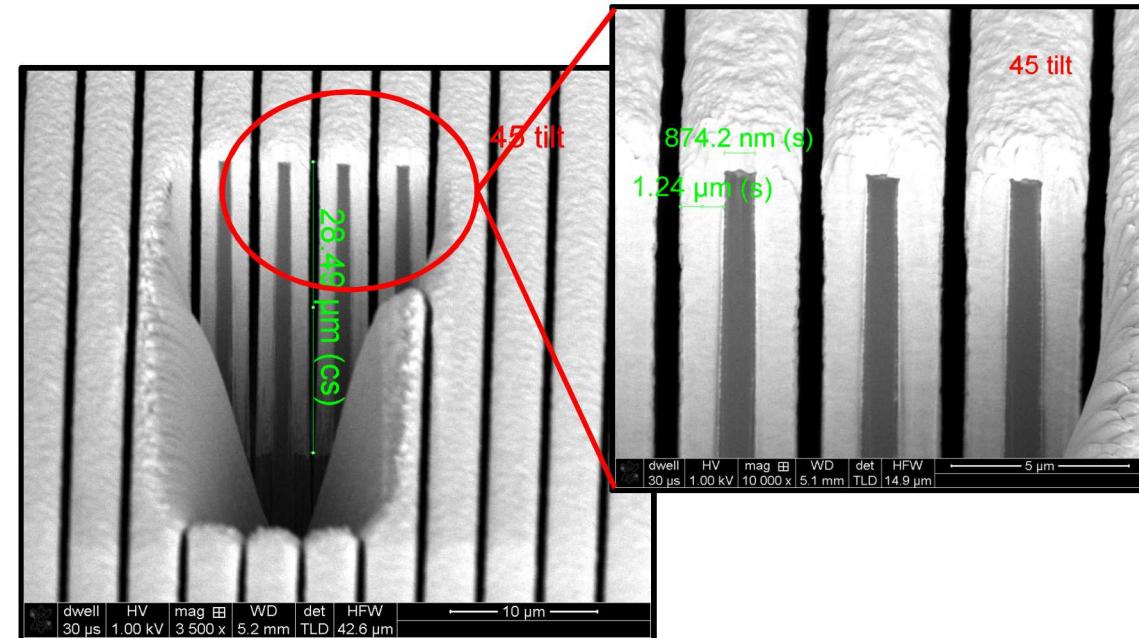
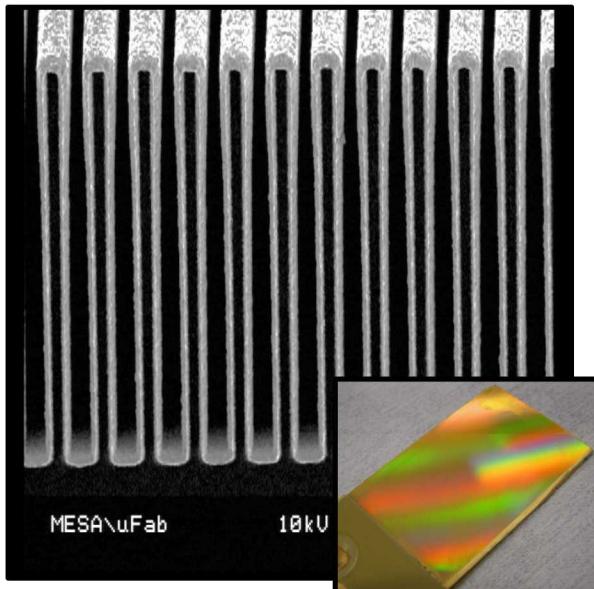
700 Hz, 25% duty

Optimizing Pulse Plating Conditions



Drastically reduced kinetic and plating rate

50:1 aspect ratio gratings



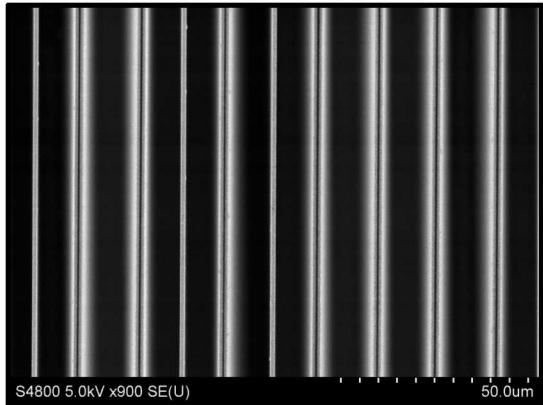
28 μm deep Si template

- Uniform plating in 28 μm deep Si templates
- Near conformal deposition in 50 μm tall Si gratings have been plated
- Uniformity can be tailored to desired aspect ratio

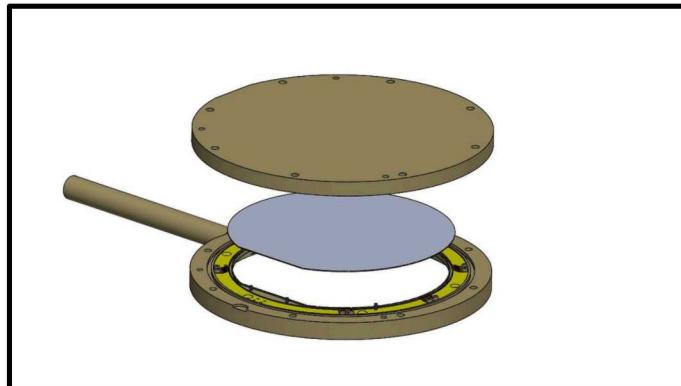
Special Care for Double Sided Gratings



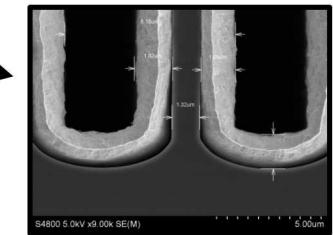
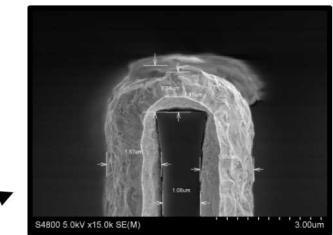
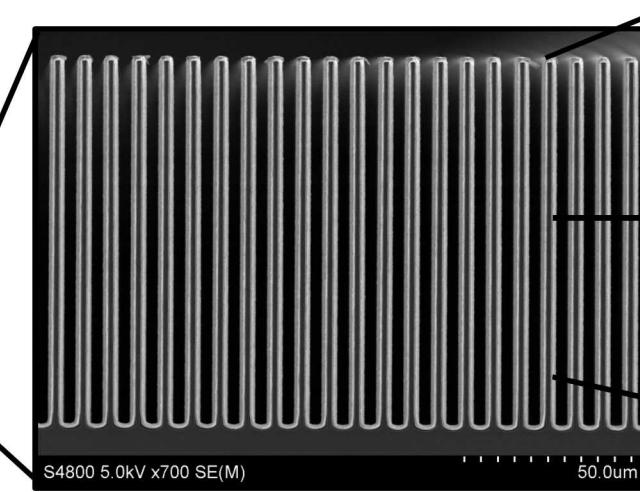
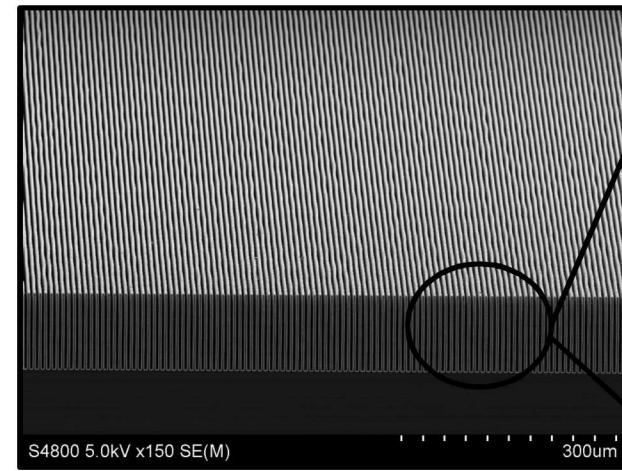
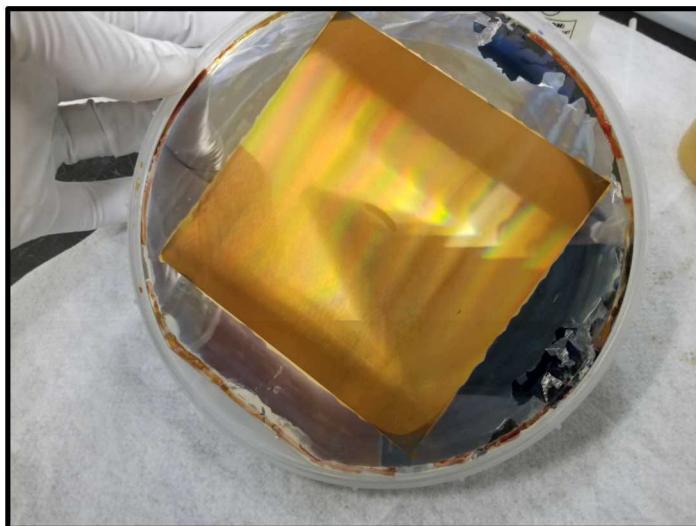
Initial Plating Attempt



Custom Plating Fixture



- Custom fixturing to protect backside grating from damage due to surface tension forces
- Careful drying process required post plating to yield un-damaged grating features



- 67 hr deposition, uniform deposition in 100 μm deep features across 4 in. x 4in. area

Acknowledgements

- **TSVs** - Christian Arrington, Todd Bauer, Matthew Blain, Jason Dominguez, Ron Goeke, Edwin Heller, Robert Jarecki, Becky Loviza, Jaime McClain, Lyle Menk, Anathea Ortega, Jamin Pillars, Paul Resnick, Robert Timon
- **XPCI** - Amber Dagel, Christian Arrington, Patrick Finnegan, Kalin Baca, Steve Volk, Paul Resnick, Jaime McClain, Kate Musick, Ryan Goodner, Steven Grover, Kyle Thompson, Jonathan J. Coleman, Carlos Perez,



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We are hiring! Looking for entry level staff interested in microelectronics fabrication and post fab processes for 2.5D/3D integration!

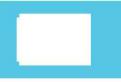
NATIONAL PRIORITIES



Thank you – Questions? Feedback?

Andrew E. Hollowell - aehollo@sandia.gov - 505.844.8301

Supported by the Laboratory Directed Research and Development program at Sandia National Laboratories, a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA-0003525. This paper describes objective technical results and analysis. Any subjective views or opinions that might be expressed in the paper do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

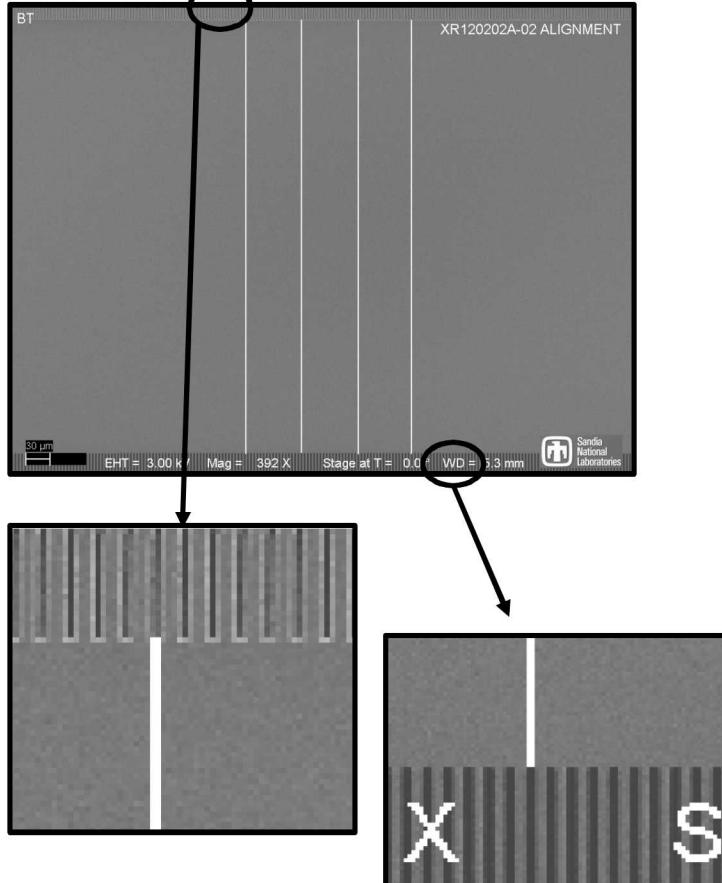


Backup Slides

Measuring Front to Back Alignment Accuracy

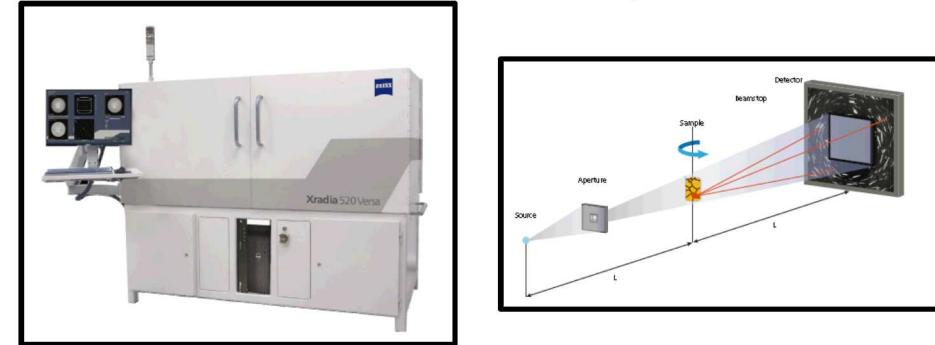
Large separation distance and small feature sizes makes it difficult to obtain quantitative alignment measurements

Cross-section SEM Image

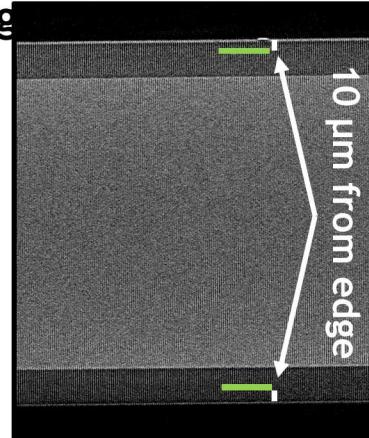


SEM imaging is not capable of quantifying alignment

Zeiss Xradia 520 Versa NanoCT System



Side View CT Scan of BSA Grating



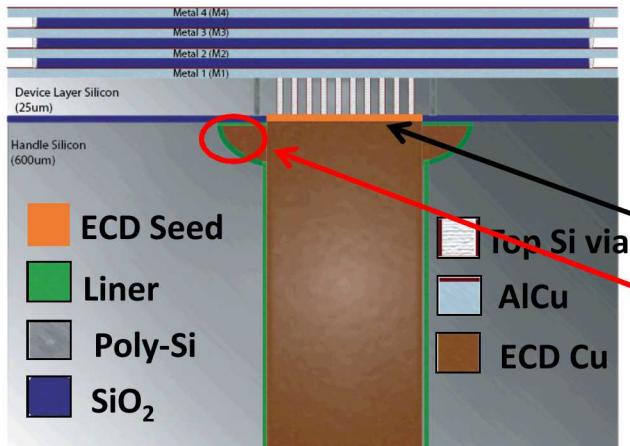
Qualitatively our alignment is within 0.5 μm as each pixel from the CT scan is 0.5 μm

Superimposed Pitch Measurements



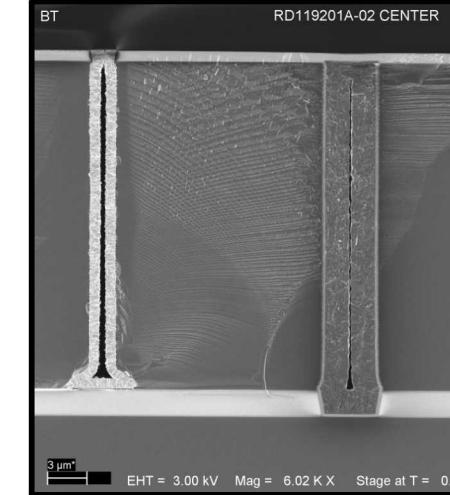
TSV Integration - Hybrid W via first, Cu via last Approach

A. E. Hollowell, et. al. "A Unique 3D Integration Approach for SOI Substrates – Mating CVD W Filled TSVs with ECD Cu Filled TSVs." ECS PRiME October 2016

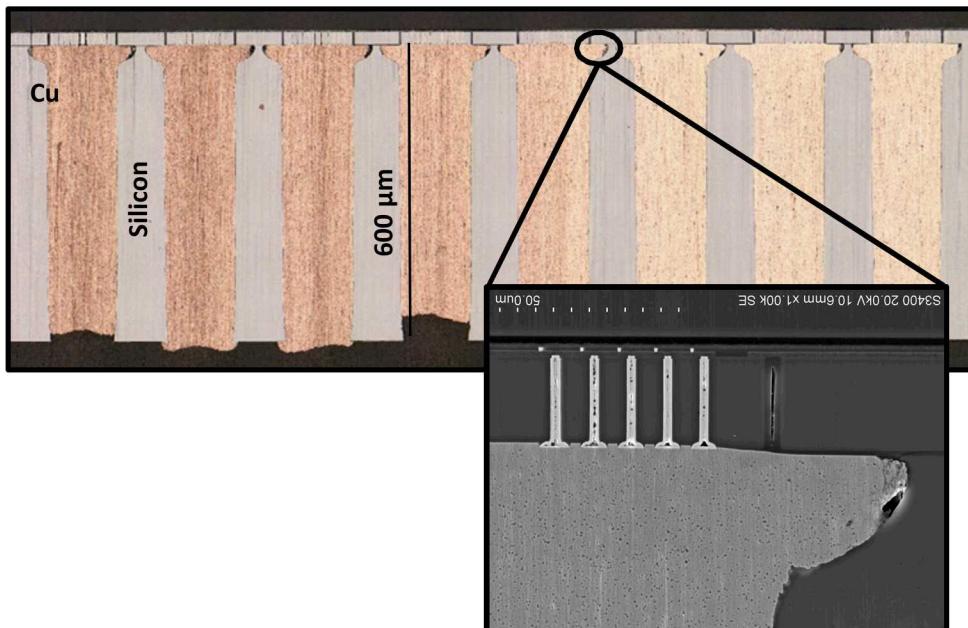


Through mask Cu filling from a discontinuous evaporated seed

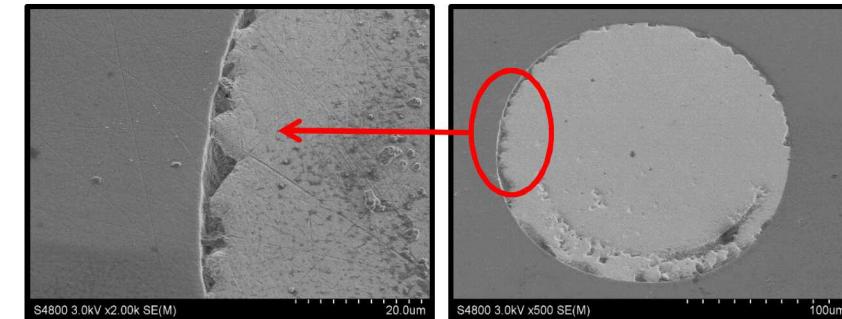
- Top Si vias to connect Cu TSV through BOX to M1
- Isolation trench to electrically isolate the vias from the device Si layer
- ECD seed deposited only at the bottom of the TSV
- A void free fill of the notch is impossible to achieve
- Less than 10 mΩ per TSV



Through Mask Plating Cross Section

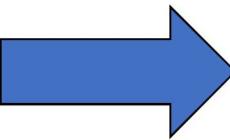
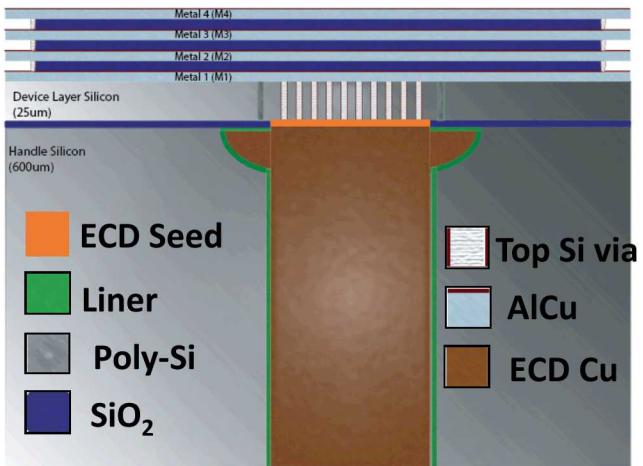


SEM after Parallel Delayering

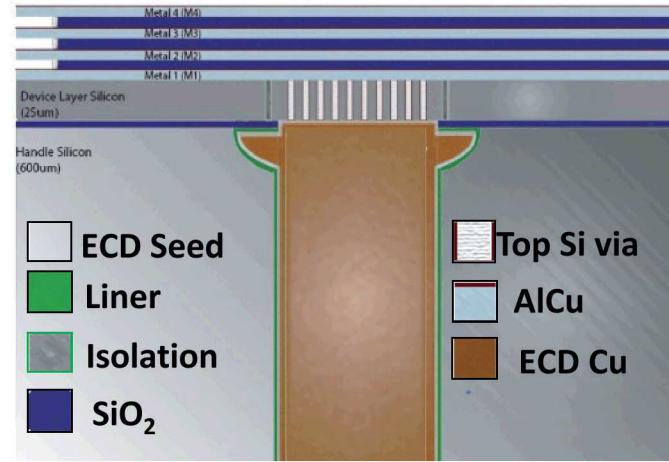


Bottom Up Filling from an ALD Pt Seed

Through Mask Plating



Bottom Up Plating From Continuous Pt Seed Metal



Superfilled Bottom Up Plating

- Adapted from research by Josell and Moffat at NIST-Gaithersburg
- **Void free filling**
- **Reasonable deposition times**
- **Complex balance between applied bias and electrolyte composition**
- **Plating conditions for void free filling is dependent on TSV geometry**

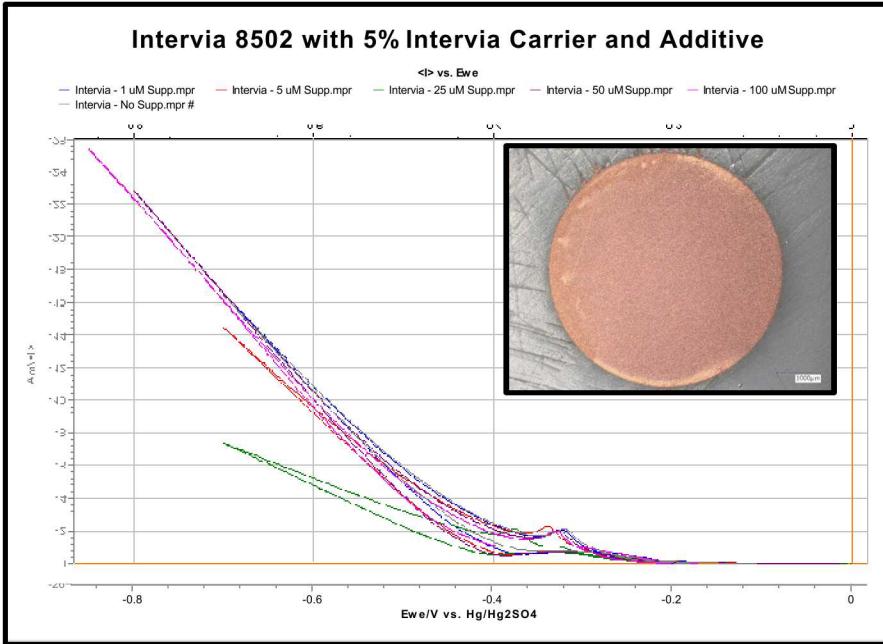
Full Wafer Production Scale Filling

1. Production plating tools do not have reference electrodes
2. Establish voltage controlled super filling
3. Derive current controlled void free filling from potentiostatic filling results

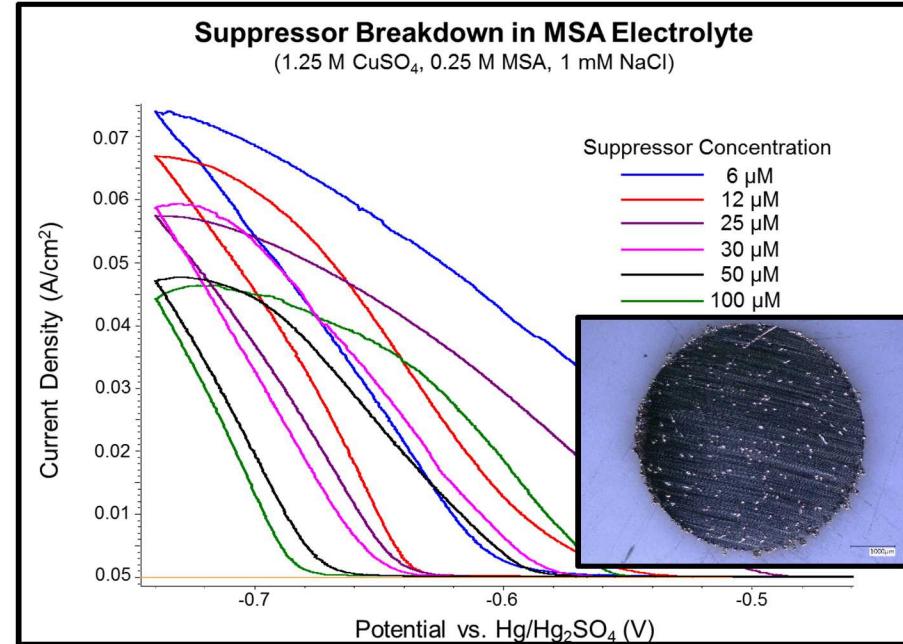
3-Additive Commercial Chemistry vs MSA Electrolyte with Tetronic 701 Suppressor

- Commercial plating chemistry does not exhibit S-NDR characteristic
- Methane Sulfonic Acid (MSA) has a higher solubility limit
- MSA + Tetronic 701 exhibits CV hysteresis and S-NDR mechanism

Commercial H_2SO_4 Plating Chemistry

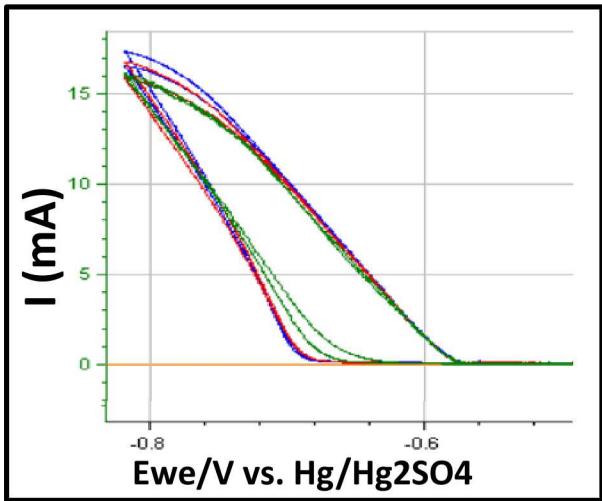


MSA Electrolyte w/ Tetronic 701 Suppressor

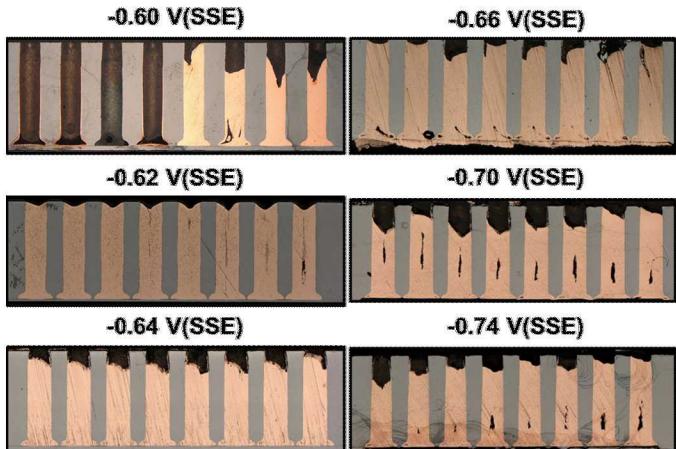


Investigating the Effect of Suppressor Organics on Galvanostatic Deposition

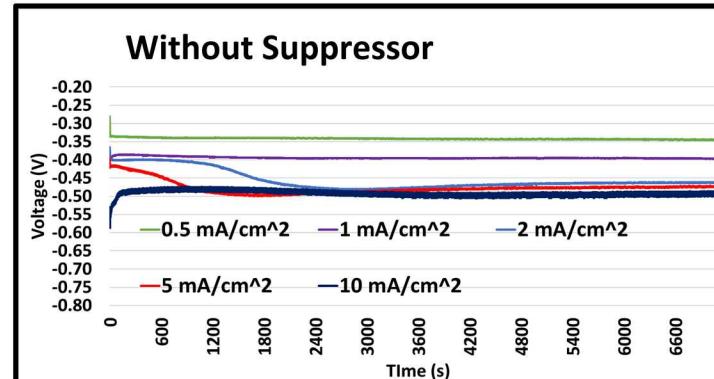
Plating Electrolyte CV Curve



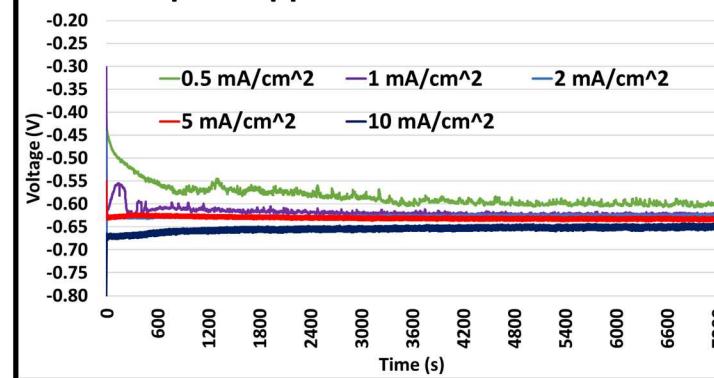
Potentiostatic plating is very sensitive to applied voltage



Chronopotentiometry on Unpatterned Sample Coupons



50 μ M Suppressor



- Larger voltage window w/o suppressor
- Suppressor pins voltage to > -0.55 V(SSE)