SAND2019-9504C

Flip-Chip and Backside Techniques

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Purpose

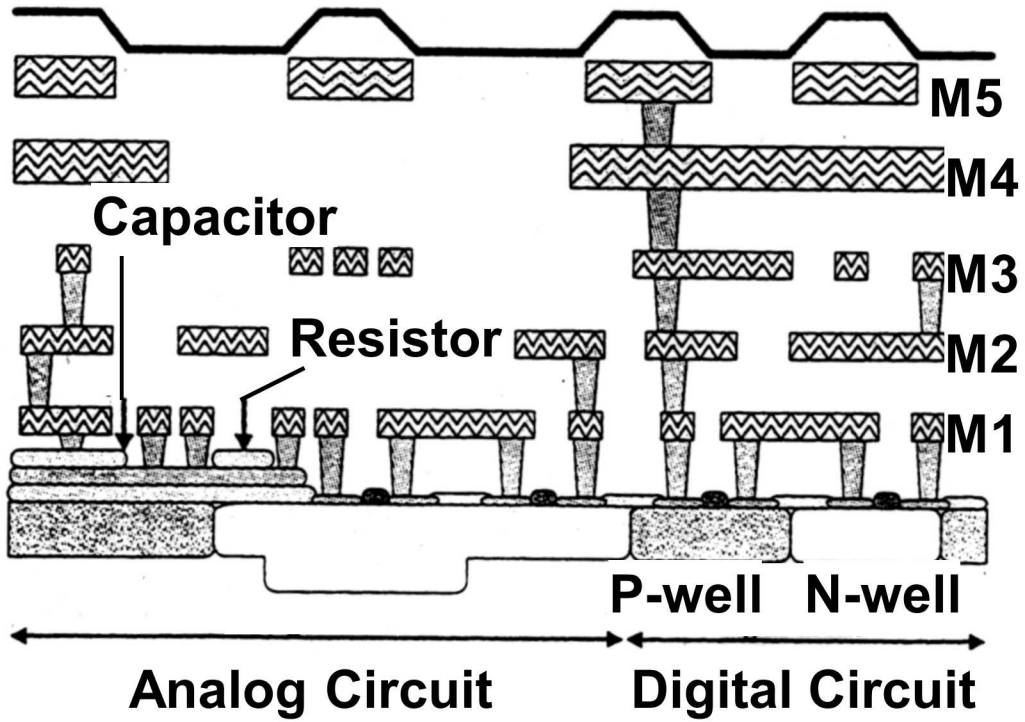
To describe the basic physics needed to understand backside technique application and physical preparation of samples for backside IC analysis

Outline

- Introduction
- Basics
  - Light transmission through silicon
  - Optical image formation through silicon
- Backside preparation techniques
  - Global Si thinning
  - Local Si thinning/Precision probe hole milling
- Conclusions

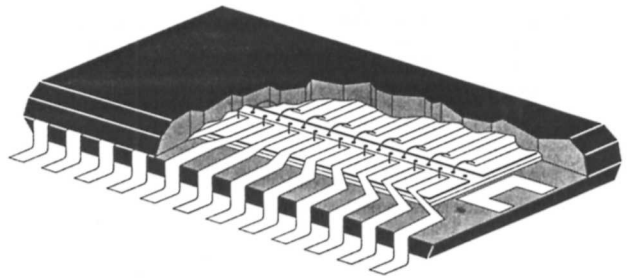
Why FA from the Backside of the Die?

Multi-layer metallization

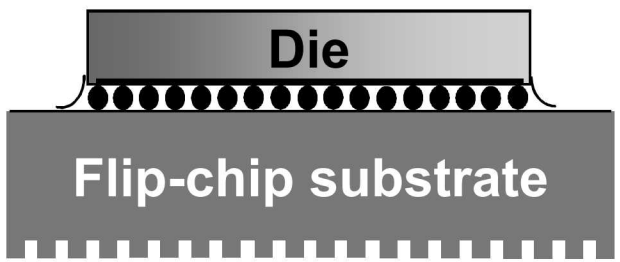


new packaging techniques e.g.

LOC (Lead On Chip)

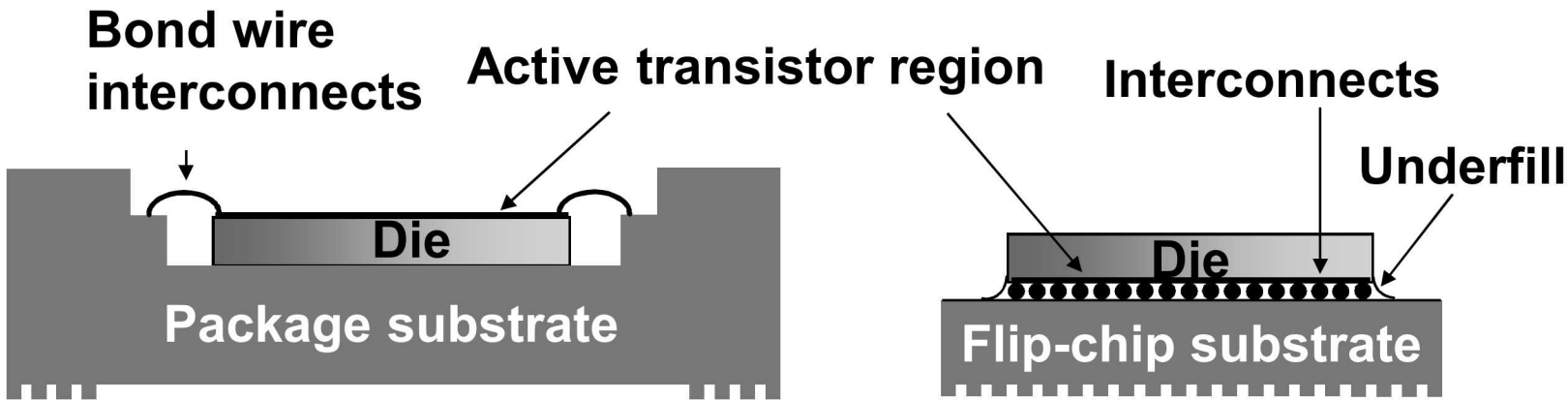


Flip-Chip



Data taken from Fujitsu

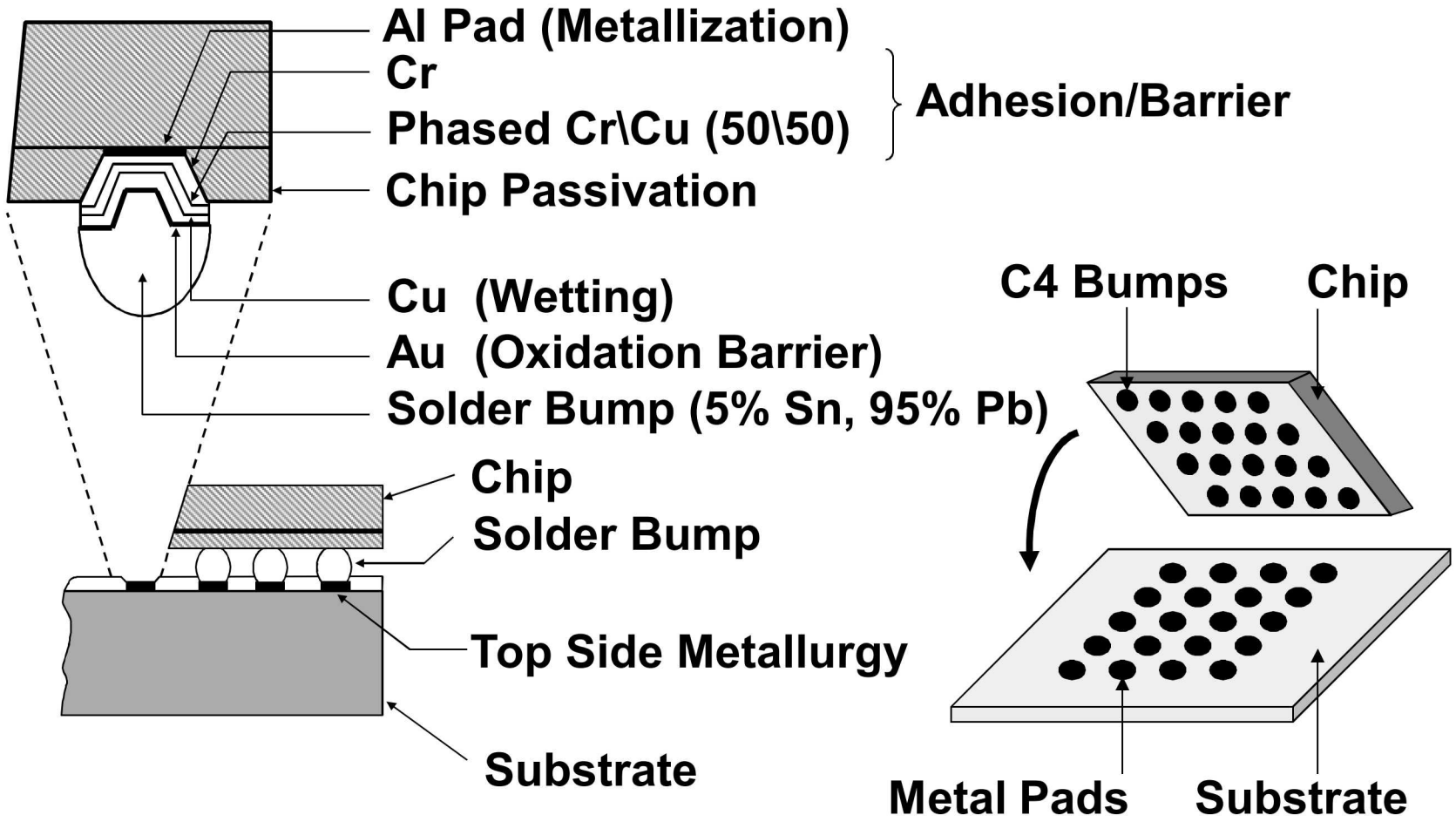
Wirebond vs. Flip-chip Packaging



Wirebond package die

Flip-chip packaged die

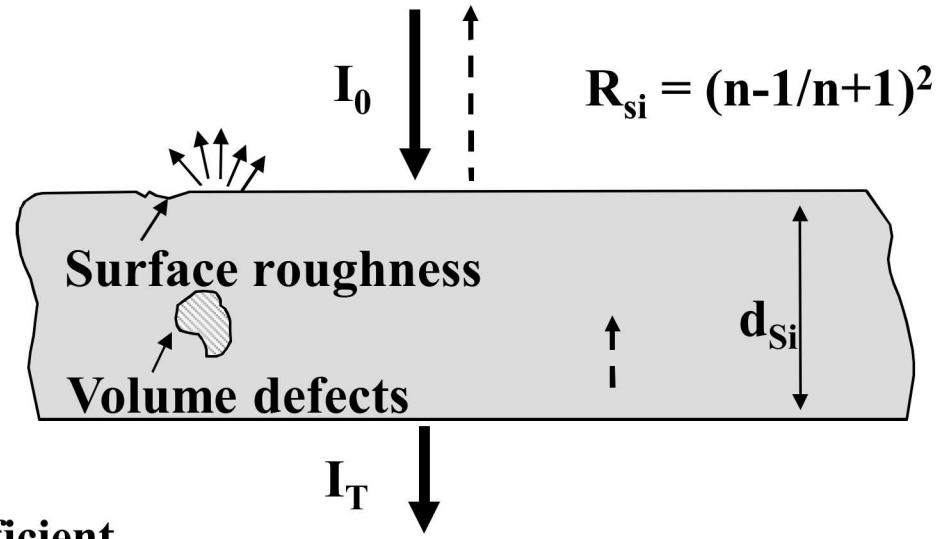
C4 (Controlled Collapse Chip Connection) Technology



Major Benefits of Flip Chips

- Flip chips are more slim and compact ---> lighter weight products
- Flip chips permit higher speeds and enhanced electrical performance (electrical parasitics and paths are reduced)
- Flip chips permit a higher I/O (input/output) density at smaller chip size
- Flip chips permit a higher power dissipation/enhance thermal dissipation
  ----> flip chips are used in multimedia products, portable electronic products, audiovisual products, (notebook) PC‘s, workstations (microprocessors), etc.

Transmission Through Bulk Si



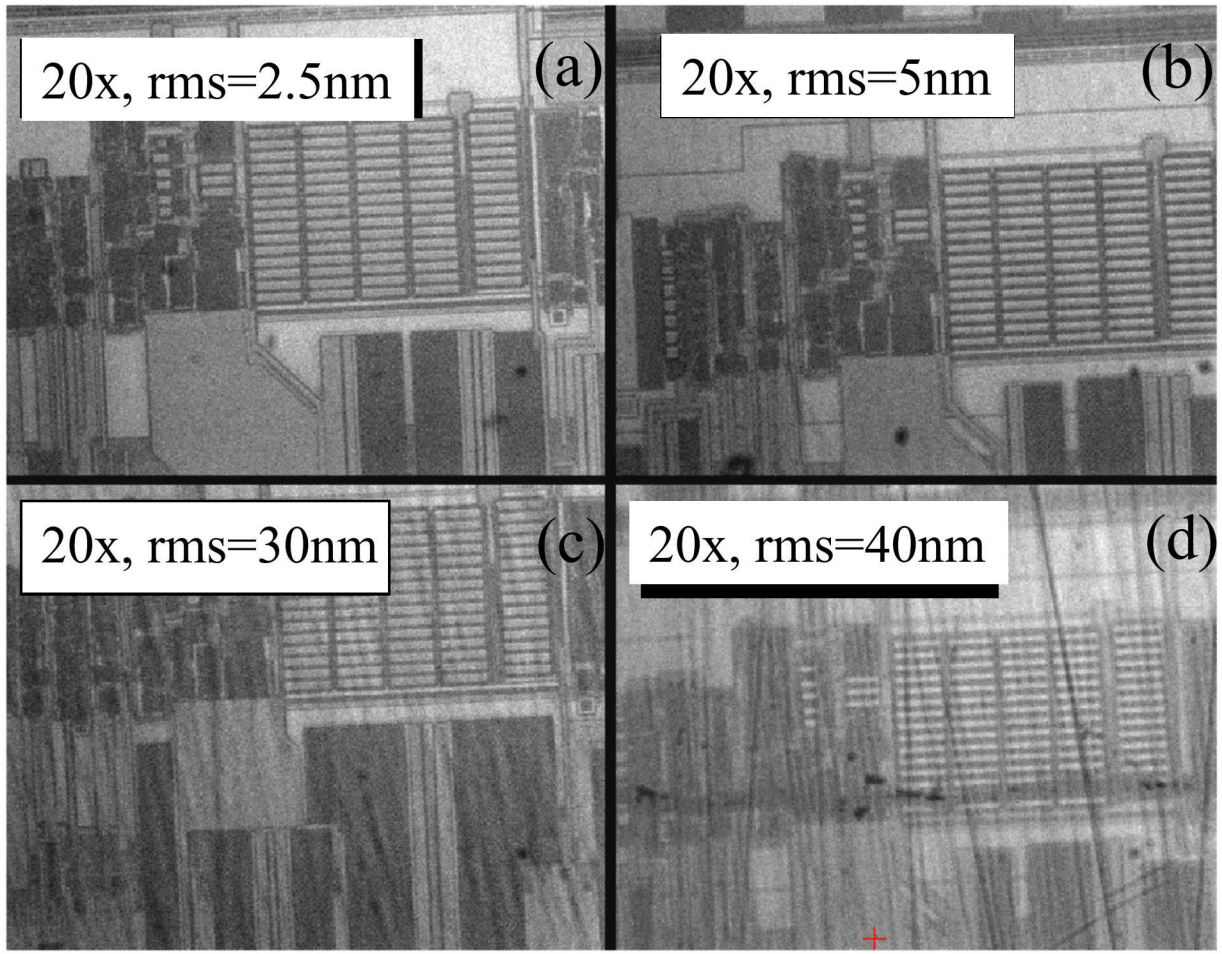
I_0 = Incident intensity
I_T = Transmitted intensity
R_{Si} = Reflection intensity
n = index of refraction
T_{Si} = Si transmission coefficient
α = Absortion coefficient
d_{Si} = Si thickness

$$T_{Si} = I_T / I_0 = (1-R_{Si})^2 \bullet \exp(-\alpha\, d_{Si})$$

α factors
- $\alpha_{Si}(\lambda)$ = bandgap related absorption
- $\alpha_{n,p}(\lambda)$ = free carrier absorption
- α_{volume} = scattering due to volume defects (neglect)

Scattering Due to Surface Roughness

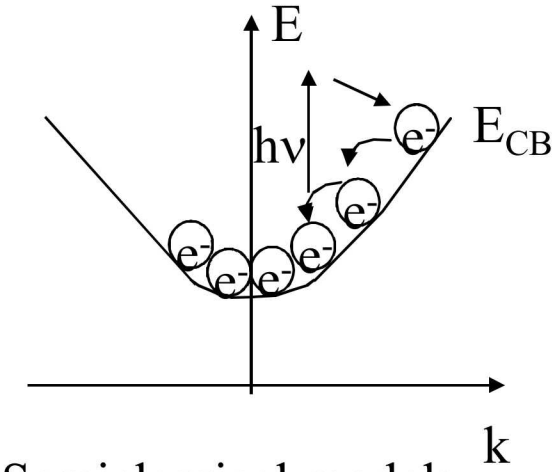
Images (a) - (d): substrate doping 1 x 10^{15} cm^{-3}; d_{Si}= 150µm



⇒ rms (root mean square) < 5nm

Free Carrier Absorption

(intraband absorption, α)



Semiclassical model:

wavelength doping concentration

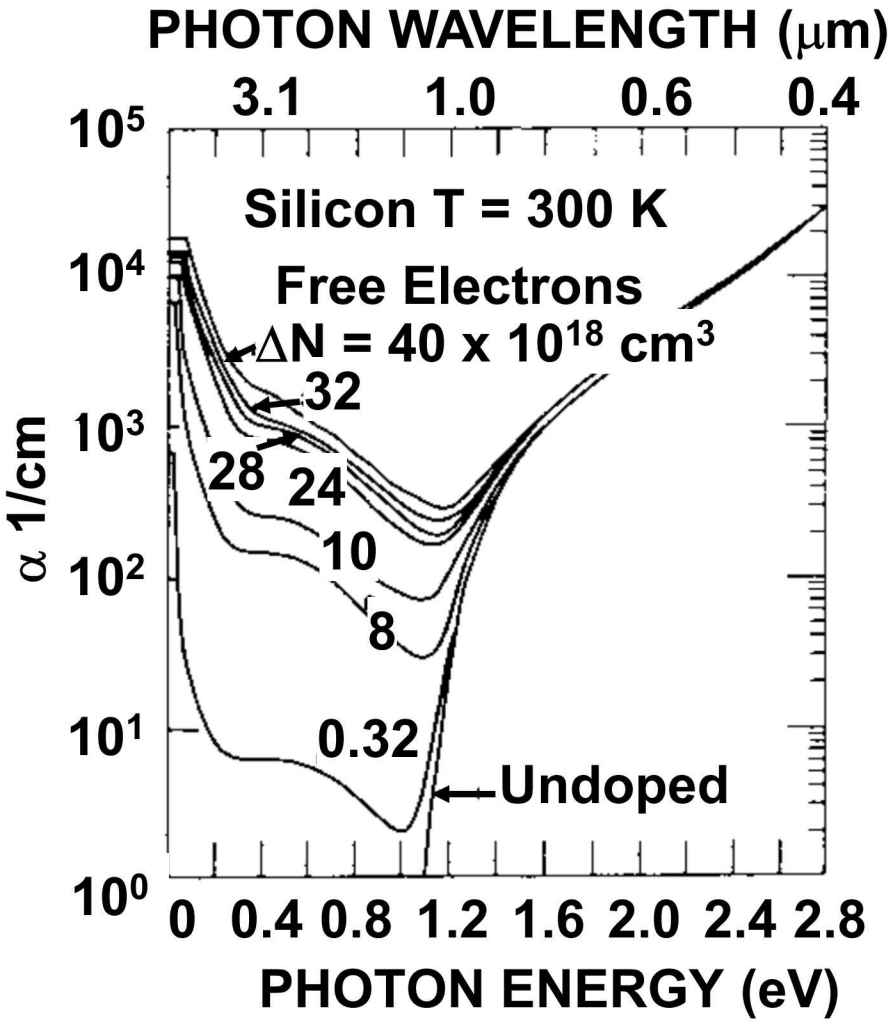
α prop. to $\frac{\lambda 2n}{(m^*)2\mu}$

mobility

effective mass

$N_e = 5 \times 10^{18}\ cm^{-3} \Rightarrow$

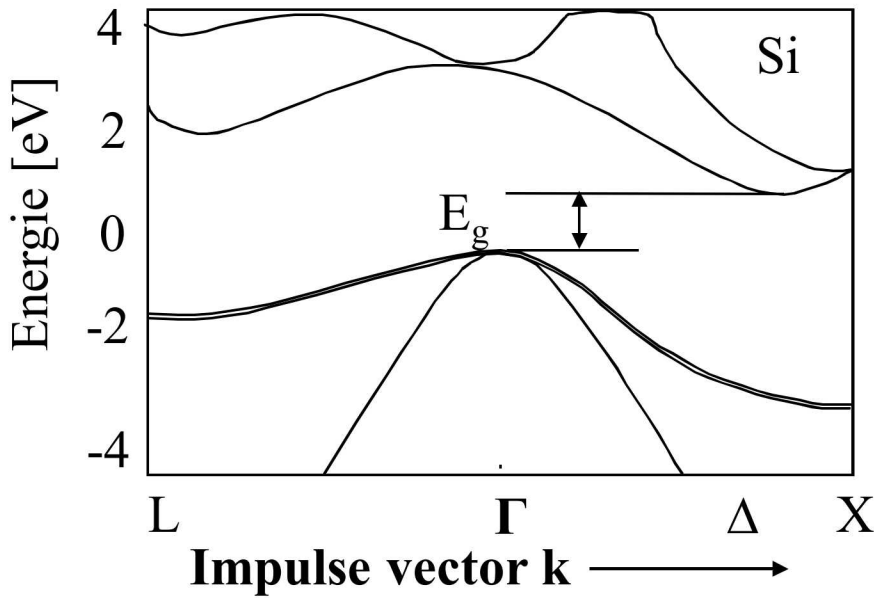
$\alpha_{change} \approx 4\%$ (d = 400 μm, 1.3 μm)



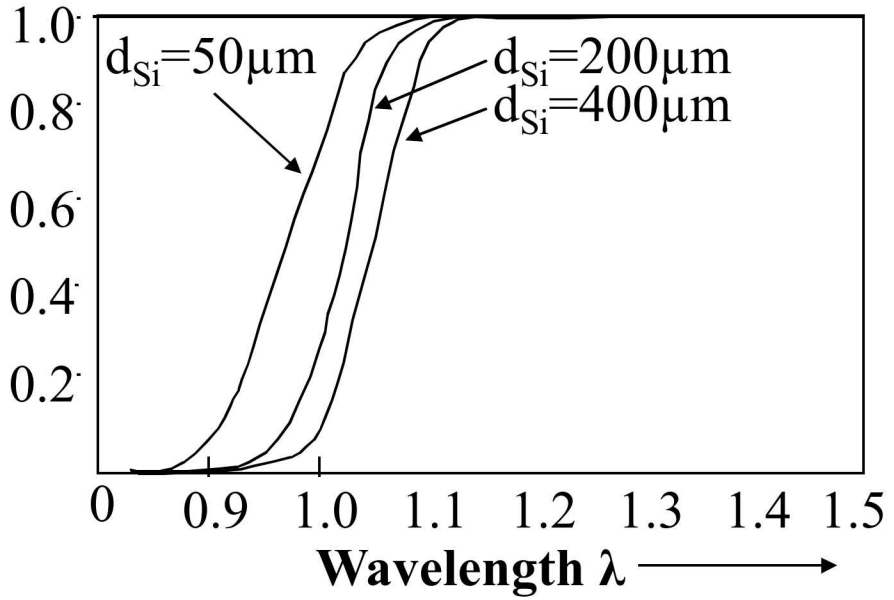
Band-gap Related Absorption

(Interband Absorption)

Band diagram of Si



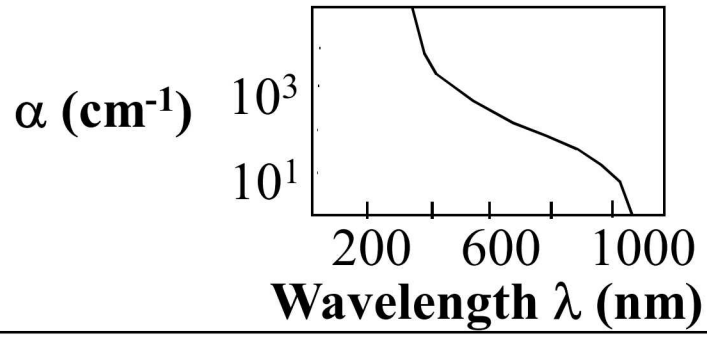
Transmission of undoped Si



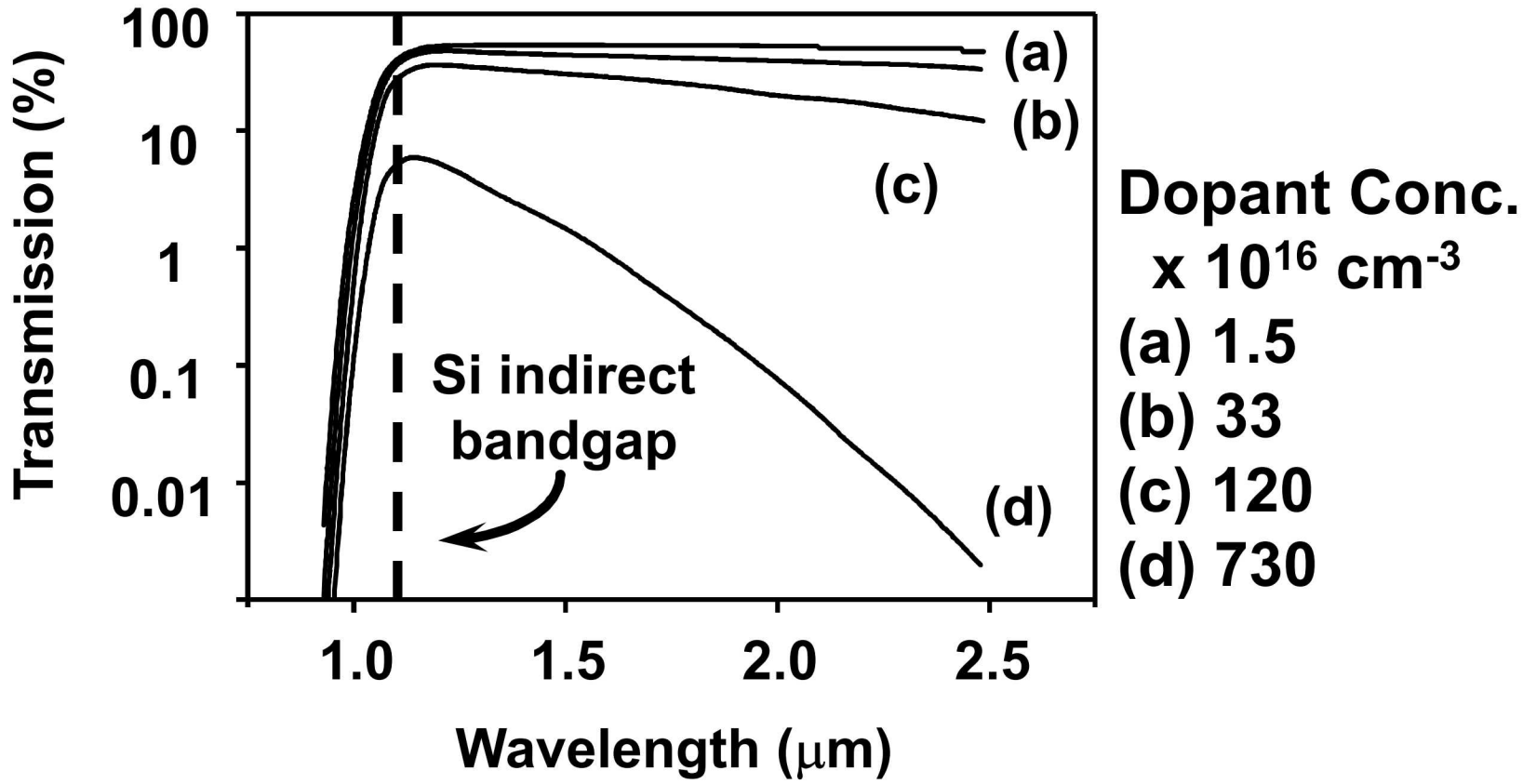
E_g=1.12 eV (300 K)

Si (E_g=1.12eV or 1107nm)

Γ proportional to $e^{-\alpha d_{Si}}$

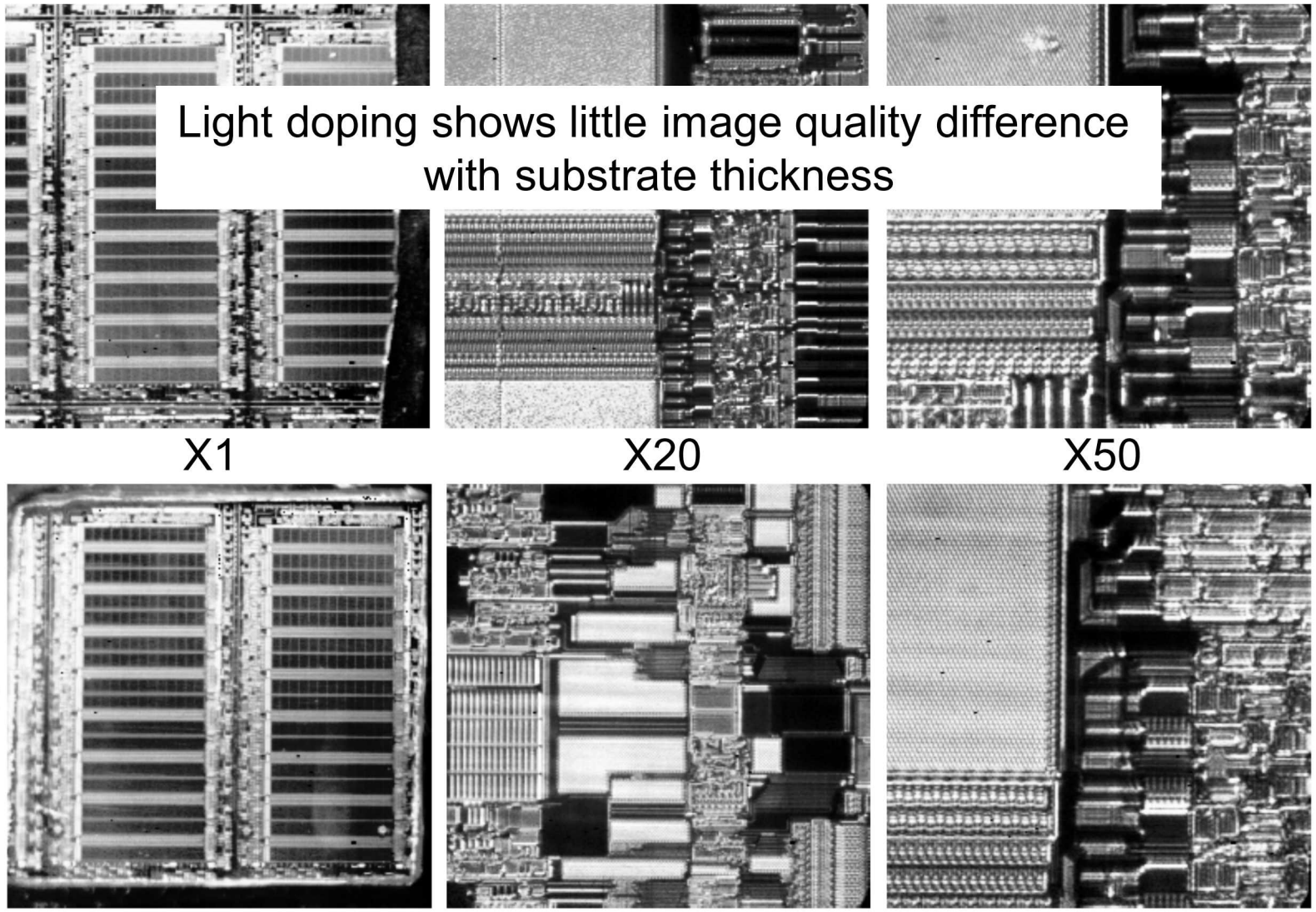


IR Transmission
625 μm of p-Doped Silicon



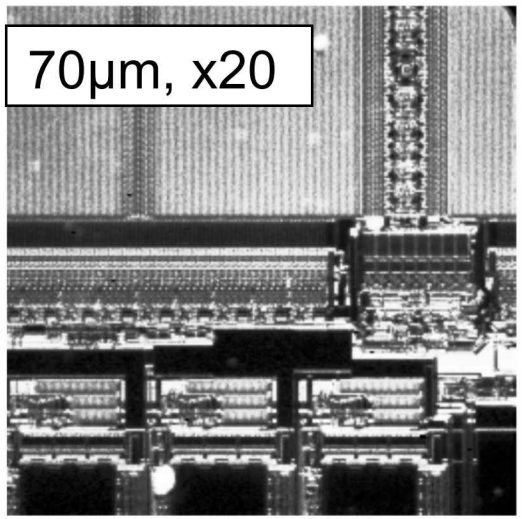
IR Backside Imaging

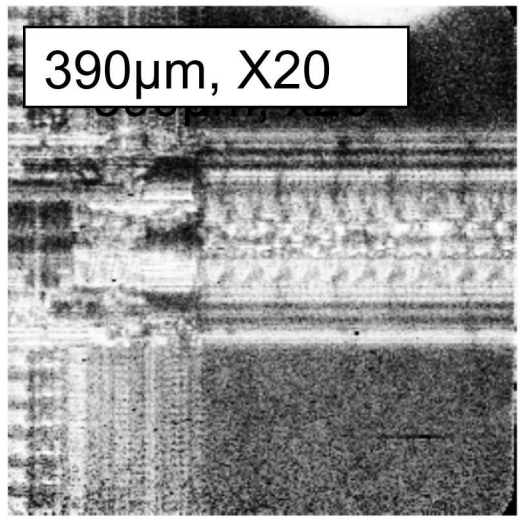
Illuminated images: $p_{substrate}=1*10^{15}cm^{-3}$; HgCdTe detector (IR Labs)

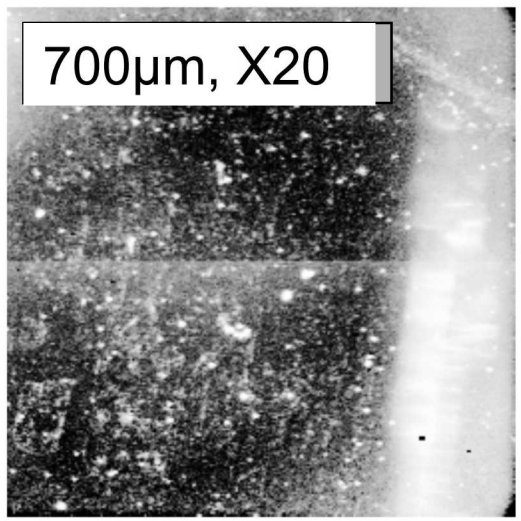


IR Backside Imaging

Illuminated images: $p_{substrate}=1*10^{19}cm^{-3}$; HgCdTe detector (IR Labs)

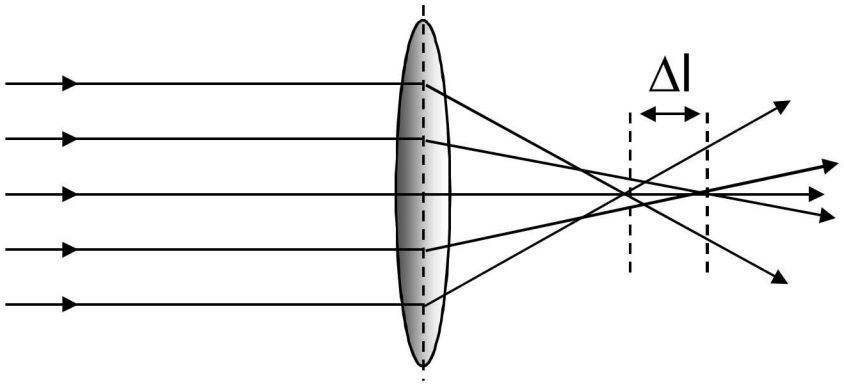




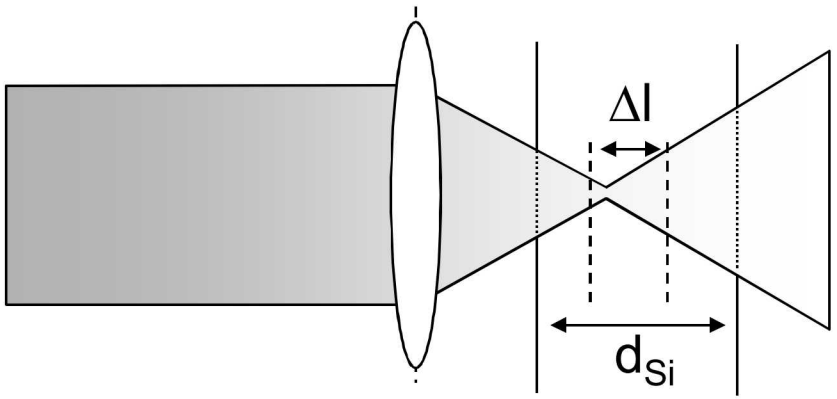


heavy doping shows significant image quality differences
with substrate thickness

Spherical Aberration



Thin biconvex lens, intensity varies depending on ray position



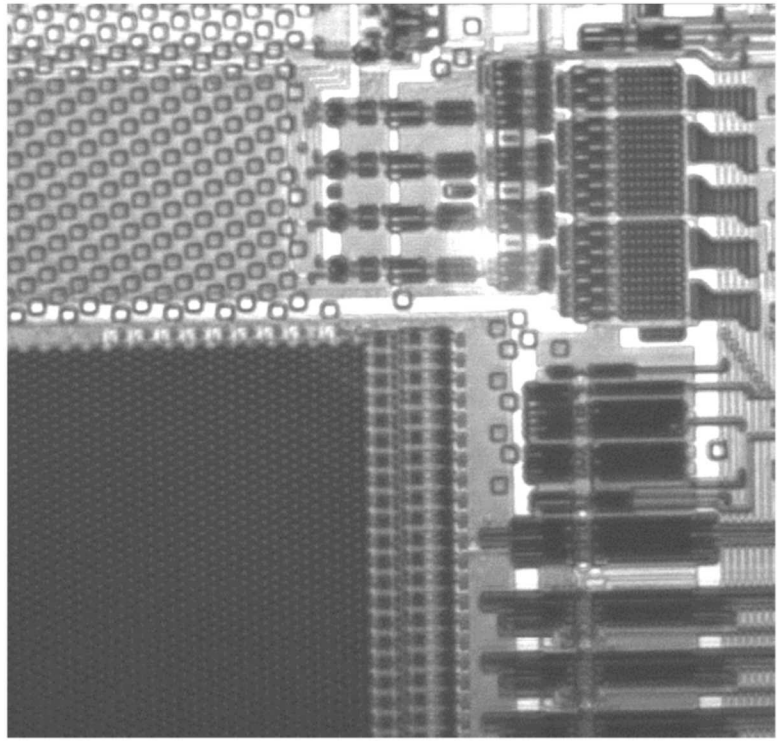
Planar, parallel Si complicates focusing

Δl effected by Si and lens properties d_{Si}, n, NA (numerical aperature)

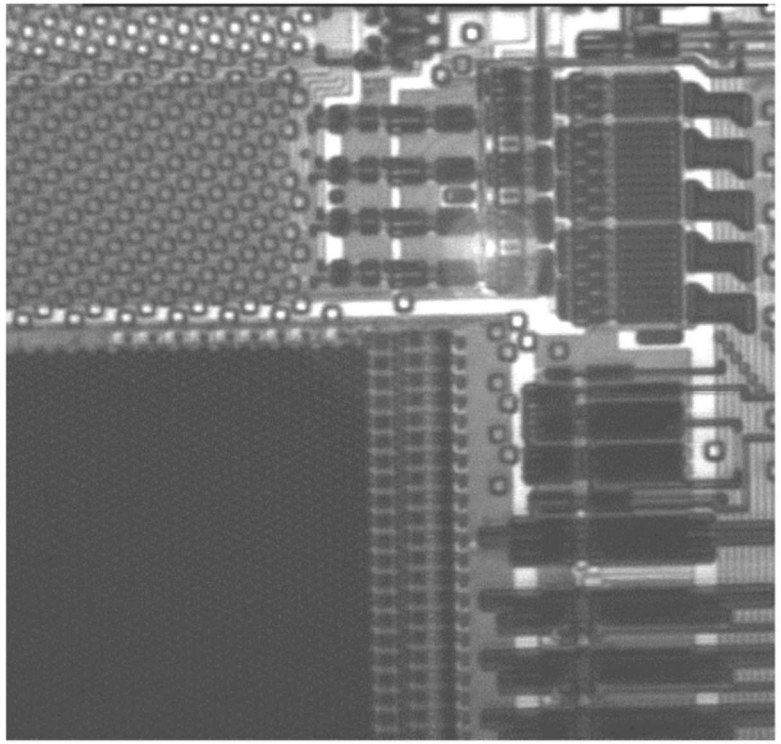
$\Rightarrow$ **sperical aberration increases with d_{Si}**

Zeiss IR Confocal Laser Scan Microscope (LSM), 1152 nm

100x/0.9, d=0.22mm, sph. corrected



100x/0.9, d=0.22mm, sph. *NOT* corrected



$p_{substrate}$ = 1x$10^{19}$$cm^{-3}$; d=220µm; 100x objective NA=0.9

Optical Image Formation from the Backside of the Die: Key Issues

$$res = \frac{0.61 \cdot \lambda}{NA}$$

λ (wavelength)

- **Surface roughness: rms < 5nm**
- **Reduced lateral resolution:**
  best image formation: confocal laser scanning microscope
- **Lens failure for large NA: sperical aberration use of a corrected microscope objective (100X) or thinning the die**

Backside Preparation Techniques

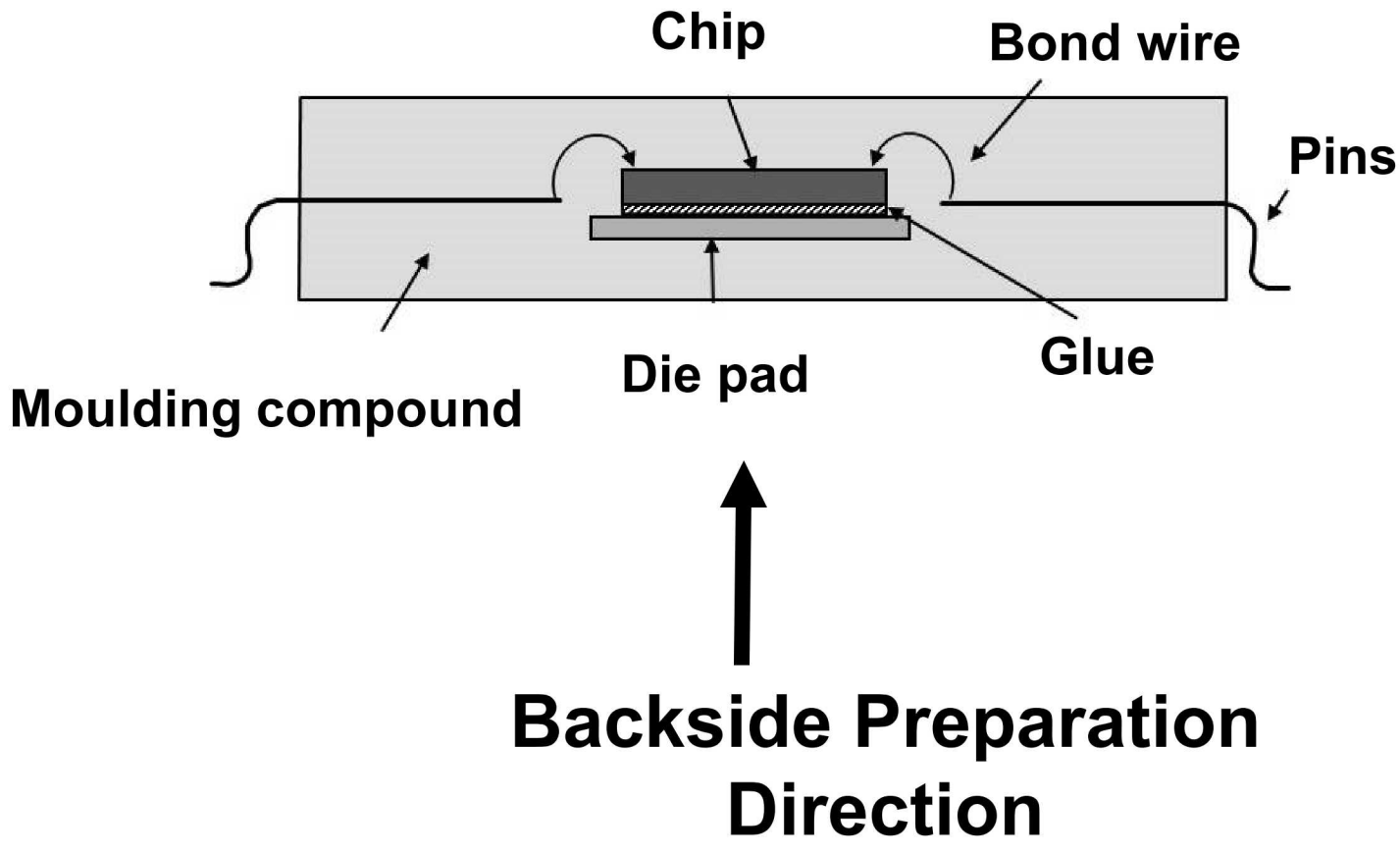
Global Si thinning

- CNC milling (Computer Numerically Controlled)
- mechanical grinding/polishing
- RIE (Reactive Ion Etching)

Local Si thinning/Precision probe hole milling

- FIB (Focused Ion Beam)
- LMC (Laser MicroChemical)

Cross-section : plastic package

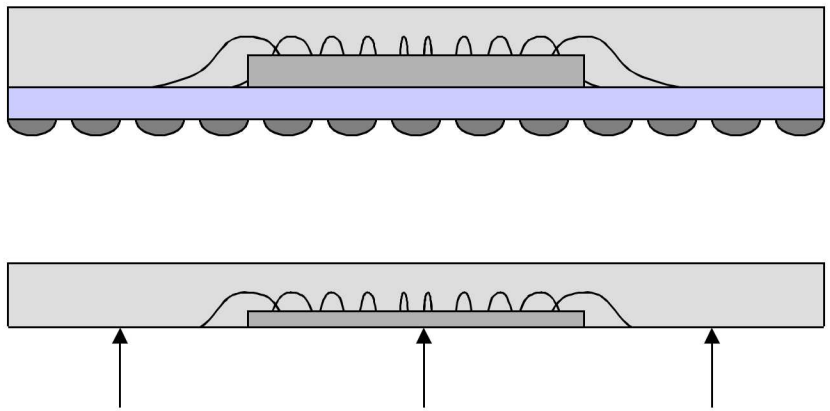


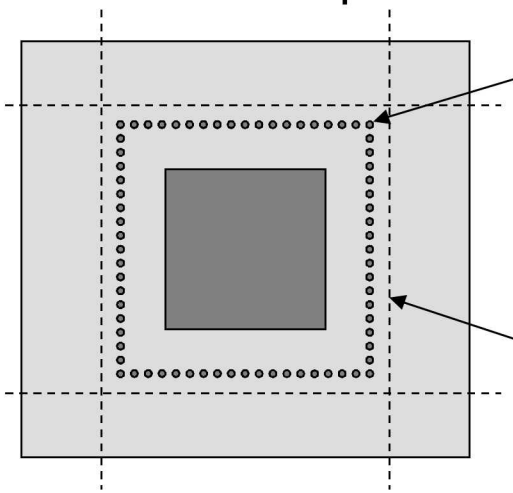
Maintaining Electrical Continuity

Step 1: Grind/polish through bumps and circuit board

Step 2: Cut excess material away from BGA (ball grid array) package

Step 3: Place remaining BGA package in PGA (pin grid array) package and rebond to exposed wire shafts

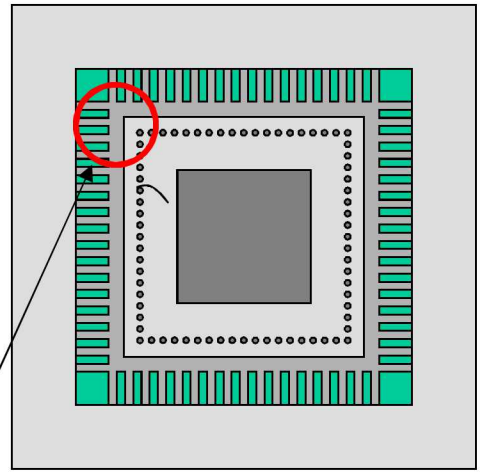


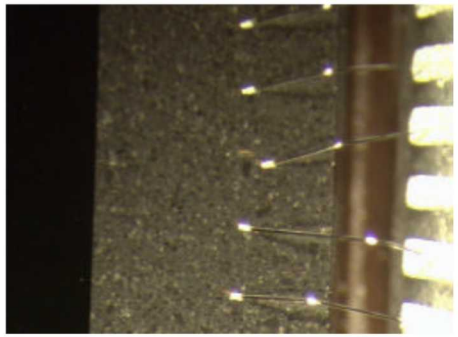


Exposed bond wire shafts

Package cut lines

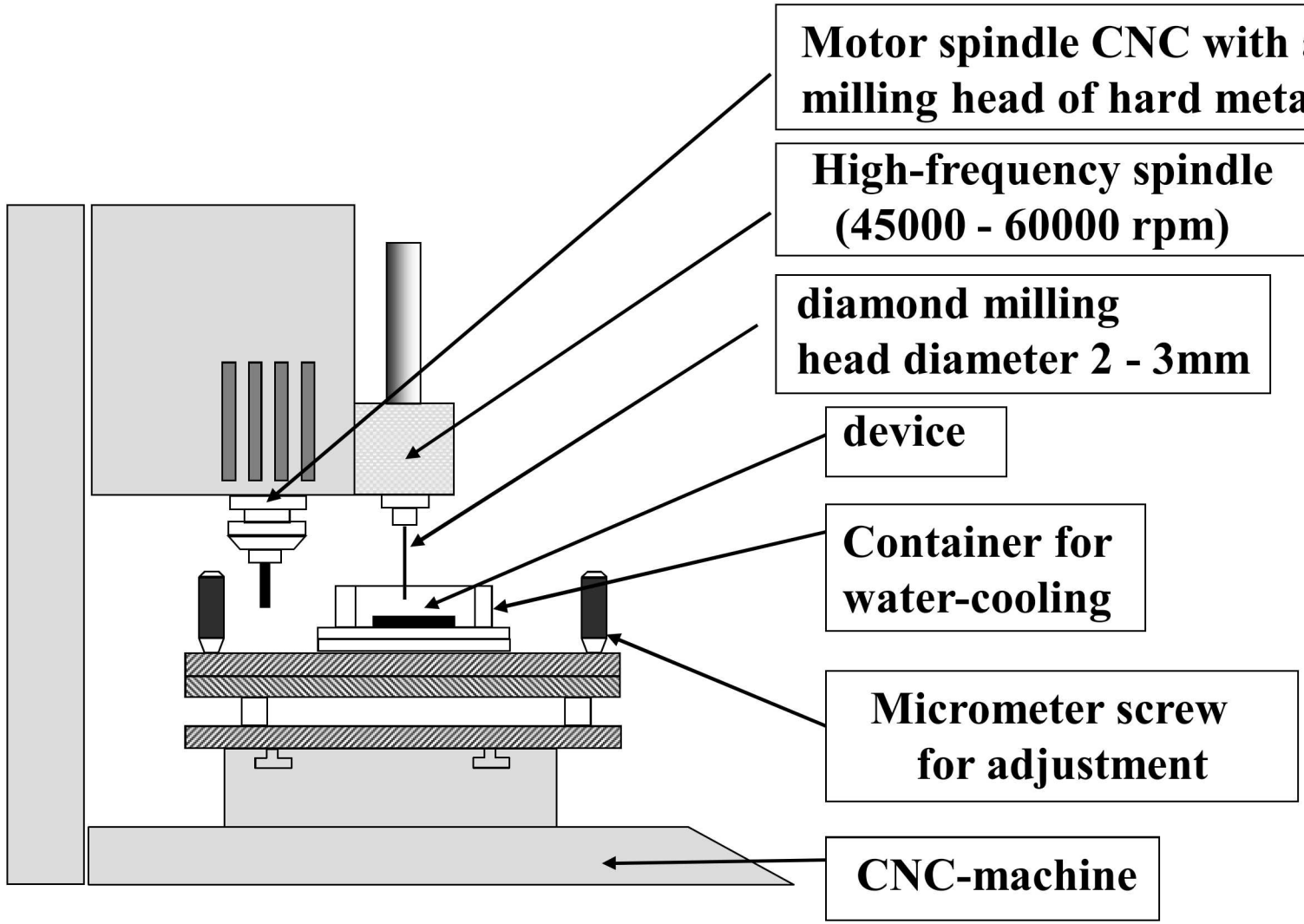
New bond wires



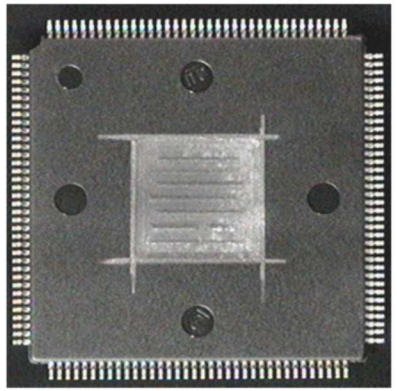


From: "BGA and Advanced Package Wire to Wire Bonding for Backside Emission Microscopy", Jim Colvin, ISTFA 1999, pp 365-374.

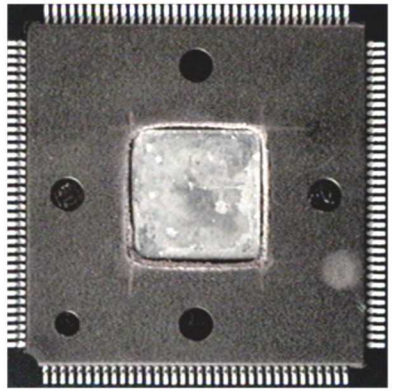
Schematic View of the CNC Milling Machine



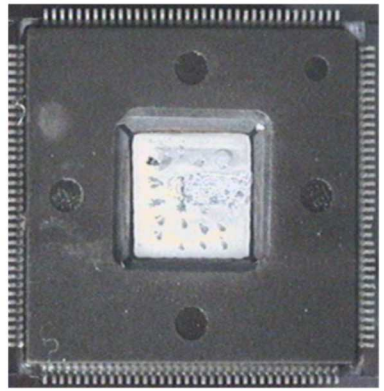
CNC Milling: Process Steps



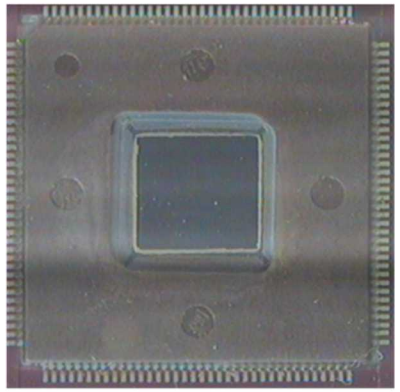
Chip size marked, plastic milled



Plastic removed down to the leadframe



Lead frame removed down to the glue



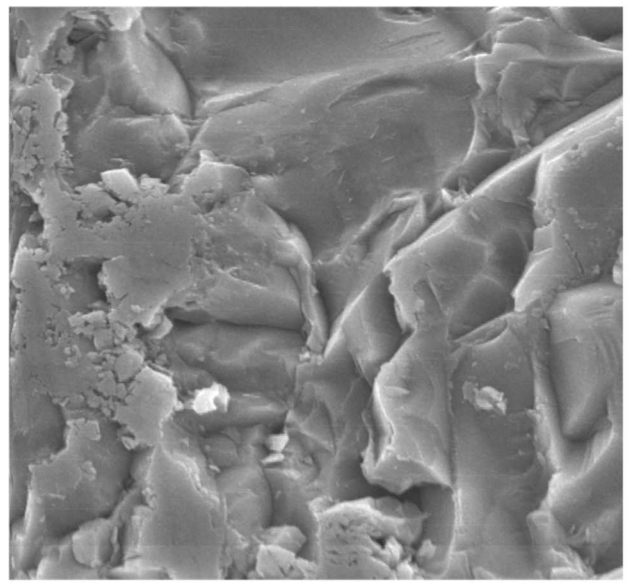
Glue removed

Milling of the Si substrate

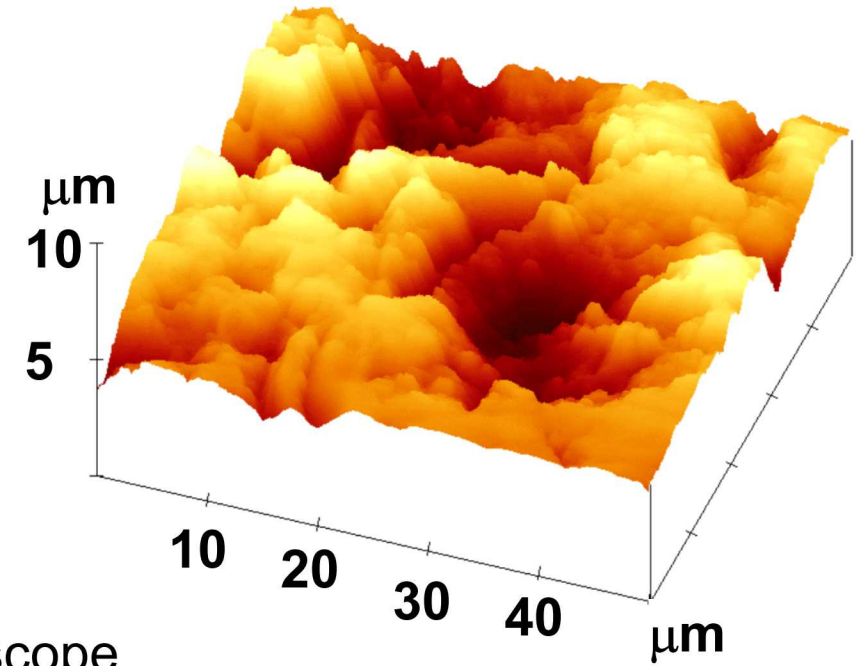
Si substrate polished

Si Substrate Surface after CNC Milling

SEM image (1500 x)

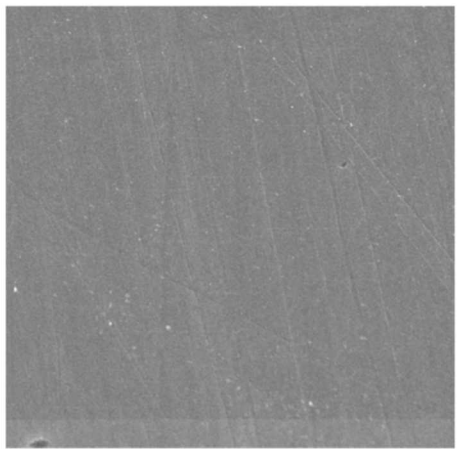


Surface topography (AFM)

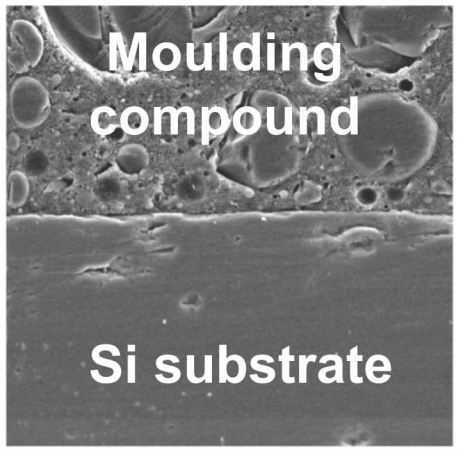


SEM-Scanning Electron Microscope
AFM-Atomic Force Microscope

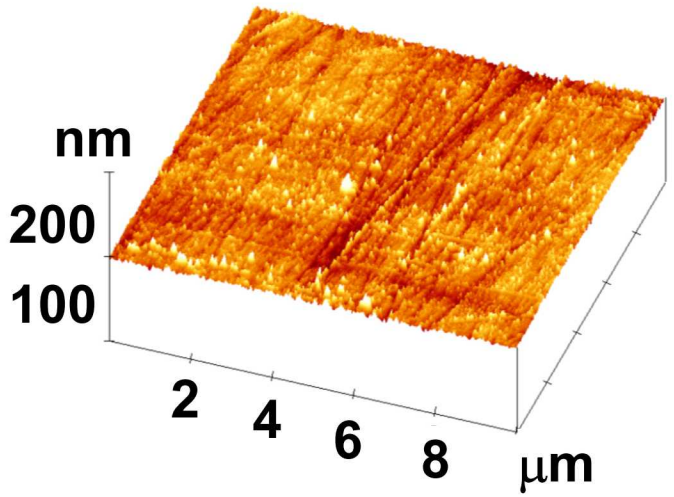
Si Substrate Surface after Mechanical Polishing



Si backside
SEM image
(700 x)



Si/Compound
Interface
SEM image
(1500 x)



Si Surface topography
(AFM)

CNC Milling

- Global thinning of Si
- min. remaining Si thickness: ca. 100 µm
    - Much thinner (~3 µm) has been demonstrated
- large areas >= 1 cm^2
- planarity/surface homogeneity preserved

(ca. 20 µm at 1 cm^2)

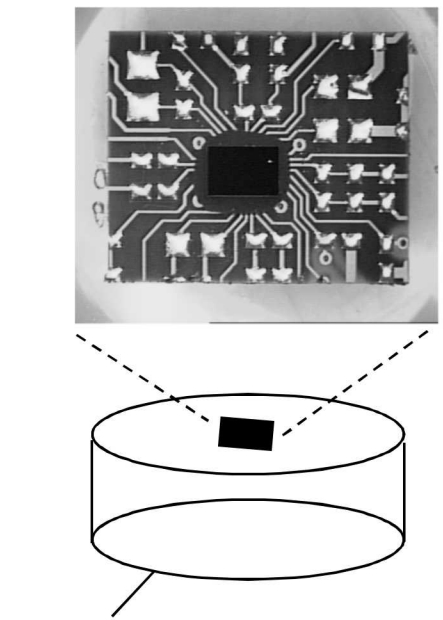
- surface roughness: rms <= 3-5 nm
- suited for packaged devices, flip-chips, wafer level

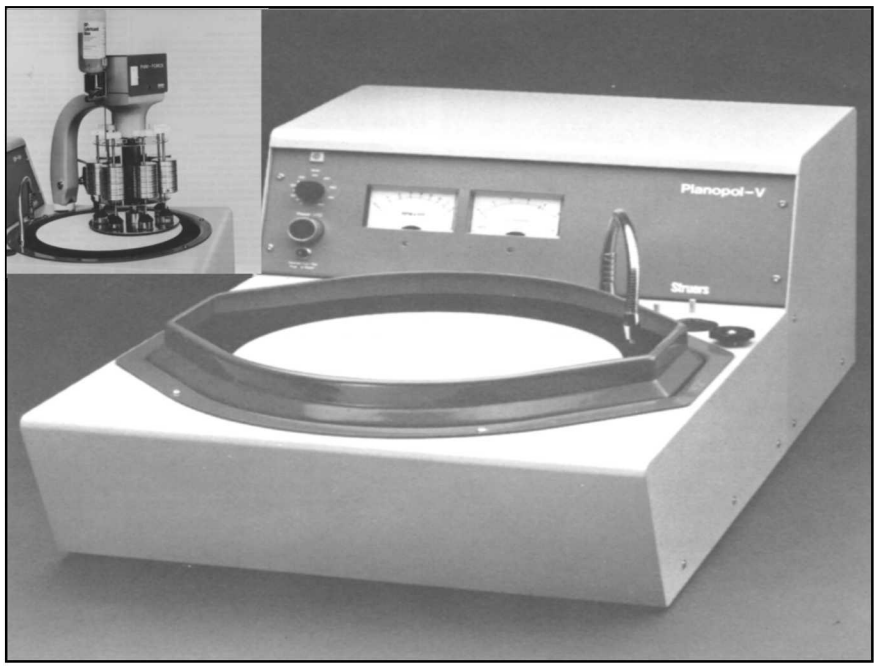
CNC Milling Advances

- Recent control from optical analysis
  - Maintain target thickness with controlled height
  - Improved polishing for SIL applications
  - Complements additional techniques
    - FIB, LMC, RIE, etc.
- Heated samples to reduce stress and curvature during milling
- See vendors for more details

Mechanical Grinding/Polishing

Encapsulated grinding

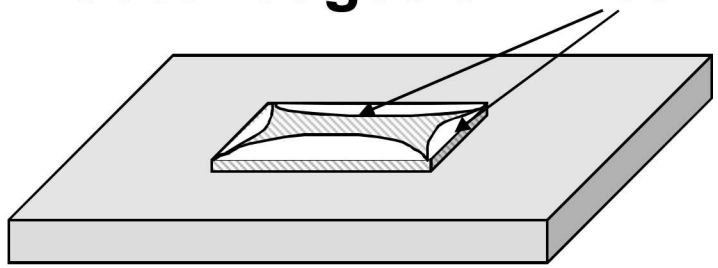




Grinding/Polishing

- Global thinning of Si
- min. remaining Si thickness: ca. 100 µm
- surface roughness: rms < 3-5 nm
- use for packaged devices limited
- major challenge: even surface

Outer edges thinned more than the center



Silicon Removal by Dry Etching

Requirements:

- High etch rates (> 10 µm/min)
- Highly reflective shiny surface after etching
- Uniformity
- Remaining Si thickness after etching ca. 100 µm
- Preserve chip functionality

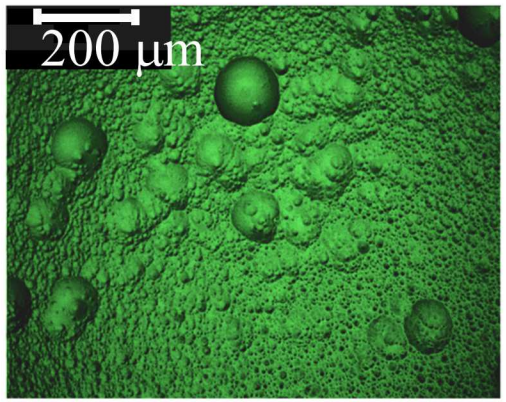
Solutions:

High etching rates due to high plasma density e.g.:

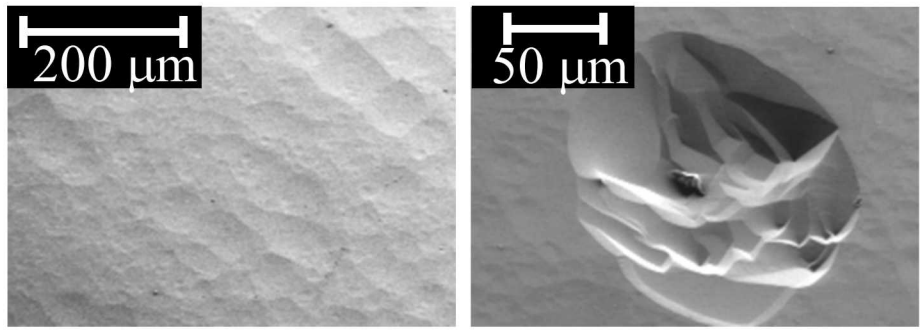
- Microwave plasma + RIE
- ICP (Inductively Coupled Plasma) + RIE
- ECR (Electron Cyclotron Resonance) + RIE

RIE - Backside Etching

Die thinned to 50 µm using a Nextral NE860 instrument, with a high density SF_6Plasma



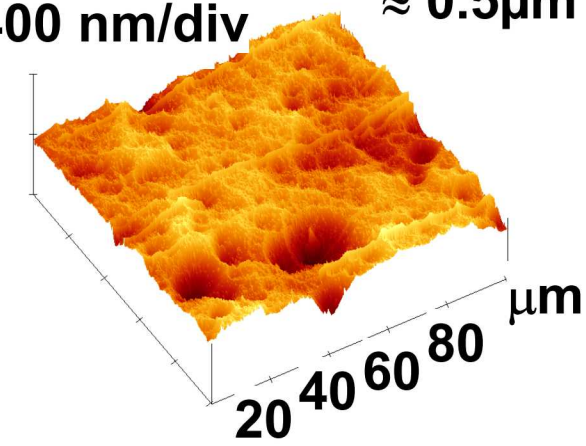
Surface in optical microscope



Surface viewed in SEM

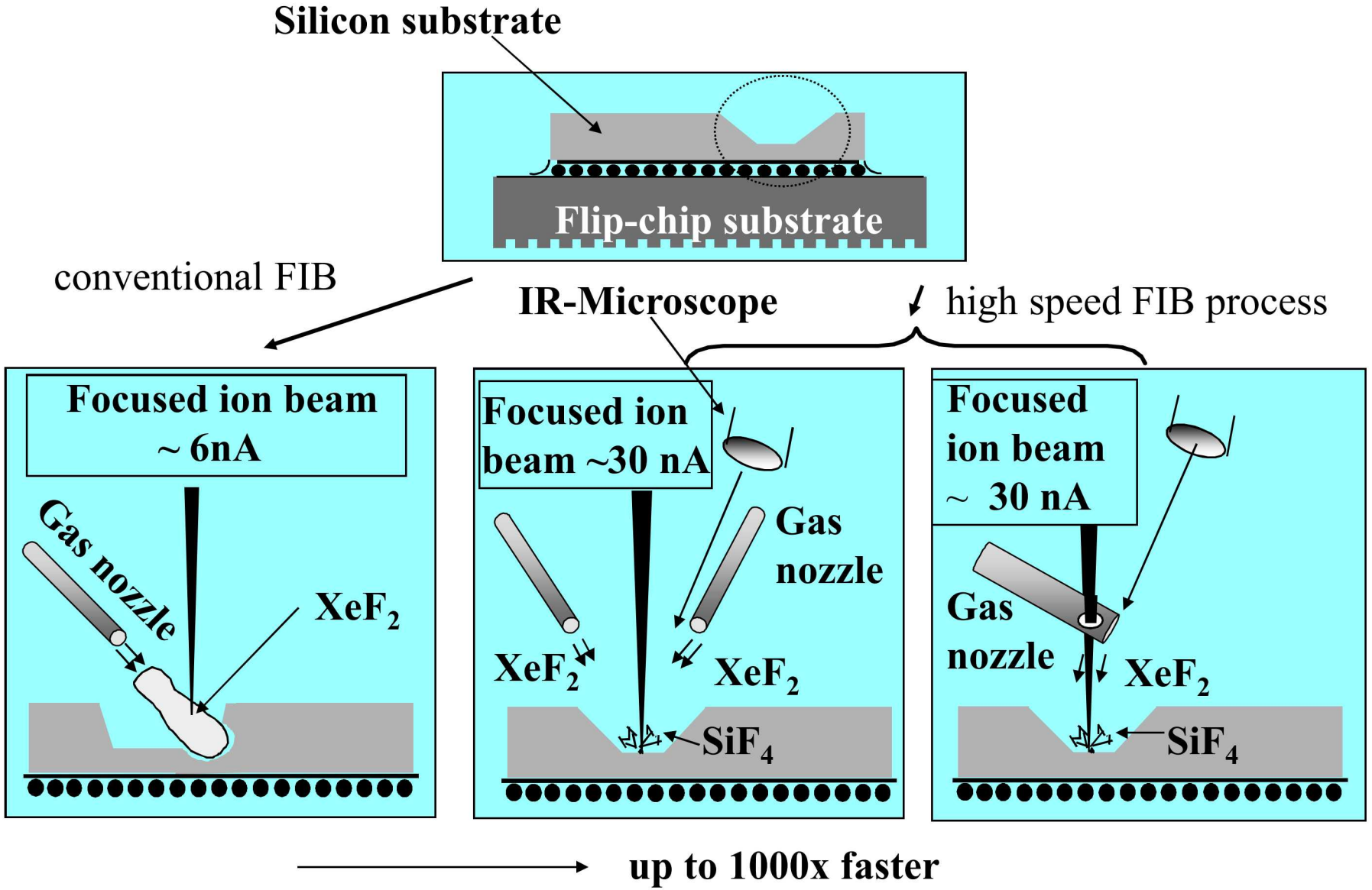
•AFM Topology peak to peak ≈ 0.5µm

X – 20 µm/div
Z – 400 nm/div

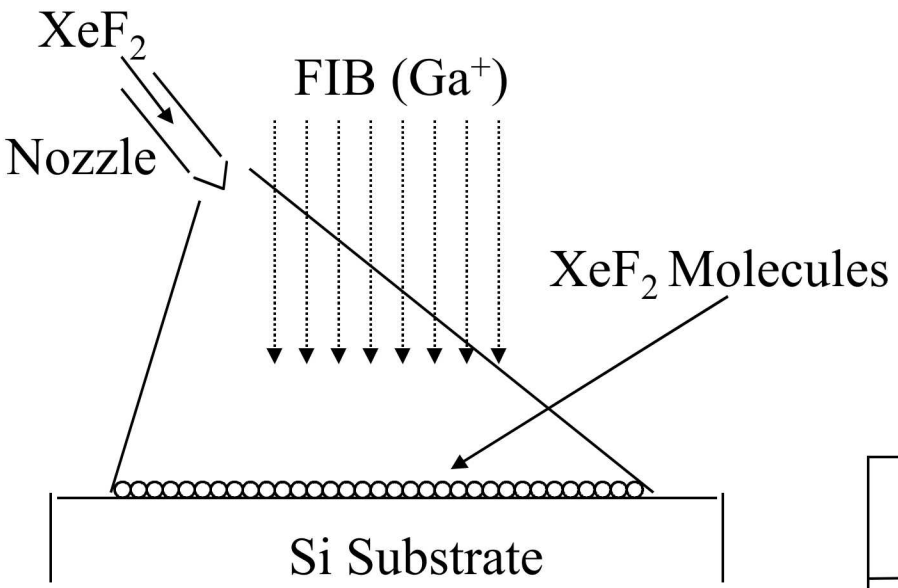


Adequate surface roughness is achievable

FIB


Silicon substrate
Flip-chip substrate
conventional FIB
IR-Microscope
high speed FIB process
Focused ion beam
~ 6nA
Gas nozzle
XeF2
Focused ion
beam ~30 nA
Gas
nozzle
XeF2
XeF2
SiF4
Focused
ion beam
~ 30 nA
Gas
nozzle
XeF2
SiF4
up to 1000x faster

Gas-Assisted Etching (GAE) of Si with FIB



- Enhanced material removal
- no redeposition
- selectivity

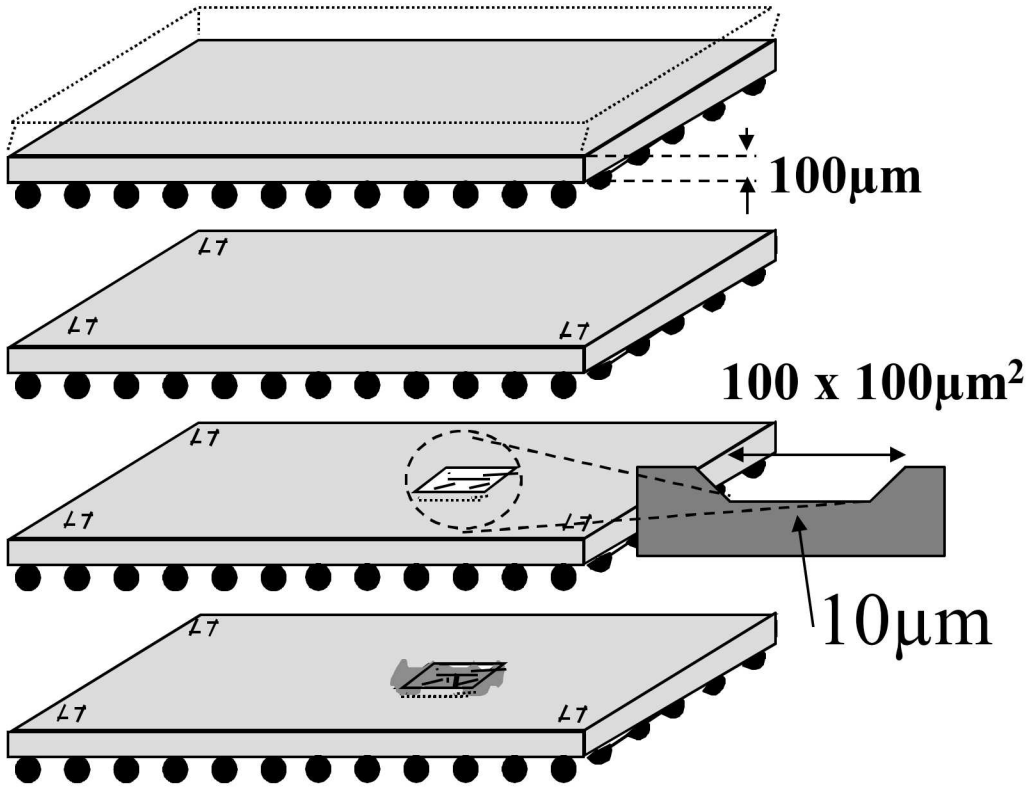
Relative GAE Selectivity

	Al	W	Si	SiO_2/Si_3N_4
XeF_2	0	>10	>10	>10

(FIB assisted) surface reaction:

$$Si + 2\,XeF_2 \xrightarrow{(Ga^+)} SiF_4\uparrow + 2\,Xe\uparrow$$

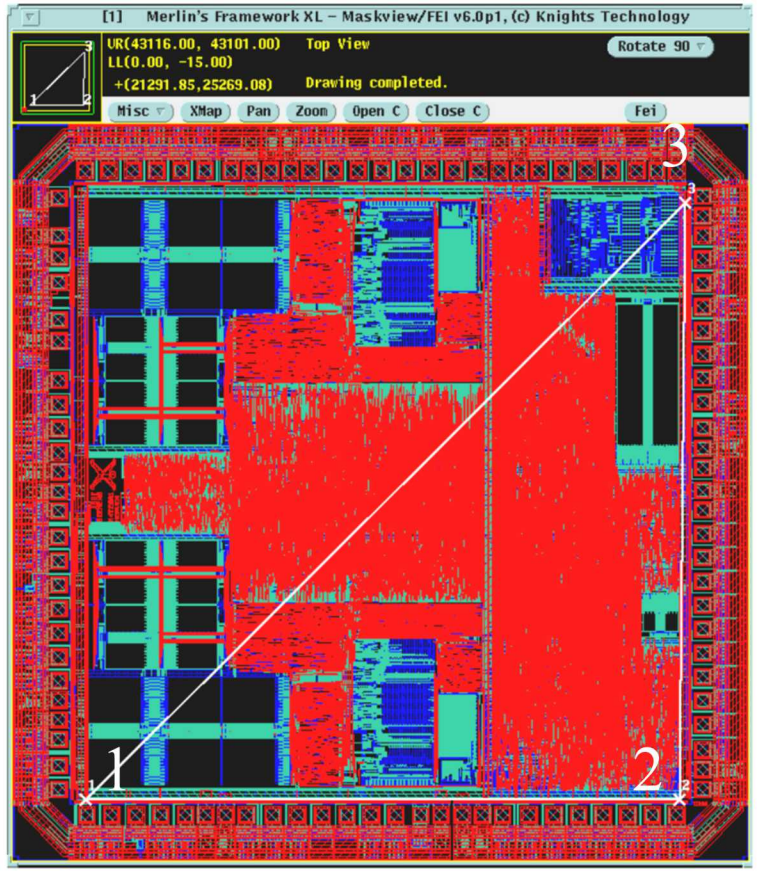
Backside FIB Preparation

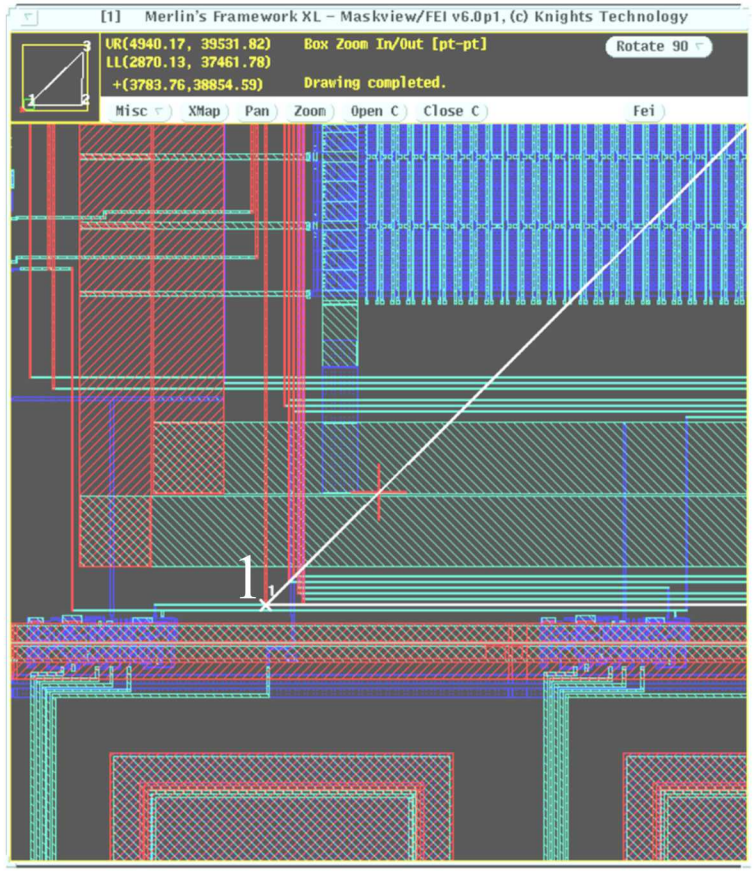


1. Global Si thinning
2. Identification of alignment points for CAD (Computer Aided Design) navigation
3. Local Si thinning with high-speed FIB etching process (time required: ca. 10 min)
4. Precision Probe hole milling with FIB

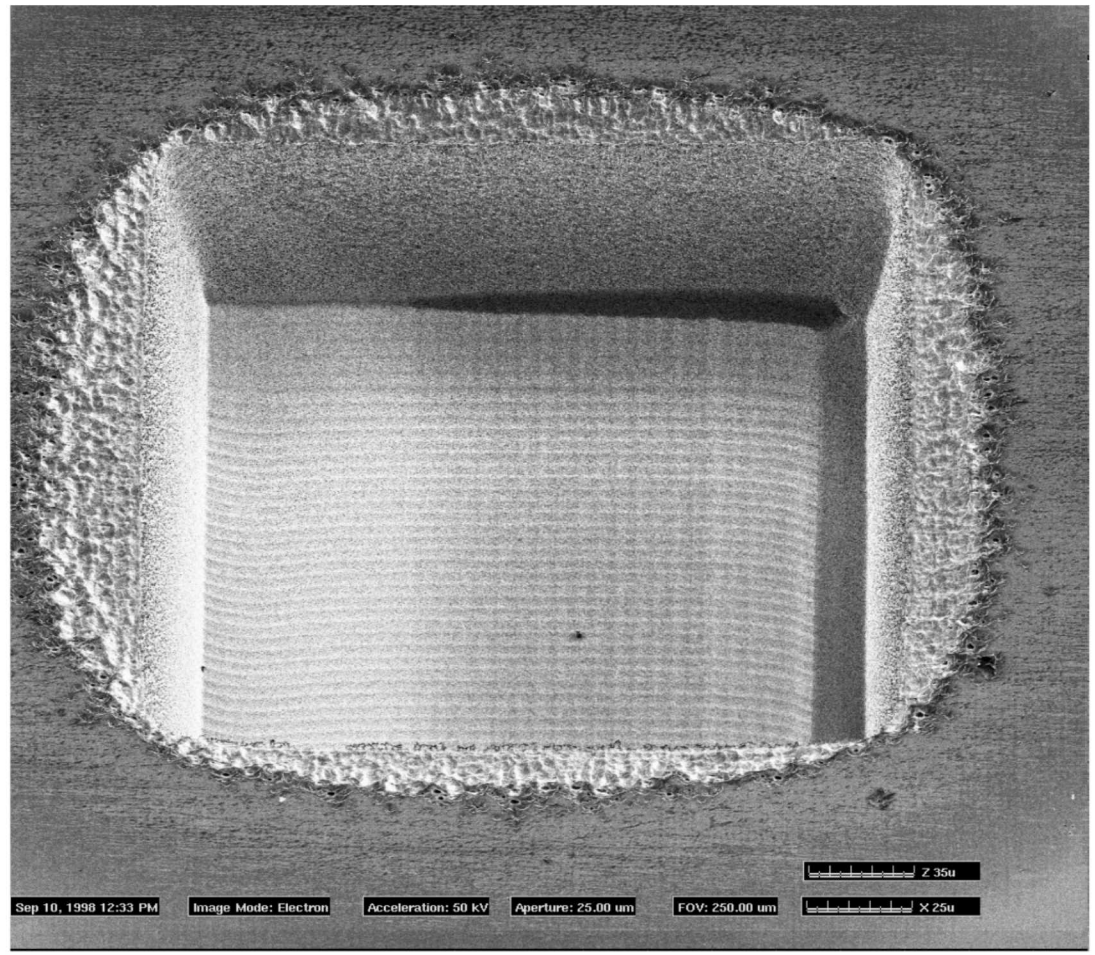
Supporting Navigation by Correlating to CAD-Data

3 Point Alignment of Layout to x-y-table of FIB using CAD-Navigation



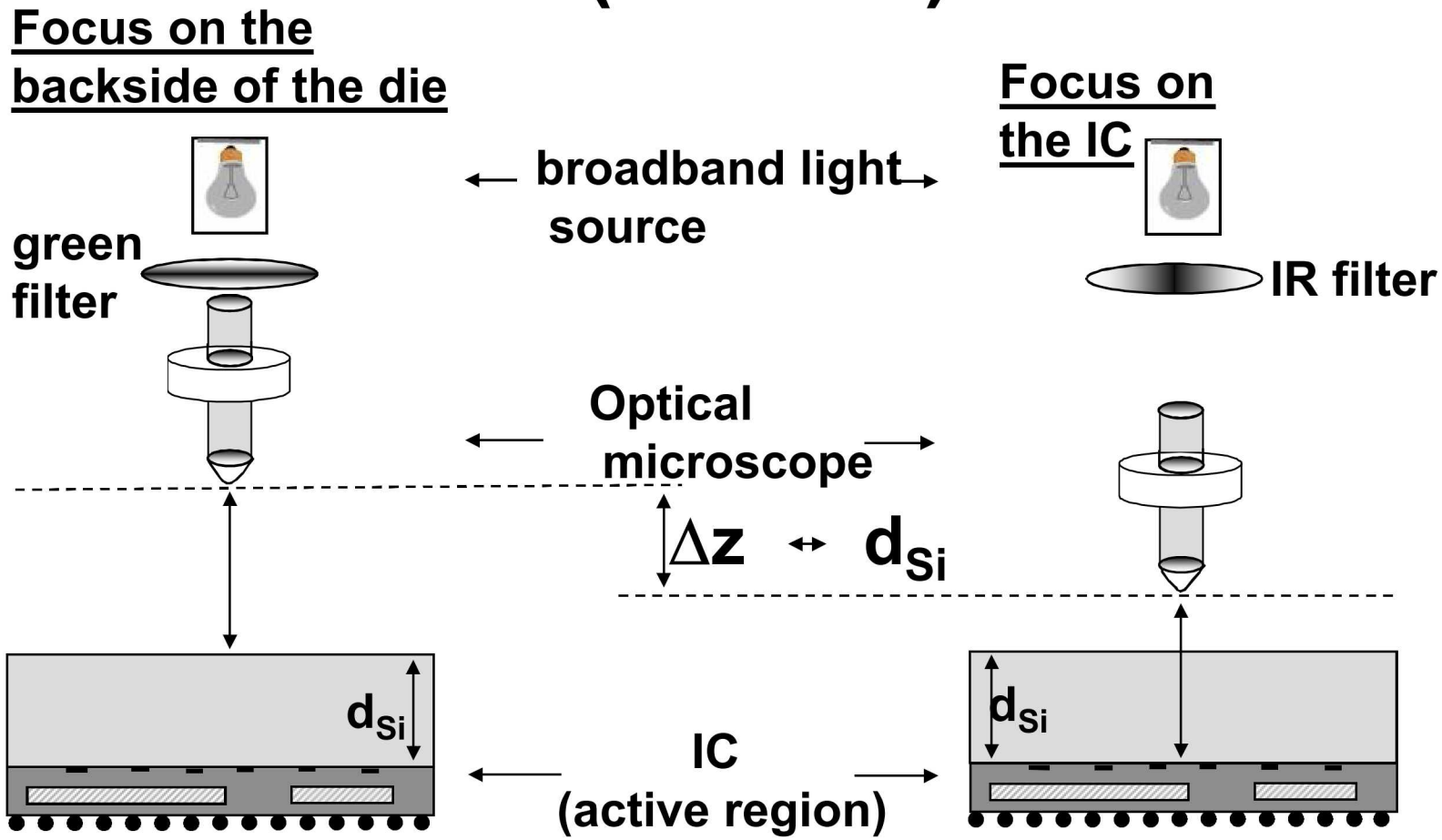


FIB Etched Trench (Micrion)

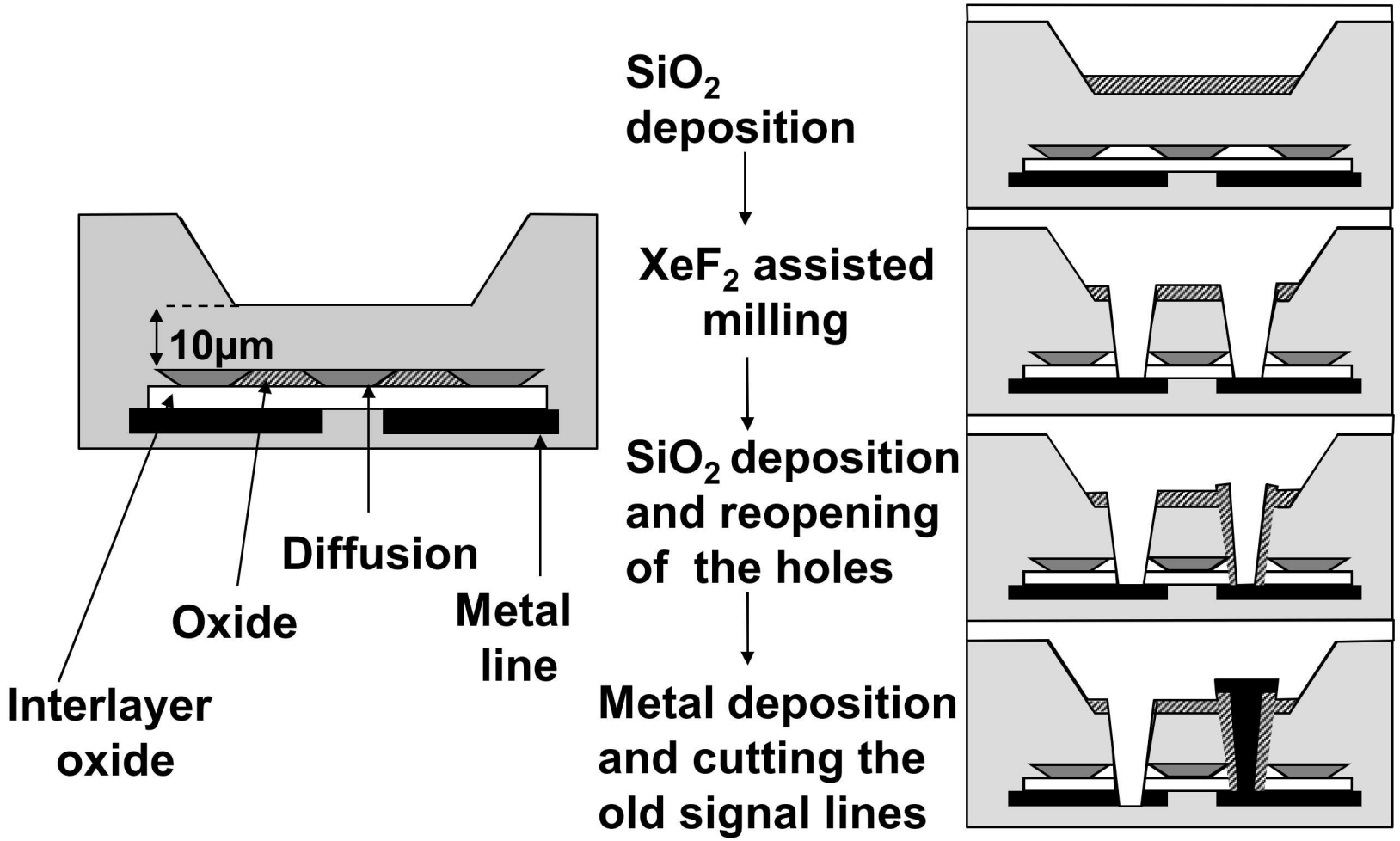


$p_{substrate} = 1x10^{19}cm^{-3}$

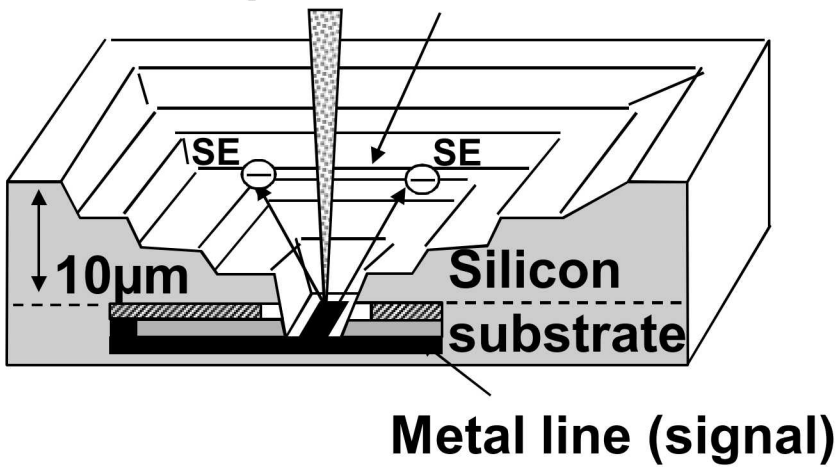
Endpoint Detection with FIB (Micrion)

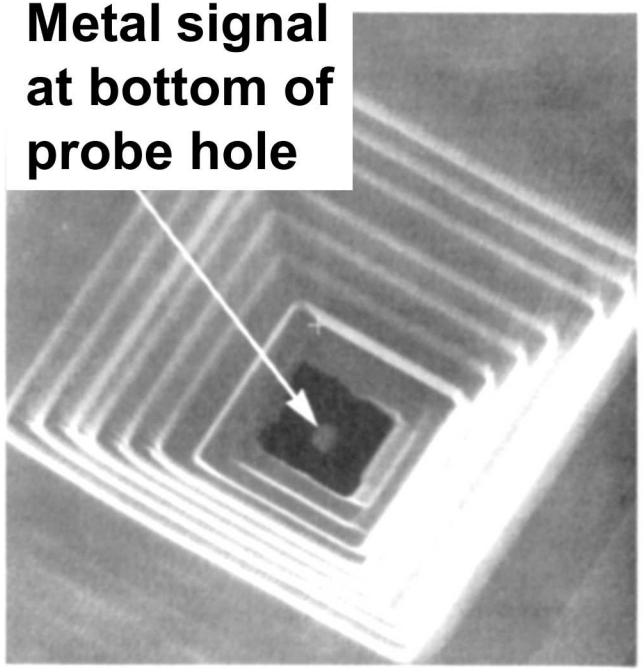


Precision Probe Hole Milling



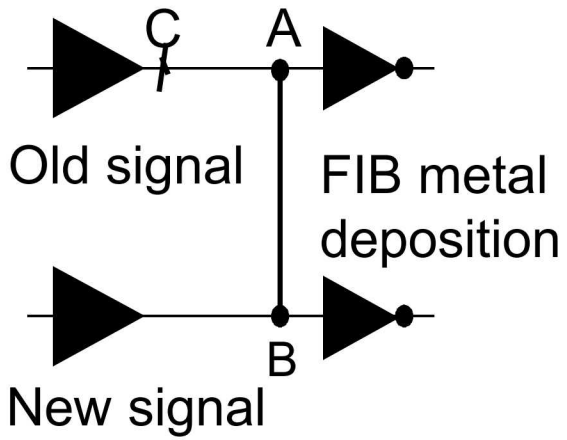
FIB Precision Probe Hole

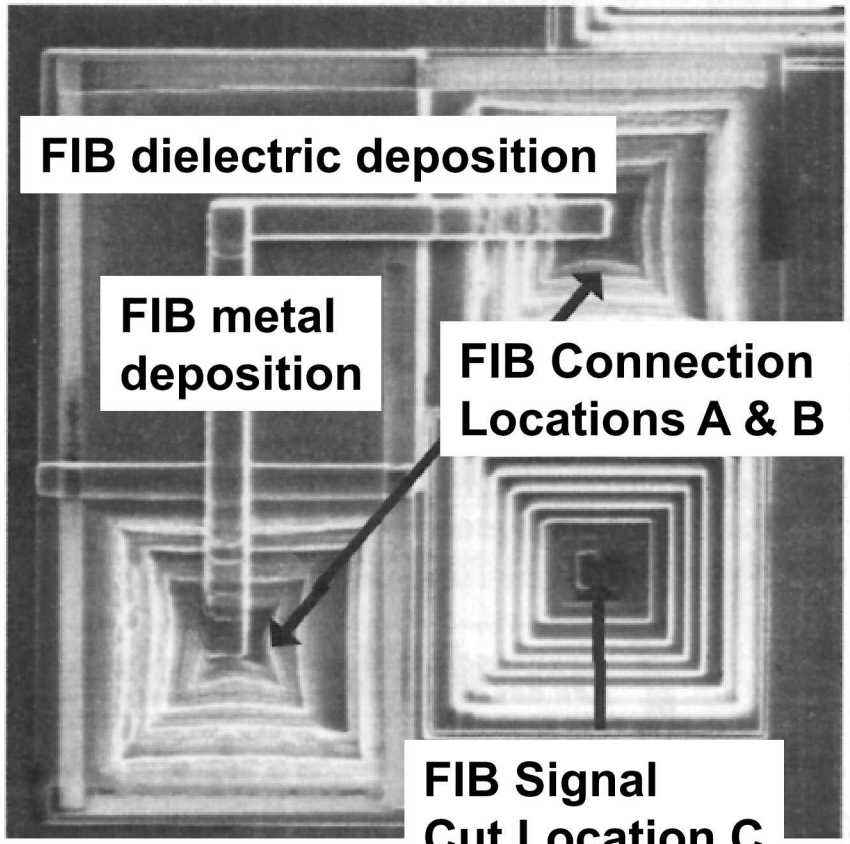




Device Modification from the Backside of the Die

Circuit Edit Schematic





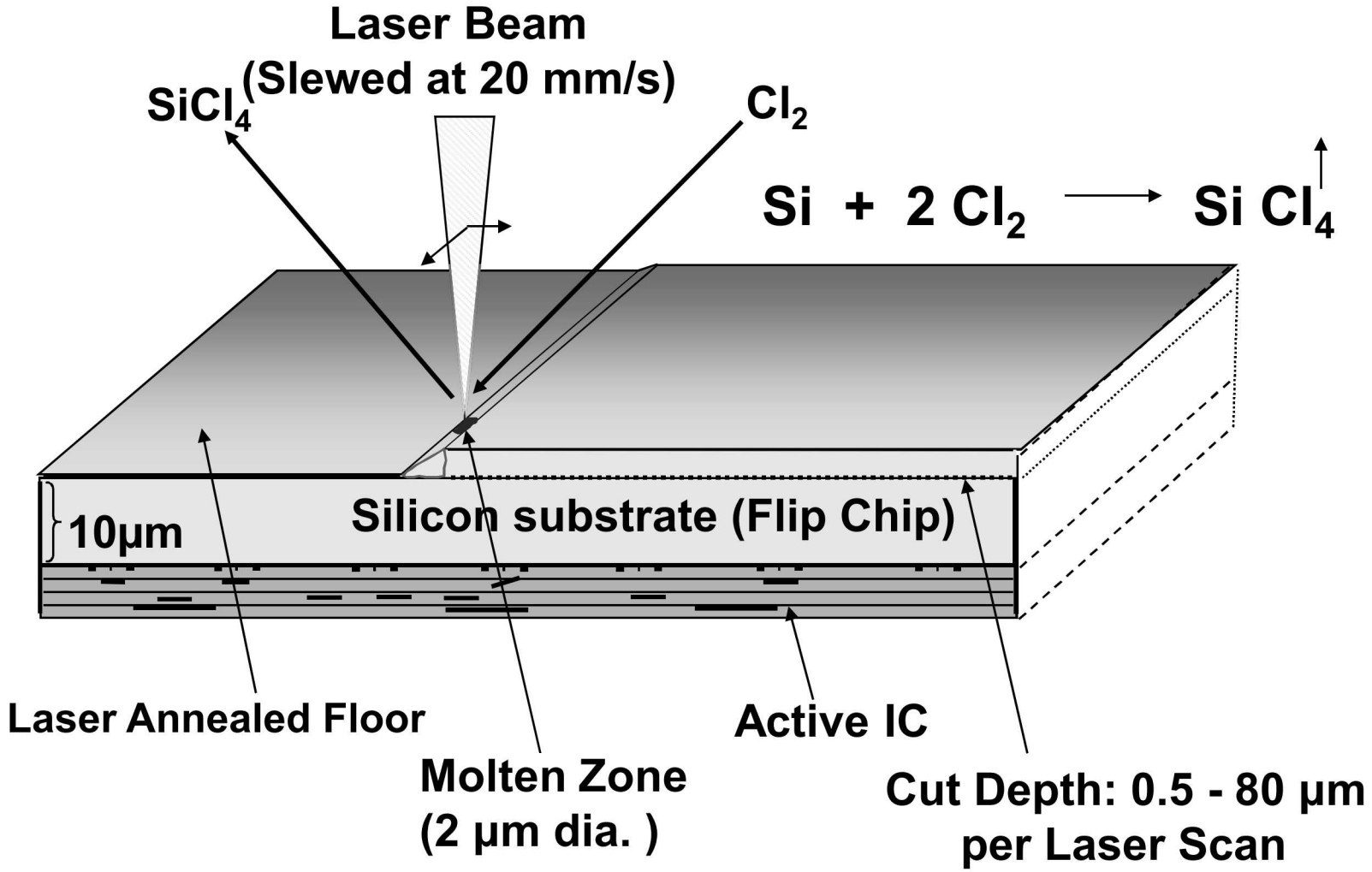
FIB for Backside Preparation

- Applications of FIB for backside FA
  - •device modification mechanical or e-beam probing

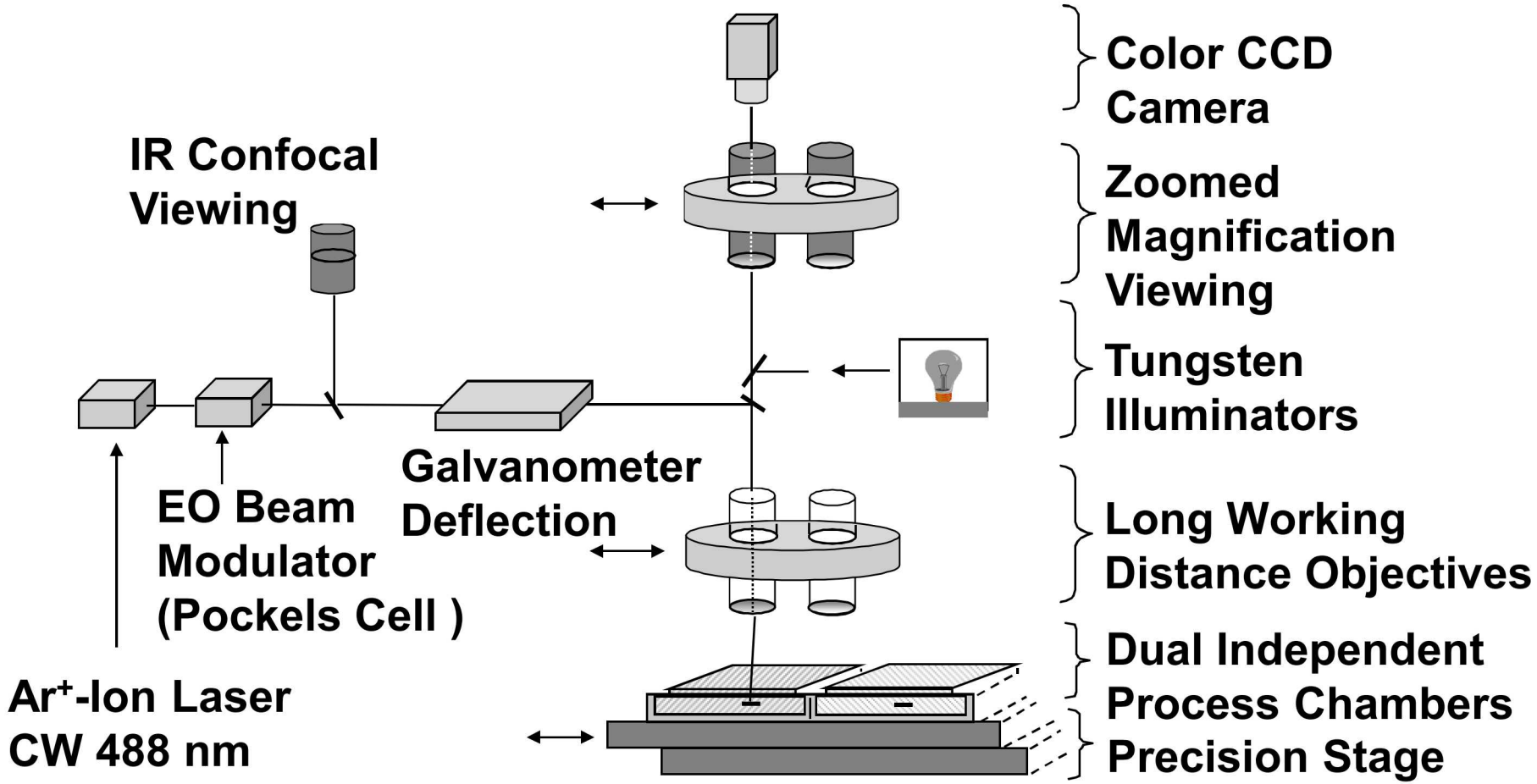
- High speed FIB etching process: local thinning of Si (typically 100 x 100 μm^2)

- Precision probe hole milling similar to standard FIB frontside process with spatial resolution < 0.1µm → FIB is the **most precise** tool for backside preparation

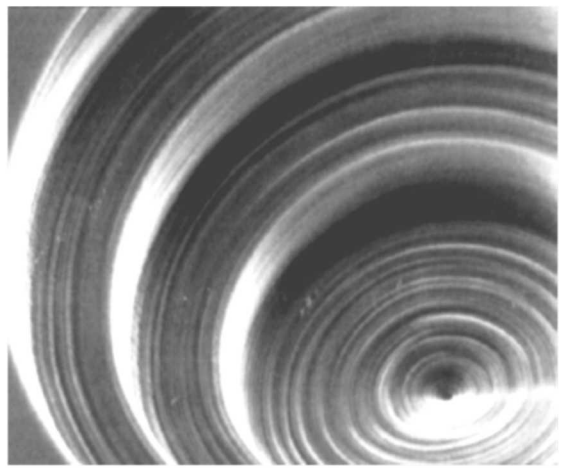
Laser MicroChemical (LMC) Etching



Schematics of Setup for LMC Si-etching

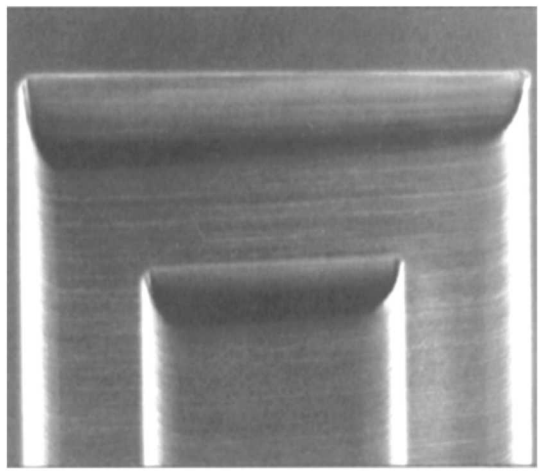


LMC Etching and Deposition



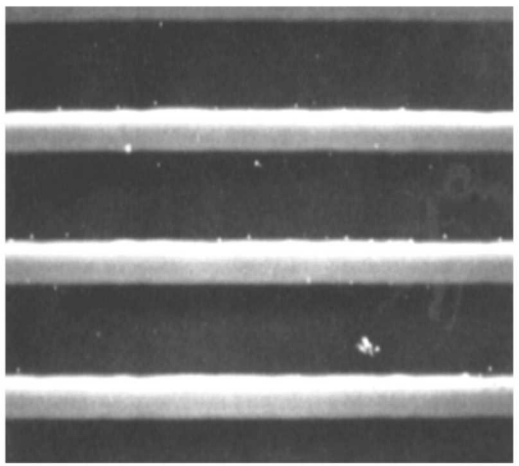
10µm

Silicon etch at
100000 µm^3/s



10µm

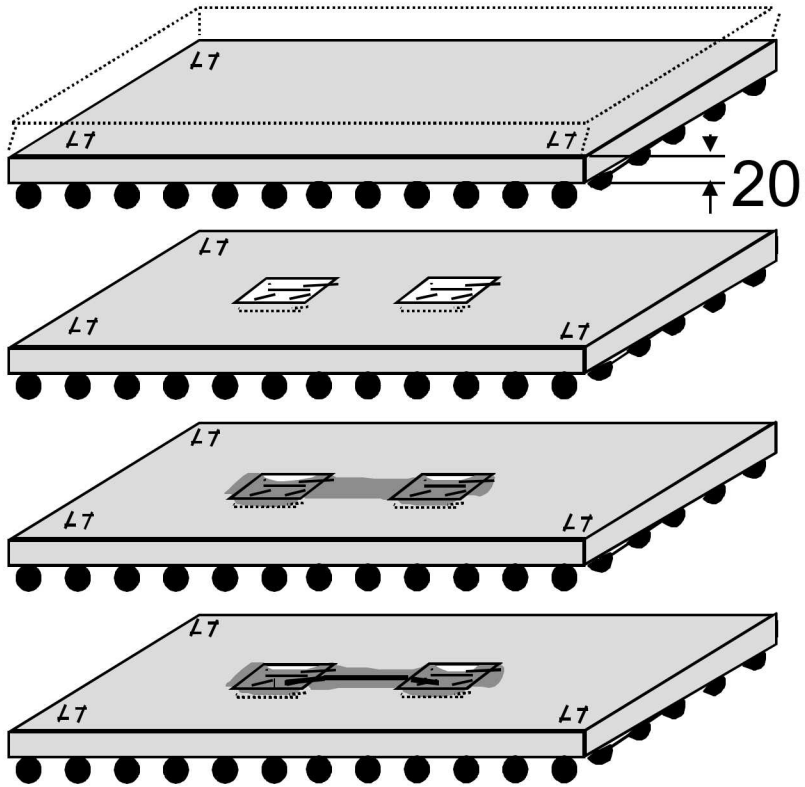
Silicon etch at
100000 µm^3/s



10µm

Platinum deposition at
100 µm/s

LMC Process for Backside FA Applications



1. Global thinning of Si (e.g. CNC milling); LMC reveals alignment fiducials;

2. LMC etching of trenches over the regions of interest (typical area 500 x 500 µm^2)

3. Deposition of a dielectric isolation e.g. laser deposited oxide

4. Local repairs at the base of the isolated trenches typically using a FIB. For longer interconnects (interconnects between trenches), laser deposition is used.

Benefits of LMC Technique

- Speed enhancement of several orders of magnitude (microchemical reaction) compared to FIB
- Process spatial resolution $\Delta x, \Delta y <= 0.5\mu m$
  $\Delta z <= 0.1\mu m$: endpoint detection via OBIC (Optical Beam Induced Current)
- Surface roughness achieved:rms typically 30nm
- Applications for backside FA: in combination with FIB sample preparation for e-beam/mech. probing and device modification
- outlook for backside FA: optimization of the illuminated image and signal strength for various backside localization techniques

Ultra-Thinning Motivation

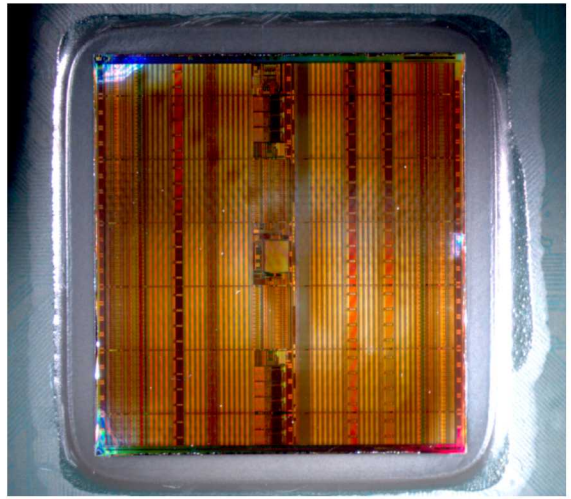
Thinning silicon devices

- Established methods include lapping, milling, etching, etc.
- Typical target RST > 50 µm
- Suitable for larger node sizes or older technology

Changes in semiconductor industry

- Node sizes are approaching 7 nm
  - No longer able to enhance numerical aperture
  - Reductions in wavelength needed to keep optical circuit analysis tools viable at advanced technology nodes
  - Shorter wavelength requires thinner silicon
- Stacked Die
- Die are thinned before dicing/packaging
  - More bow due to strain

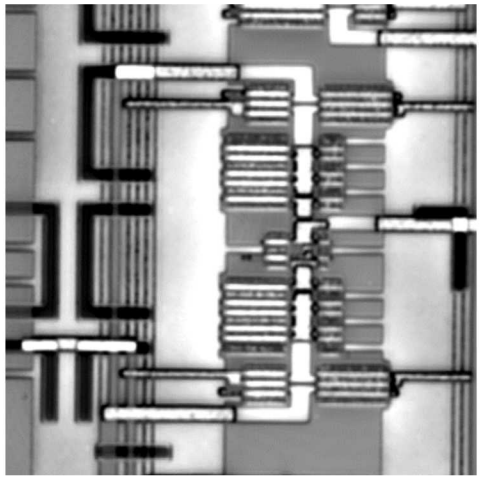
Ultra-Thinning Results



Optically transparent
- Regions of interest

Utilize visible light
- < 700 nm

Enhanced spatial resolution
- Feature sizes < 200 nm



1320 nm

633 nm

Improved Spatial Resolution

Global Thinning

Adaptive Milling

- Multi-axis mills
  - 3-axis and 5-axis
  - Silicon is removed in iterative steps using a grinding bit
  - Diamond embedded bits for grinding and cloth covered bits for polishing
- Use optical thickness metrology measurements to provide feedback

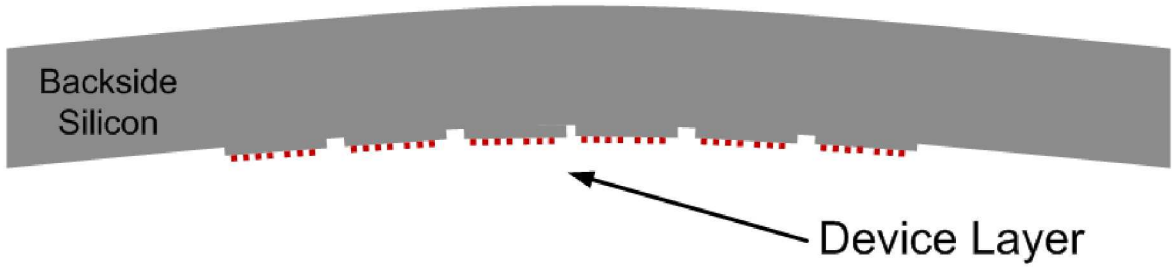
Global lapping

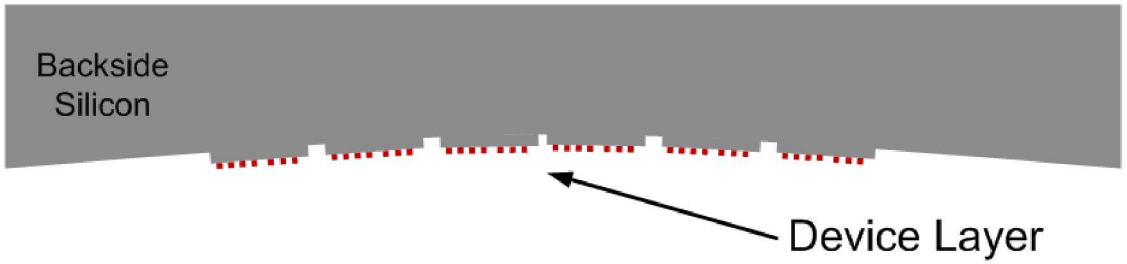
•Diamond Lapping films and polishing slurries

- Fine polishing or course material removal depending on slurry and lapping film parameters

•Rotating platen and head

•Variable downforce and speeds





Ultra-Thinning by Adaptive Milling

Uses

Mill small areas 3 x 3 mm^2

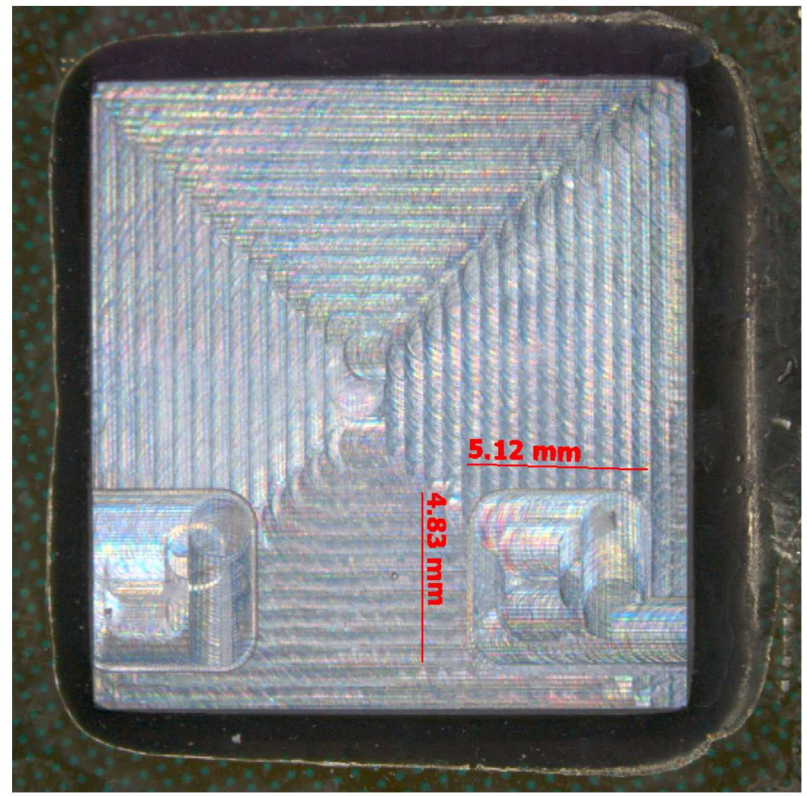
Results

3 µm +/- 1.5 µm

Limitations

Milled region must be accessed from die edge

Polishing difficulty



Ultra-Thinning by LMC

Typical Process

Pyrolytic

532 nm Laser (green light)

Chlorine gas

Integrated spectrometers

Endpoint capable

Uses

Silicon etching of small areas ≤ 3-4 mm^2

20x Faster than Gas Assisted Focused Ion Beam (FIB)

Results

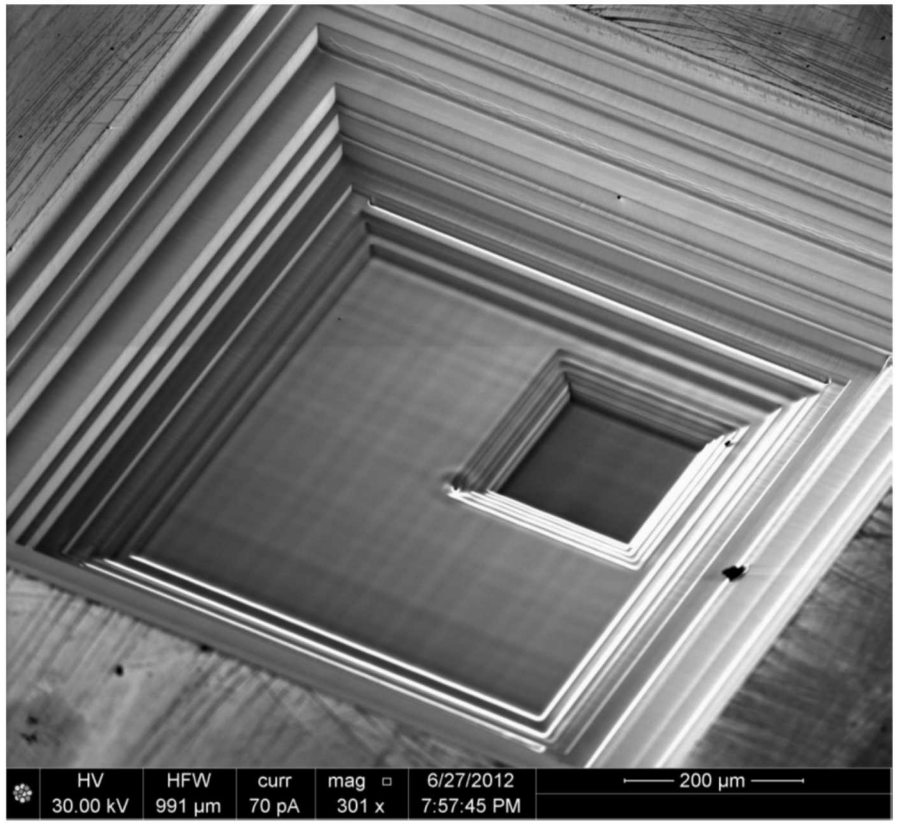
1 µm +/- 1 µm

Clean smooth surface finish ~ 200 nm

Limitations

Localized heating can cause preferential etching

Chlorine environment



Global Thinning - Etching

Reactive Ion Etch (RIE) System

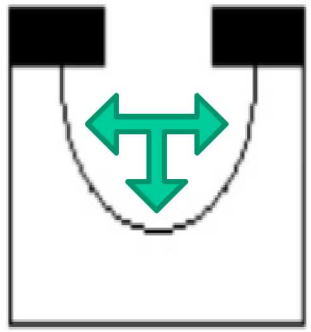
- Plasma etch (Pressure & DC bias control)
- Isotropic or Anisotropic etch profile
- Various gases – SF_6, CF_4, CHF_3, O_2, N_2, Etc.
- Endpoint detection

Uses

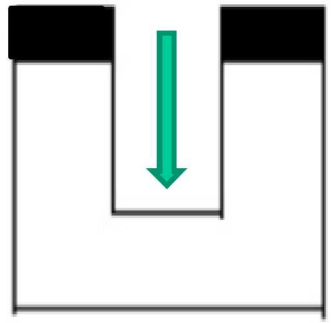
- Etches silicon, dielectrics, metals, photo resist
- Stable Si Etch rate - 1 µm/min

Results

- 2 µm +/- 1.5



Isotropic



Anisotropic

Limitations

- Pre-thinning necessary using other methods
- Thermal Issues
- Ion-induced damage potential ~ 100 nm deep
- Non-volatile materials can result in micromasking or rough surfaces
- Clean pre-etch surface necessary

Local Thinning - Etching

Reactive Ion Etch (RIE) System

Uses

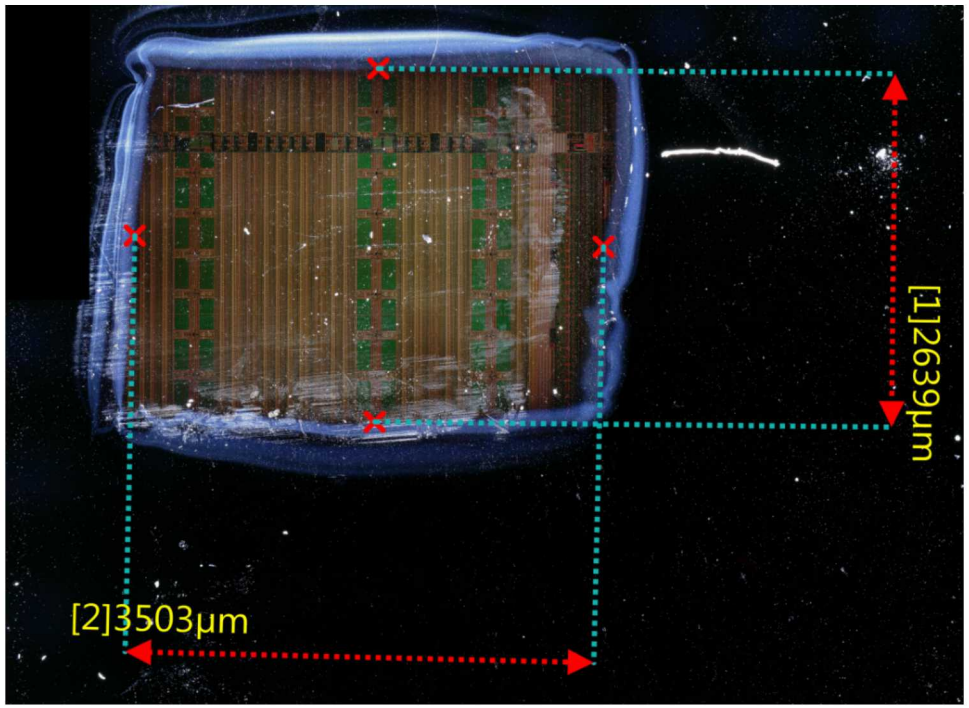
- Etch unmasked area

Results

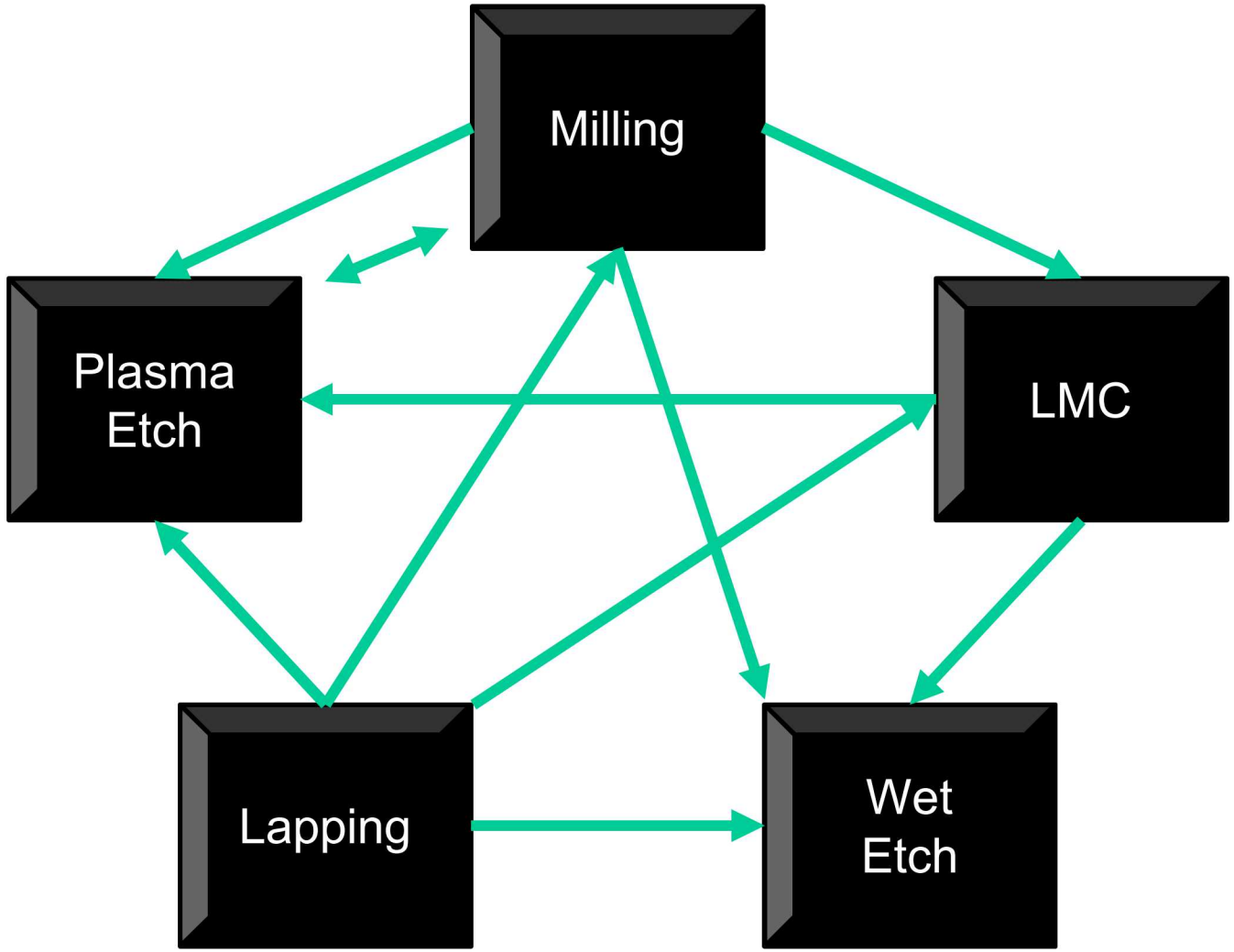
- 1 µm +/- 0.5 µm

Limitations

- Pre-thinning necessary using other methods
- Thermal Issues
- Ion-induced damage potential
- Non-volatile materials can result in micro-masking or rough surfaces
- Clean pre-etch surface necessary



Hybrid Methods

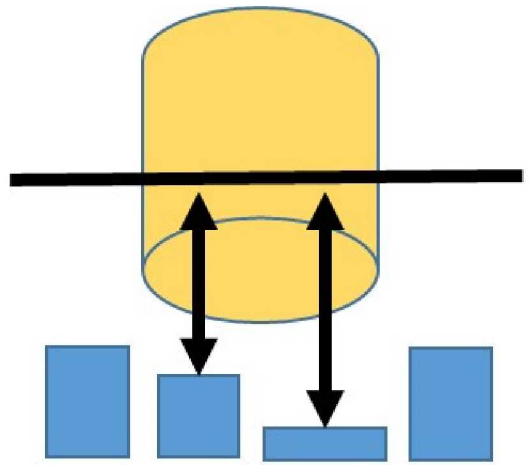


- Combination of processes
  - based on end goals
  - dictated by physical constraints
  - Limited by available methods
  - Reliant on technical expertise

Ultra-Thinning Challenges-I

Metrology

- Multiple factors create non-ideal measurements
  - Varying underlying layer depth within area leads to accuracy uncertainty
  - NIR wavelengths reach limits around 5 µm RST
  - Visible wavelengths are absorbed in thick Si measurements
  - High dopant densities cause signal attenuation
    - Block measurements in relatively thick silicon
- High confidence in measurement data is difficult
  - Requires metrology tool technical master
  - Requires cumulative knowledge of metrology/sample interactions
    - Different samples interact differently with the metrology tools
    - Due to factors explained above



Ultra-Thinning Challenges-II

Uniformity

- Maintaining uniformity while silicon relaxes during bulk removal
- Loss during polishing

Subsurface damage

- Up to ~ 5 μm

Control

- Limitations with direct mechanical positioning
- Rigidity, vibration, tolerances of motors & spindles
- Grinding bit diameters, grit sizes, bit wear
- Variable etch rates

Cost and Sources

- Expensive tools - $25K – 1.2M
- Limited suppliers available

Ultra-Thinning Considerations

- Multiple methods to achieve ultra-thin silicon
  - Global and Local
- Hybrid methods may be required to reach end goal
  - Dependent on available tools
  - Limited by staff expertise
- Multiple challenges in producing ultra-thin devices
  - Different technologies
  - Variety of packages
- Nuanced and specialized
  - Each type of sample requires a customized approach

Backside Preparation Techniques

Global Si thinning

- CNC milling
- mechanical grinding/polishing
- RIE

large areas >=1 cm^2
min. remaining Si thickness: ca. 100µm

Local Si thinning

- LMC technique
- FIB (high speed process)

areas up to 500 x 500 $µm^2$
min. remaining Si thickness: ca. 10µm
spatial resolution limited (ca. 1 µm)

Precision probe hole milling

- FIB

high spatial resolution (ca. 0.1 µm)

Ultra-thinning

- Global andl local

facilitates shorter wavelength light examination

Conclusions

- Growth of flip-chip packaging and multi-level metallization processes drives development of backside preparation and analysis techniques
- Major capabilities rely on enabled photon analyses
  - Light emitted by the circuit, changes in operation from light, changes in detected optical properties
- Continued use and development of techniques for the foreseeable future
  - Sample preparation
  - Sample analysis