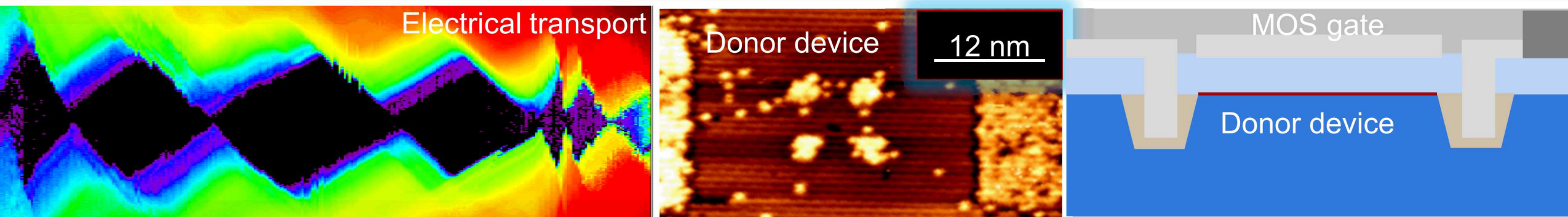


Electrical transport of single electrons in a surface-gated atomic crystal

10/10/2019

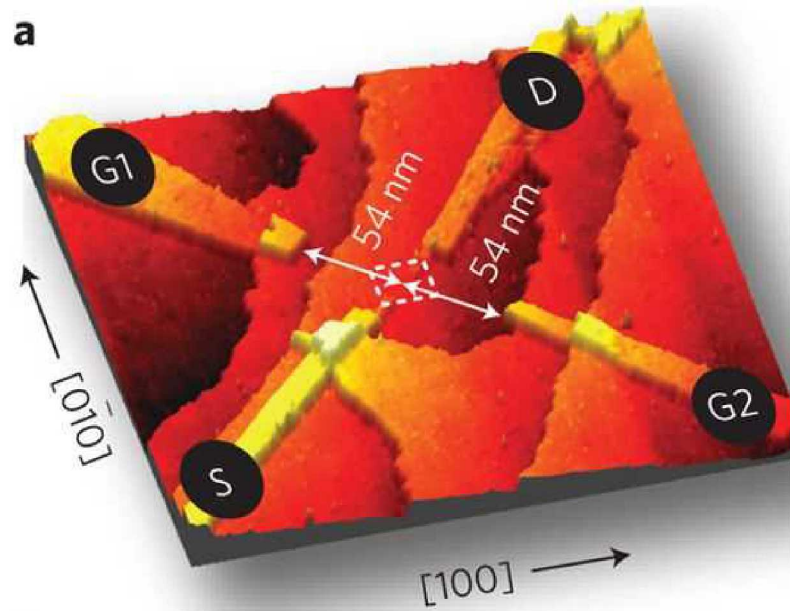


Surface gated atomically precise single electron Islands

Dan Ward, Evan Anderson, Leon Maurer, DeAnna Campbell, Mike Marshall, Lisa Tracy,
Andrew Baczewski, Tzu-Ming Lu, Shashank Misra

Atomic precision advanced manufacturing (APAM)

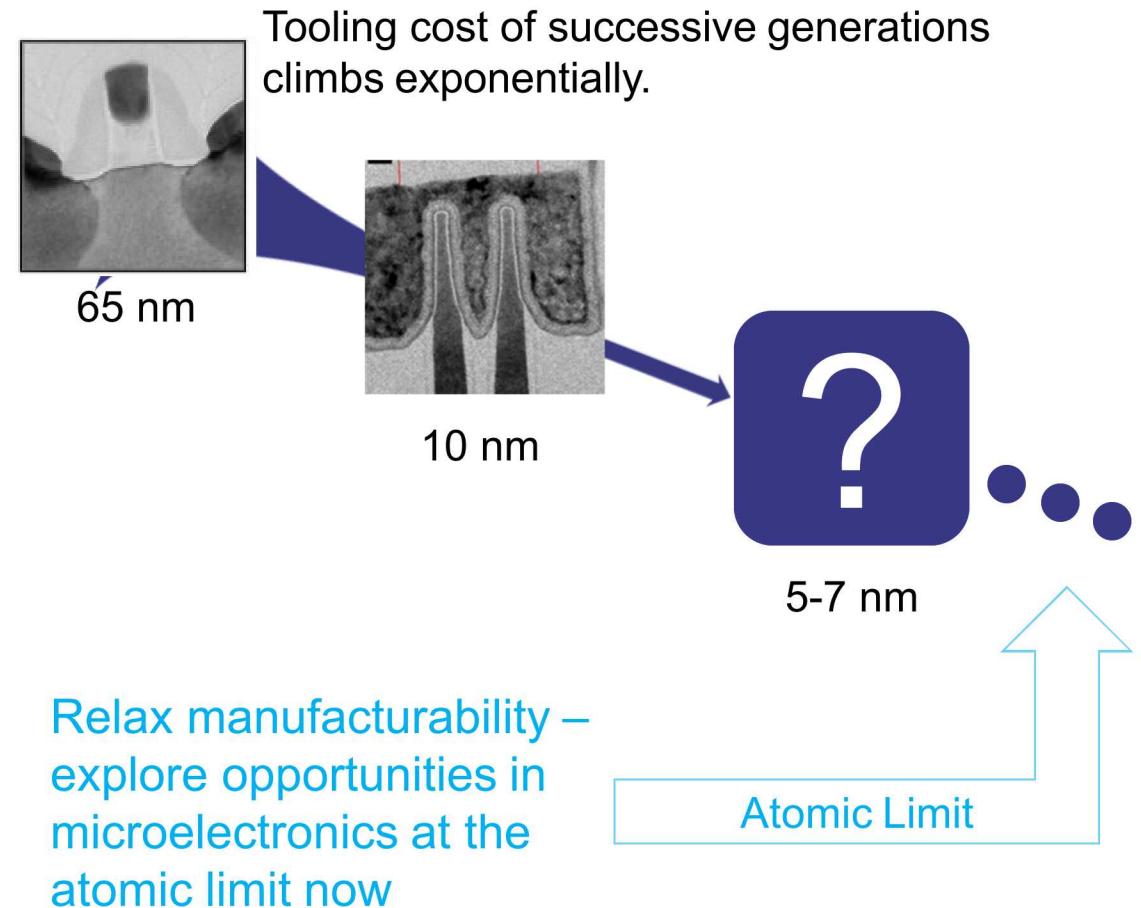
STM-based fabrication of physics-focused devices



Fueschle, Nat. Nano (2012)

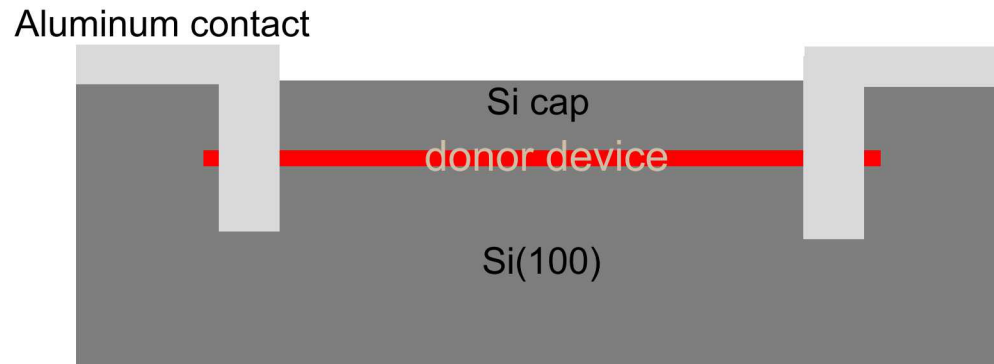
UNSW, SNL (historically), NIST

Sandia project targeting microelectronics



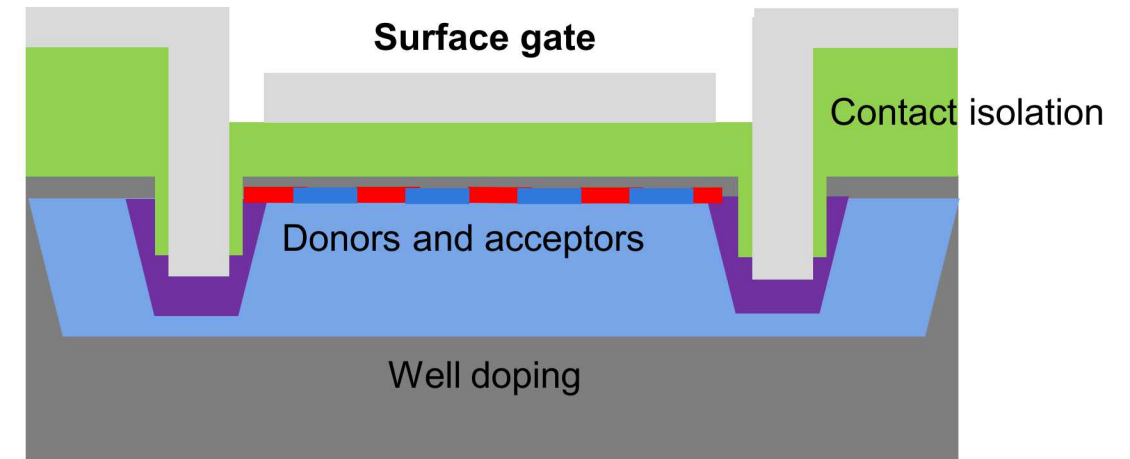
Sandia goal: Increase sophistication of APAM devices

2018



Device cross section

2021 goal



Device cross section

Need more sophisticated devices to find application to microelectronics...

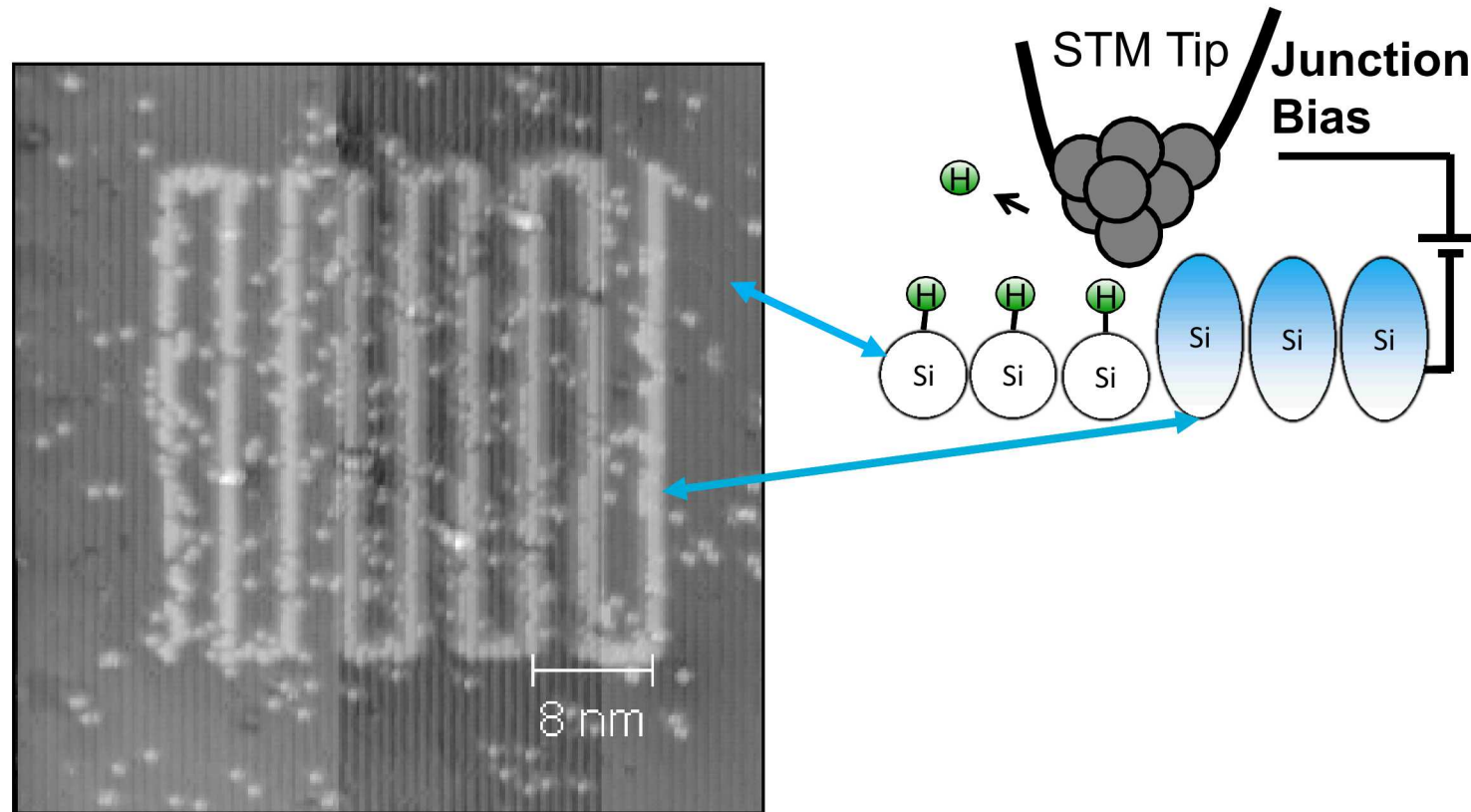
- high gain
- room temperature operation
- complementary transistors

Requires development of surface gates.
Useful for atomic precision quantum devices too!

How does APAM work?

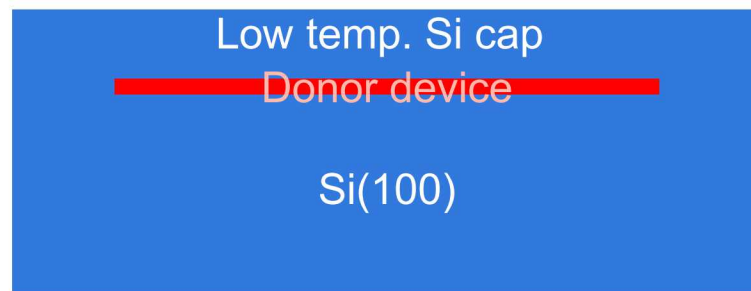
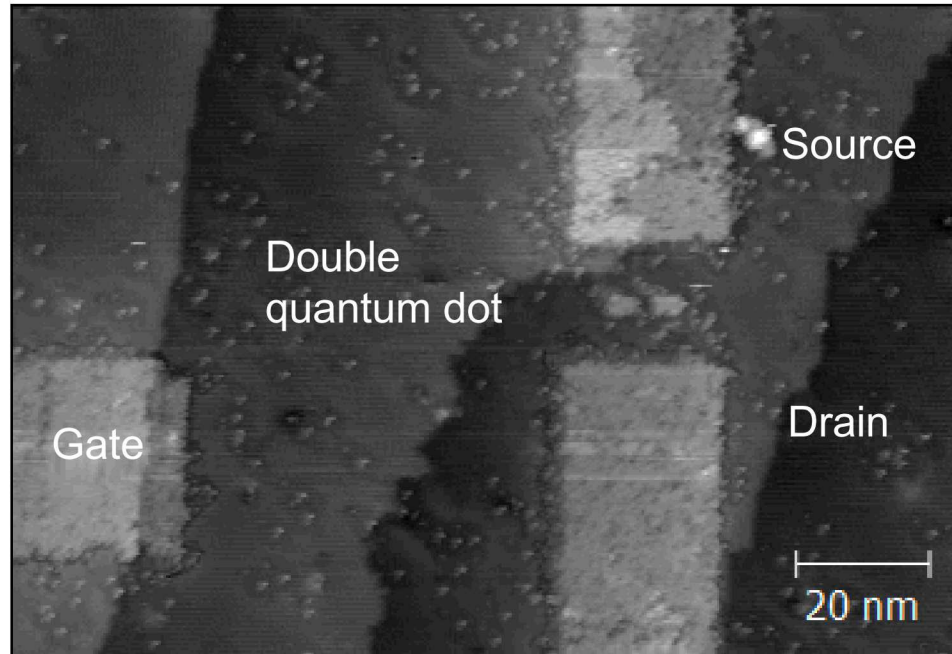
“Chemical contrast” at Si surface

- Unterminated Si: 1 reactive bond/ atom
- H-terminated Si: unreactive



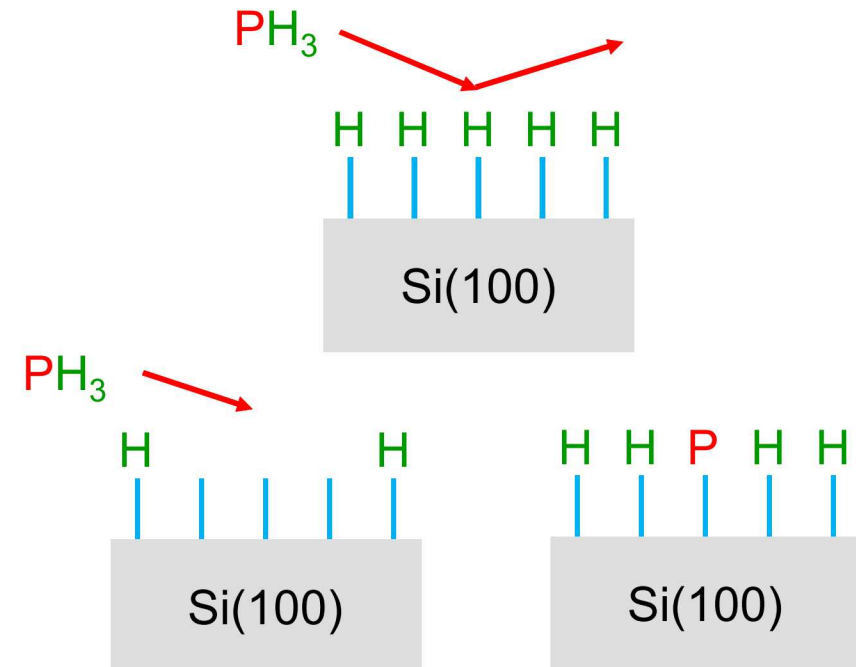
Phosphine produces donor-based devices

Top view

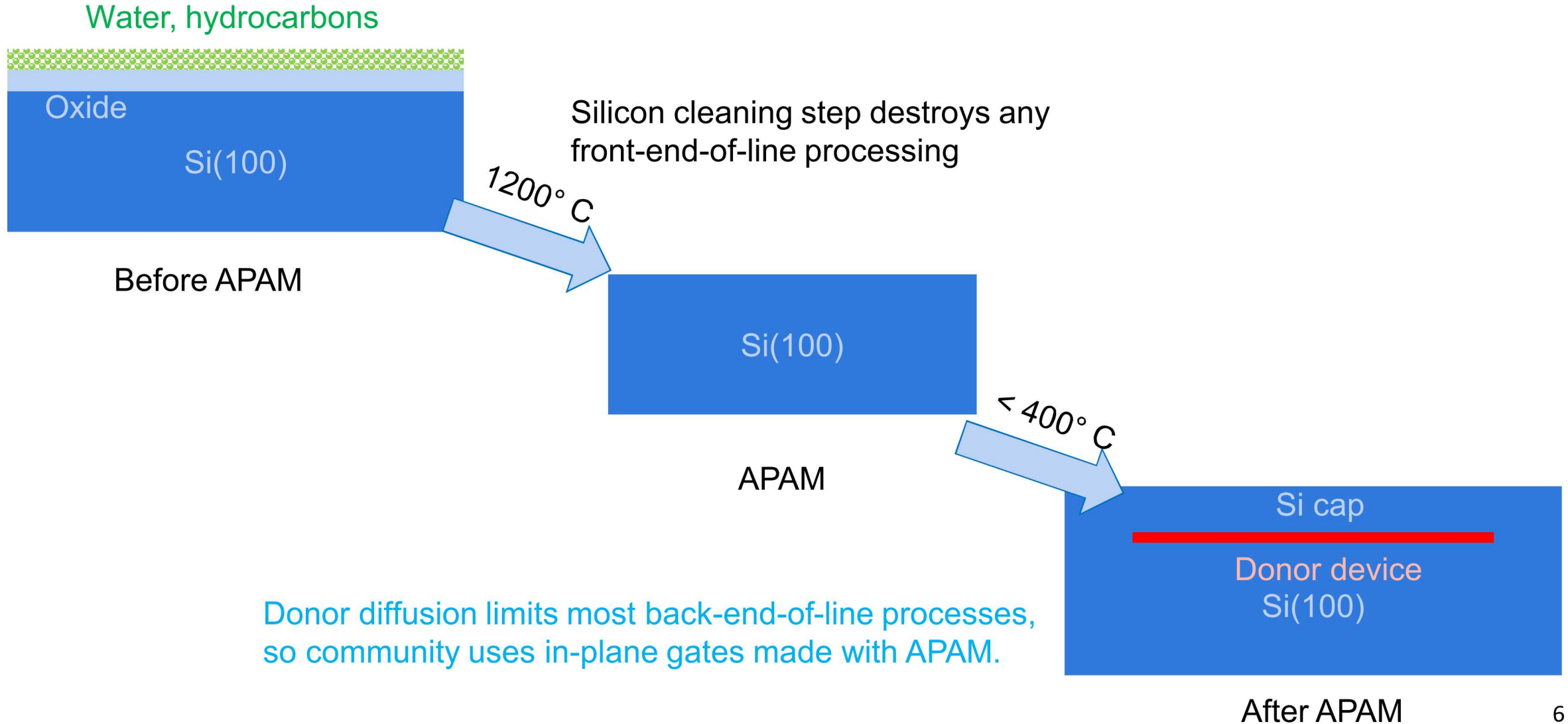


Device cross section

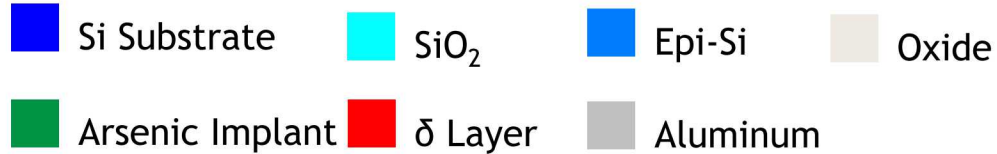
Phosphorus 'donates' an electron to silicon.



Why is gating an APAM device hard?



Back-end-of-line fabrication process (after APAM)



1. Device as it arrives in BEOL after STM



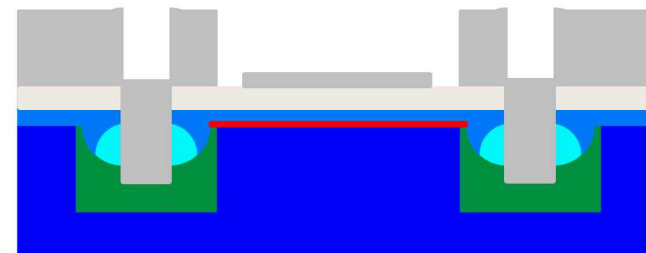
2. Low temperature oxide deposition
(many choices)



3. Vias are etched through oxide, Si Cap,
remaining oxide, and into the implanted
region



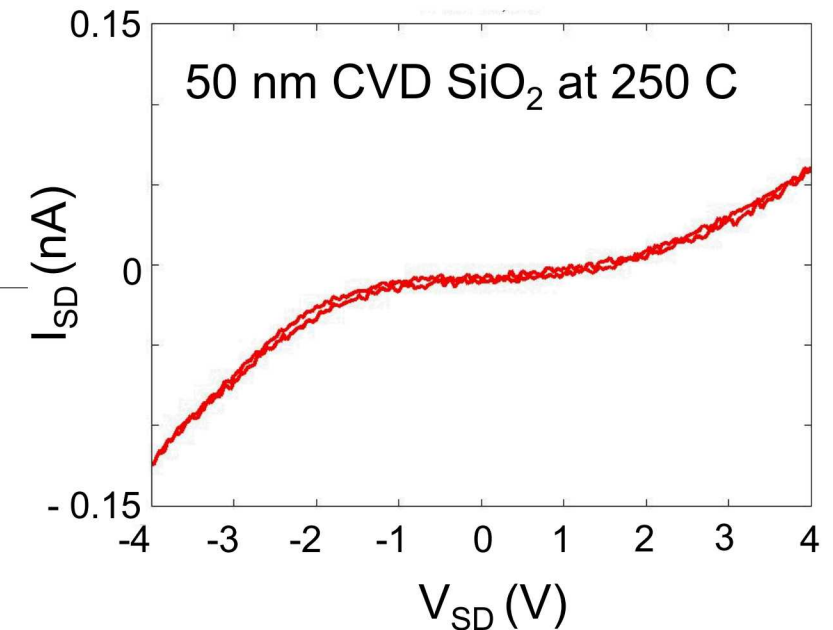
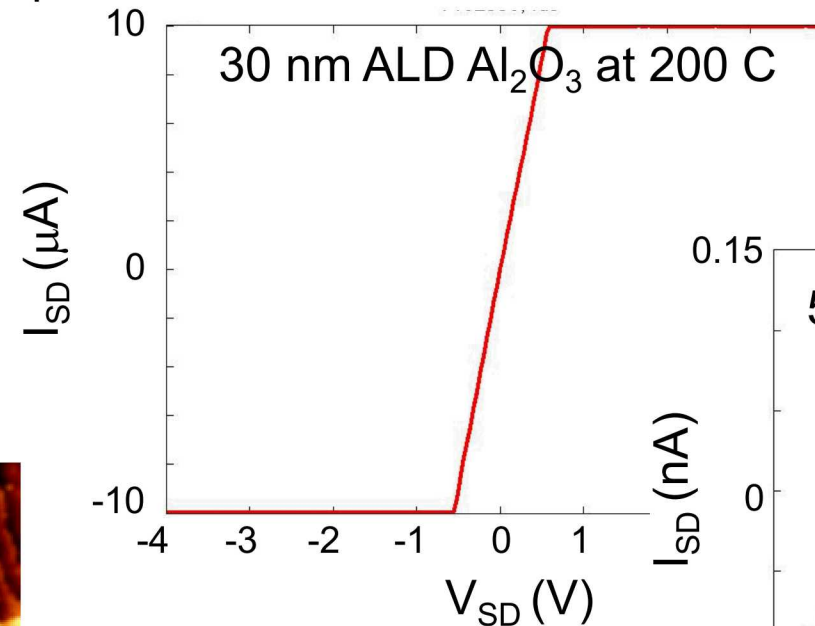
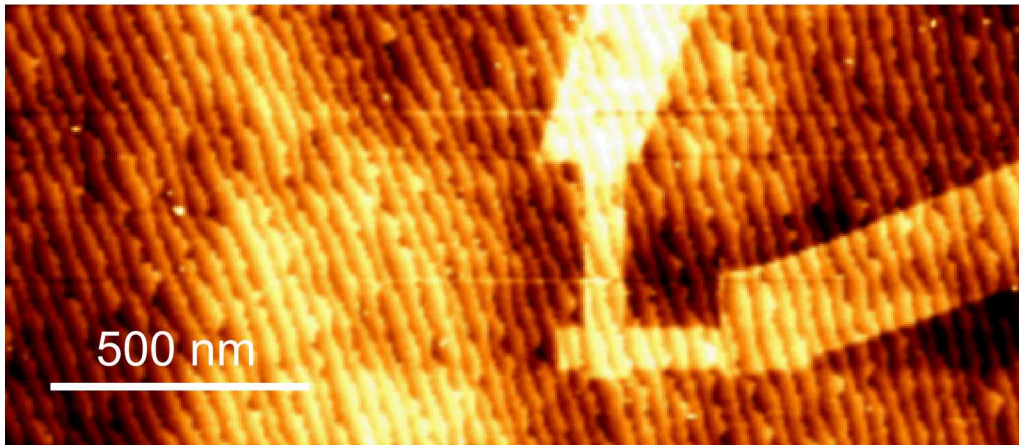
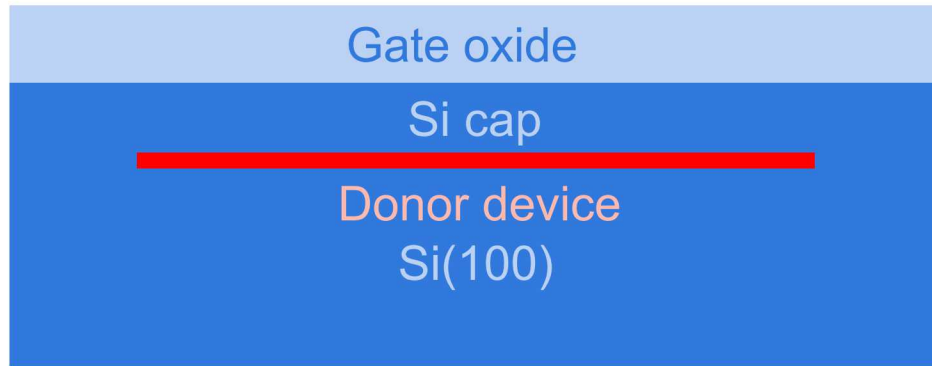
4. Aluminum top gate defined by EBL is
deposited over patterned device.



5. Aluminum contacts are deposited into
vias and connect to macroscopic bond pads

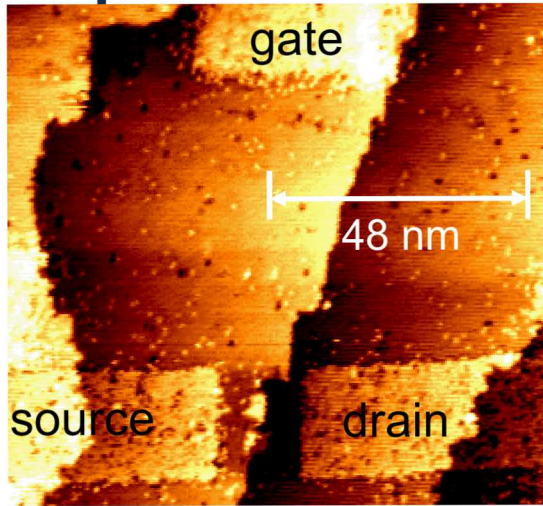
Nanowires for gate oxide evaluation

1. Pattern nanowire.
2. Deposit range of dielectrics with a range of recipes.
3. If nanowire no longer conducts, discard recipe.

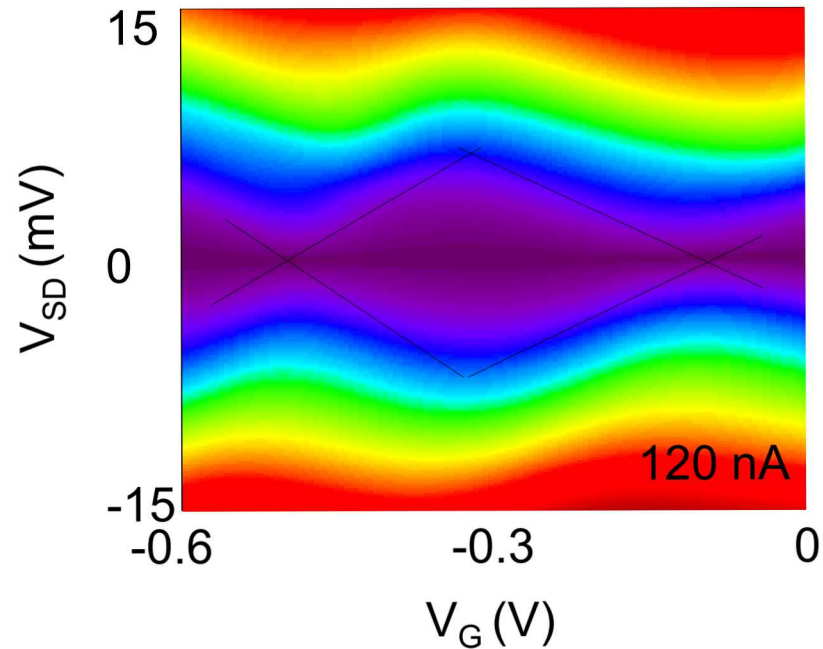


Wire survives, for ALD Al_2O_3

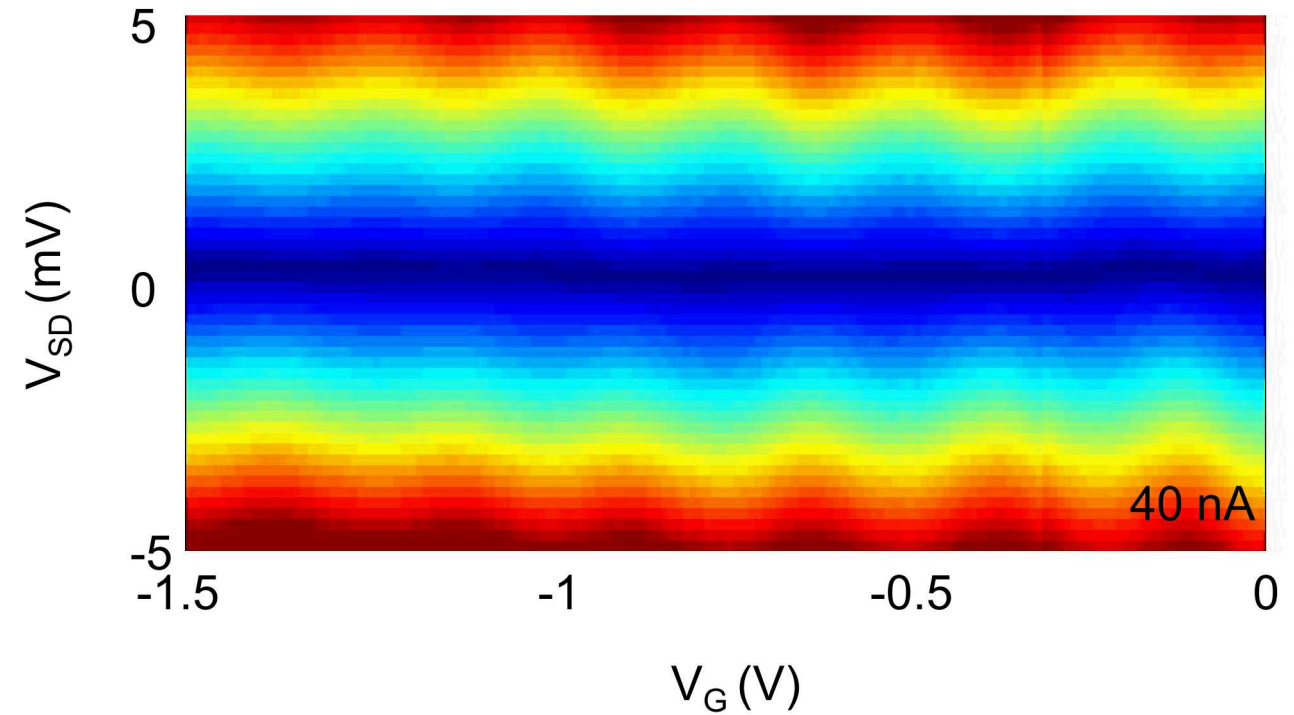
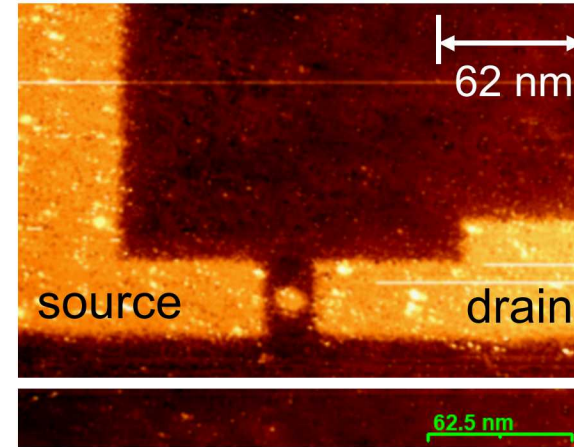
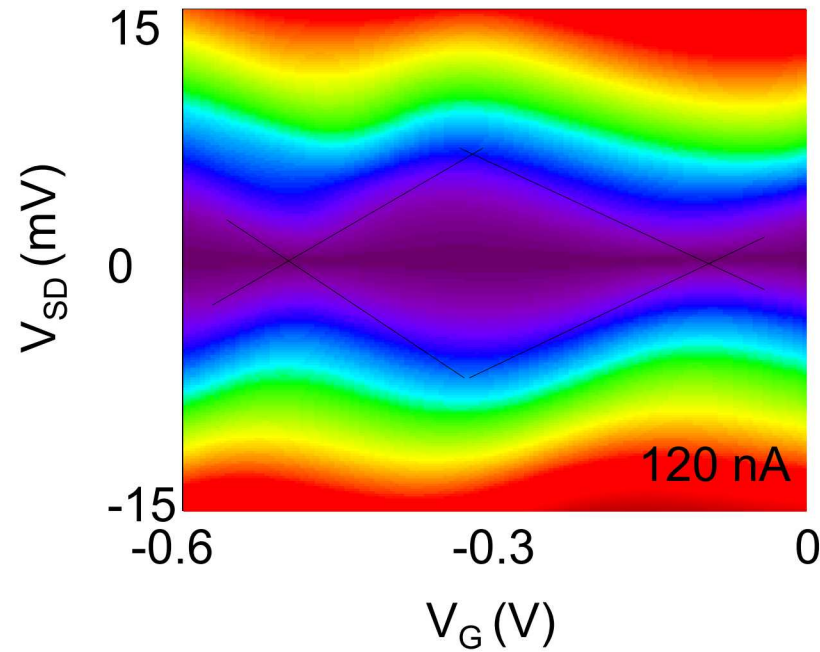
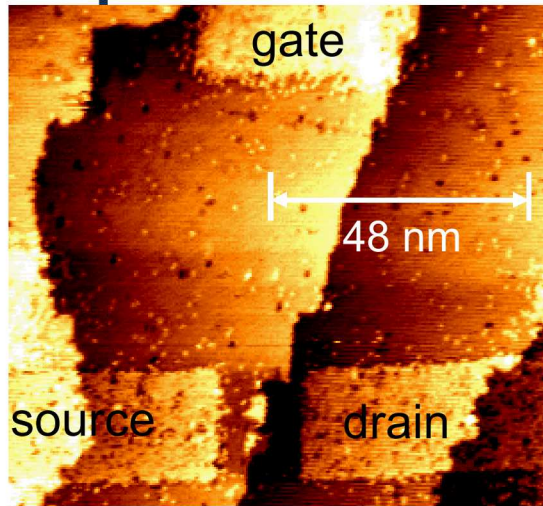
In-plane and surface gates qualitatively similar



Gate SET. Strongly coupled to lead.

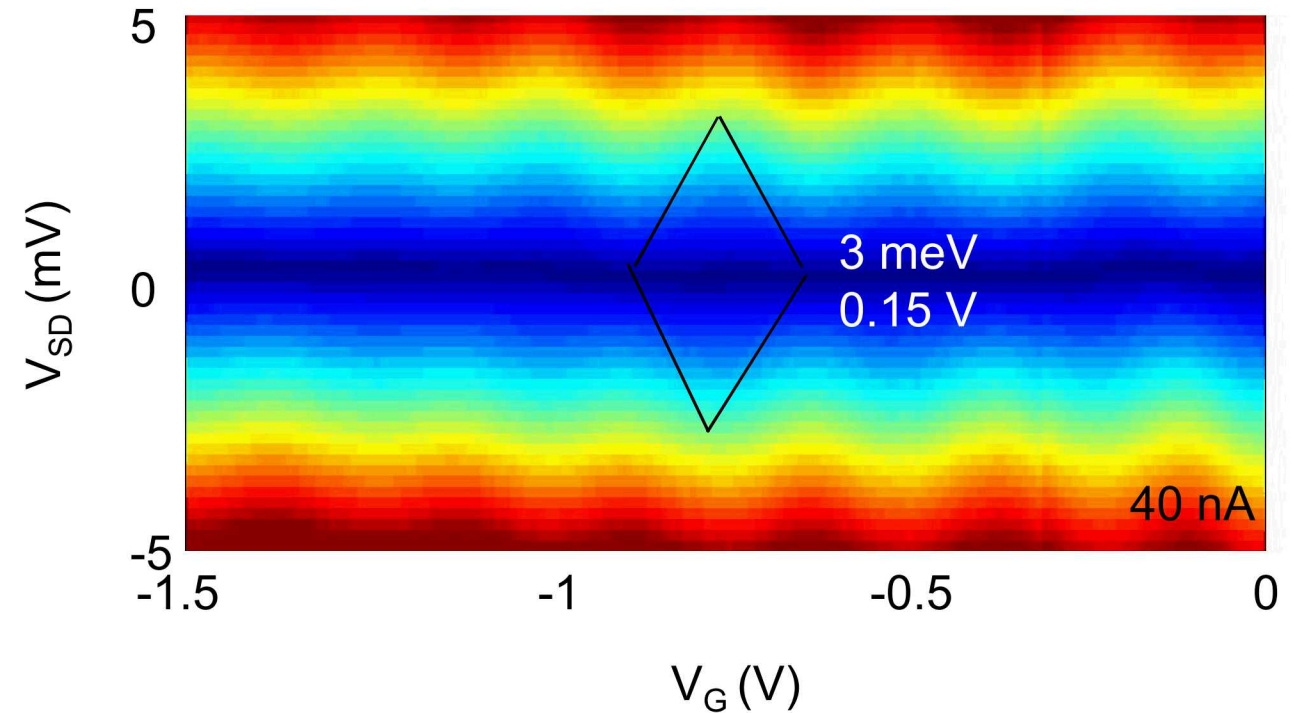
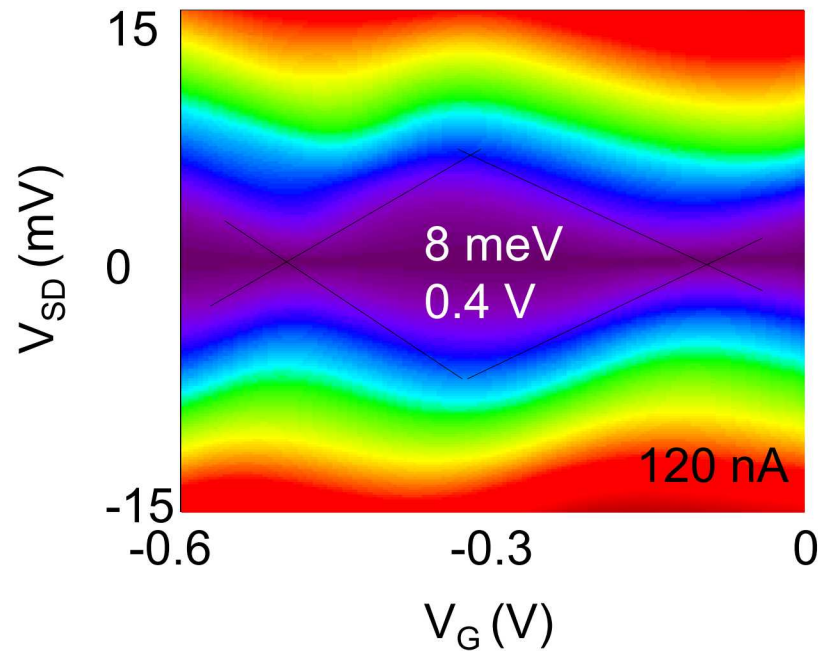


In-plane and surface gates qualitatively similar



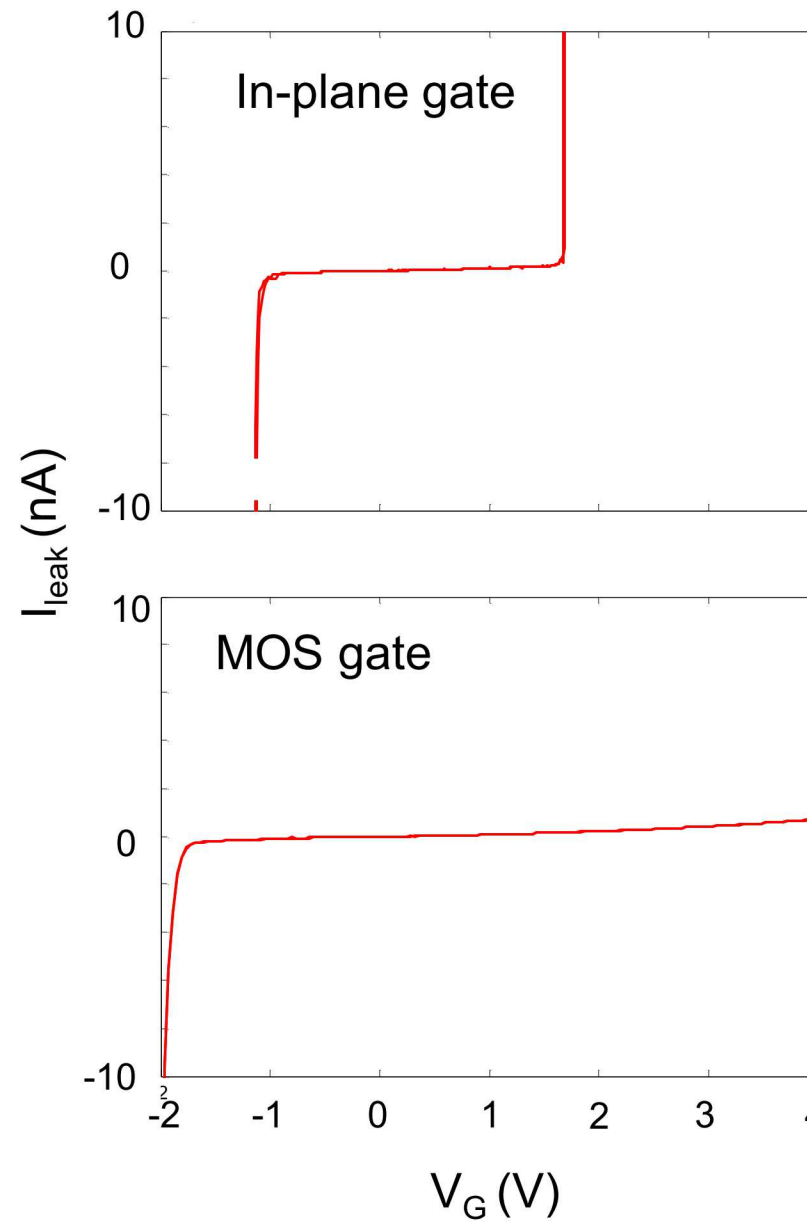
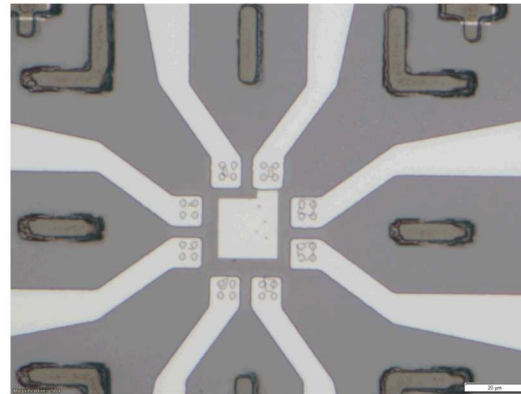
In-plane and surface gates qualitatively similar

Unclear why these are so similar



Improved gate range

MOS Gate

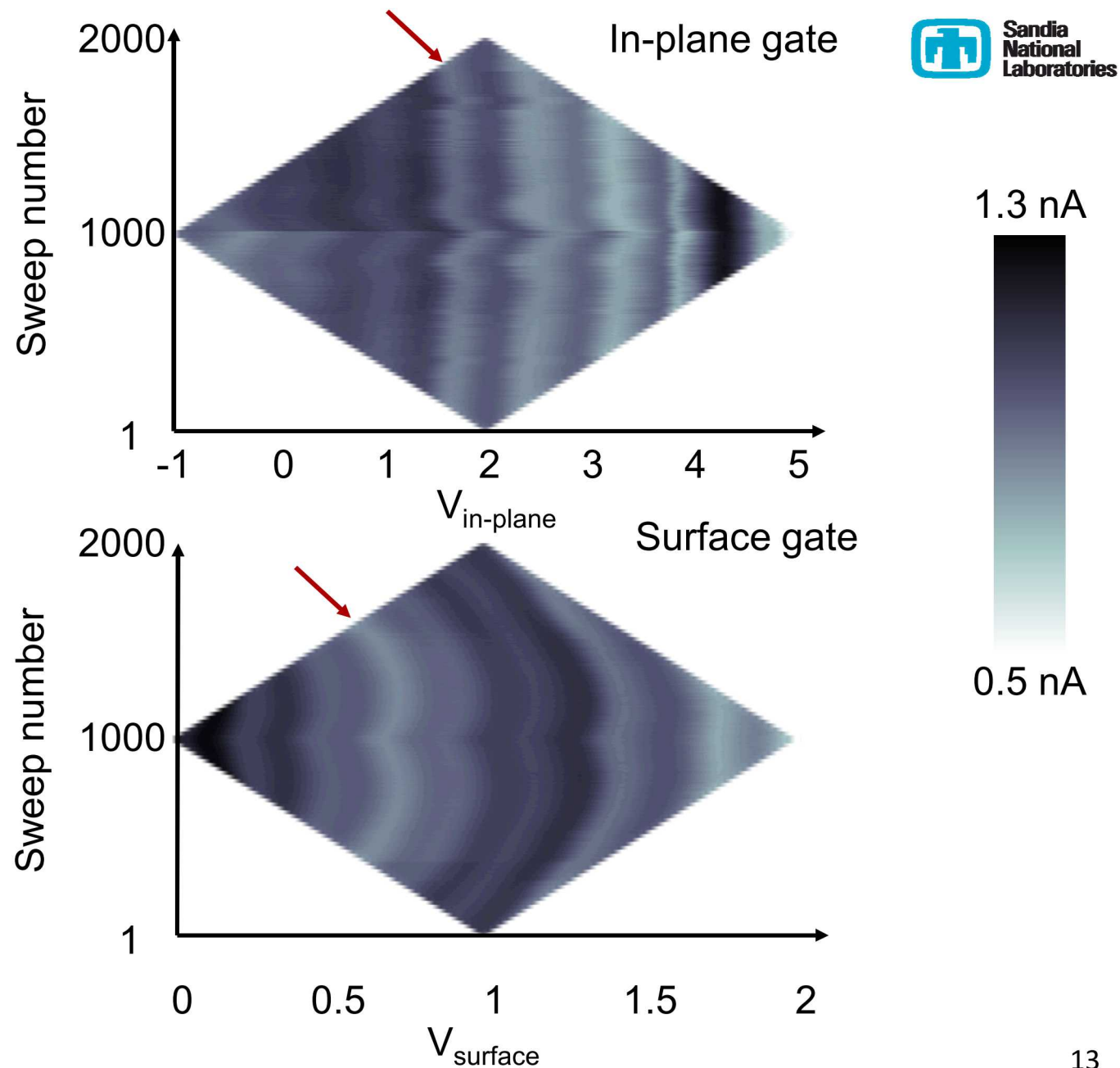


Expect low leakage to +/- 10 V in next design (need to isolate metal from silicon)

Gate hysteresis

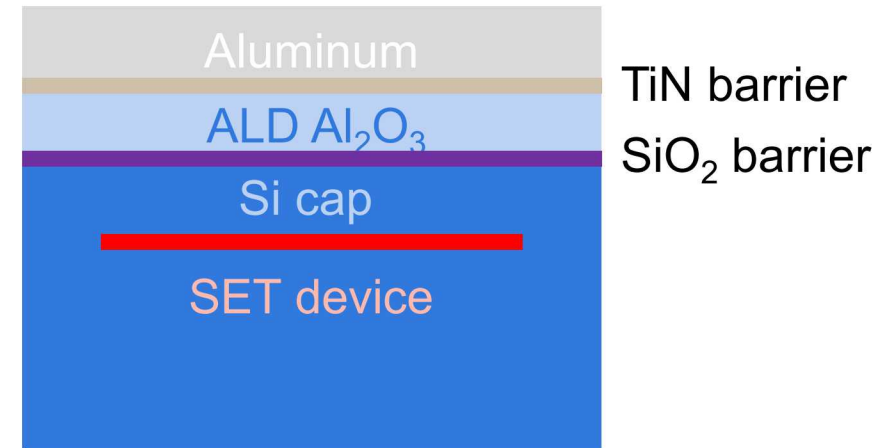
Repeat gate sweep across charge lines – should be straight

Surface gate is less 'glitchy'
Surface gate is more hysteretic



What's next?

1. Diffusion barriers to improve interface quality

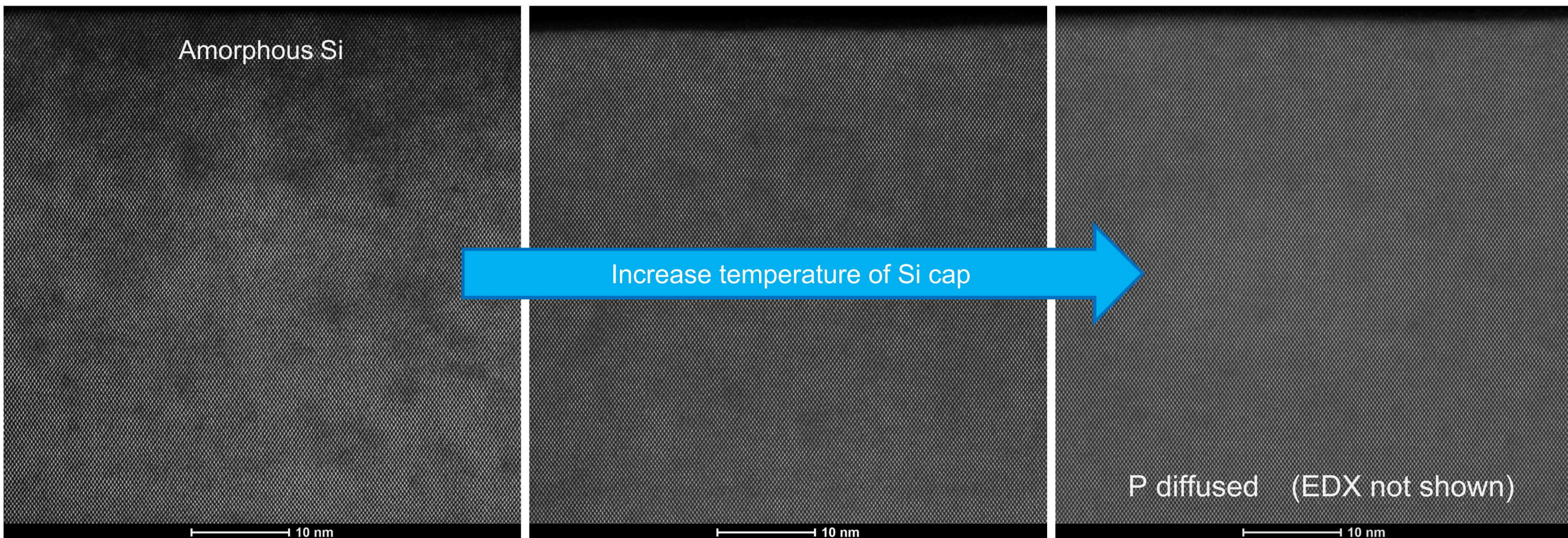


Requires significant process development:

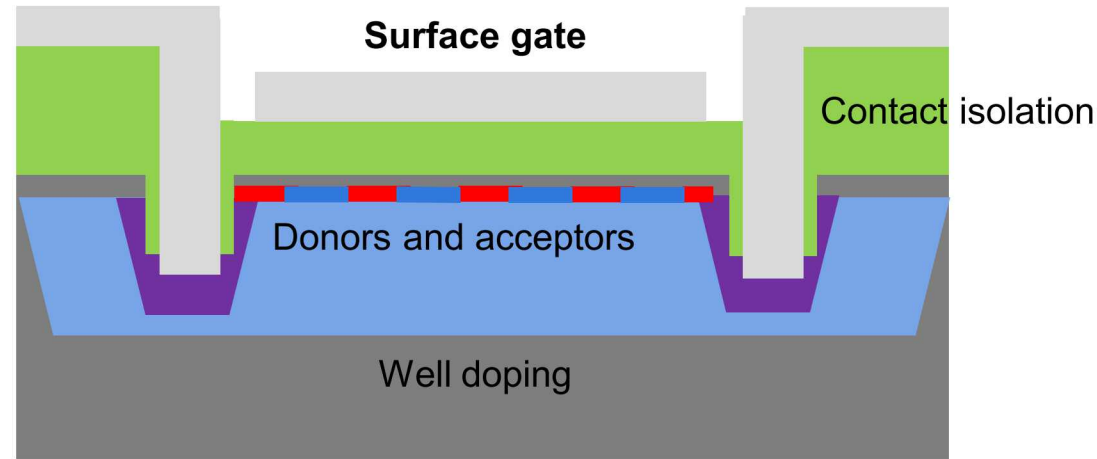
- Low temperature SiO_2
- Dual evaporation of metal
- Etched metal (not liftoff)

What's next?

2. Quality of low temperature materials – e.g. Si cap, oxide



Conclusion



Device cross section

Surface gate applicable to both APAM physics-focused devices and ultra-scaled transistors

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