



Tracking atomic-scale interface disorder in Si/SiGe qubit materials

Luis F. Peña, Justin C. Koepke & Ezra Bussmann (ebussma@sandia.gov)
Center for Integrated Nanotechnologies, Sandia National Laboratories New Mexico USA

Introduction

- SiGe heterostructures are host material for ongoing quantum electronics discovery & SiGe qubits have good key traits for larger QC in Si [1-4]
- Challenge/opportunity: theory indicates critical interplay between material & quantum electronic properties may impact qubit performance[3]
- Our goal: first, measure materials properties, and then connect structure with quantum electronic properties
- Approach:** Grow SiGe heterostructure via molecular beam epitaxy & track evolution *in vacuo* via scanning tunneling microscopy (STM)

Background

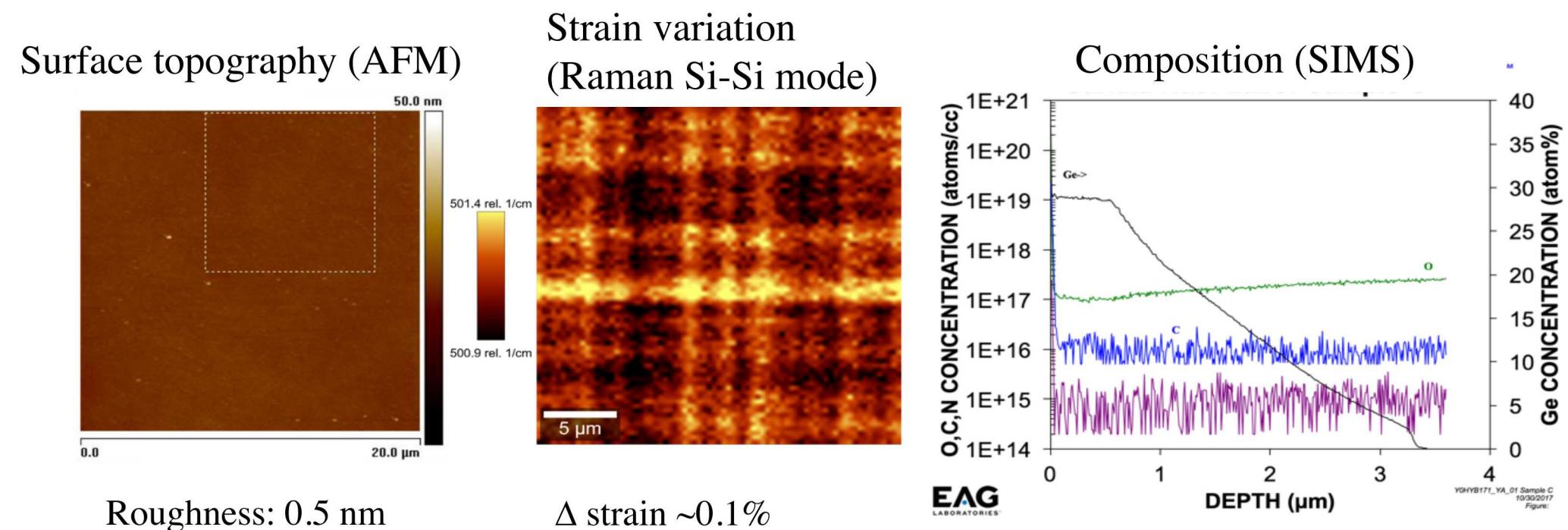
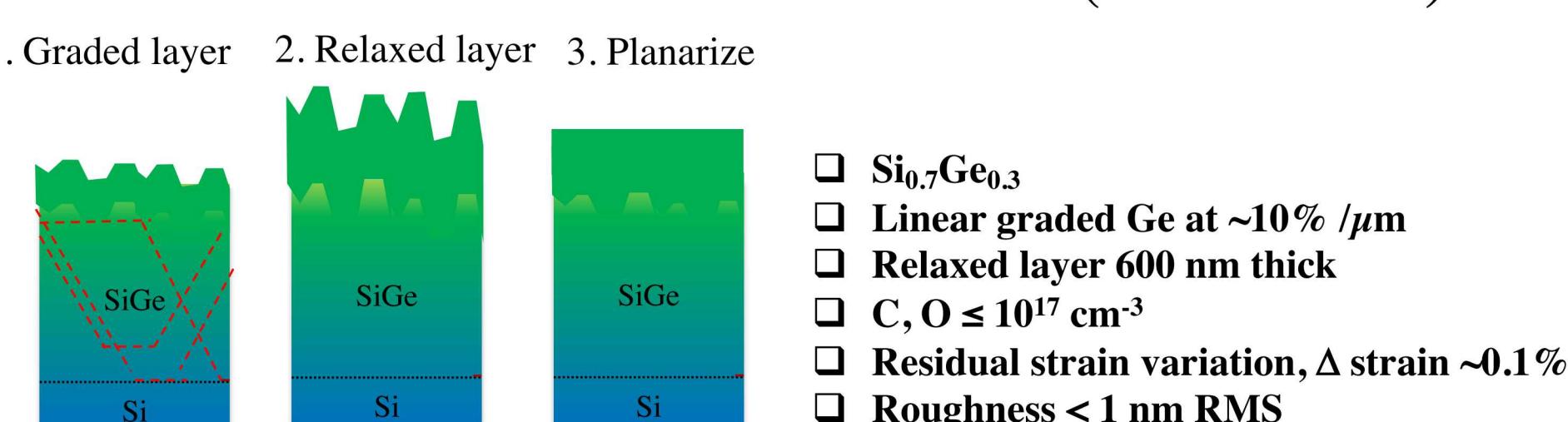
- Six degenerate conduction band minima (valleys) in Si
- For spin qubits, must remove (split) valley degeneracy [1]
- Strain + interface confinement splits valleys
- But theory indicates valley splitting in 2D e- gas, quantum dots, suppressed by atomic-scale disorder at interfaces [1-4]
- For SiGe qubits, this may underpin interdevice variability, decoherence thru degeneracy [3, 4]

Materials & methods

- Prior studies [5-9] showed general principles driving interface disorder, we focus on specific methods & materials for contemporary qubits [4]
- Buried interface challenging to measure in 3D
- Common method of cross-sectional TEM provides 2D slice thru structure & extrapolations must be made to 3D
- Our approach: image growth surfaces that become buried interfaces as layered structure is deposited

Substrate

- Commercial virtual substrate (LSRL, Inc)
- Virtual substrate characteristics (as-received)



Toolset MBE+STM



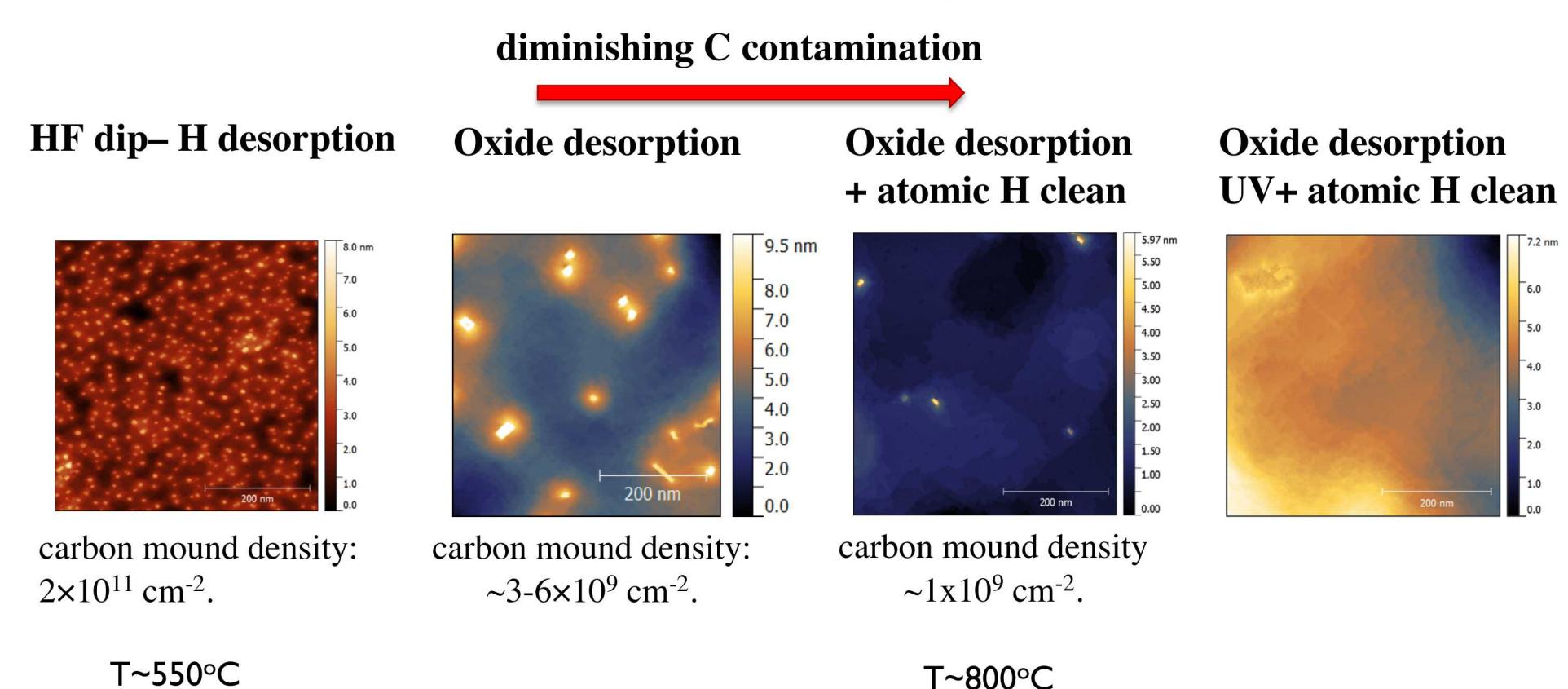
- Coupled MBE+STM (*Omicron*), vacuum 2×10^{-10} Torr
- Si source e-beam heated rod-fed (*Thermionics Inc*)
- Ge source Knudsen cell (*MBE Komponenten*)
- RHEED (*Staib*) to monitor surface during growth
- Band edge thermometer for T measurement

References

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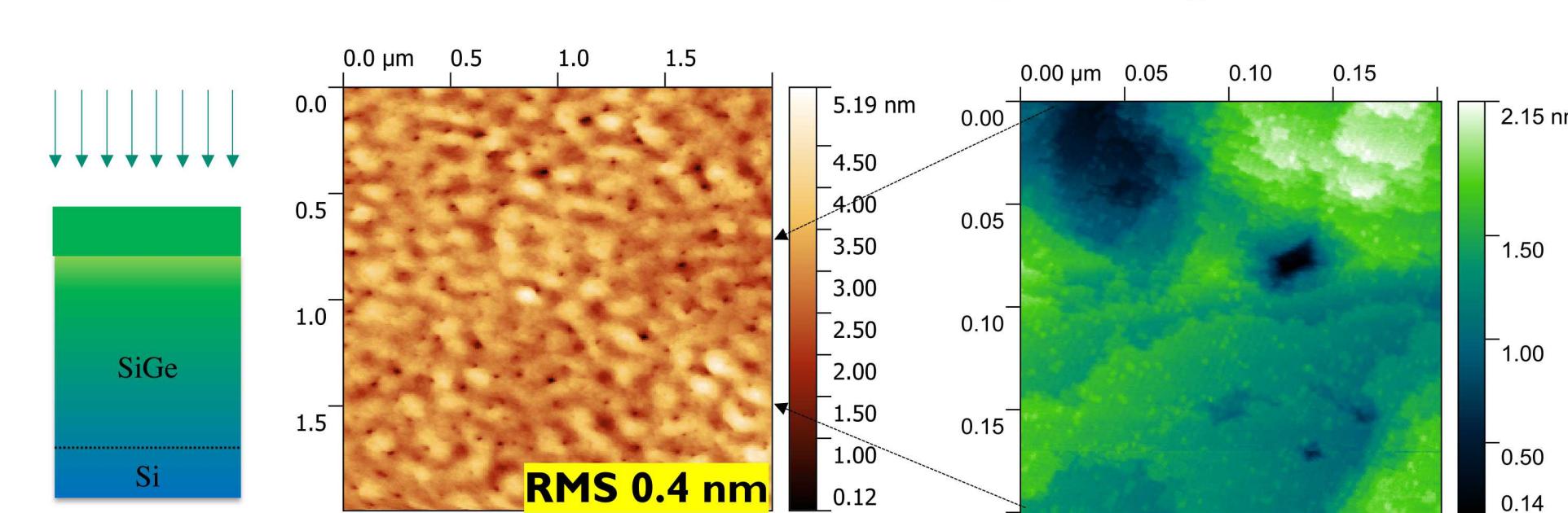
Heterostructure growth tracked by *in vacuo* STM

1. Clean substrate – reduce C, O, H via wet chem + annealing in vacuum



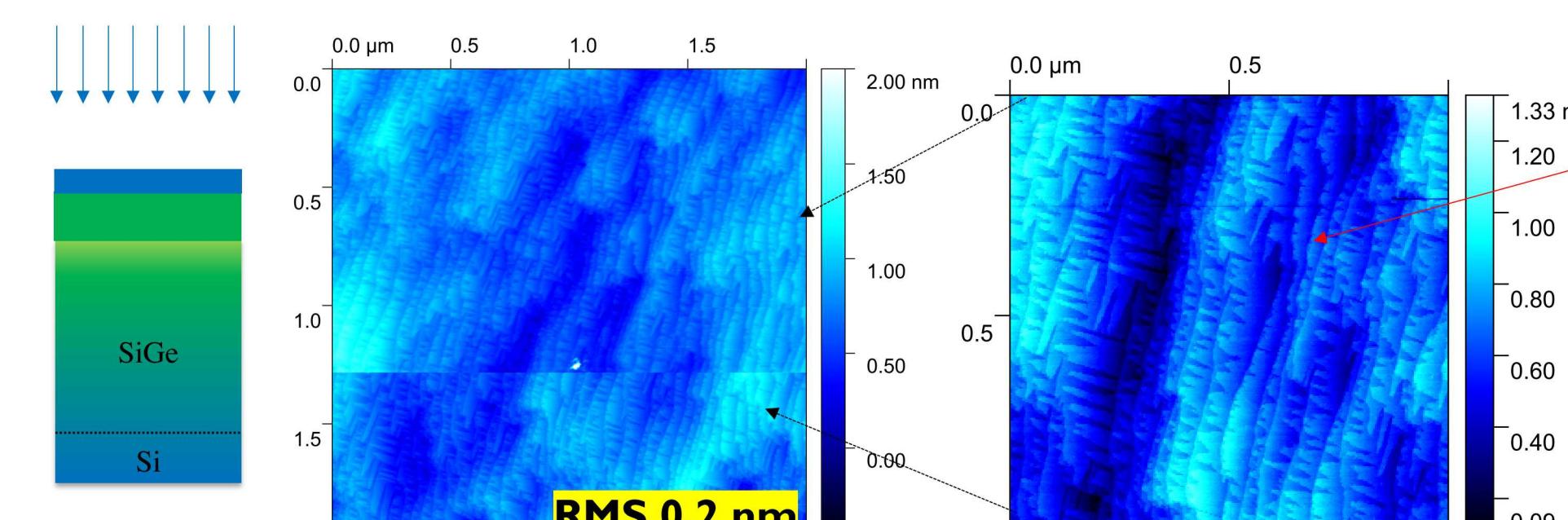
- Compared a few cleans
- Chemical oxide, H annealing, & UV ozone yielded reasonably clean but rougher surface

2. After relaxed SiGe buffer layer deposition



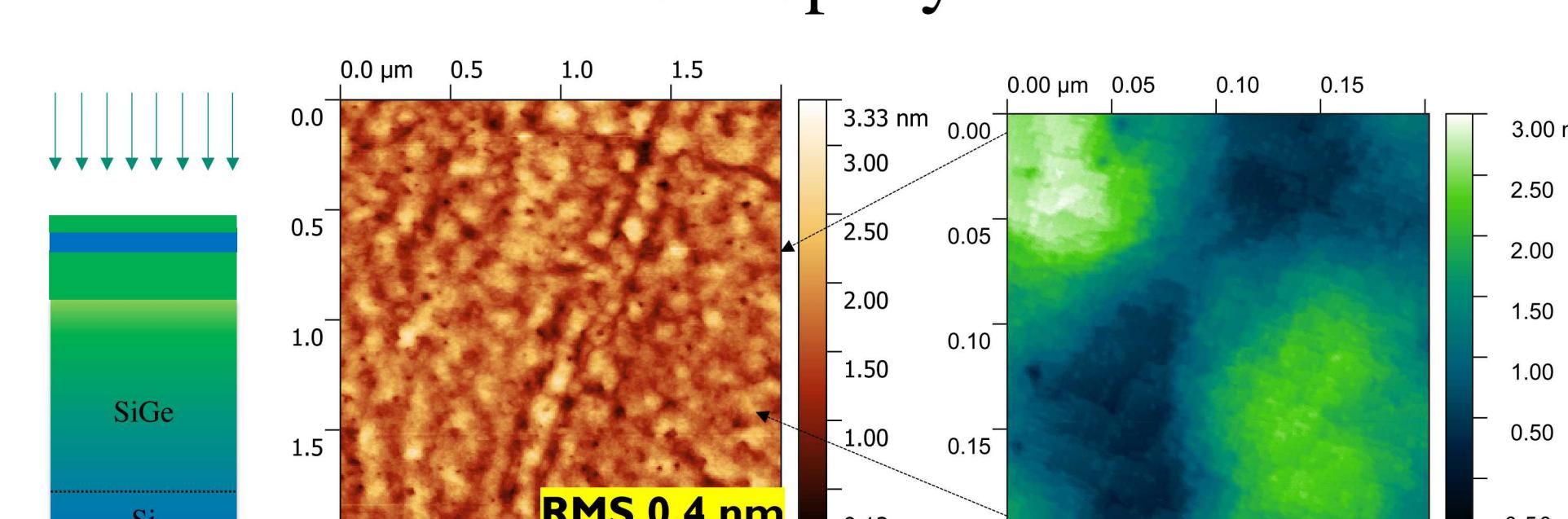
- Composition $Si_{0.7}Ge_{0.3}$
- Isolate subsequent quantum well from disorder at initial surface
- Roughness can be introduced in this layer**
- 80 nm thick, 2.1 nm/min growth rate, T=550°C

3. After strained-Si quantum well



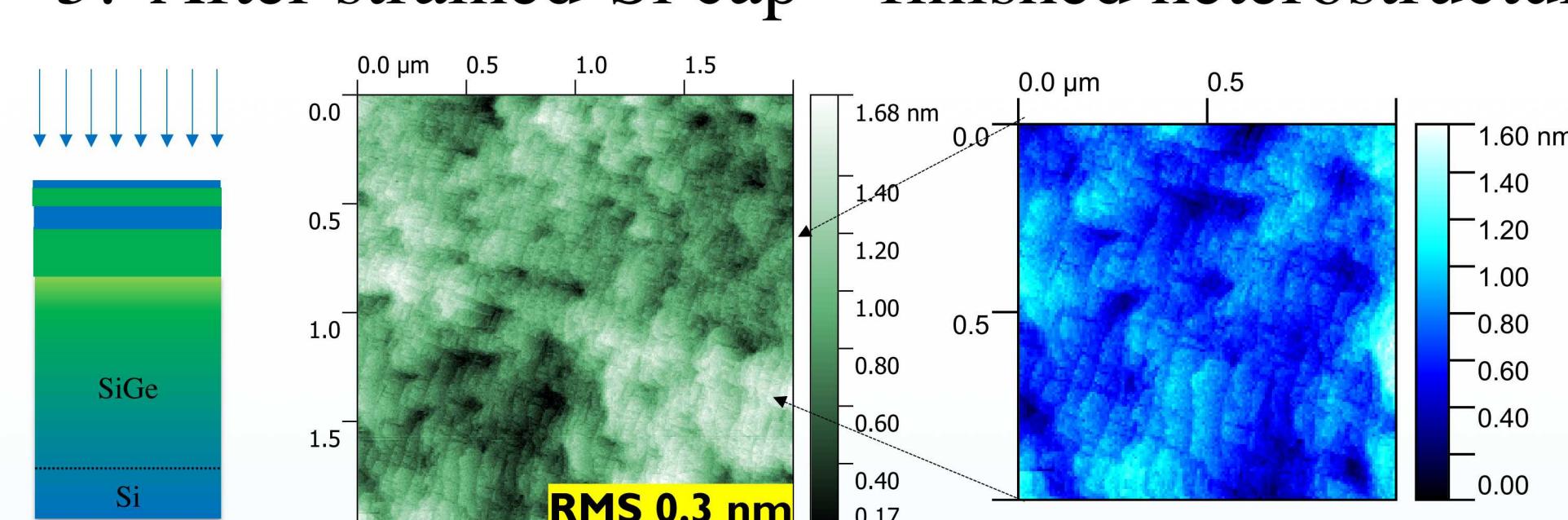
- Smoothing in this step
- Dense atomic steps with nonuniform distribution**
- Likely owing to tensile strain, higher surface energy, and pure composition
- 10 nm thick, 1.5 nm/min growth rate, T=550°C

4. After relaxed SiGe top layer



- Isolate s-Si quantum well from disorder at finished top surface and subsequent gate stack
- Roughness can be introduced in this layer**
- Composition $Si_{0.7}Ge_{0.3}$
- 50 nm thick/ 2.1 nm/min growth rate, T=550°C

5. After strained-Si cap – finished heterostructure surface



- Smoothing in this step
- Likely owing to tensile strain, higher surface energy, and pure composition
- 3 nm thick, T=550°C/ 1.5 nm/min growth rate

Conclusions & outlook

- Variable step density across surface following each stage of growth process
- Steps do not follow miscut, but rather local growth kinetics & strain fields
- STM at stage 3 and 5 above point to correlation between well & top-surface roughness
- Next work: correlate atomic disorder & quantum electronic properties, in collaboration with M. Eriksson UW-Madison