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Sandia National Laboratories

Option 1: Qubits in Gate-Defined Silicon Quantum Dots Charge Noise Assessment Platform

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What can fabrication do to improve charge noise in Si-based qubits?

- What parameters most influence charge noise?
- What are the metrics?
  - Absolute charge noise level
  - Deviations in charge noise

How can we assess charge noise improvements?

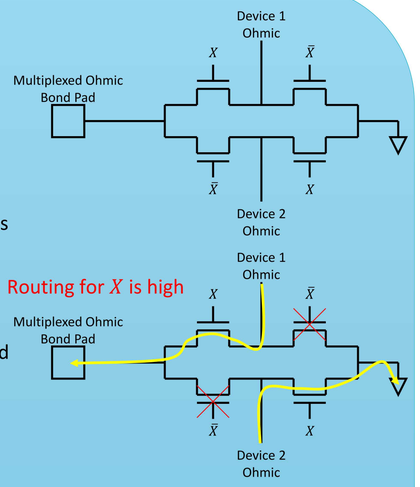
- Need statistics – measure lots of devices
- Need fast measurement of multiple devices
- Maximize throughput of devices assuming a single cool down
- "Simple" devices – Double QD with SET

Throughput increases:

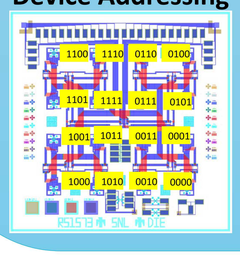
- Multiple devices per die - Quickly run out of control lines
- Multiplexing
  - Shared gate connections
  - Ohmics are multiplexed with on-chip switches
  - For DQD+SET requires 22+2*n connections for 2^n devices
  - 16 devices (n=4) requires 30 connections → 32 charge noise measurements!

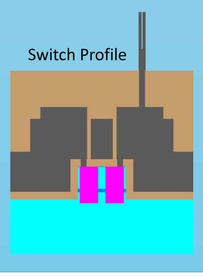
Multiplexing Setup

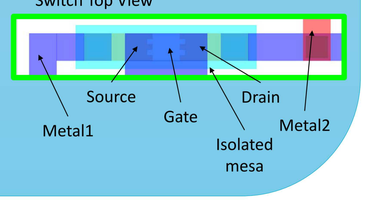
- Multiplexing greatly reduces number of connections needed
- Our design requires 2*n connections
  - Providing digital signal line (X) and its compliment ($\bar{X}$)
- On-chip inverter is impractical
  - NMOS only without additional implants
  - NMOS inverters require large power dissipation
- Critical that devices not under measurement be grounded
  - Device on → ohmic routed to bond pad
  - Device off → ohmic routed to ground
- Each ohmic requires two switches per split



Device Addressing



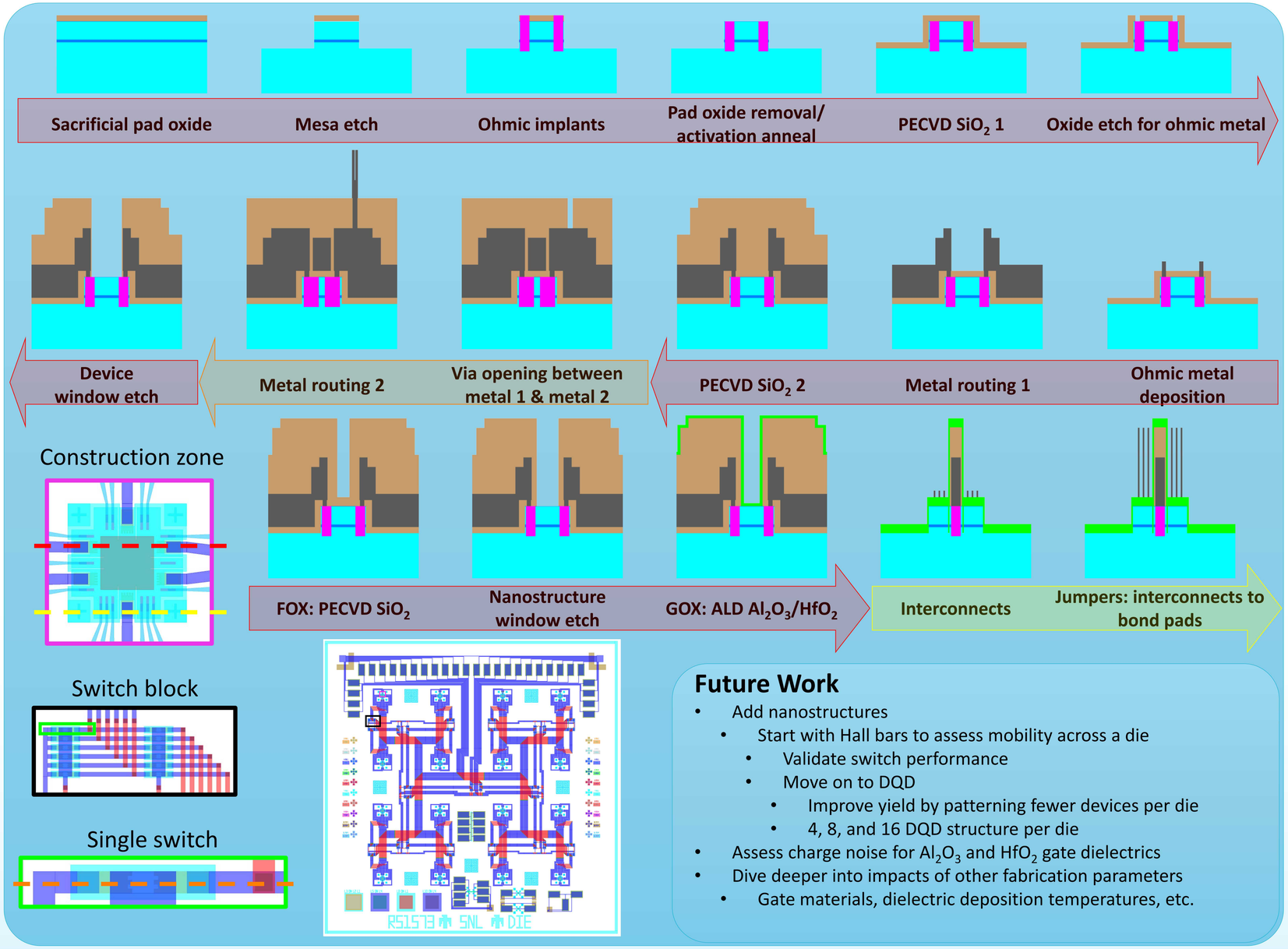




MESA complex:
Class 1 Si cleanroom (CMOS)
Class 10 Mixed materials (III-V R&D)
Capabilities:
Up to 8" wafer processing, novel integration, small volume production.

CINT complex:
Class 100 cleanroom
Capabilities:
Up to 4" wafer processing, user facility for visiting collaborators.

Special thanks to Lisa Edge for providing SiGe wafers



Construction zone

Switch block

Single switch

Future Work

- Add nanostructures
  - Start with Hall bars to assess mobility across a die
    - Validate switch performance
    - Move on to DQD
      - Improve yield by patterning fewer devices per die
      - 4, 8, and 16 DQD structure per die
- Assess charge noise for Al_2O_3 and HfO_2 gate dielectrics
- Dive deeper into impacts of other fabrication parameters
  - Gate materials, dielectric deposition temperatures, etc.

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