



Gate-Defined Quantum Dots in Ge/SiGe Quantum Wells as a Platform for Spin Qubits

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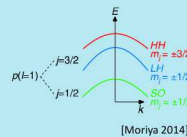
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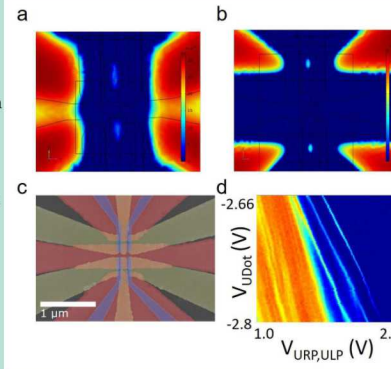
Introduction

- GOAL:** Hole spin qubits are an attractive alternative to electrons. Our goal is to demonstrate and characterize hole qubits in Ge/SiGe.
- PROGRESS:** We have demonstrated multi-metal-layer gated device architectures, device tuning protocols, and charge-sensing capabilities.
- Strained Ge/SiGe:** novel material system with many compelling properties:
 - Absence of valley states
 - Low disorder, $\mu \geq 6 \times 10^4$ cm²/Vs
 - Large spin-orbit coupling for all-electrical spin control
 - Small effective mass, $m^* \sim 0.08 m_0$
 - Weak hyperfine interactions; can be isotopically enriched
 - CMOS compatible
 - Many-hole qubits demonstrated in transport [Hendrickx 2019]



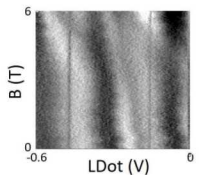
Iterative Device Improvement

- COMSOL simulations performed with realistic gate potentials and material stack parameters
- Confirmed that upper/lower reservoirs tend to merge (a), which is undesired
- Modified simulation with additional horizontal isolation gate \rightarrow better isolation (b)
- Confirmed experimentally in next device iteration (c)
- Narrower Coulomb blockade lines: reduced tunnel broadening between the dot and the reservoirs (d)
- Broad, relatively featureless conduction abruptly transitions to narrow Coulomb blockade
- Sudden onset in tight confinement of the holes in the quantum dot
- Typical for these styles of devices in Ge/SiGe



In-Plane g-Factor

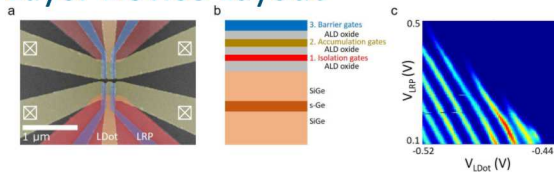
- Charge sensed lines appear insensitive to in-plane B-field $\rightarrow g_{\text{in-plane}} \sim 0$
- Next experiment: apply B out-of-plane
- g-factor anisotropy expected [Lu 2017, Sammak 2019]



Future Directions

- Remotely determine the dot's occupation number down to the last hole
 - Confirm with charge sensing and magnetospectroscopy
- Single-shot readout, single spin electric dipole spin resonance (EDSR)
- Pave the way toward a single-spin hole qubit demonstration in this device architecture.

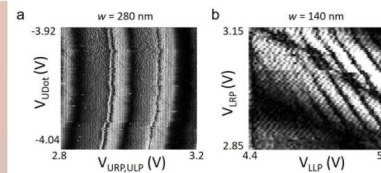
3-Layer Device Layout



- Ge/SiGe wafer:
 - 70nm thick SiGe buffer layer with 28% Si
 - Pure strained Ge quantum well 20 nm thick
 - 2DHG mobility $\mu > 1\text{E}5$ cm²/Vs.
- Original device design: 1 layer of gates (see [Hardy 2019])
 - Broad, shallow potential landscape \rightarrow wide Coulomb blockade lines.
 - Not sufficiently tunable. Need overlapping gates.
- Multilayer device architecture (layout inspired by [Zajac 2015]):
 - 3 layers of Ti/Pt gates
 - ALD oxide dielectrics
 - Ga⁺ implanted ohmics
- Coulomb blockade achieved, but cannot tune up both channels simultaneously (reservoirs tend to merge together)

Charge Sensing

- Comparison of charge sensing with 2 isolation gate widths:
 - 280 nm / 140 nm
- Charge sensing achieved in both device designs
- Signal is $\sim 150\%$ larger for isolation gate width of 140 nm than for 280 nm
- No change in fabrication yield for the narrower gate
- Faster-than-linear increase in sensitivity with decreasing gate width is expected
- $1/\sqrt{2}$ relationship is not fully realized, likely due to the influence of surrounding potential landscape



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