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Atomic Layer Etching of Silicon Using a Conventional ICP Etch Chamber for Failure Analysis Applications

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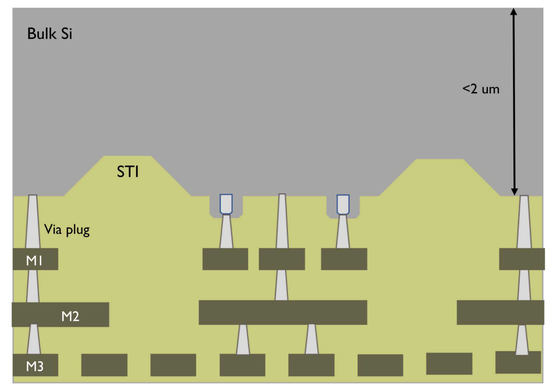
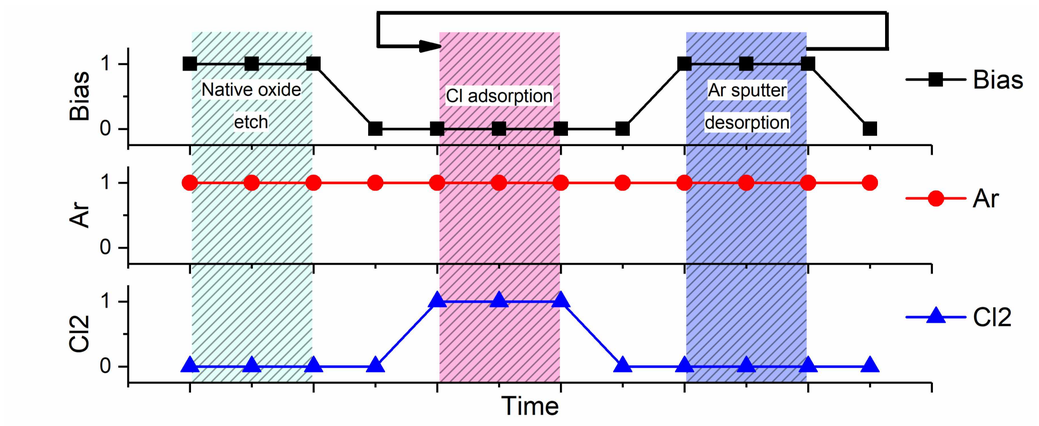
Motivation

- Conventional failure analysis techniques are not optimized for backside thinning of SOTA devices
  - Bulk die-level thinning capability: typically 2-3 µm minimum RST with ~1 µm uniformity range
  - Ion sources: ~150 nm^2 features, 10:1 maximum aspect ratio, significant substrate damage
- ALE is a fit for this application: precise etch rates control, high uniformity, low damage
- Challenges include: large removal amounts, precise energy and reactant control, die processing
- Toolset: Plasma-Therm Versaline ICP etch platform



Approach

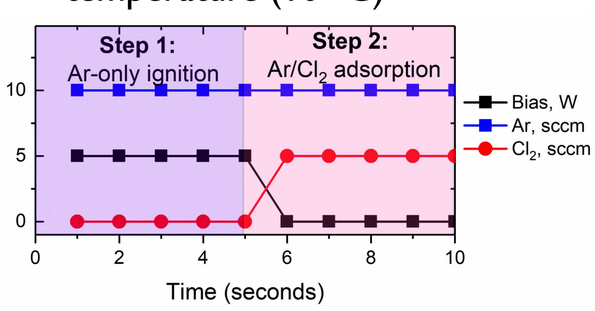
- Surface modification: bias-free Cl_2/Ar plasma
- Sputter: tuned Ar etch

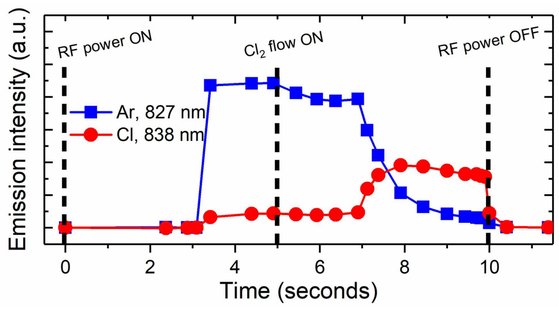


Initial Etch Development

Achieving a stable bias-free Cl_2/Ar plasma

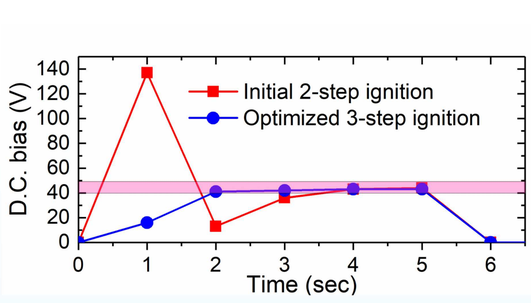
- Constants: Pressure (20 mTorr), ICP power (300 W), bottom electrode temperature (10 °C)

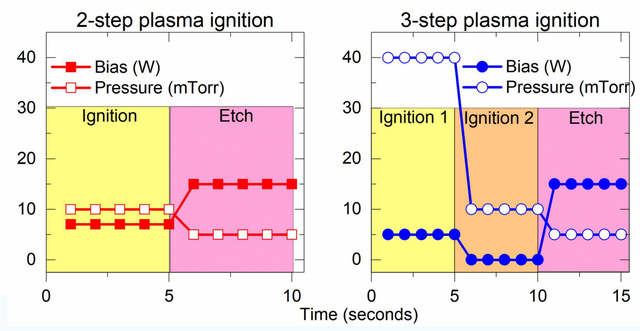




- Step 1: generated D.C. bias remains below sputter threshold
- Step 2: Cl_2 injected into stable plasma, bias power turned off
- OES: significant delays in (1) initial plasma ignition and (2) Cl_2 reactant delivery

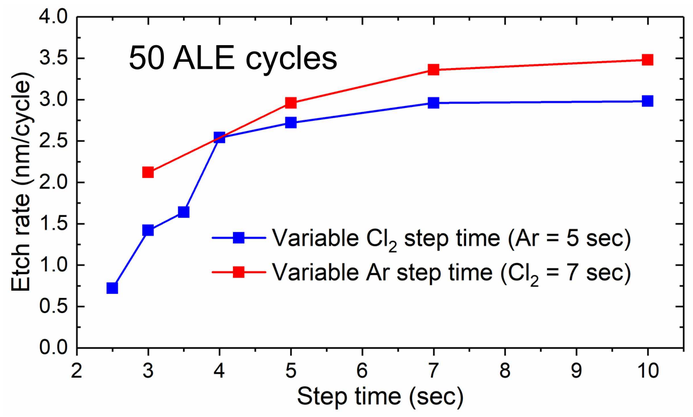
Controlling bombardment energy during Ar desorption step





- 2-step etch: bias tuning overshoots sputter energy target
- Modified 3-step etch ramps D.C. bias to target without overshooting
- Software limitations prevent more detailed interrogation of bias profile

Etch Characterization: Saturation and Synergy

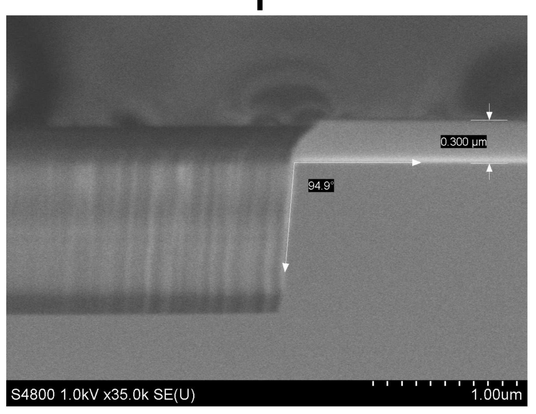


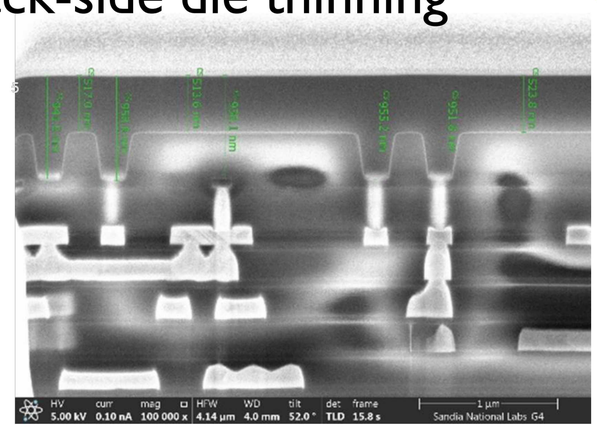
$$Synergy = \frac{E.R._{ALE} - (E.R._{Adsorb} + E.R._{Desorb}}{E.R._{ALE}}$$

	Cl_2 = 3 sec Ar = 5 sec	Cl_2 = 7 sec Ar = 7 sec
ALE (nm/cycle)	1.42	3.36
Cl_2 (nm/cycle)	0.10 (7%)	0.60 (18%)
Ar (nm/cycle)	0.24 (17%)	0.22 (7%)
Synergy	0.76	0.75

- Etch rate saturates with Cl_2 dose *and* Ar sputter etch time
- Removal rate can be tuned by modifying Cl_2 step time
- Ar sputter time does not increase etch rate in the absence of Cl_2 injection
- S < 0.8: unintended etching is not completely eradicated

Etch profile and back-side die thinning





- Patterned features have near-vertical sidewall angle
- 65 nm device backside thinning: smooth surface, targeted R.S.T. (~0.5 µm shown)
- Sequential precision thinning and patterned substrate removal provide myriad options for failure analysis

Summary and Future Work

- Multi-step plasma ignition is used to minimize etching when etching is not desired, but there is room for improvement
- Throughput and precision can be balanced by tuning Cl_2 exposure time
- ALE approach can be used for precision thinning and fine feature etching to analyze packaged advanced node devices

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