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Single-Event Characterization of the 16 nm FinFET Xilinx UltraScale+™ RFSoC Field-Programmable Gate Array under Proton Irradiation

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***Abstract*—This study examines the single-event upset and single-event latch-up susceptibility of the Xilinx 16nm FinFET Zynq UltraScale+ RFSoC FPGA in proton irradiation. Results for SEU in configuration memory, BlockRAM memory, and device SEL are given.**

I. Introduction

THIS study examines the single-event effects susceptibility of the Xilinx UltraScale+ RFSoC device families. UltraScale+ devices are built on TSMC's 16 nm FinFET process technology. The purpose of this work is to determine the flight-worthiness and feasibility of utilizing these parts in low Earth orbit (LEO) space environments. The RFSoC device under test (DUT) was irradiated with protons with energies ranging from 60 MeV to 200 MeV at the Northwestern Medicine Chicago Proton Facility in Warrenville, IL on December 21, 2018. This paper presents measured single-event upset (SEU) results for the FPGA configuration memory, block random-access memory (BlockRAM™), and single-event latch-up (SEL) results. The secondary goal was to evaluate the ADC, DAC, and part performance during proton testing, however, due to complications that arose when modifying the development board for beam testing, this portion of the test could not be performed.

II. Test Description and Setup

A. Zynq UltraScale+ RFSoC DUT

The Zynq UltraScale+ RFSoC device is very similar to the Xilinx UltraScale+ MPSoC family line with the addition of high speed analog-to-digital converters (ADC) and digital-to-analog converters (DAC) incorporated into the programmable logic (PL) making it ideal for software defined radio and other high-speed radio frequency (RF) applications. The PL features the same programmable fabric as the Kintex UltraScale+ and the RFSoC processing subsystem (PS) incorporates multiple ARM processors, GPU, and a host of supporting peripheral IP.

The specific RFSoC part tested was the XCZU28DR-2FFVG1517E mounted to the commercially available Xilinx ZCU111 development board. The board can be seen below in Fig. 1. This part is comprised of the following features [1]:

Processing Subsystem:

- Quad-core ARM Cortex-A53 Application Processing Unit
- Dual-core ARM Cortex-R5 Real-Time Processing Unit
- 256 KB on-chip memory with ECC
- ARM Mali-400 GPU
- Integrated memory and DMA controllers
- 4 High-speed serial transceivers (6.0 Gb/sec)
- Supporting IP (PCI Express blocks, SATA, DisplayPort controller, Ethernet MACs, USB, CAN, SPI, UART, etc.)
- Management units for power gating, configuration, and security
- PS System monitor ADC

Programmable Logic:

- 930,300 System Logic Cells
- 850,560 Flip-flops
- 425,280 Look-up tables for combinatorial logic
- 1080 BlockRAM modules (36 Kb each, approximately 38.9 Mb total)
- 4 Clock management tiles
- 4,272 Digital signal processing slices
- PL System monitor ADC
- 16 GTY Transceivers (up to 28.21 Gb/sec)
- 8 12-bit, 4.096GSPS RF-ADC w/ DDC

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- 8 14-bit, 6.554GSPS RF-DAC w/ DUC
- 8 Soft-decision forward error correction (SD-FEC)

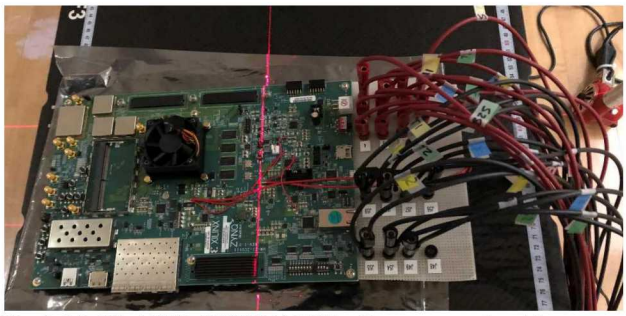

Fig. 1. Modified RFSoC ZCU111 DUT with power supply cables connected in the test facility.

B. *Hardware Setup*

In addition to the ZCU111 DUT, the full test setup included several important instruments located outside of the beam: two Keysight N6705C DC power analyzers, several laptops that interfaced to the power supplies and DUT FPGA board, and an oscilloscope. An external JTAG Configuration Manager (JCM), created by Brigham Young University, was used to monitor and fix bit flips in the configuration memory during testing and was connected to the DUT via JTAG [2]. All these devices, except for the JCM, were located in a control room 50 feet way from the beam testing room. The JCM was connected by an 18" JTAG cable and placed on a surface approximately 12" away beneath the DUT.

Board temperature was monitored periodically throughout the test using the on-board temperature sensor that could be accessed through the Xilinx Vivado software.

Two ZCU111 development boards were modified to attempt mitigation of any potential destructive latch-up events during proton testing. Power regulators on the development board had to be disconnected from the part to allow us to monitor power levels and to impose safe current limits during testing. The voltage regulators for the 0.85V, 1.2V, 3.3V, 2.5V, 1.8V, 0.925V, and 0.6V supplies were bypassed and provided externally using the two Keysight power supplies. Force and sense connections to the power supplies were utilized to maintain voltage levels after IR drop across the long power cables.

Modifications to the first board ended up being more complicated than previously thought due to the additional components for the ADC/DAC. ADC/DAC PLLs were not receiving power after these modifications and after multiple iterations, the PLLs were not retrievable. Due to a mistake in the modification of the second board, incorrect supplies were provided to the part which damaged it and the processor DDR memory. As a result, ADC and DAC testing was not able to be performed and the testing performed was limited to observing SEU in configuration memory and BlockRAM, and SEL for the device using the first, undamaged board.

A custom python script ran on one of the laptops for monitoring and controlling the power supplies. From other UltraScale+ family irradiations, a SEL sensitivity on the VCCAUX supply rail was expected which made monitoring and mitigating current spikes while testing crucial. The script would set current limits for each rail on the power supply, continuously monitor the current delivered on each channel, and attempt to mitigate any SEL events observed on any given channel. A high current state which caused the channel to deliver current at or near the current limit was flagged as a SEL event. When these were observed, the channel was lowered to a voltage below the holding voltage of the SEL site (typically 0.95V for rails at or above 1.2V nominal, or 0.05V for rails below 1.2V nominal). The voltage was held here for 0.75 seconds, then returned to the nominal level, which cleared the SEL site.

The oscilloscope monitored a 200 MHz clock generated by the processor subsystem that was fed to the PL. The loss of this "heartbeat" clock signal indicated that the board had experienced some kind of unrecoverable error. When one of these events was noted, the current beam run was stopped.

C. *Programable Logic Design*

The addition of high speed ADCs and DACs to the PL of the RFSoC make it a tempting candidate for RF LEO applications. The secondary goal of this testing was to characterize the ADCs and DACs in a proton environment, however, due to complications in modifying the ZCU111 development board to prevent damage from latch-up event these components were unable to be tested. For completeness though, the software defined radio (SDR) design created for this test is defined now.

The resources utilized by this design are shown in TABLE I. Fig. 2 gives a top-level view of the design, including the processor subsystem, SDR interface, and data flow using the AXI buses. Fig. 3 shows the processor-PL interface and some of the blocks in the PL. The main functionality of the SDR design was to transmit a digital waveform generated by a Direct Digital Synthesizer (DDS) through the on-chip DAC provided in the Xilinx RFDC IP block. The output analog signal was then looped back through the on-chip ADC in the RFDC IP block, filtered, and then passed through a Fast Fourier Transform (FFT) IP block to verify signal content. The waveform parameters of the transmitted pulses were written to the PL through the Localbus interface, a custom bus architecture developed at Sandia National Laboratories, which is similar to the AXI bus. Control of the SDR from the PS was also achieved through the Localbus.

TABLE I
Utilization of RFSoC Programable Logic design used in testing.

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	13463	425280	3.17
LUTRAM	4077	213600	1.91
FF	34492	850560	4.06
BRAM	41.50	1080	3.84
DSP	451	4272	10.56
IO	22	347	6.34
BUFG	7	696	1.01
MMCM	2	8	25.00

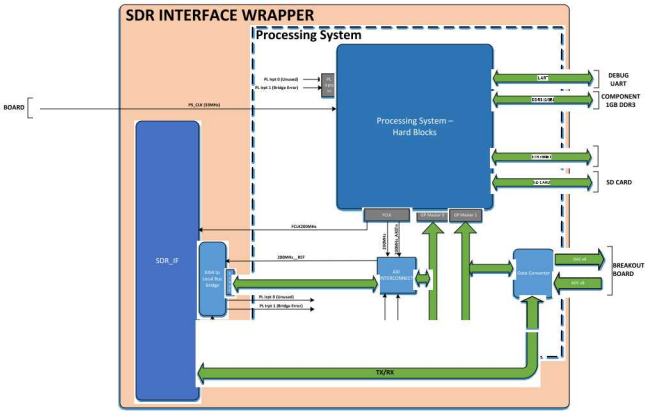

Fig. 2. Software Defined Radio Interface Wrapper block diagram.

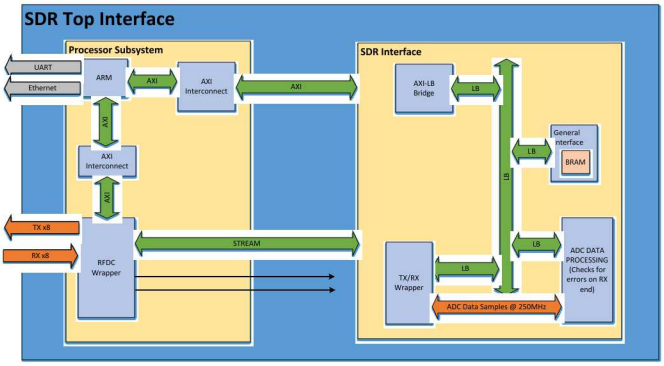

Fig. 3. Software Defined Radio Top Level Interface Block Diagram.

D. Proton Beam Properties

The RFSoC DUT was irradiated in air at the Northwestern Medicine Chicago Proton Center and can be seen in front of the beam at the facility in Fig 4. All irradiations were performed with the board rotated at normal incidence with the beam penetrating through the backside of the board. Beam energies were varied between 60, 125, and 200 MeV and total fluences are shown below in TABLE II.

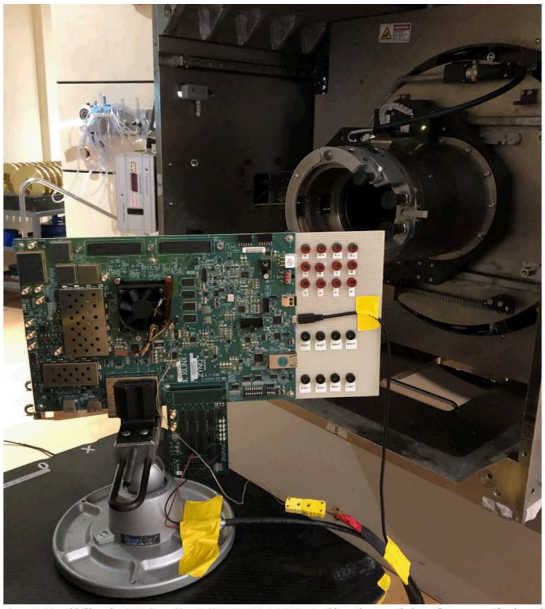

Fig. 4. Modified RFSoC ZCU111 DUT displayed in front of the beam at the test facility before final mounting.

TABLE II
PROTON BEAM ENERGIES AND FLUENCES FOR SEU AND SEL TESTING

Proton Energy (MeV)	Total Fluence (particles)
60	6.8×10^{10}
125	4.1×10^{12}
200	2.3×10^{12}

E. Test Procedure

Individual tests were run for 10 minutes if no latch-up was detected. Several failure states during irradiation also ended a test. The first failure state was the loss of the heartbeat generated by the PL where a power cycle failed to restart it. In this case the part appeared to suffer a Single-Event Functional Interrupt (SEFI) during various runs, but it is still unclear if this was a function of the self-correcting Python script working to control the power supplies and mitigate SEL. There were cases where if the power was lowered too much the part would reconfigure, so it is unclear if SEL and our conservative current limits caused voltage droop significant enough to activate the brownout circuitry and clear the part configuration. The second failure state that would end the current test was if communication to the processor was lost, which could indicate a possible SEU to the bus or somewhere in the fabric.

The goal of SEU testing is to examine the static SEU memory cells in the DUT. BlockRAM upset rates were measured by writing the test pattern 0xFFFF0000 to a range of memory locations and monitoring it from software running on one of the ARM cores. Configuration memory upset rates were measured by reading the memory back after irradiation and comparing this to a “golden readback” performed after configuration, but prior to the start of irradiation.

Testing was typically conducted with the die temperature elevated to 70 degrees Celsius, except when noted in the

discussion of results. Voltage rails were at nominal biases, but current limited to prevent a destructive latch-up.

III. Results

A. SEU and SEL Results

Single event upset (SEU) results are now reported for the configuration memory and BlockRAM as well as the number of latch-up events that were recorded over the range of Proton energies test. Cross-sections results for BlockRam, configuration memory, and single event latch-up (SEL) were calculated based on the data obtained from irradiation and can be seen in Fig. 5, Fig. 6, and Fig. 7 respectively. The cross-section is a measure of susceptibility of a given resource with lower numbers corresponding to better performance. In this figure configuration and BRAM cross-sections are per bit and SEL cross-section is per device.

The SEL runs were all performed at nominal biases but with elevated temperature at 70 degrees C. Two runs at 60 MeV proton energy were conducted at 81 degrees C to a total fluence of ~$1.8x10^{10}$ particles. One run, also at 60 MeV, was conducted at 100 degrees C (which is above the 85 degrees C specified maximum part temperature, per the device datasheet and this part grade) to a fluence of $1.8x10^{10}$. No SEL events were noted at either of these elevated temperatures. This elevated temperature data was combined with the remainder of data taken at 70 degrees C to obtain the final cross-sections for SEL events.

Weibull curves fitted to the data cross-sections are shown in Fig. 5. Low-energy proton results were not available, so curves were estimated by extrapolating down to ~10MeV energies since 10MeV was estimated as a threshold to approximate shielding effectiveness. In this figure statistical error bars are shown with two standard deviations (2-sigma).

The Cosmic Ray Effects on Micro-Electronics 1996 revision (CREME96) software was used to estimate the on-orbit event rates of the RFSoC when operating on-orbit. The orbital parameters used for rate estimates are given in Table III.

Event rates for the configuration memory and BlockRAM SEU, and device SEL, were calculated using the cross-section data and orbital parameters in average proton fluxes. The total configuration memory size is approximately 202 Mbit and the total BlockRAM is approximately 38.9 Mbit. The results are given in TABLE IV.

TABLE III.
Orbital parameters used in the CREME96 calculations for the RFSoC.

CREME96 Orbital Parameters
550km altitude at apogee & perigee
45 degree orbital inclination
AP8MIN average proton models
Solar minimum conditions
100 mils of aluminum shielding

To the best of our knowledge this is the first proton irradiation test of a Xilinx RFSoC. Previous proton testing on the closely related Xilinx MPSoC using 64 MeV and 105 MeV protons have reported BRAM SEU rates in the same range as the RFSoC but with higher configuration RAM SEU's, $3.3x10^{-16}$ cm^2/bit at 64MeV and $0.12x10^{-15}$ cm^2/bit at 105 MeV [3-5]. No SEL events were observed in [3], however, the authors of [5] did report them for proton test at 64 MeV and also present the analysis of why 16 nm FinFET technologies in Xilinx UltraScale+ devices are more susceptible to SELs than 20nm UltraScale devices that use planar technologies.

TABLE IV.
Event Rates calculated using cross-section data and orbital parameters.

Cross-Section	Event Rate (Average)
BRAM (38.9 Mbit)	~260K years/upset/bit
	2.39 days/upset/device
Configuration Memory (202 Mbit)	~23M years/upset/bit
	41.58 days/upset/device
Latch-up	~90 years/event

IV. Conclusion

The Xilinx RFSoC offers a unique solution to having an almost fully digital front end for SDR applications. One particularly interesting operational space for this device would be in low earth orbit. This paper presents the proton irradiation tests results on a modified ZCU111 development board at the Northwestern Medicine Chicago Proton Center. The results seen in this testing indicate that the part will rarely see latch-ups at LEO, with about 90 years per event at an average flux. The SEU events should be easily mitigatable. Future evaluation of the ADC and DAC component of the chip in a radiation environment is still required. A custom board for this testing is highly recommended for this future testing due to the complexity of modifying the existing development board.

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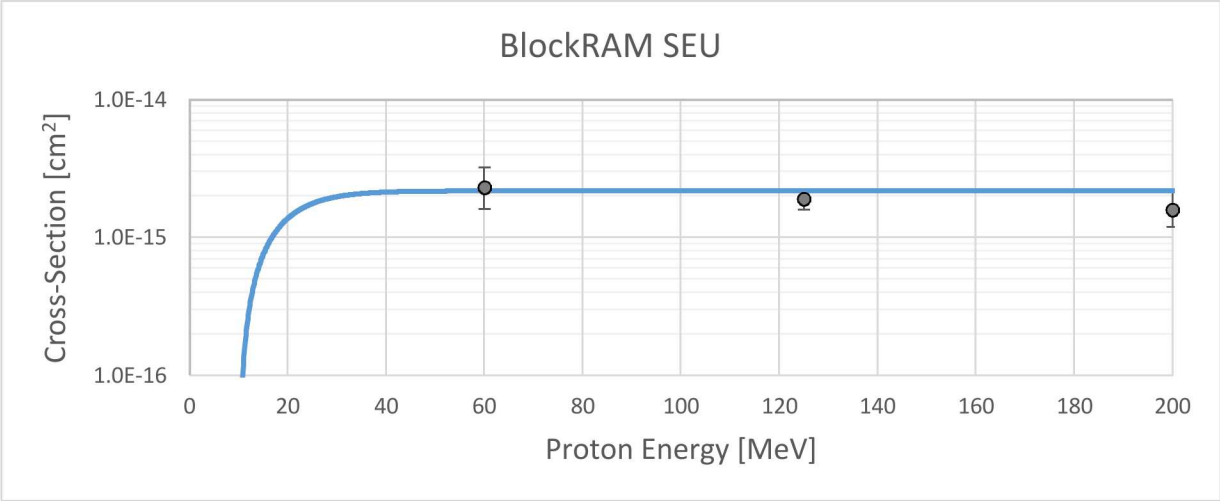

Fig. 5. Data points for BlockRAM SEU with corresponding Weibull curve.
BRAM cross-section is per bit.

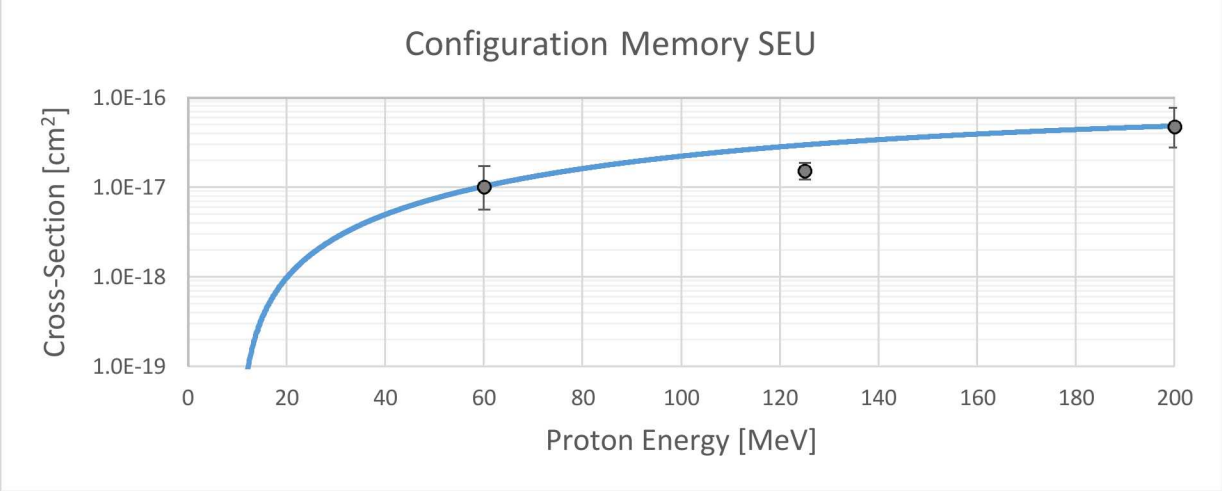

Fig. 6. Data points from configuration memory with corresponding Weibull curve.
Configuration cross-section is per bit.

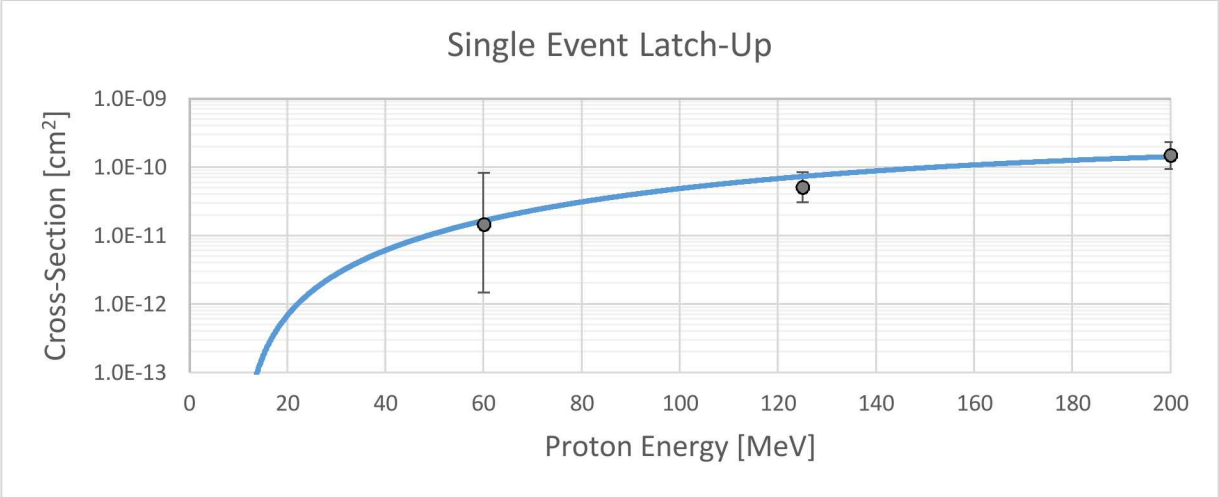

Fig. 7. Data points from SEL events with corresponding Weibull curve.
SEL cross-section is per device.