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SAND2019-7538C

Single-Event Characterization of the 16 nm FinFET Xilinx UltraScale+™ RFSoC Field Programmable Gate Array under Proton Irradiation

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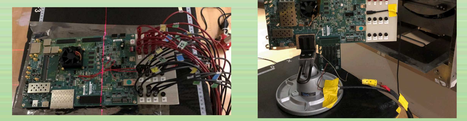
This study examines the single-event upset and single-event latch-up susceptibility of the Xilinx 16nm FinFET Zynq UltraScale+ RFSoC FPGA in proton irradiation. Results for SEU in configuration memory, BlockRAM memory, and device SEL are given.

INTRODUCTION

- Determine the flight-worthiness and feasibility of utilizing Xilinx UltraScale+ RFSoC parts in low Earth orbit (LEO) space environments.
- The device under test (DUT) was irradiated with protons with energies ranging from 60 MeV to 200 MeV at the Northwestern Medicine Chicago Proton Facility in Warrenville, IL.
- Proton effects on the DUT were recorded for
  - Single-event upset (SEU) for the FPGA configuration memory
  - Block random-access memory (BlockRAM™)
  - Single-event latch-up (SEL) results

ZYNQ ULTRASCALE+ RFSOC DEVICE OVERVIEW

- RFSoC similar to Xilinx UltraScale+ MPSoC family line.
- Incorporates high speed analog-to-digital converters (ADC) and digital-to-analog converters (DAC) into the programmable logic (PL).
- Ideal for software defined radio and other high-speed radio frequency applications.
- Processing Subsystem:
  - Quad-core ARM Cortex-A53 Application Processing Unit
  - Dual-core ARM Cortex-R5 Real-Time Processing Unit
  - 256 KB on-chip memory with ECC
  - ARM Mali-400 GPU
- Programmable Logic:
  - **8 12-bit, 4.096GSPS RF-ADC w/ DDC**
  - **8 14-bit, 6.554GSPS RF-DAC w/ DUC**
  - 930,300 System Logic Cells
  - 850,560 Flip-flops
  - 425,280 Look-up tables for combinatorial logic
  - 1080 BlockRAM modules



Modified RFSoC ZCU111 DUT at Test Facility

TEST HARDWARE SETUP

- ZCU111 dev board modified to mitigate potential destructive latch-up events during proton tests.
- Power regulators disconnected from the part to allow monitoring and online current limits during tests.
  - Voltage regulators for the 0.85V, 1.2V, 3.3V, 2.5V, 1.8V, 0.925V, and 0.6V supplies bypassed and provided externally using two Keysight power supplies.
  - Power supply force and sense connections utilized to maintain voltage levels.
- JTAG Configuration Manager (JCM), located 12" from the DUT in beam testing room, was used to monitor and correct bit flips in configuration memory during testing [2].
- Board modifications more complicated due to the additional components for the ADC/DAC.
  - ADC/DAC PLLs were not receiving power after these modifications and the PLLs were not retrievable.
  - Due to this, custom SDR PL application was not testable during irradiation.
- Custom python script used to monitoring and controlling the power supplies.
- SEL sensitivity on the VCCAUX supply rail was expected from previous UltraScale+ family tests.
- Monitoring and mitigating current spikes while testing was crucial to mitigate any SEL events.
- High current state causing a channel to deliver current near the limit was flagged as a SEL event.
  - When observed, the channel was lowered to a voltage below the holding voltage of the SEL site.
  - Voltage was held there for 0.75 seconds, then returned to the nominal level, which cleared the SEL site.

TEST PROCEDURE

- 10 minute runs if no latch-up detected.
- Run ended if
  - Power cycle did not return PL heartbeat possibly caused by device encountering Single-Event Functional Interrupt (SEFI)
  - Loss of communication with processor indicating possible SEU to bus or fabric.
- BRAM upset rates were measured by monitoring changes to stored test pattern.
- Configuration memory upset rates were measured by comparing memory content after each irradiation trial with the original "golden" copy.
- SEL runs performed at 70 degrees C with voltage rails at nominal biases
  - Current limited to prevent destructive latch-up.

Proton Energy (MeV)	Total Fluence (particles)
60	$6.8x10^{10}$
125	$4.1x10^{12}$
200	$2.3x10^{12}$

Proton Beam Energies and Fluences for SEU and SEL Testing

RESULTS

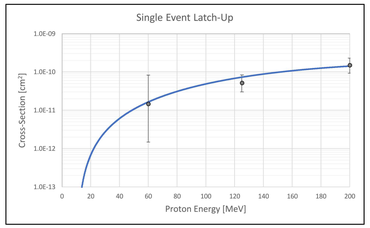
- SEU results reported for the configuration memory and BlockRAM as well as the number of latch-up events recorded over the range of Proton energies test.
- The Cross-sections results calculated based on the data obtained from irradiation.
  - The cross-section is a measure of susceptibility of a given resource with lower numbers corresponding to better performance.
  - Configuration and BRAM cross-sections are per bit and SEL cross-section is per device.
- Several elevated temperature trials resulted in no SEL events
  - Two runs at 60 MeV proton energy at 81 degrees C to a total fluence of ~$1.8x10^{10}$ particles.
  - One run at 60 MeV and 100 degrees C (above specified part max rating) to a fluence of $1.8x10^{10}$.
- Elevated temperature data was combined with the remainder of the data taken at 70 degrees C to obtain final cross-sections for SEL events.
- Weibull curves fitted to the data cross-sections.
  - Statistical error bars shown with two standard deviations (2-sigma).
- Low-energy proton results were not available, so curves were estimated by extrapolating down to ~10MeV energies since 10MeV was estimated as a threshold to approximate shielding effectiveness.
- The Cosmic Ray Effects on Micro-Electronics 1996 revision (CREME96) software was used to estimate the on-orbit event rates of the RFSoC when operating on-orbit.

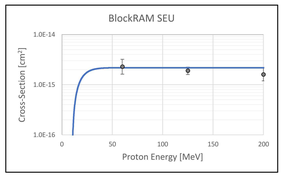
CREME96 Orbital Parameters
550km altitude at apogee & perigee
45 degree orbital inclination
AP8MIN average proton models
Solar minimum conditions
100 mils of aluminum shielding

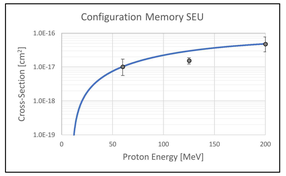
Orbital parameters used in CREME96 calculations for RFSoC.

Cross-Section	Event Rate (Average)
BRAM (38.9 Mbit)	~260K years/upset/bit
	2.39 days/upset/device
Configuration Memory (202 Mbit)	~23M years/upset/bit
	41.58 days/upset/device
Latch-up	~90 years/event

Event rates calculated using cross-section data and orbital parameters.







SEL event cross-section per device, BlockRAM SEU cross-section per bit, and Configuration memory SEU per bit with corresponding Weibull curves.

CONCLUSION

- The Xilinx RFSoC opens the possibility of having an almost fully SDR digital front end that could operate in low earth orbit.
- Testing indicates that the part will rarely see latch-ups at LEO, with about 90 years per event at an average flux.
- Mitigation of SEU events should be possible with correct monitoring.
- Future evaluation of the ADC and DAC component of the chip in a radiation environment is still required.
- A custom board for this testing is highly recommended for this future testing due to the complexity of modifying the existing development board.

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This work was supported by a collaborative research and development agreement between Sandia National Laboratories and Collins Aerospace.

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