Current Controlled Operation of Cascaded H-Bridge Converter for Fast SoC Balancing in Grid Energy Storage

SAND2019-7407C

Amir Hussain, Electrical & Computer Engineering, University of Houston
Kaushik Rajashekara, Electrical & Computer Engineering, University of Houston
Krishna Raj, Electrical & Computer Engineering, University of Houston
Harish Krishnamoorthy, Electrical & Computer Engineering, University of Houston
Stanley Atcitty, Sandia National Laboratories

***Abstract*: In grid energy storage systems based on batteries, the interface converter topology plays a significant role in the optimized operation of the system. Among different types of multi-level converters, cascaded H-bridge converter (CHBC) provides the advantage of utilizing isolated battery pack (BP) with a lower number of series-connected cells and can perform state of charge (SoC) balancing by controlling the power flow to/from each BP. However, the rate of SoC balancing is limited due to low balancing current when the amount of power exchange is low. This paper proposes a new power control method using hybrid modulation strategy with extended operating region (HMSEOR) which enables the CHBC to perform fast SoC balancing at constant current irrespective of the amount of power exchange between the battery system and the grid. The HMSEOR allows power flow from a BP with a higher SoC to a BP with a lower SoC without compromising power exchange with the grid. The performance of the proposed SoC balancing method is validated through real-time hardware-in-the-loop (HIL) simulation and compared with the conventional SoC balancing at unity power factor operation.**

***Keywords*: Battery Management System, SoC balancing, Energy Storage System, Cascaded H-Bridge Converter, Nearest Level Control.**

I. INTRODUCTION

The increasing penetration of variable renewable energy sources into modern power systems has driven interest in grid-scale energy storage systems (ESS) to accommodate the stochastic power deficit or excess from these sources to meet the power demanded by grid or load [1]. Battery-based ESS (BESS) is the most popular technology for such applications, with strong research focused on improving energy density and the cost of Lithium-ion batteries [2]. The most elementary building block of a battery is a battery cell, whose voltage and current ratings, in the order of few volt and ampere, are modest compared to its application in grid-scale ESS. Therefore, several cells are connected in series and parallel to increase voltage and current rating of the resulting set [3], which is referred to as battery pack (BP) in this paper. Series connection of a large number of cells brings challenges to the efficient and reliable operation of BESS. This is because of differences in cell parameters, even in the seemingly identical cells. Differences in cell parameters starts with a slight variation during manufacturing processor operating conditions and continue to grow as cells age. In a series-connected configuration, all cells are loaded with same current. If a cell mismatch is left uncompensated, the weak cells in the BP tend to get deeply discharged or overcharged during operation, thereby adversely affecting the lifespan of the cells. Therefore, a battery module (BM) is provided with a battery management system (BMS) to monitor the cell voltage, current, and temperature and to disconnect the BM in case the monitored variables reach unsafe values. It also balances the state-of-charge (SoC) of the cells, either by dissipating the energy of the cells with higher SoC or by transferring energy among the cells [4]-[5].

A battery system for grid energy storage requires a relatively high voltage rating to meet the required power demand with reasonable efficiency. To obtain a high voltage BM, a very large number of cells need to be connected in series, which makes the BMS circuitry complex, inefficient and less reliable. In addition, building a custom BP for each specific application leads to a high dispersion of BPs which is not economically viable. Therefore, a standard BM with a relatively low number of cells in series and parallel is configured to reach the minimum voltage and current rating. Then these standard BMs are combined in series-parallel combination to meet the rating of a particular BESS [6]-[7]. This option takes advantage of scaling economy as well as efficiency with more reliable BMS for a BM. The SoC balancing and other battery management tasks among the different BMs are just as important as they are among the cells within a BM. Several methods have been proposed for SoC balancing among BMs, which largely depends on the configuration in which the BMs are connected. Conventionally, a two-level inverter uses a series connection of BMs which requires an external circuit for performing SoC balancing among BMs. Further, the two-level inverter suffers from the disadvantages of using a bulky transformer, large filter, and switches of a higher rating. On the other hand, multi-level converters can accomplish the task of SoC balancing very efficiently by adjusting the power flow from each BM, according to their current SoC. This balancing process is non-dissipative and does not need additional circuitry for this purpose.

The main multilevel topologies—namely, neutral point clamped, flying capacitor and cascaded converters—and their variants have been proposed for the integration of battery-based energy storage [8]-[9]. Generally, among these topologies the cascaded multilevel converter has the lowest installed switch power rating, lowest *LC* filter stored energy [10], and the best reliability and fault tolerance owing to its modularity—a feature that enables the inverter to continue operating at lower power levels even after cell failure. Most of the BM SoC balancing methods that employ cascaded converters are based on the sorting-based algorithm that differs from each other based on the modulation strategy used. A modulation technique based on nearest level control (NLC) was used in [11] for SoC balancing by employing a cascaded H-bridge converter (CHBC). NLC operates an appropriate number of CHBC modules to produce

either positive, negative or zero output voltage as required by the voltage level to be synthesized. The switching state of CHBC corresponding to positive or negative output voltage is termed as active state while the zero-output voltage is termed as idle state in this paper. As an improvement to NLC, a hybrid modulation strategy (HMS), is used in [12]. HMS operates one of the CHBC modules in pulsed width modulation (PWM) mode, in addition to operating other modules in active or idle state, resulting in a good compromise between output voltage distortion and switching loss. HMS with an extended operating region is presented in [13] for capacitor voltage balancing in CHB rectifier. In this scheme, one CHB module operates in PWM mode and all other CHB modules are operated in active mode. Another modulation scheme based on the first ON - first OFF principle is presented in [14] and draws the equal amount of power from BMs when the SoC difference among the modules is within a hysteresis band. Despite the methods described above, the rate of SoC balancing among BMs is still an issue which needs to be addressed given that the BESS must always be in operating condition. In most of the SoC balancing methods implemented through control of a multilevel converter, the rate of SoC balancing varies proportionally with the grid current which depends on the amount of power exchange between the BESS and the grid at unity power factor (UPF). Therefore, the rate of SoC balancing decreases as the amount of power exchange is decreased and the SoC balancing is stopped when there is no power exchange between the BESS and the grid. In such a case, rate of SoC balancing among BMs is slow with lower power exchange of BESS with the grid and balancing may not occur if there is no power exchange.

In this paper, a faster SoC balancing method for BMs based on rated current operation of a nine-level CHBC employing HMS with extended operating region for grid-connected BESS is proposed for the first time. The rated current operation of CHBC maintains the rated line current which enables the CHBC to perform SoC balancing at a higher rate during the event of lower amount of power exchange between the BESS and the grid. The rated current operation also allows the CHBC to operate at lower voltage level which further enhances the rate of SoC balancing. The HMS with extended operating region enhances the rate of SoC balancing by allowing lower SoC BPs to absorb power even when the BESS delivers power to the grid, and vice-versa. Real time hardware-in-the-loop simulation has been performed to verify the proposed SoC balancing strategy and the effectiveness of balancing scheme is validated through comparison results under the rated current operation and UPF operation.

II. SOC BALANCING USING CHBC

A three-phase CHBC interfacing battery energy storage to the grid is shown in Figure 1. It employs N battery modules in one phase which are shown as BM_1, BM_2, BM_n. Each BM comprises of a BP, a DC-DC bidirectional converter (BDC) and an H-bridge converter. The BDC maintains constant input voltage to the H-bridge converter irrespective of the SoC of the BM. It also filters the second harmonic current from the BP which could otherwise adversely affect the battery life. The output voltage,

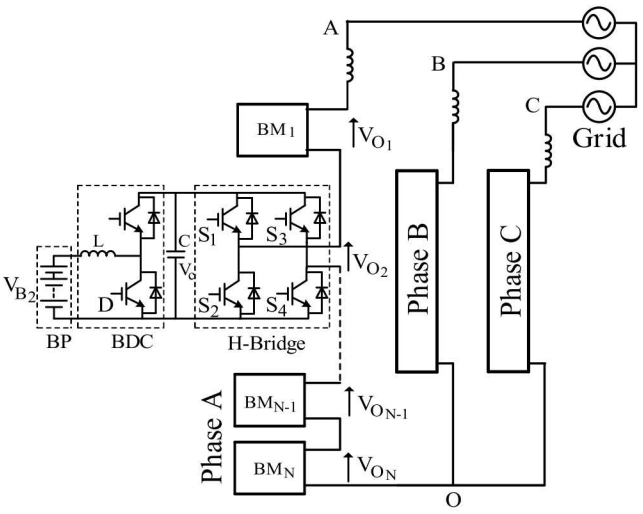

Figure 1. Three-phase CHBC connected to the grid.

$V_{O,}$ of a BM can be V_C, 0 and $-V_{C,}$ which are represented by mode 1, mode 0 and mode -1 operation of the BM. Since the outputs of the BMs are cascaded, the current flowing through each BM is same while the output voltage of a phase is the sum of the output voltages of the BMs. The CHBC shown in Figure 1 can generate 2N+1 voltage levels ranging from $-NV_C$ to NV_C. Since the output voltage is alternating, it takes all the levels between $-NV_C$ to NV_C. When the CHBC is required to synthesize a lower level of voltage, it exhibits flexibility in terms of selecting a BM to operate it in mode 1, mode 0 or mode -1. This flexibility is utilized to control the direction of power flow from a BM. The BPs are sorted based on their SoC such that the H-Bridge converter with lowest SoC is controlled to supply the lowest amount of power to the grid and absorbs the highest amount of power while charging the BESS.

In Figure 2(a), an example of a nine-level CHBC is shown to compare the operation of NLC [11] with the proposed hybrid modulation strategy with extended operating region (HMSEOR) at UPF operation and rated current operation. Figure 2(b), Figure 2(c) and Figure 2(d) compare the modulation based on NLC, HMSEOR at UPF operation and the proposed rated current operation employing HMSEOR, respectively. The four BMs are represented as BM_1 to BM_4, having BP with voltages VB_1 to VB_4 respectively. The SoCs of the BPs are assumed to be in descending order from BM_1 to BM_4. Power delivered or absorbed by a BM during an interval is indicated by P_{del} and P_{ab} respectively. The positive cycle of CHBC operation for SoC balancing using NLC is depicted in Figure 2(b). During the interval t_1 to t_2, the voltage level V_C is synthesized by mode 1 operation of BM_1. The rest of the three CHB modules are operated in mode 0. As a result, BM_1 starts supplying current at the instant t_1 while the other three BMs are in idle state. The idle state of a BM is indicated by Z in Figure 2(b). Similarly, BM_2, BM_3 and BM_4 start supplying current at t_2, $t_{3,}$ and t_4 respectively to synthesize the required voltage levels. Note that the instantaneous current from each BM is the same, but the duration of their operation is different. This results in a difference among average currents supplied by different BMs which eventually leads to SoC balancing.

The rate of SoC balancing, as well as the quality of output waveform, is enhanced by employing the proposed HMSEOR as shown in Figure 2(c). HMSEOR is a combination of low-frequency square wave modulation and high frequency sinusoidal pulsed width modulation (SPWM). The low frequency square wave modulation is used to balance the SoCs while SPWM operation of CHB modules improves output current waveform. Contrary to NLC, HMSEOR does not operate the CHB modules in mode 0. Instead, all the CHB modules are operated either in mode 1 or mode -1 except for the one which is operated in PWM mode. For example, during t_2 to t_3 in Figure 2 (c), the reference voltage can be synthesized by operating BM_1 and BM_2 in mode +1, BM_4 in mode -1 and BM_3 in positive PWM mode. It can be observed that BM_1, BM_2 and BM_3 supply power while BM_4, having the least SoC, is able to absorb power which was not possible in the case of NLC.

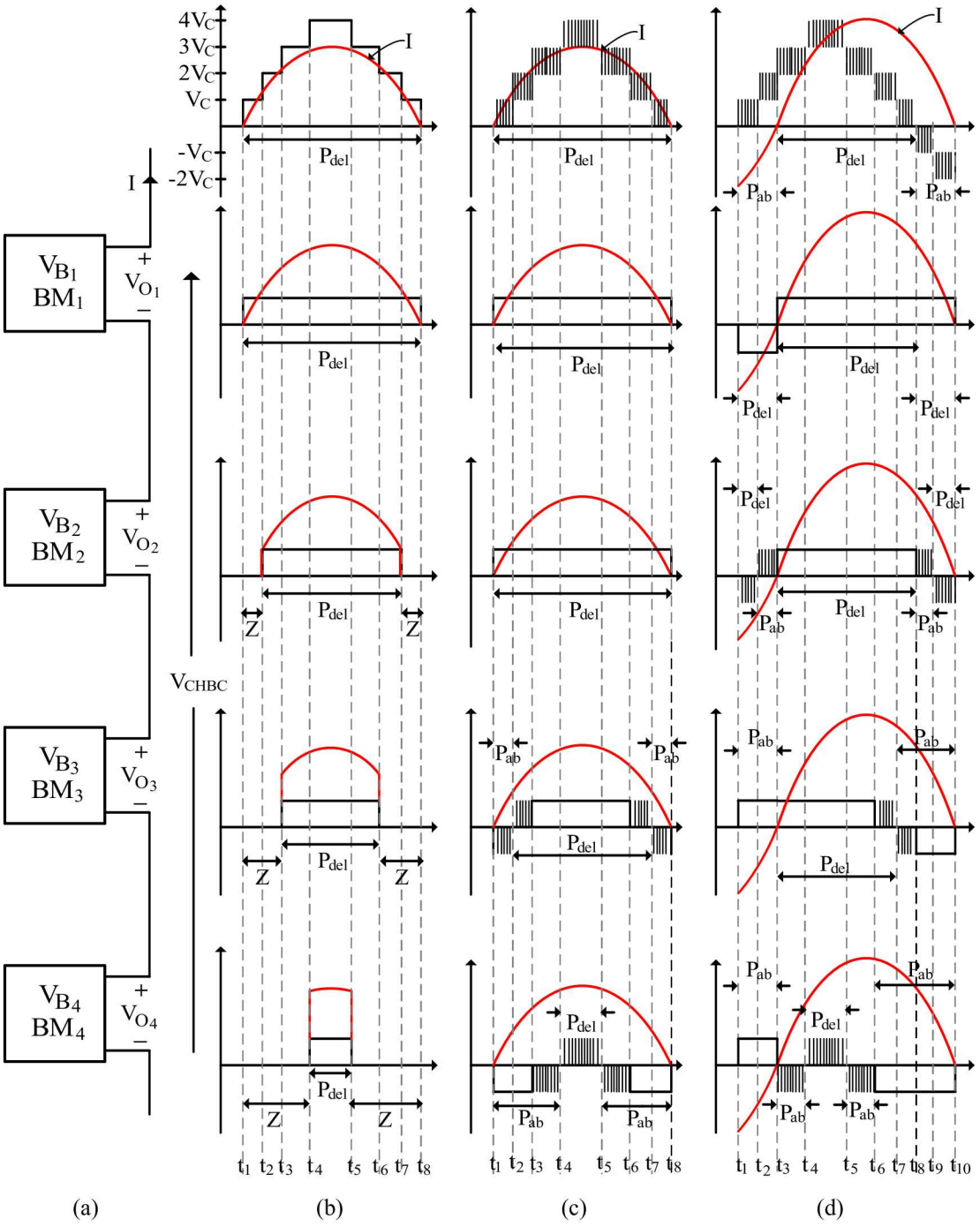

Figure 2. Voltage and current waveform from the four BMs considering BM_1, having highest SoC and BM_4 having lowest. (a) Nine-level CHBC. (b) NLC (c) HMSEOR with UPF (d) HMSEOR with rated current operation.

Therefore, HMSEOR can discharge a BP with the highest SoC and charge the one with the lowest SoC while synthesizing a voltage level. Figure 2(b) and Figure 2(c) show the operation of SoC balancing when CHBC is controlled to operate at UPF. In this case, the balancing rate is limited proportionally to the amount of power exchange between the BESS and the grid. The maximum instantaneous current matches with the maximum voltage when the BP with the lowest SoC must supply power to the grid. On the other hand, Figure 2(d) shows the proposed rated current operation of CHBC, which improves the rate of SoC balancing in two ways: first, it increases the operating current to the rated current for the same amount of power exchange and second, it reduces the average discharge current from the lowest SoC BM by providing a phase shift between peak voltage and peak current. Note that the BM_4 is required to supply power during t_4 to t_5, but the peak of instantaneous current occurs during t_5 to t_6 which reduces the average discharging current from BM_4.

III. RATED CURRENT OPERATION OF CHBC

The amount of power delivered or absorbed by the BESS is contingent on the mismatch between the load demand and generation, which may take any value between 0 to the rated BESS power, P_{rat}. For a lower amount of power exchange at UPF, the balancing current is proportionally low, which results in a lower rate of SoC balancing. To overcome this issue, the controller is designed to operate at rated current irrespective of the amount of power exchange between the BESS and the grid. The rated current operation for a lower amount of power exchange enables the CHBC to synthesize relatively lower voltage levels, which is shown to further enhance the speed of SoC balancing. This can be explained with the help of phasor diagrams shown in Figure 3(a)-(d). Figure 3(a) depicts the single line diagram of the CHBC-grid system with grid voltage as a reference. Figure 3(b) depicts the condition when the BESS is supplying rated power to the grid at rated current and UPF. The angle δ is exaggerated for the clarity of the diagram. In practice, the line inductance is chosen to be within 5% of the base impedance, which maintains minimum power angle for UPF operation. In Figure 3(c), the operation of BESS is shown for a lower amount of power exchange at UPF. Notes that the height of the vector $j\overline{I_a X_s}$ varies in accordance with the magnitude of the actual power P_{act}. Figure 3(d) shows the actual power exchange during rated current operation. This is achieved by controlling the CHBC output voltage such that the magnitude of actual current equals the rated current. Figure 3(b)-(d) shows that the UPF operation and rated current operation converge to the same point of operation if the rated amount of power is exchanged with the grid. Therefore, the rate of SoC balancing will be same for UPF operation and rated current operation. As the amount of power exchange decreases, the rated current operation maintains the rated current with a reduction in CHBC voltage while the UPF operation decreases the current proportional to the power nearly at constant CHBC voltage. As a result, rated current operation enhances the rate of SoC balancing for a lower amount of power exchange while the opposite is true for UPF operation. It is also worth mentioning that CHBC is operated at rated current only until the SoC is balanced and switched back to UPF operation once the SoCs are balanced. Figure 4 shows block diagram of the proposed rated current operation of CHBC for SoC balancing among BMs. It is assumed that the reference power, $P_{ref,}$ is made available through a higher level control. The actual amount of power is calculated by sensing the grid voltage and line current and is compared with the reference power. The output of the PI controller I generates reference for the direct axis current.

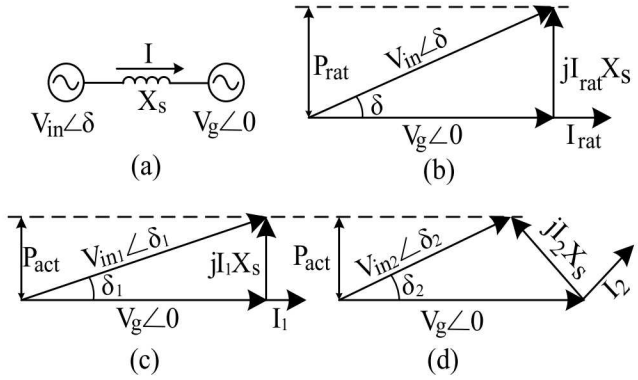

Figure 3. (a). Single line diagram of CHBC-grid system, (b) Rated power operation at UPF, (c) Actual power operation at UPF, (d) Actual power operation at rated current.

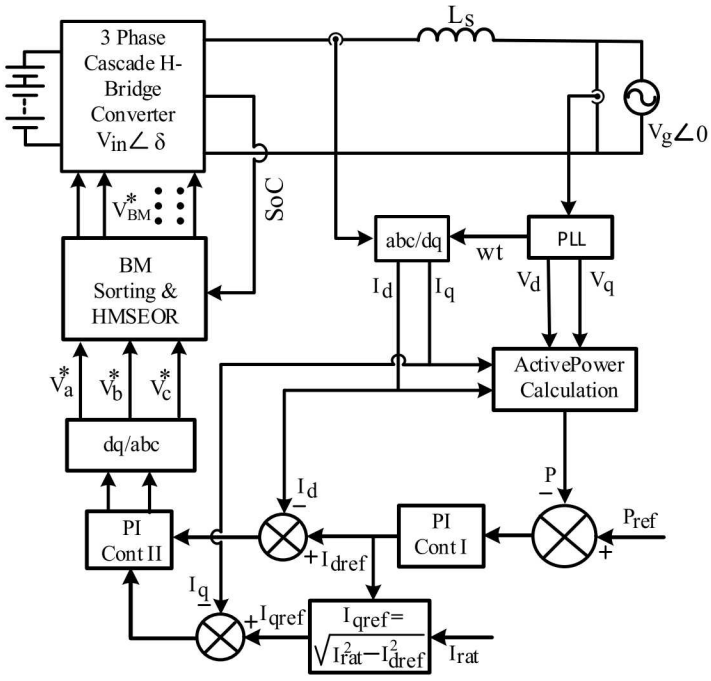

Figure 4. Block diagram implementing rated current operation of CHBC with HMSEOR.

The reference for the quadrature axis current is calculated using the rated current and the reference of the direct axis current as shown in Figure 4. The output of the PI controller-II sets the reference voltage to be obtained from the CHBC. The reference voltage to be synthesized from each BM is calculated based on SoC and the HMSEOR as explained in Section III.

IV. REAL-TIME HIL SIMULATION

To validate the proposed SoC balancing method, a three-phase, nine-level, 100kW CHBC is modeled using Typhoon real-time simulator. The rated phase to neutral voltage and line current is taken as 1.33kV and 25A respectively. The specification of the BM and the remaining simulation parameters are provided in Table 1. First, the system is simulated for rated power flow from BESS to the grid using the proposed rated current operation of CHBC. Figure 5 depicts the waveforms of the CHBC nine-level voltage, grid voltage, and the line current. In this case, rated current of 25A flows in the line. Note that the instants of maximum current and the maximum grid voltage are the same which justifies that the rated current operation leads to UPF in case of rated power flow between the CHBC and the grid. Figure 6 and Figure 7 show the variation of SoC and current from the four BPs during the SoC balancing process. The initial SoCs of the BPs is given in Table 1. The instants of SoC balancing among different BPs are indicated in Figure 6. Figure 7 shows that the BP_1, having the highest SoC, supplies the highest amount of current while the BP_4, having the lowest SoC, supplies the lowest amount of current. In the second case, CHBC is controlled to deliver 50kW power to the grid at UPF. The corresponding waveforms of the CHBC voltage, grid voltage, and the line current are shown in Figure 8. In this case, the RMS value of line current has decreased to 18A due to decrease in power transfer at UPF. Figure 9 and Figure 10 show the variation of SoC and current drawn from the four BPs. The rate of SoC balancing for 100kW and 50kW power transfer can be compared from Figure 6 and Figure 9. Note that the rate of proposed rated current operation can be compared from Figure 9 and Figure 12. For 50kW power transfer, the SoCs of all the BPs is balanced at t = 930s and t = 315s under UPF operation and the rated current operation respectively. For the case of rated power transfer, both methods converge to the same point of operation and take 700s to balance the SoCs of all the BPs.

Table 1. Simulation Parameters

Discription	Symbol/Value
Number of BMs	N = 4
BP Nominal Voltage	V_{nom}= 360V
BP Capacity	C_{nom}= 30Ah
Initial SoC	SoC_1 = 60% SoC_2= 55% SoC_3= 50% SoC_4= 45%
BDC Output Voltage	V_O= 500V
BDC inductance	L = 5mH
BDC Capacitance	C = 50mF
BDC Switch. Frequency	f_{BDC}= 20kHz
Inverter Switch. Frequency	f = 2kHz
Grid Voltage	V_g= 1320V
Line Inductance	L_s= 25mH

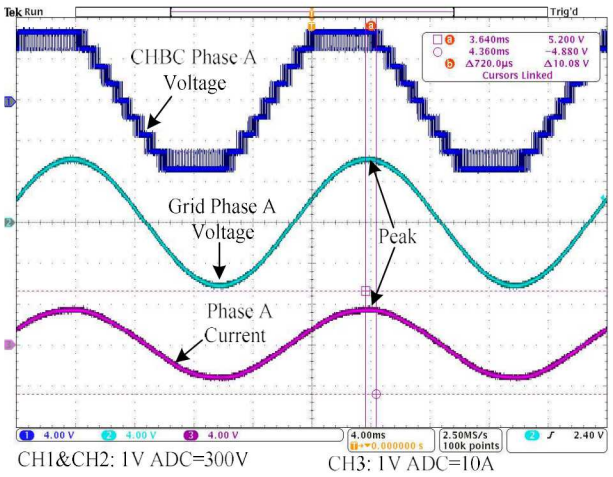

Figure 5. Waveforms of CHBC voltage, grid voltage, and line current during 100kW power transfer from BESS to the grid at rated current operation.

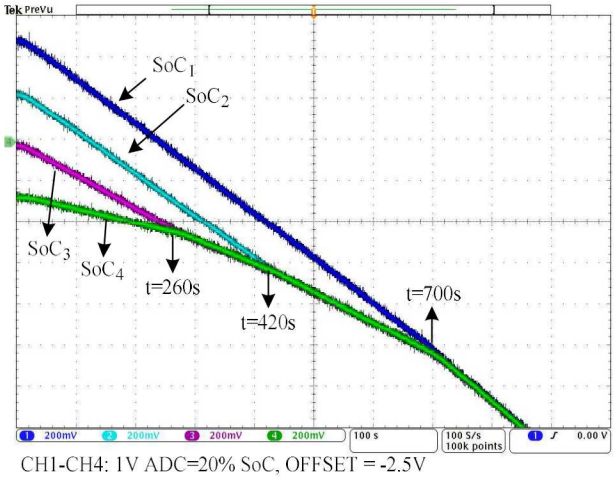

Figure 6. Variation of SoCs of the four BPs during 100kW power transfer from BESS to the grid at rated current operation.

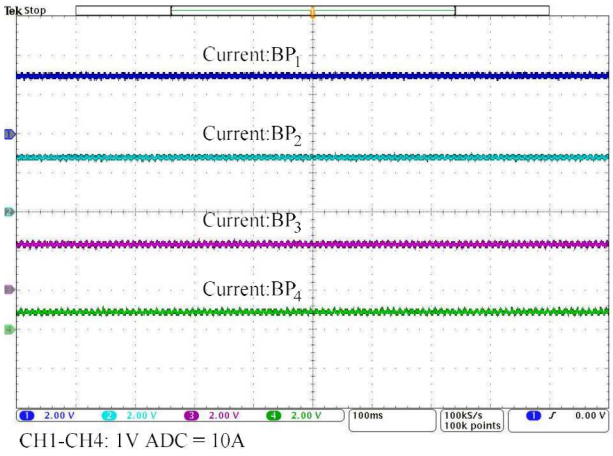

Figure 7. Waveforms of current from the four BPs during 100kW power transfer from BESS to the grid at rated current operation.

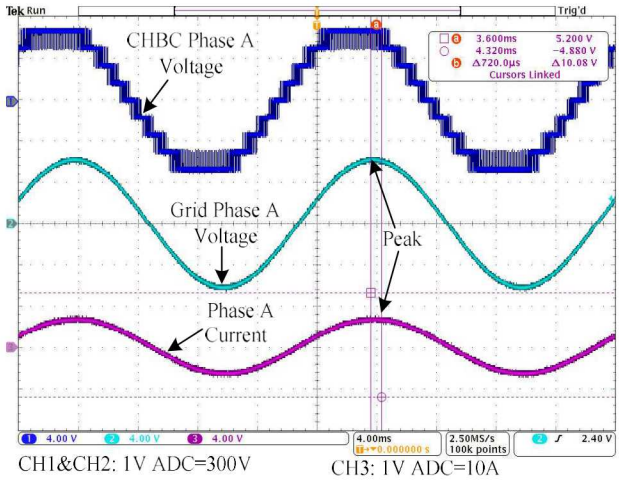

Figure 8. Waveforms of CHBC voltage, grid voltage and line current during 50kW power transfer from BESS to the grid at UPF operation.

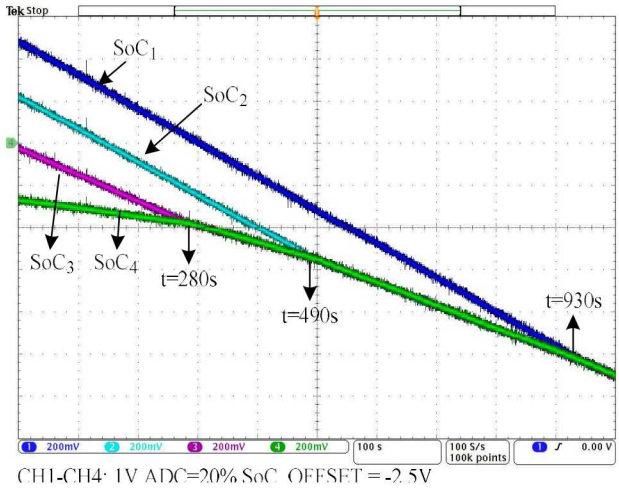

Figure 9. Variation of SoCs of the four BPs during 50kW power transfer from BESS to the grid at UPF operation.

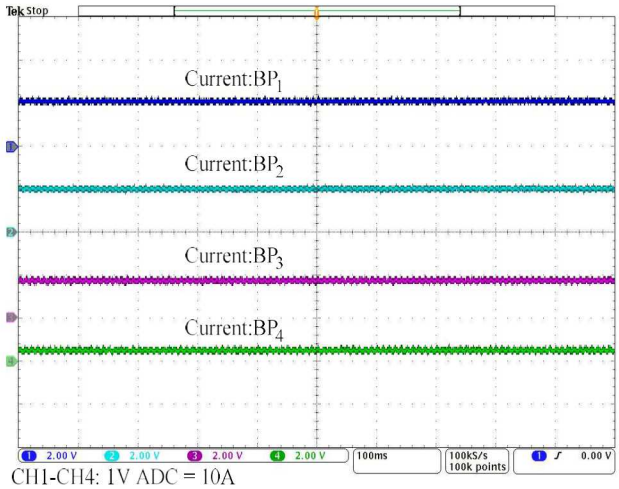

Figure 10. Waveforms of current from the four BPs during 50kW power transfer from BESS to the grid at UPF operation.

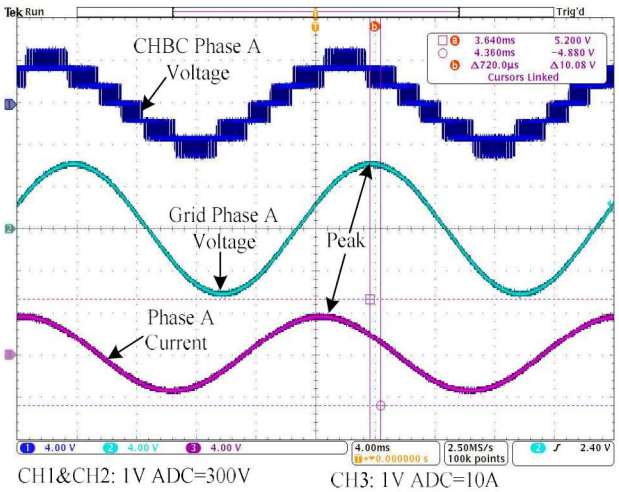

Figure 11. Waveforms of BESS voltage, grid voltage, and line current during 50kW power transfer from BESS to the grid at rated current operation.

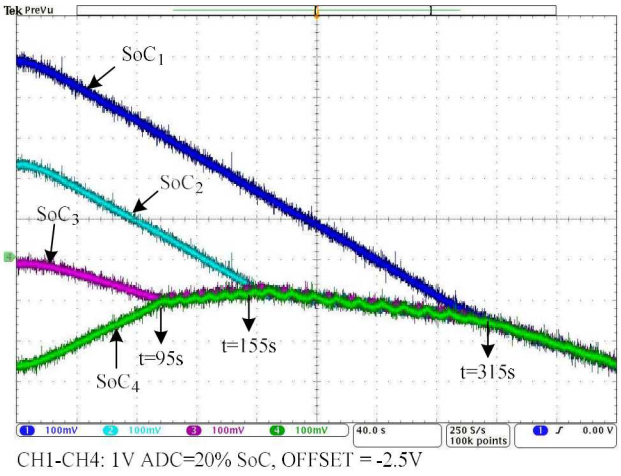

Figure 12. Variation of SoCs of the four BPs during 50kW power transfer from BESS to the grid at rated current operation.

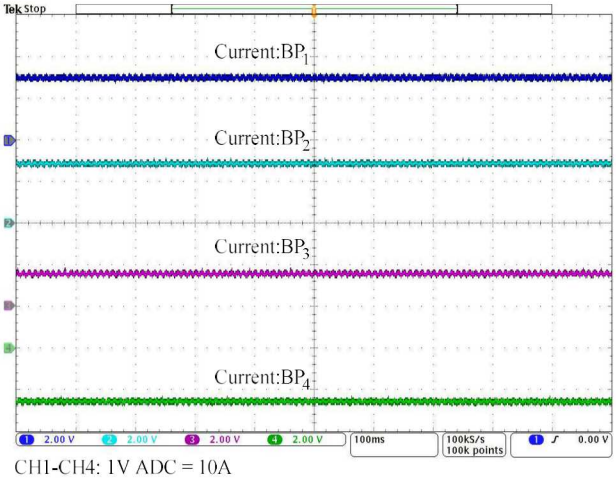

Figure 13. Waveforms of current from the four BPs during 50kW power transfer from BESS to the grid at rated current operation.

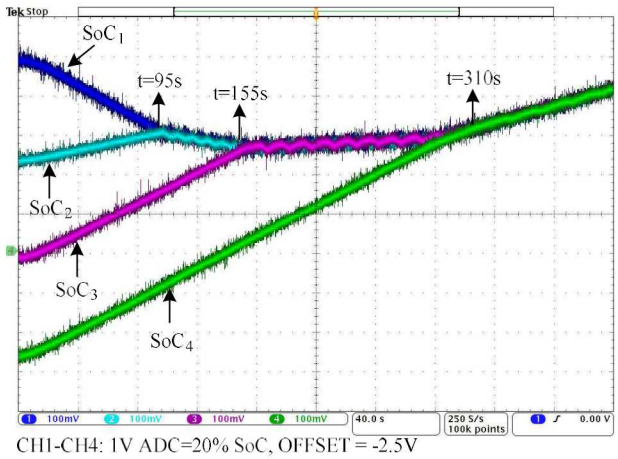

Figure 14. Variation of SoCs of the four BPs during 50kW power transfer from the grid to BESS at rated current operation.

Figure 13 shows the current waveforms from the four BPs in the case of 50kw power transfer using the proposed method. Figure 13 shows that the proposed method with HMSEOR allows the lowest SoC BP_4 to charge while other BPs are being discharged. This leads to a faster SoC balancing, as observed from Figure 12. Although HMSEOR is applied in the case of UPF operation of CHBC, it does not enable the lowest SoC BP to charge. This is because the CHBC must synthesize a higher voltage level for UPF operation. The proposed method is also tested for charging of the BESS at 50kW. The performance of the SoC balancing is shown in Figure 14 and is similar to the case of discharging of the BESS.

V. CONCLUSION

This paper presents a fast SoC balancing method of battery-fed CHBCs for grid energy storage applications. The rate of SoC balancing can be enhanced by operating the CHBC at rated current when the amount of power exchange is less than the rated power. The proposed method is validated through real-time hardware-in-the-loop simulation for charging as well as discharging of the BESS. The performance of the proposed method is compared with conventional SoC balancing at UPF operation. The rate of SoC balancing using the proposed method is same as that of UPF operation for rated amount of power exchange between the BESS and the grid. As the amount of power exchange is decreased, the rate of SoC balancing increases using proposed method, while the UPF operation decreases the rate of SoC balancing. For modulation of the CHBC, the HMSEOR is applied which enables power exchange among the BPs without compromising the amount of power exchange between the CHBC and the grid. The HMSEOR also enables the BPs with a lower SoC to charge when the BESS operates at a lower level of the output voltage.

VI. ACKNOWLEDGEMENT

The authors gratefully acknowledge support for this work from Dr. Imre Gyuk and the Energy Storage Program in the Office of Electricity Delivery and Energy Reliability at the U.S. Department of Energy. Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia LLC, a wholly owned subsidiary of Honeywell International Inc. for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

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