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Grid-forming Inverter Experimental Testing of Fault Current Contributions

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Abstract — **Historically, photovoltaic inverters have been grid-following controlled, but with increasing penetrations of inverter-based generation on the grid, grid-forming inverters (GFMI) are gaining interest. GFMIs can also be used in microgrids that require the ability to interact and operate with the grid (grid-tied), or to operate autonomously (islanded) while supplying their corresponding loads. This approach can substantially improve the response of the grid to severe contingencies such as hurricanes, or to high load demands. During islanded conditions, GFMIs play an important role on dictating the system's voltage and frequency the same way as synchronous generators do in large interconnected systems. For this reason, it is important to understand the behavior of such grid-forming inverters under fault scenarios. This paper focuses on testing different commercially available grid-forming inverters under fault conditions.**

Index words: grid-forming, distributed energy resources, fault, microgrid.

I. Introduction

With increasing penetrations of inverter-based generation on the grid, largely coming from PV and energy storage distributed energy resources (DER), the grid support functions and inverter capabilities, such as volt-var, frequency-watt (FW) and ride-through (RT) capabilities, continue to become more critical with an ever-expanding list of capabilities to ensure grid stability under generation variability. Added to this list are grid-forming inverters (GFMI) that have the capability to provide their own voltage and frequency reference and island from the main grid. Similar to the desire to protect an area electrical power system (EPS), it is also desired to ensure that the devices connected to a microgrid remain healthy after a fault occurrence. However, unlike other distributed energy resources (DER), inverters use various control schemes that vary between manufacturers. Therefore, the dynamic responses of GFMI during fault conditions are not fully known and can vary significantly between devices. Applying faults to GFMIs from a variety of manufacturers is necessary to quantify the degree of difference and similarity to fault response. Using the Low Voltage RT (LVRT) requirement from IEEE 1547-2018, a fault will be defined as condition that causes the GFMI to output a voltage level below 88% of the nominal voltage (V_{nom}).

Although DERs are not required to have the functionality required by IEEE Std 1547-2018 [1] while operating on an islanded microgrid, some of these functionalities are beneficial when an inverter is tied to a low inertia system, primarily the FW function. This functionality allows for proper load sharing of grid-following inverters (GFLI) when tied to a droop control GFMI. However, with LVRT capabilities enabled, when a fault occurs that causes the output voltage of the GFMI to be reduced to less than 50% of $V_{nom,}$ any GFLI would go into a momentary cessation if the event lasts longer than 5 cycles. This event would also require other DER such as synchronous generators to cease to energize after 10 cycles. This could result in driving the voltage even lower as the overall injection of current would be only that of the devices without these capabilities enabled. Additionally, with GFLIs operating with their frequency RT capabilities enabled the inverters are susceptible to nuisance trips if the circuit load is not properly balanced with a droop control GFMI controlling the voltage frequency. Any frequency outside of 58.5 – 61.2 Hz must trip after 5 minutes of continuous operation, and any frequency outside of 56.5 – 62 Hz must trip within 10 cycles. This can lead to further issues within the microgrid.

Due to the low inertial characteristics of a microgrid, fault causing events, such as damage to power lines, are more detrimental to the system [6]. A fault condition in the microgrid could lead to the load demand exceeding the maximum production of the DERs capacity. When the GFMIs experiences these type of scenarios, the inverter reduces its voltage output due to the reduced grid impedance, [4].

With the high current demand of an inductive motor start up, it is desired that a GFMI be capable of providing current above its rated value for a short duration to supply the increased current draw from the inductive motor start and keep voltage reduction in the microgrid to a minimum. While conventional GFLI may only inject 1.1 to 1.2 p.u. current during a fault, GFMIs that utilize energy storage can be designed (either via controls, for short duration events <10 cycles or hardware for longer duration) to be capable of outputting current levels 2 to 3 times greater than their rated outputs during an overload condition. In order reduce low voltage events due to inductive motor starts, as well as to properly coordinate the protection system, understanding the fault current characteristics of GFMIs is very important [2]-[9].

This paper is organized in the following manner. Section II describes the basic configuration of a microgrid and how the GFMI was subjected to fault conditions. Section III contains

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the results for the faults imposed on the two inverters evaluated. The conclusion is in Section IV.

It is within the scope of this paper to perform experimental tests on GFMIs to gain insights into their dynamic behavior under fault scenarios. Such information can be later used to help farther understand the response if GFMIs to high impedance faults in order to improve protection coordination, future IEEE standards, etc.

II. Test Configuration

Microgrids can contain multiple DERs to support the system load. Energy storage systems (ESS) are utilized for backup power during times where production from other DERs cannot meet the load requirements. Additionally, DERs such as load following gas generators, wind turbines, and PV inverters are connected to the microgrid for load support as well as maintaining a safe state of charge in the ESS.

Fig 1 shows the diagram of the test setup. For the purposes of this study, no generator support will be used as synchronous generators have been well characterized during fault conditions. Furthermore, inverter response will be evaluated without PV support, since the GFMI is being evaluated and not the charge controller.

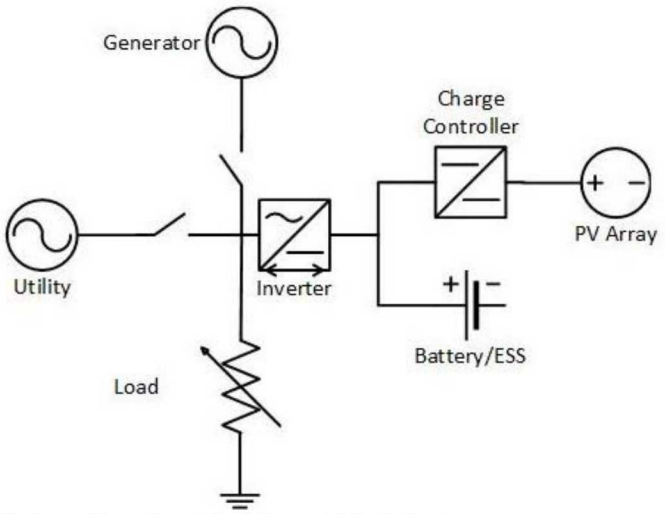

Fig 1. Test Circuit for Microgrid Fault Study

With the inverter either removed from the EPS or in an islanded state, a variable load is utilized to source current from the inverter. By increasing the absorbed power of the load to a value greater than that the rated power of the inverter, the voltage will drop below nominal, similar to that of a line-to-line or line-to-neutral fault [10]. Note that the GFMIs tested can operate in grid-following or grid-forming modes but cannot be grid-forming *and* grid synchronized.

For the results documented below, the voltage and current of the GFMI were measured at the terminals of the equipment under test with Tektronix P5200A High Voltage Differential Probes and Pearson Electronics 101 Wideband Current Monitors. The data was captured on an oscilloscope or National Instruments data acquisition system.

This paper evaluates different commercial grid-forming inverters at Sandia's Distributed Energy Technologies Laboratory (DETL) for their experiment fault current characteristics. The results provided below are for a single phase, 240V grid-forming inverter in the 5 kVA rated power output range.

III. Experimental Results

While operating in grid-forming mode and without a load present, the inverter will output a voltage signal to the circuit, but does not export any power, also known as being in standby mode. Fig 2 demonstrates a load, which is slightly lower than 1.00 p.u. of the inverters (GFMI #1) rated power, introduced to the circuit.

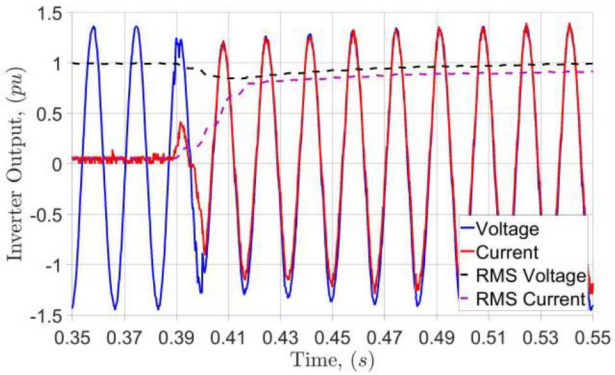

Fig 2. Load Introduced to Grid-forming Inverter to Operate Near Rated Power (GFMI #1)

During the initial energizing of the load, the voltage is reduced for a few cycles to approximately 0.85 p.u. but returns to within 99% of nominal voltage within 10 cycles. Furthermore, the current is injected slowly and does not produce any transient spikes, similar to that of a PV GFLI. This ensures that there are not any undesired current transients rapidly injected into critical loads.

Table I displays the output of GFMI #1 at various loaded conditions This includes, from left to right, the output of the inverter with a load equivalent to the inverter rated power (shown in Fig 2), a load near the inverter maximum advertised overload support (2.0 p.u.), and various load profiles that cause a fault condition at increasing load values. The final column shows the output of the inverter after a fault introduced while the inverter was operating near rated power.

From the data shown in Table 1, when the applied load is increased above approximately 4.5 p.u., the output current of the GFMI is less than 88% of nominal voltage. By subjecting the inverter to an additional load, greater than 4.5 p.u. to cause a high impedance fault (fault impedance greater than 10 times

TABLE I
FAULT CURRENT RESULTS OF GRID FORMING INVERTERS AT VARIOUS LOADS

Grid Forming Inverter #1							
	Near Rated Power	Overload Support	Fault #1	Fault #2	Fault #3	Fault #4	Fault during Operation
Initial Load (p.u.)	0.00	0.00	0.00	0.00	0.00	0.00	0.91
Final Load (p.u.)	0.91	1.82	4.55	6.36	9.09	13.64	10.00
Output Voltage (p.u.)	0.99	0.96	0.89	0.59	0.24	0.17	0.23
Output Current (p.u.)	0.92	1.76	2.03	2.11	2.26	2.26	2.25
Output Power (p.u.)	0.91	1.69	1.81	1.24	0.54	0.38	0.52

that of a bolted fault or approximately 1 ohm or greater), it can be observed that the voltage of the inverter drops well below nominal, and causes the inverter to output a current greater than 2 p.u. This can be seen in Fig 3.

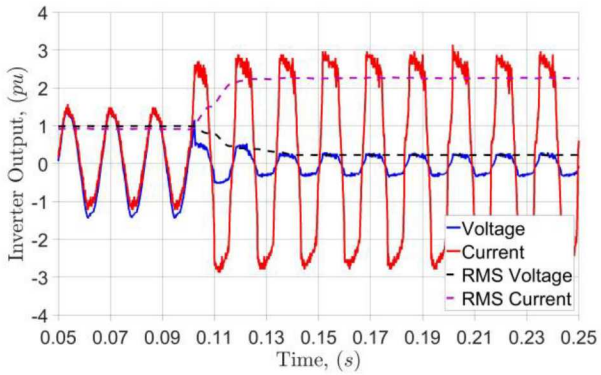

Fig 3. Adding Load During Inverter Operation to Cause Fault Condition (GFMI #1)

Although the increase in current is rapid, there are no transient spikes present. Therefore, the inverter enters a fault condition smoothly, as compared to the transient response of a non-GFMI [10]. This reduces the chance of subjecting any critical loads to undesired transients.

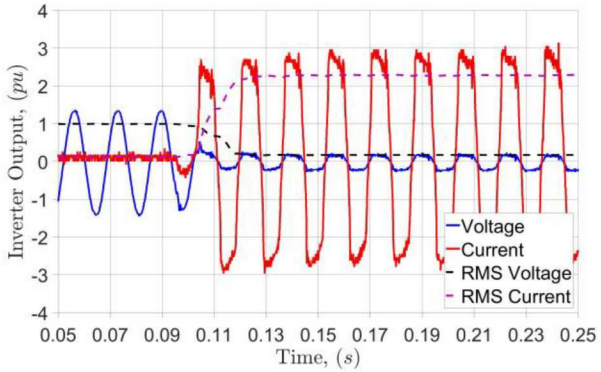

Fig 4. Fault Condition on GFMI #1 Operating in Standby Mode

Moreover, if a large load, greater than 4.5 p.u., is introduced while the GFMI is in a standby mode, the inverter will output current above 2 p.u., as seen in Fig 4. Similar to that seen in Fig 3 there were no transient spikes.

As can be seen in Fig 5 when the load applied to GFMI #1 is greater than approximately 4.5 p.u. the voltage output of the inverter decreases until the load reaches 9.0 p.u. Moreover, with loads greater than 2.0 p.u. the output current slowly increases with the load until it reaches the DERs maximum output current; in this case is 2.26 p.u.

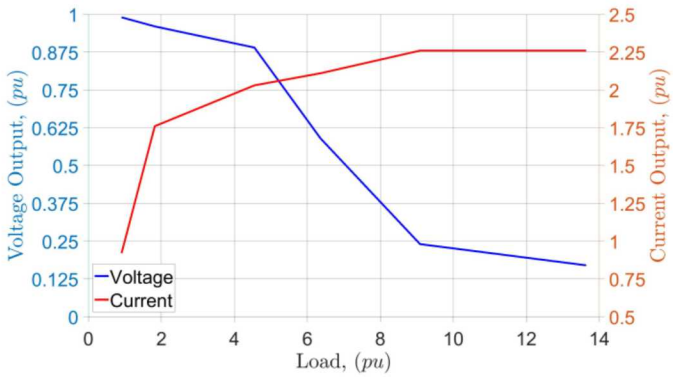

Fig 5. GFMI #1 Response to Increasing Load

The inverter evaluated above has surge overload capability (SOC) allowing voltage regulation to be maintained to a value close to the nominal value during large load starts, this is not the case for all GFMIs. The second inverter tested in this study (GFMI #2) is another single-phase device of similar size to the above GFMI. This GFMI does not seem to have overload support. Without this overload support, it can be seen how quickly the output voltage of the GFMI can be collapsed while under load (Fig 9). Table II shows GFMI #2 output at various load increasing from rated power to 5 p.u. of the inverter rated power. As seen in the column under Fault #1 the output power is slightly greater than 1 p.u., but is far from reaching the load demand of 1.4 p.u.

To establish a baseline of the inverters response to a block load being applied, the inverter was subjected to a 1.00 p.u. load from its standby state, similar to that shown in Fig 2. The results shown in Fig 6 show that the inverter is capable of accepting a load at its rated power without any deviation in the

TABLE II
FAULT CURRENT RESULTS OF GRID FORMING INVERTERS AT VARIOUS LOADS

Grid Forming Inverter #2 (Resistive Faults)						
	Rated Power	Fault #1	Fault #2	Fault #3	Fault #4	Fault #5
Initial Load (p.u.)	0.00	0.00	0.00	0.00	0.00	0.00
Final Load (p.u.)	1.00	1.40	2.00	3.00	4.00	5.00
Output Voltage (p.u.)	1.02	0.97	0.65	0.45	0.34	0.28
Output Current (p.u.)	1.07	1.18	1.32	1.37	1.39	1.40
Output Power (p.u.)	1.09	1.14	0.86	0.62	0.47	0.39

output voltage, unlike that of GFMI #1.

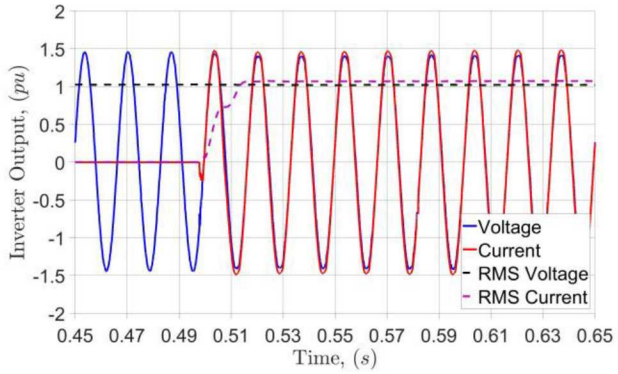

Fig 6. Load Introduced to Grid-Forming Inverter to Operate at Rated Power (GFMI #2)

To demonstrate the effects of not having overload support functionality, a load of 2.00 p.u. was applied (see Fig 7). At this load, the voltage collapses to approximately 0.65 V_{nom}. Although the inverter does not have overload support, the output current is capable of values greater than 1.00 p.u., similar to most PV inverters [10]. Fig 7 shows the results at 2.00 p.u. load.

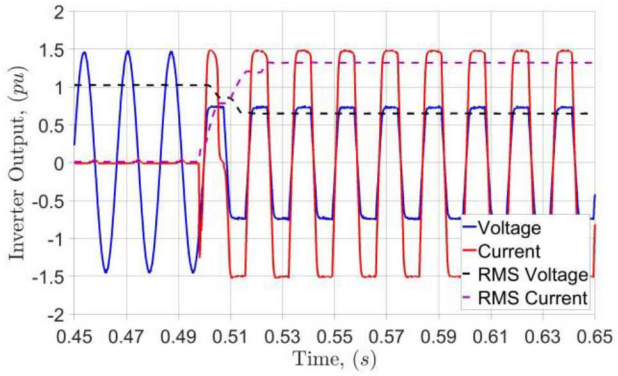

Fig 7. Fault Condition on GFMI #2 Operating in Standby Mode

By applying additional load, the voltage continues to drop and the output current approaches a saturation limit of approximately 1.40 p.u. At a load of 5.00 p.u., the output voltage is reduced to nearly 0.25 V_{nom}; this voltage level does not occur in the first inverter tested until a load of approximately 9.00 p.u. was applied. These results are illustrated in Fig 8 (a). Note that there is an initial transient similar to those commonly seen from PV inverters during high impedance faults [10]. This is shown in Fig 8 (b).

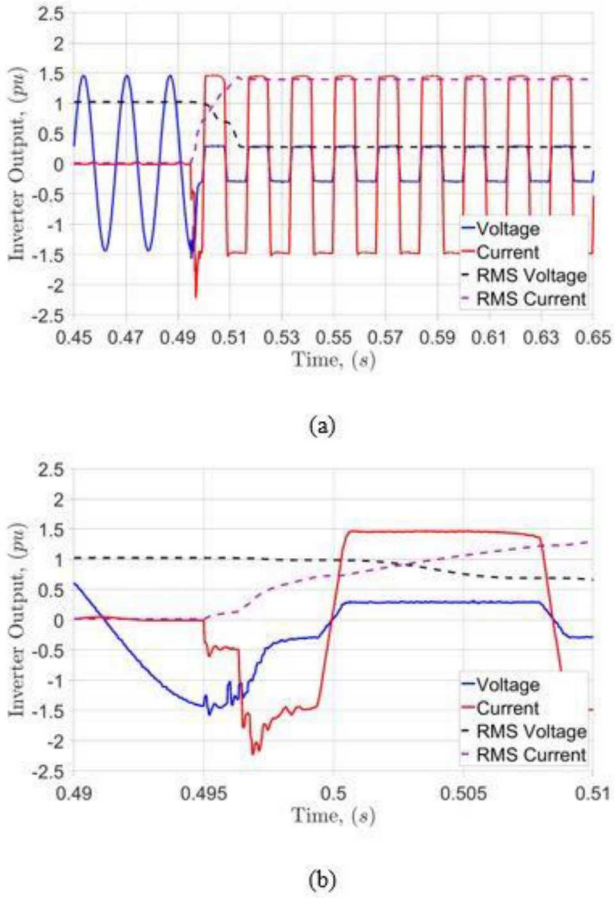

Fig 8. GFMI #2 Near Current Saturation, (a) Operating at steady state during the fault condition, (b) zoom into initial transient at start of fault

TABLE III
FAULT CURRENT RESULTS OF GRID FORMING INVERTERS AT VARIOUS LOADS

Grid Forming Inverter #2 (Inductive Faults)						
	Near Rated Power	Fault #1	Fault #2	Fault #3	Fault #4	Fault #5
Resistive Load (p.u.)	1.00	1.00	1.00	1.00	1.00	1.00
Inductive Load (p.u.)	0.60	1.20	1.80	2.40	3.00	3.90
Output Voltage (p.u.)	0.93	0.86	0.68	0.57	0.50	0.43
Output Current (p.u.)	1.07	1.29	1.36	1.37	1.38	1.49
Output Watts (p.u.)	0.76	0.70	0.43	0.31	0.25	0.18
Output Vars (p.u.)	0.46	0.72	0.72	0.64	0.58	0.51

Fig 9 demonstrated the output voltage and current of GFMI #2 while subjected to the high impedance faults. There is a rapid increase in output current to attempt to compensate for the overload event, however the saturation limit is quickly approached and the voltage collapses.

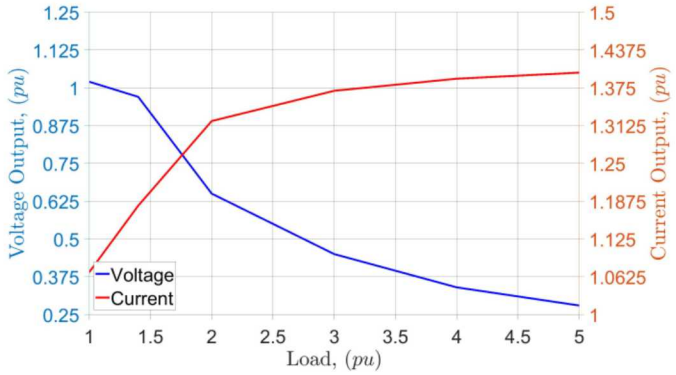

Fig 9. GFMI #2 Response to Increasing Load

In addition to the resistive overloads, GFMI #2 was subjected to inductive overloads. The test circuit had a resistive load applied to allow the GFMI to operate at rated power. While a motor is primarily a resistive load, an event where the motor is damaged or unable to start could cause an inductive overload. Furthermore, with the low-inertia of a microgrid, a large motor start could extend several cycles as seen in reference [11].

By adding a small inductive load (approximately 0.60 p.u.) to the test circuit, an initial look into of how the GFMI reacts to an inductive fault can be seen. Fig 10 shows that the GFMI output voltage drops by 7% from nominal voltage. However, the initial injection of current from the inverter is substantially greater than the steady state value. Furthermore, the current output has a slight DC offset of about 0.12 p.u. when the GFMI reaches steady state. This could result in the damage of some loads.

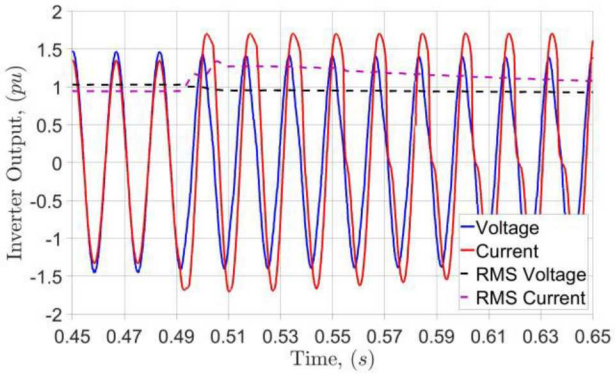

Fig 10. GFMI #2 Subjected to Small Inductive Load While Operating at Rated Power

By increasing the inductive load, it can be seen in Fig 11 that the voltage output collapses while the current approaches its saturation limit. Moreover, the output waveform is further distorted.

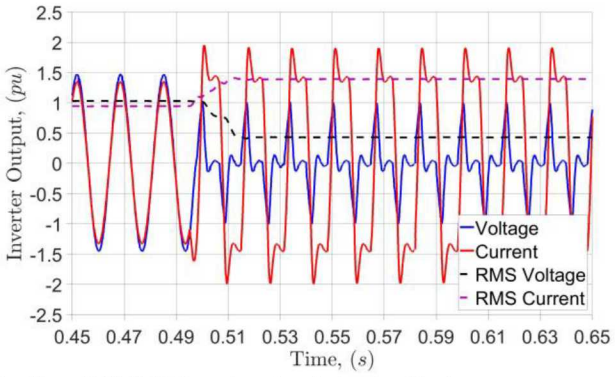

Fig 11. GFMI #2 Introduced to Inductive Fault

Fig 12 shows the resulting output voltage and current of various inductive loads added to the test circuit. The output follows a similar trend to that of the resistive overload tests.

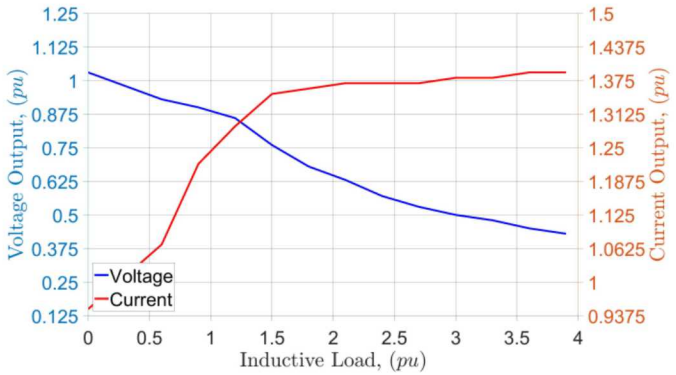

Fig 12. GFMI #2 Response to Inductive Loads

IV. Conclusions

By applying various high impedance faults onto the test circuit, it can be observed how different GFMI respond to overload events. While there is a desire for SOC functionality within GFMI, it can be seen that not all inverters are equipped with a control scheme to allow for this functionality. However, some inverters such as GFMI #1 possess the capability for load support over the rated power value for a short time, usually less than a couple seconds. This provides allowance for larger load starts that would normally sag the output voltage too much on the low-inertia grid that is being fed by the DER.

If the voltage were to sag too low when a load is trying to start, this could result in the load continuously trying to start, maintaining a low voltage level until the GFMI or an external protection device trips. Furthermore, maintaining a low voltage level for too long could cause damage to other devices tied to the microgrid.

Acknowledgement

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References

[1] IEEE. 1547-2018–IEEE Standard for Interconnecting and Interoperability Distributed Resources with Electric Power Systems Interfaces. Published April 6, 2018. Institute of Electrical and Electronics Engineers, Inc., New York, NY.

[2] S. S. Venkata, M. J. Reno, W. Bower, S. Manson, J. Reilly and G. W. Sey Jr, "Microgrid Protection: Advancing the State of the Art," Sandia National Laboratories, SAND2019-3167, Albuquerque, 2019.

[3] J. Seuss, M. J. Reno, R. J. Broderick, and S. Grijalva, "Maximum PV Size Limited by the Impact to Distribution Protection," IEEE Photovoltaic Specialists Conference, 2015.

[4] M. E. Elkhatib, J. Hernandez-Alvidrez, and A. Ellis, "Fault Analysis and Detection in Microgrids with High PV Penetration", Sandia Technical Report, SAND20175472, 2017.

[5] B. Kroposki, B. Johnson, Y. Zhang, V. Gevorgian, P. Denholm, B. Hodge, B. Hannegan, "Achieving a 100% Renewable Grid: Operating Electric Power Systems with Extremely High Levels of Variable Renewable Energy," IEEE Power and Energy Magazine, 2017.

[6] J. Hare, X. Shi, S. Gupta, A. Bazzi, "Fault diagnostics in smart micro-grids: A survey," Renewable and Sustainable Energy Reviews, 2016.

[7] S. Gonzalez, N. Gurule, M. J. Reno, and J. Johnson, "Fault Current Experimental Results of Photovoltaic Inverters Operating with Grid-Support Functionality". IEEE Photovoltaic Specialists Conference, Waikoloa, HI. June 10-15, 2018.

[8] Chunsheng Wu, Hua Liao, Zilong Yang, Yibo Wang, Honghua Xu, "Voltage and frequency control of inverters connected in parallel forming a micro-grid". In 2010 International Conference on Power System Technology, Hangzhou, China December 13, 2010.

[9] J. Hernandez-Alvidrez, A. Summers, N. Pragallapati, M. J. Reno, S. Ranade , J. Johnson, S. Brahma and J. Quiroz, "PV-Inverter Dynamic Model Validation and Comparison Under Fault Scenarios Using a Power Hardware-in-the-Loop Testbed," in *IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC)*, Waikolola Village, HI, USA, 2018.

[10] S. Gonzalez, J. Johnson, M. Reno and T. Zgonena, "Small Commercial Inverter Laboratory Evaluations of UL 1741 SA Grid-Support Function Response Times," in *43rd IEEE PVSC*, New Orleans, 2016.

[11] R. H. Lasseter, J. H. Eto, B. Schenkman, J. Stevens, H. Volkmmer, D. Klapp, E. Linton, H. Hurtado, J. Roy, "CERTS Microgrid Laboratory Test Bed," IEEE Transactions on Power Delivery, 2011.

[12] J. Hernandez-Alvidrez, A. Summers, M. J. Reno, J. Flicker, N. Pragallapati, "Simulation of Grid-Forming Inverters Dynamic Models using a Power Hardware-in-the-Loop Testbed," IEEE Photovoltaic Specialists Conference (PVSC), 2019.