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Unintentional Islanding Evaluation Utilizing Discrete RLC Circuit Versus Power Hardware-in-the Loop Method

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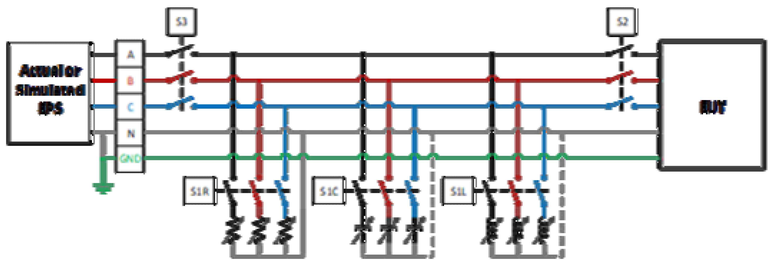
Summary

Unintentional Islanding (UI) test are performed using RLC UI test balanced circuit, with the resistive element adjusted to consume the power generated by the equipment under test and the inductive and capacitive tuned to resonate at 60 Hz and for a Q factor of 1, meaning the Var of each element are set to equal the active power generation. This and be expensive to difficult set up so efforts are underway to meet the UI requirements using power-hardware-In-the Loop methods.

Background

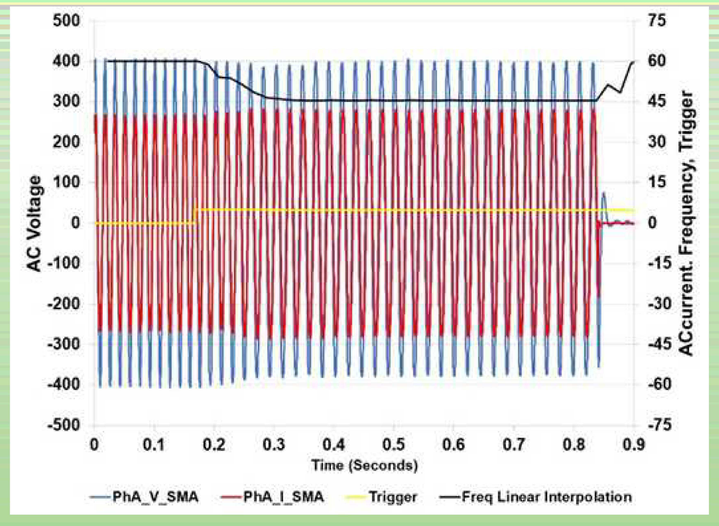
IEEE P1547.1 inverter interconnection test procedure implements the new interconnection requirements and associated capabilities. A test matrix has been created and concerns that autonomous unintentional islanding (UI) algorithms are not sufficient to prevent an unintentional island. An RLC circuit, like the circuit below is utilized to show compliance.



RLC unintentional islanding circuit

Unintentional Islanding Testing using RLC Loads

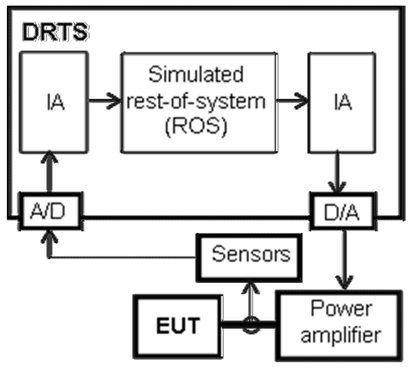
The oscillatory data that is captured during the UI tests provides the high-fidelity information on the response of the inverter to the loss of utility event while configured with the worst-case scenario



UI islanding results using balanced RLC loads

PHIL Unintentional Islanding

An alternative to the resonant RLC UI test balanced circuit is using the same concept of the RLC circuit and the test matrix shown in Table 1, however the test is accomplished using a power hardware-in-the loop (PHIL).



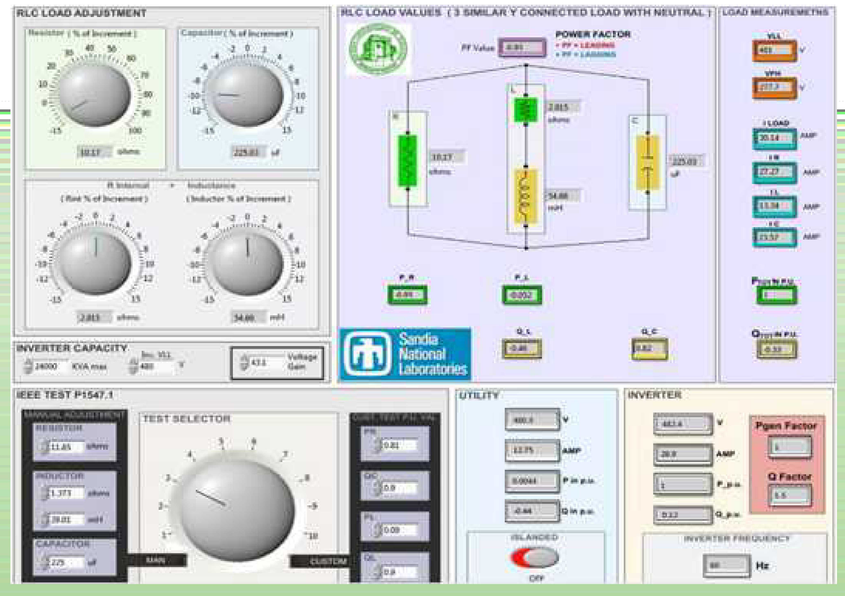
Power hardware-in-the-loop configuration

Integral equation expression provides the basis for the dynamic inductive and capacitive component model.

$$I_L(t) = \frac{1}{L}\int (\, v_L(t) + R_{int} * i_L(t)\,)dt$$

$$V_C(t) = \frac{1}{C}\int (I_t(t) - I_r(t)\,)\,dt$$

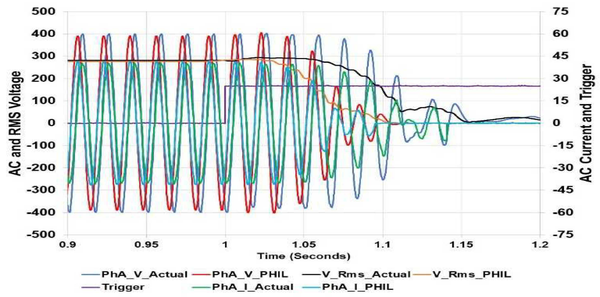
Graphical user interface provides voltage, current, power and other vital parameter measurements. It also provides knobs to step through test matrix and to adjust the resistive, inductive, and capacitive loads.



Graphical user interface with parameter display and knobs on loads

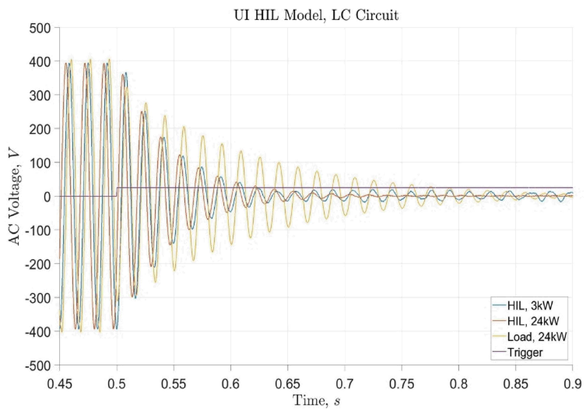
PHIL Validation

Through laboratory UI evaluations a comparative assessment of the RLC UI balanced circuit test and the PHIL UI test was conducted.



RLC and PHIL with similar Run-on-Times

The inductance and capacitance of the RLC balanced circuit are set to resonate at 60Hz and if just the LC exist, when the utility is removed a ring-down of the stored energy can be observed and quantified for both the RLC balanced circuit and the PHIL methods.



Conclusion

A key attribute of PHIL is the elimination of costly, bulky, and heat generating RLC loads and the validation of PHIL indicates a good representation of the RLC balanced circuit method suggesting a viable method to assess UI conformance.

REFERENCES

[1] "IEEE Standard 1547-2018: Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power System Interfaces," IEEE, 2018.

[2] "IEEE Draft Standard P1547.1, Standard Conformance Test Procedures for Equipment Interconnecting Distributed Energy Resources with Electric Power Systems and Associated Interfaces."

[3] K. Schoder, J. Langston, J. Hauer, F. Bogdan, M. Steurer, and B. Mather, "Power Hardware-in-the-Loop-Based Anti-Islanding Evaluation and Demonstration," NREL, NREL/TP-5D00-64241, Oct. 2015.

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