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Unintentional Islanding Evaluation Utilizing Discrete RLC Circuit Versus Power Hardware-in-the Loop Method

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***Abstract*—The high penetration of photovoltaic (PV) distributed energy resources (DER) facilitates the need for today's systems to provide grid support functions and ride-through voltage and frequency events to minimize the adverse impacts on the distribution power system. These new capabilities and its requirements have created concerns that autonomous unintentional islanding (UI) algorithms are not sufficient to prevent a condition were the loss of utility is detected. Type tests in IEEE 1547-2018 have evolved to thoroughly evaluate DER capabilities and a new method includes power hardware-in-the-loop (PHIL) testing. Sandia National Laboratories is performing a detailed laboratory comparison of the tuned Resistive, Inductive, Capacitive (RLC) circuit method using discrete elements and the PHIL that applies the PV inverter equipment under test (EUT), real-time simulator, and a power amplifier. The PHIL method allows UI assessments without the need for potentially expensive, large, heat generating discrete loads.**

***Key words*—unintentional islanding, RLC circuit, PHIL**

I. Introduction

Today's DER are required to meet IEEE 1547-2018 *Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power System Interfaces* [1], which has implemented voltage and frequency ride-through requirements as well as voltage and frequency regulating capabilities. The voltage and frequency ride-throughs have increased the operating regions of DER substantially and under extreme voltage variations, i.e., voltage less than 50% of nominal, require a DER to momentarily cease to export power. If voltage recovery occurs within the prescribed duration, the DER will re-energize the electric power system (EPS). Voltage and frequency regulating capabilities can be implemented autonomously through monitoring utility conditions and the regulating function's algorithms operate accordingly or the capabilities can be commanded or scheduled to help address voltage and frequency anomalies and help mitigate adverse effects of a variable DER.

These additional features have caused the number of tests needed for a thorough evaluation of the equipment under test (EUT) to increase, causing the complexity of configuring the RLC resonant circuit to become more challenging. The UI test comprises connecting resistive, inductive, and capacitive loads placed in parallel with the output of the EUT as shown in Figure 1. The method of connecting the loads has proved to be rather important because when the EUT and loads are isolated during the UI tests and the loads are not referenced, the loads can become unbalanced and the EUT can detect this unbalanced condition. Using a passive unintentional islanding approach looking for the unbalanced condition can lead to false positives and may not necessarily reliably identify when an island has occurred. An updated RLC circuit is provided below that will help meet the circuit criteria.

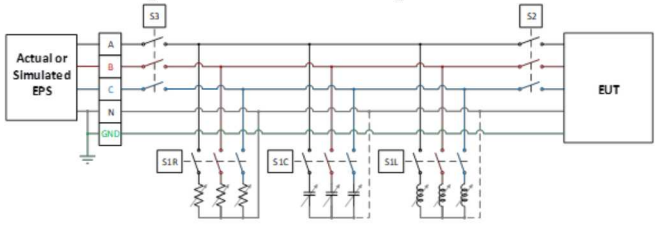


Fig. 1 RLC unintentional islanding circuit

IEEE P1547.1 [2] includes different methods to meet unintentional islanding requirements. These methods are mentioned here but are out of scope for this paper. The following two unintentional islanding testing methods can be evaluated, clearing the way for implementation of these types of methods. Regardless, if they are allowed in accordance with the area EPS, these methods will require the EUT cease to energize the area EPS within 2 seconds as does the RLC method:

- Powerline conducted permissive signal test
- Permissive hardware-input test

The test procedure to validate the permissive signal methods is much more straightforward because the AC source is not removed and there is no need for balancing a resonant circuit.

TABLE I
RLC UNINTENTIONAL ISLANDING TEST MATRIX FOR CATEGORY B

Test case	EUT power level (p.u.)		Reactive power mode			Active power mode settings		Initial RLC load (p.u.)			*Quality factor*
	P_{EUT}	Q_{EUT}	Mode & setting		Response time (s)	VW	FW	$P_R+P_L+P_C$	Q_C	Q_L	*QF*
1B	1.00	0.00	Constant Power factor	PF = 1.00	n/a	Default	Default	-1.00	1.00	-1.00	1.00
2B	0.50	0.00						–0.50	0.50	–0.50	1.00
3B	0.90	–0.44	Constant Power factor	PF = –0.90	n/a	Off	LA	–0.90	0.90	–0.46	1.00
4B	0.90	0.44		PF = 0.90				–0.90	0.46	–0.90	1.00
5B	1.00	0.00	Voltage-reactive power	MA	1.00	MA	MA	-1.00	1.00	-1.00	1.00
6B	0.50	0.00		Default	10.00			–0.50	0.50	–0.50	1.00
7B	0.50	0.00	Active Power-Reactive power	Default	n/a			–0.50	0.50	–0.50	1.00
8B	1.00	0.00		MA				-1.00	1.00	-1.00	1.00
9B	0.50	–0.44	Constant reactive power	Q = –0.44	n/a			–0.50	0.50	-0.06	1.00
10B	0.50	0.44		Q = 0.44				–0.50	0.06	-0.50	1.00

NOTE—LA = least aggressive; MA = most agressive.

The EUT responds to the loss of the permissive signal and like the RLC circuit where the AC source is removed, it must respond within 2 seconds once the permissive signal is removed

II. RLC UI TEST PROCEDURE

The RLC unintentional islanding test is intended to be a worst-case scenario that balances the load to the generation of the EUT. By adjusting the loads shown in the test circuit shown in Figure 1 until the active and reactive current is less than 2% of the EUT rated power. For this test, discrete passive components are connected in parallel with the output power generated by the EUT, as shown in Figure 1. The UI tests are conducted for each of the test cases in Table 1. The table provides the power level on a per unit basis with a tolerance of ± 0.05 p.u. It is important to note the power is listed in the generator frame of reference. The voltage and frequency regulating functions are set to ±0.44 p.u. The most aggressive setting results in a curve without a dead band and maximum reactive power is delivered at ± 0.02 p.u. of nominal voltage. The table provides different operating conditions for each of the 10 tests cases and for all test cases its important to establish a balanced load condition for each test case. The following two equations provide the tolerance of active and reactive power balance that should be met for each case:

$$P_{S3} = P_{EUT} + P_R + P_C + P_L <= 0.02 \text{ p.u.} \quad (1)$$

$$Q_{S3} = Q_{EUT} + Q_R + Q_C + Q_L <= 0.02 \text{ p.u.} \quad (2)$$

Adjustments to the AC source voltage and/or frequency and EUT power are permitted to meet the load balance requirements of Equations 1 and 2, as long as the EUT power meets the power levels specified in Table 1 and are within ± 0.05 p.u.

A. Unintentional Islanding Results using RLC Loads

Unintentional islanding tests are conducted using passive elements in a balanced configuration that results in minimal changes in voltage and frequency once S3 in Figure 1 is opened. Once the conditions of Equation 1 and 2 are met, the power flow through S3 will be within 2% of the EUT rated power.

Verifying the load setup has been configured correctly is an important step in the balance RLC test procedure and is vital to the power hardware-in-the-loop procedure. Figure 2 shows the result of test case 1 of Table 1, and for this test the UI algorithm has been disabled so for this balanced condition the result should be a long to continuous unintentional island. Under this condition the EUT should continue to operate while isolated from the utility.

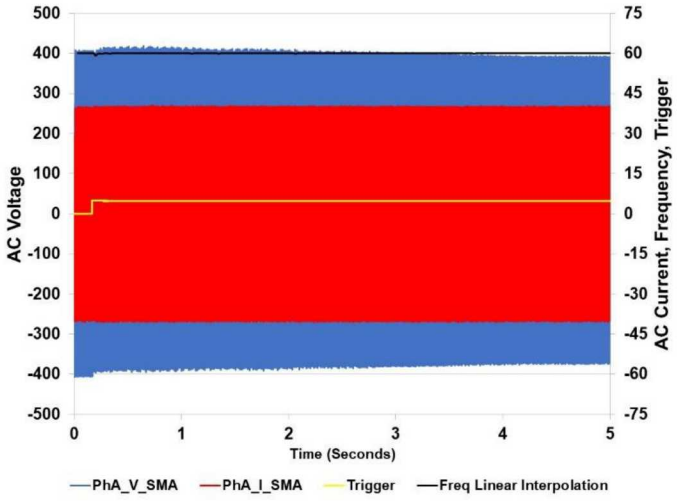


Fig. 2 Balanced 1B RLC UI test with UI off

While the EUT is islanded, adjustments to the RLC loads are implemented to bring the voltage and frequency closer to nominal values, therefore making this test condition the most difficult to pass. During the islanding, the frequency remains near 60Hz, which is another indicator the UI algorithm is off. This is true only for an algorithm that is based on a frequency-shift type function.

After fine adjustments are made to the loads, the UI algorithm is re-instated, and the test is conducted having been fine-tuned for a balanced condition. Figure 3 shows the result of the UI test of a balanced load and the inverter operating at unity power factor, rated power, and with voltage and frequency regulating functions on. The plot shows the run-on time (ROT) well within the 2-second requirements and shows how the UI algorithm shifts the frequency during the island to about 45Hz.

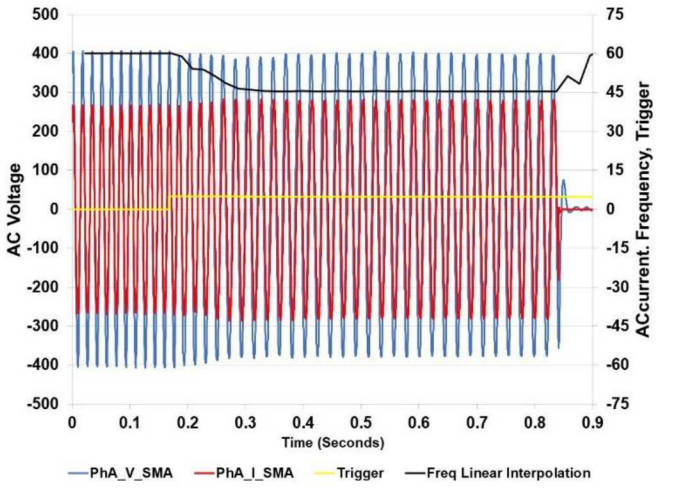


Fig. 3 UI islanding results using balanced RLC loads

The oscillatory data that is captured during the UI tests provides the high-fidelity information on the response of the inverter to the loss of utility event while configured with the worst-case scenario.

*B. Unintentional Islanding Tests using Power Hardware-in-the-Loop Method*An alternative to conducting the resonant RLC UI test balanced circuit is using the same concept of the RLC circuit and the test matrix shown in Table 1, however the test is accomplished using a power hardware-in-the loop (PHIL) concept [2]. This process requires specialized equipment and extensive programming to make it work, which is a simulation-based approach with the following test and setup requirements:

- The simulation includes the RLC load bank, balance of system (BOS) components, and an interface algorithm that uses an electromagnetic transient-type simulation and uses actual hardware's instantaneous voltage(s) and current(s).
- Simulated circuit behavior must be verified. This requires disabling the EUT's UI algorithm, and the EUT must be operated at unity PF and with the regulation functions deactivated.
- The PHIL simulation setup amplifier must be capable of 800Hz. The voltage harmonic magnitude must be at least 1% of the nominal voltage while operating as a standalone voltage source.
- Alternatively, an impedance measurement approach may be used to evaluate the BOS simulation capabilities at two different voltage levels.
- The PHIL simulation must be capable of recording waveform capture

Figure 4 is a one-line diagram of the components of the PHIL setup. The power amplifier is a regenerative device that can sink power from the EUT. The system monitors the EUT's current and feeds this vital parameter into the digital real time simulator. The hardware components of the RLC UI are the AC source, S3, RLC loads, and any interfacing components in the circuit shown in Figure 1 become the simulated rest-of-system (ROS) in Figure

4. A computationally derived analog signal is delivered to the power amplifier to control the voltage and current of the system.

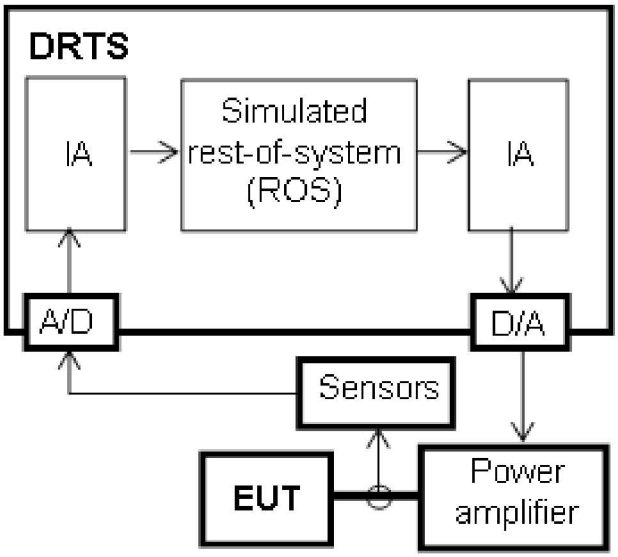


Fig. 4 Power hardware-in-the-loop configuration

C. Implementation flexibility using Power Hardware-in-the-Loop Method

The programming of the RLC circuit has a significant role in the way the tests are conducted. Creating a flexible and adjustable interface with the simulated loads that provide the necessary information to conduct the tests is essential. The implementation of the test matrix shown in Table 1 provides an automated configuration of the simulated loads. Figure 5 shows the graphical user interface (GUI) displaying monitored voltage and currents at vital circuit nodes, adjustment knobs to resistive, inductive and capacitive loads, and a test selector knob that transitions from any of the 10 tests in Table 1. The EUT capacity and operating voltage determines the load impedance for each of the tests in the UI test matrix and the PHIL GUI provides the Pgen/Pload ratio and Q factor.

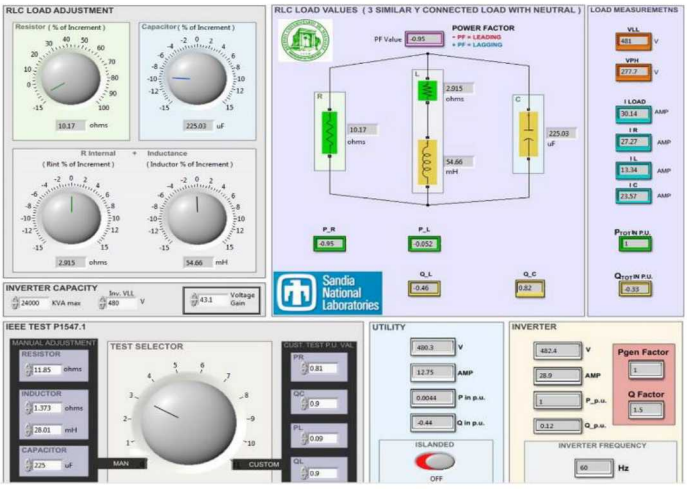


Fig.5 Unintentional Islanding PHIL GUI, showing parameter monitoring, load adjustors, and test selector

III. SIMULATED RLC CIRCUIT PARAMETERS

Developing on-the-fly adjustable RLC loads is required for stepping through the UI testing. A unique method of adjusting the simulated loads uses an equivalent circuit based on the element functionality expression through a mathematical equation. Integral equation expression (3) provides the basis for the dynamic inductive component model.

$$I_L(t) = \frac{1}{L}\int(v_L(t) + R_{int} * i_L(t))dt \qquad (3)$$

In the same manner, equation expression (4) shows a dynamic capacitive expression providing the basis for a dynamic capacitive component model.

$$V_C(t) = \frac{1}{C}\int(I_t(t) - I_r(t))\,dt \qquad (4)$$

When the test selector is turned to a test number it corresponds to that test number in Table 1, which determines EUT power settings, mode of operation, and load settings.

The following plots show the response of the PHIL UI tests and each of the plots correlate to a simulated test configuration in Figure 1 and the test correlates to the tests in the test matrix shown in Table 1. Figure 6 shows the PHIL UI

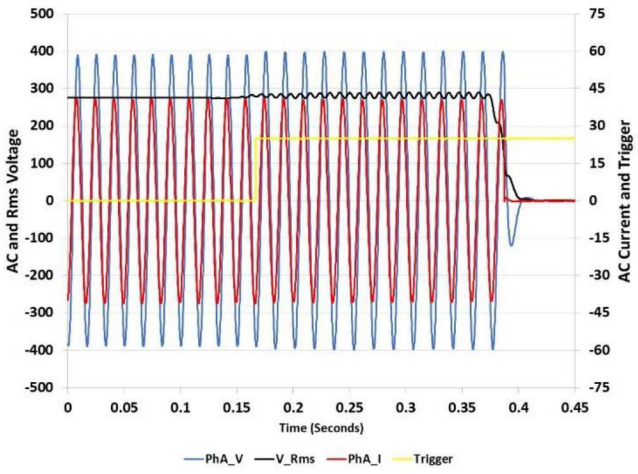


Fig. 6 PHIL test result for Category B test 3. Balanced load UI, with PF= -0.9, $P_{inverter} = P_{load}$, VV=off, FW=LA.

tests result for the EUT operating at 0.9 power factor and at rated power. For this test the EUT cannot deliver rated active power because it is delivering 44% reactive power, however the EUT is operating at rated VA. Balancing the reactive power should take into consideration the output filter of the EUT.

For each of the testing in the test matrix, the test is initially conducted with the UI algorithm off on the EUT. This is done to verify the test setup is correct and when S3 in Figure 1 is opened, the EUT will sustain an island. The test requirements set the operating ranges achievable by the EUT. For test 3B, -44% reactive power means the active power generation is reduced by about 10%, so to maintain a Q factor of 1, the active and reactive power is set to 0.9 p.u.

The next test in the test matrix for category B is 4B and while similar to 3B, the EUT's output filter will slightly influence the amount of reactive power need to achieve the target values. For test 4B, approximately 44% reactive power reduces the active power generation by 10% and the results are shown in figure 7.

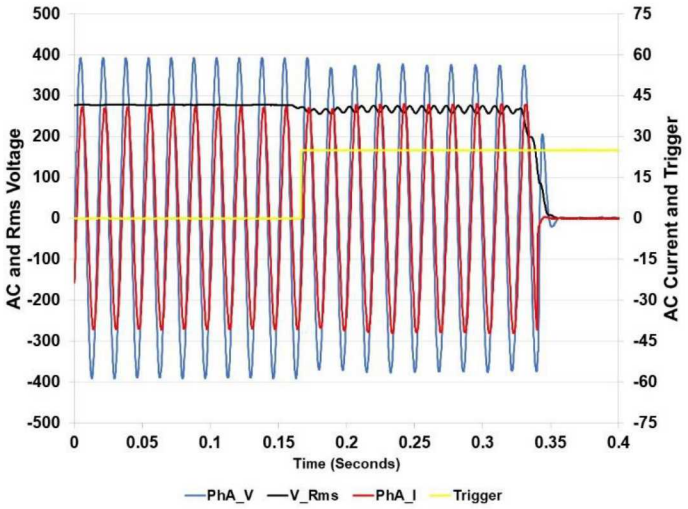


Fig.7 PHIL test result for test 4. Balanced load UI, with PF= 0.9, $P_{inverter} = P_{load}$, VV=off, FW=LA.

The next UI test using PHIL is test 5, which has both the voltage and frequency regulating functions on at their most aggressive setting. The UI test procedure provides a detail description of setting for each voltage and frequency regulating function. The EUT voltage-reactive (VV) settings are set to the most aggressive responses to voltage variation prior to conducting the tests and Table 2 provides the settings for the UI tests. This functions' reference voltage is designed to be autonomously adjustable, but this capability requires 300 seconds to determine the new reference voltage, so this capability can be either disabled or ignored because the UI test durations are much less.

TABLE II
VOLTAGE-REACTIVE POWER (VV) SETTINGS

Setting	Category A		Category B	
	Most aggressive	Default	Most aggressive	Default
	Voltage (p.u.)			
V_1	0.98	0.9	0.98	0.92
V_2	1	1	1	0.98
V_3	1	1	1	1.02
V_4	1.02	1.1	1.02	1.08
	Reactive power (p.u.)			
Q_1	0.25	0.25	0.44	0.44
Q_2	0	0	0	0
Q_3	0	0	0	0
Q_4	–0.25	–0.25	–0.44	–0.44
	Response time (s)			
Open Loop Response Time	1	10	1	5

The draft UI test procedure provides parameter setting information for to other autonomous voltage and frequency regulation functions like voltage-active power, frequency-active power, and active power-reactive power but are not shown here.

The PHIL test result for test 5B is shown below. For this test, the EUT adheres to the test requirements in Table 1 so inverters VV are set to most aggressive as are the voltage-watt and the frequency-watt. The simulated RLC loads are adjusted for the EUT operating at unity power factor and at rated power. Therefore, the reactive power for the simulated capacitive load is at 1.0 p.u. and the simulated inductive load is also at 1.0 p.u., so the load adheres to a Q factor of 1.0. The simulated resistive load accounts for the resistance in the inductive load and is set to sum to 1.0. The results for test 5B using PHIL is shown in Figure 8.

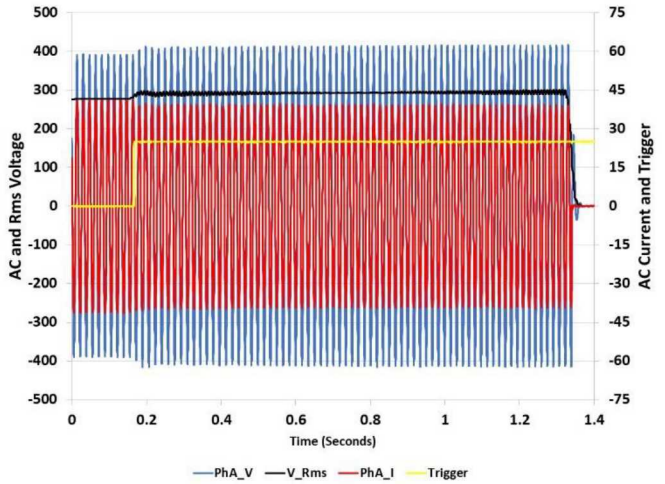


Fig. 8 PHIL test result for test 5. Balanced load UI, all voltage and frequency regulation set to most aggressive

IV. SIMULATED RLC CIRCUIT VALIDATION

Islanding tests were performed to compare the run on times (ROT) of the islanding tests on an EUT using both RLC loads and PHIL UI test methods. The only difference is one test is conducted with the configuration in Figure 1 and the other test uses the PHIL approach as shown in Figure 4. These tests were conducted with the EUT's unintentional islanding algorithm turned off.

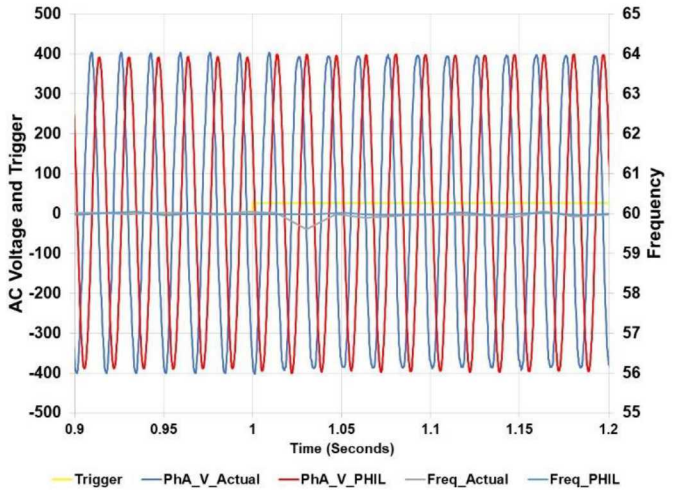


Figure 9. UI tests of RLC and PHIL with UI algorithm turned "off"

With the UI algorithm off, the EUT should sustain an island providing the test is configured to any of the 10 test sequences in the UI test matrix. Because each of the tests is a worst-case condition, where the voltage and frequency does not instantaneously change when the utility is removed because the unique load balance condition. The waveform in Figure 9 shows the close agreement on the islanding voltage and frequency values with both methods.

The response of the PHIL and the RLC load UI tests methods is repeated with the EUT's UI algorithm turned on. The EUT being used is a UL listed product, so the ROT should be within 2 seconds for the device to be in compliance. Fine tuning of the RLC loads was conducted on the previous tests, so when S3 is opened, the RLC loads are optimally balanced to the EUTs output. Figure 10 shows the results of both the RLC load UI test and the PHIL UI test. The results are very close in both duration and in the instantaneous response. In Figure 10, the removal of the utility corresponds to the trigger signal transitioning from about 0 to 25.

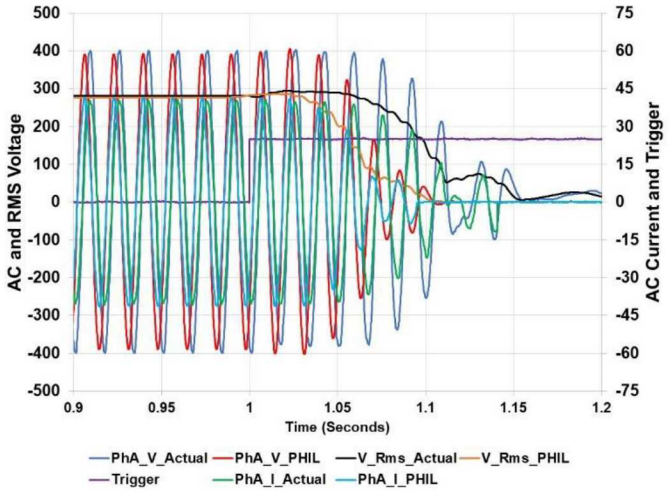
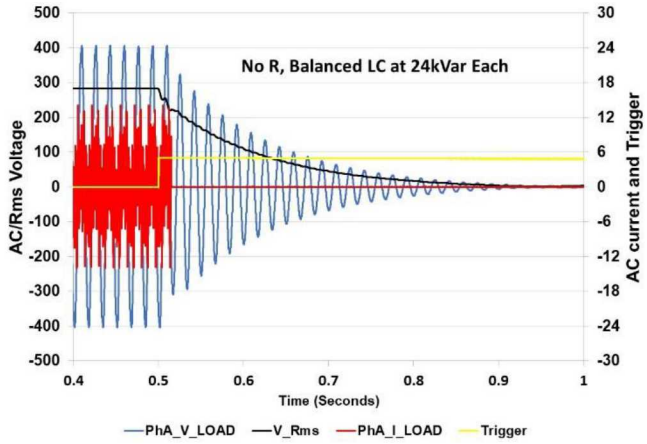


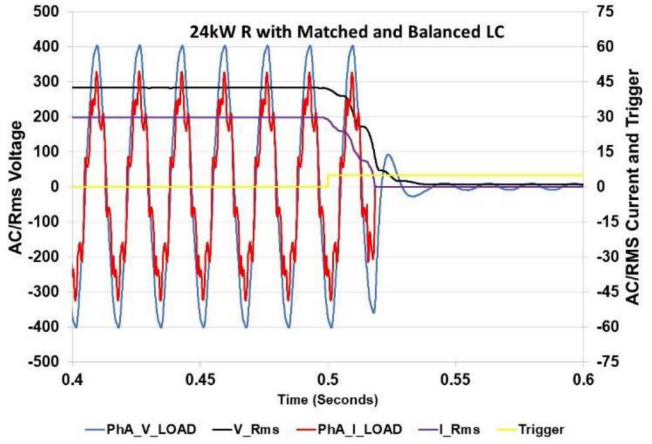
Fig. 10 RLC and PHIL with UI algorithm turned "on"

A. Inductive-Capacitive (LC) Resonant Tank Circuit Ring-Down

Aside from actual tests to verify agreement between the two methods being used, another characteristic of the LC resonant circuit that can be used to validate the characteristics of each approach. The inductance and capacitance of the RLC balanced circuit are set to resonate at 60Hz and if just the LC exist, when the utility is removed a ring-down of the stored energy can be observed and quantified. Figure 11 (a) shows the results of this test and the ring-down effect of the stored energy dissipation. If the resistive load is added to the LC resonant tank circuit, it is expected to quickly dampen the ring-down because the resistive load will dissipate the stored energy, as shown in figure 11 (b).



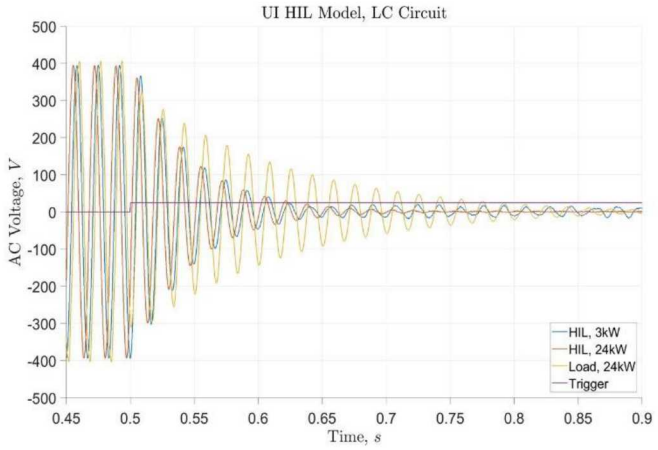
(a)



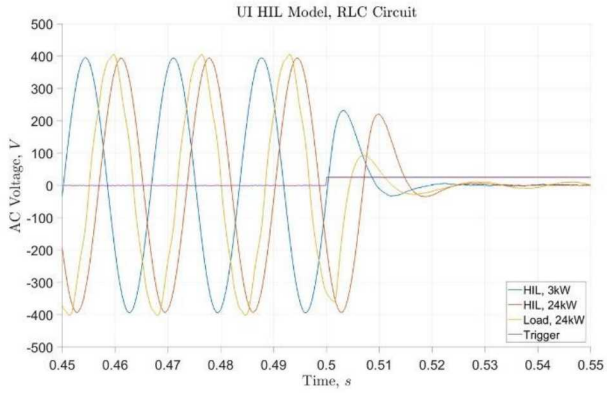
(b)

Fig. 11 (a) LC resonant circuit ring-down characteristic (b) RLC resonant circuit ring down characteristic that is balanced for a Q factor of 1

The PHIL simulation circuit can also be characterized using the LC resonant ring-down method. With the simulated RLC circuit adjusted to simulate the actual loads, the ring down characteristic should be similar. Figure 12 (a) shows the result of the PHIL LC ring- down validation test. The plot provides a ring-down for a LC configuration at 3kVar and for 24kVar. It also provides the comparison to the RLC load ring shown, shown as the yellow trace marked load 24kW. Figure 12 (b) shows the PHIL RLC ring down validation test. The test shows the damped ring down because of the presence of the resistive load element. The plot also provides a comparison to the RLC load waveform and shows a strong agreement.



(a)



(b)

Fig.12 (a) PHIL LC ring-down characterization at two power levels with RLC load comparison, (b) PHIL RLC ring-down at two power levels and with RLC load comparison

B. Real Load as part of PHIL UI Test

Implementing real load into the PHIL validation process can provide additional confidence in the simulation but it does require additional capabilities. The PHIL configuration shown in Figure 4 requires the EUT's current to be monitored during the configuration and testing the UI capabilities of the EUT using this method. A key attribute of PHIL is the elimination of costly, bulky, and heat generating RLC loads and introducing such loads as part of the testing configuration does diminish this reducing in load requirements. Figure 13 shows the additional requirement to monitor the load. If the EUT is a 3-phase device, then the load monitor will also require 3-phase monitoring.

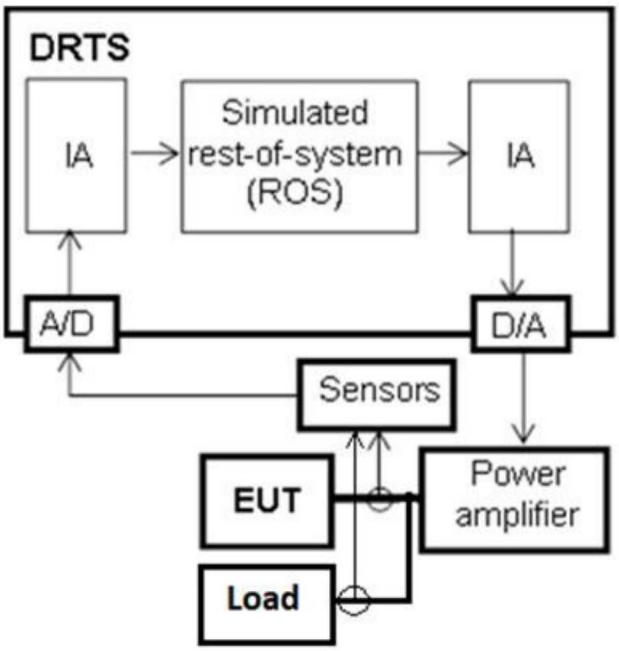


Fig. 13. Real load configuration as part of PHIL UI testing

V. Conclusion

A comparative assessment of the unintentional islanding detection of a utility interconnected distributed energy device using a RLC-balanced load configuration and a PHIL configuration was performed. Data presented in this analysis show the EUT demonstrated a continuous ROT when the UI algorithm is turned off and connected to both the RLC balanced load and to the PHIL configuration. The comparison of the two methods also shows the EUT adhere to the required 2-second response duration and demonstrate the UI waveform characteristics are similar.

Validation of the PHIL was another area of investigation and data was compared from UI tests using both methods. The results suggest strong correlation between the two methods. The validation also introduced signature ring-down characteristics of LC loads and compared the results of both methods and the results were similar. Using the same process, a resistive load was added, and the ring-down characteristic was quickly dampened by the resistive load for both configurations.

An alternative PHIL validation introduces new requirements for the PHIL configuration because an actual load is introduced to the configuration. This will diminish the no-load requirements of the PHIL and may be challenging to implement if analog signals are not available. The findings of using PHIL for UI tests have shown great potential and can be a great design tool and perhaps a certification tool as well.

References

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