國立臺灣大學
National Taiwan University

NTUEE Quantum Electronics Lab

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2nd Joint ISTDM/ICSI 2019 Conference

Modulation of Turn-On Voltage in Undoped Si/SiGe Heterostructure Insulated-Gate Field-Effect Transistors (IGFETs) for Cryogenic Memory Applications

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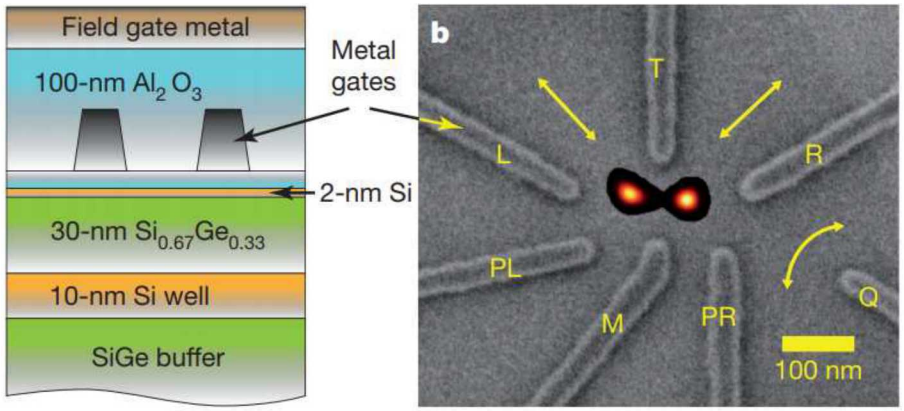
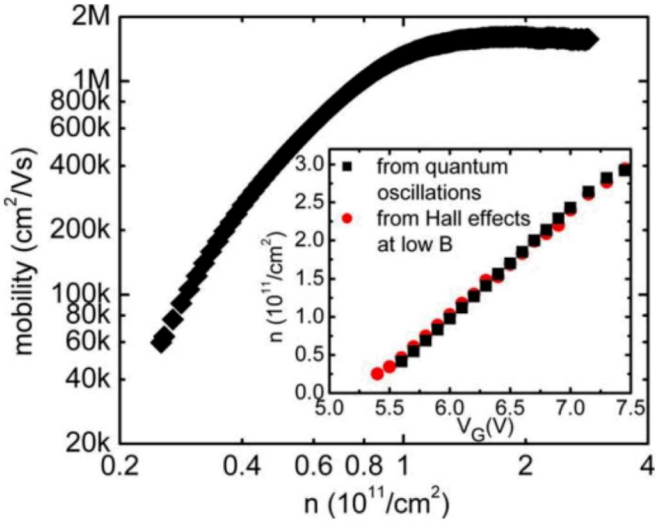
Outline

- Motivation
- Material Growth and Device Fabrication
- Device Characteristics of Si/SiGe Flash Memory
- Summary

Motivation: Si-Based Quantum Computing



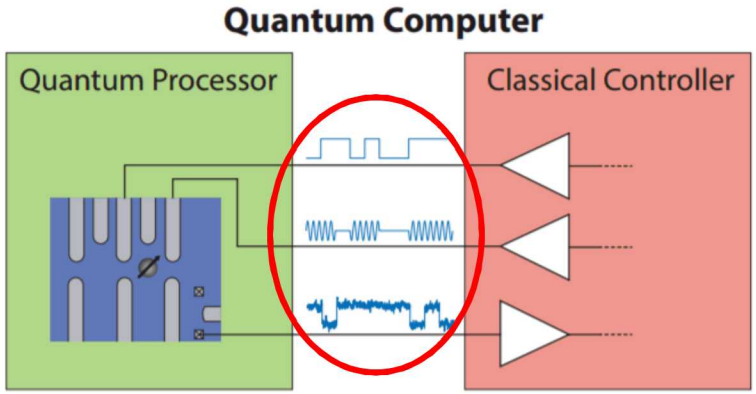
Nature (2012)

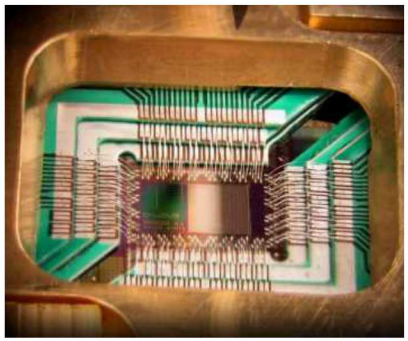


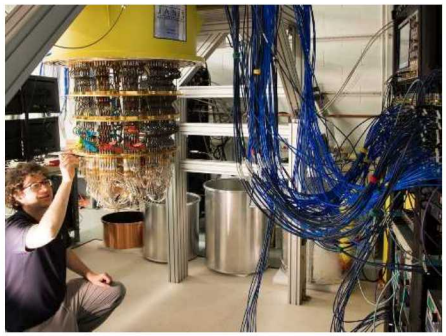
APL (2009)

- Undoped Si/SiGe heterostructures are a promising platform for quantum computing
  - Long spin decoherence times by in enriched ^{28}Si host
  - CMOS compatible
  - 2DEG mobility > 1.6× 10^6 $\mathrm{cm^2/Vs}$ at 0.3 K, low density ~ 10^{10} $\mathrm{cm^{-2}}$

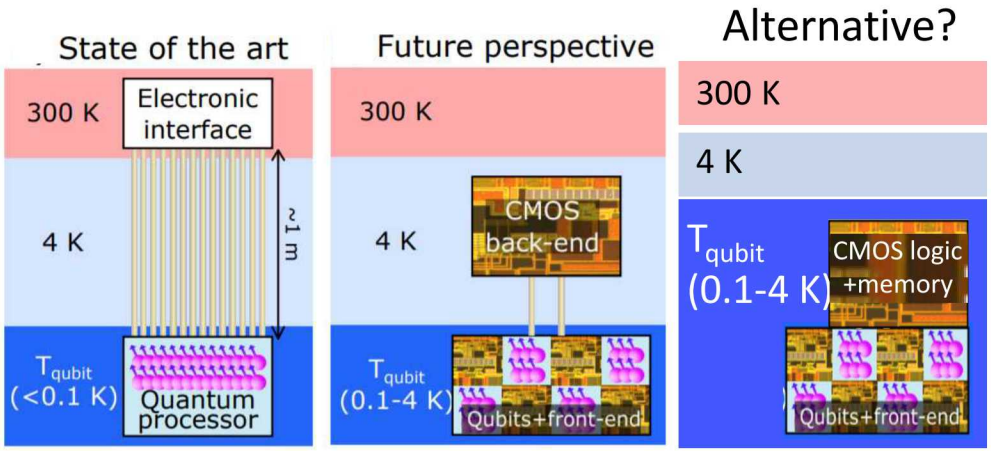
Motivation: Classical/Quantum Interface







D-Wave Systems Inc. *Google (2019)*



Microprocessors and Microsystems (2019)

- Challenges
  - Interconnects between classical (digital) and quantum computing devices (e.g. wiring, heating, efficiency and latency)
  - Only few studies on cryogenic logic and memory devices on the Si/SiGe platform

Motivation: Cryogenic Memory

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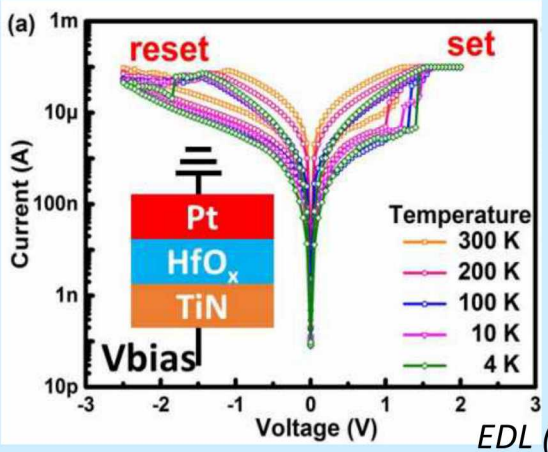
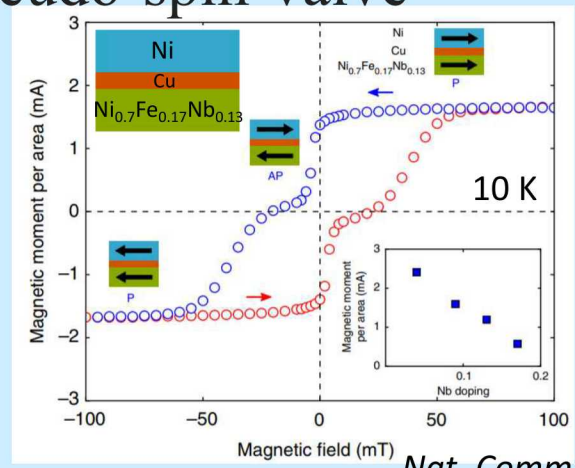
Emerging Memory

RRAM



EDL (2015)

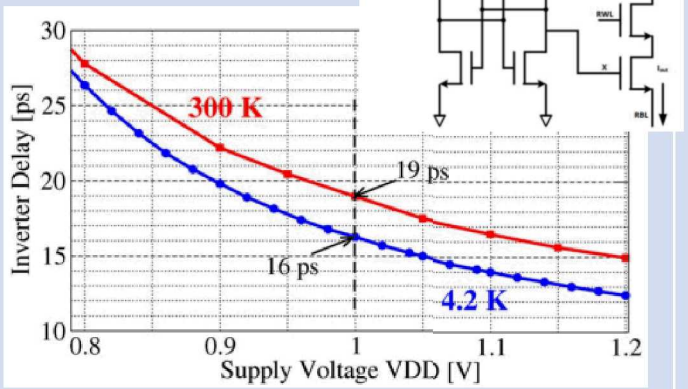
Pseudo-spin-valve



Nat. Commun. (2014)

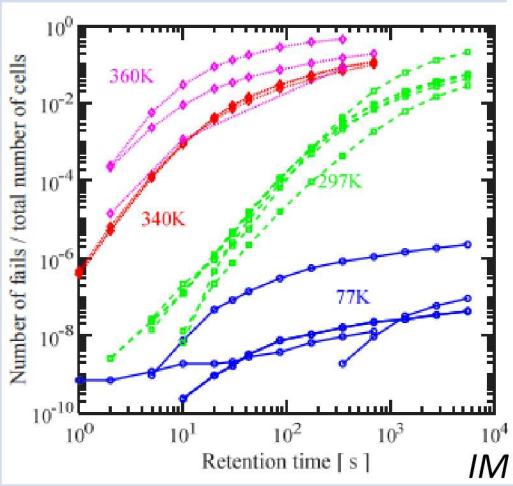
CMOS Memory

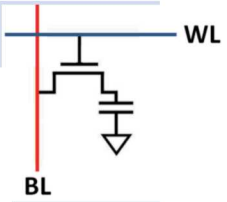
SRAM



IEEE Trans. Appl. Supercond. (2012)

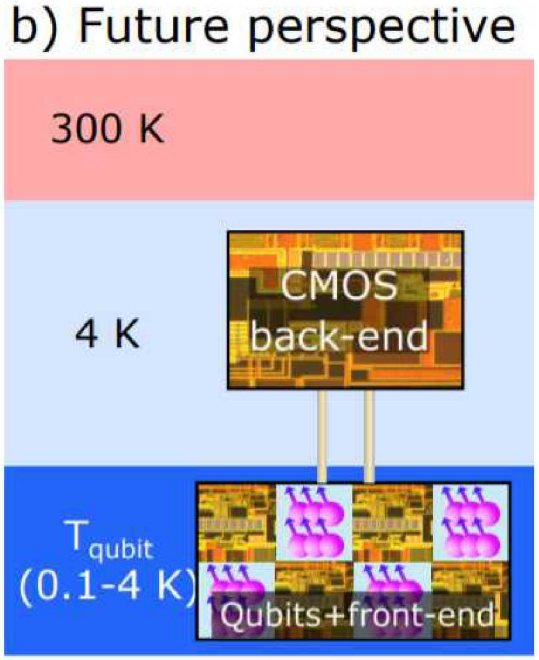
DRAM

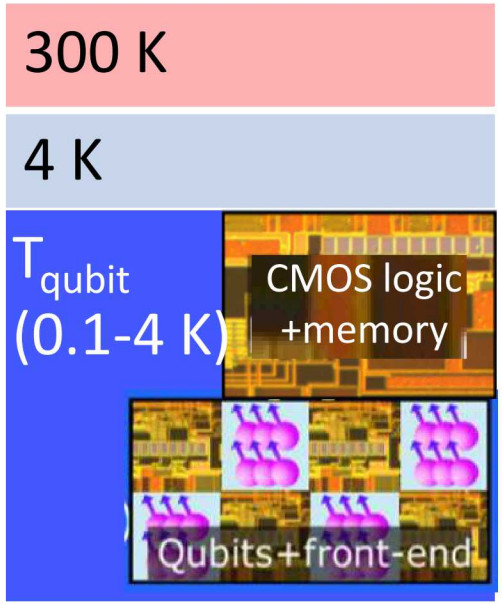


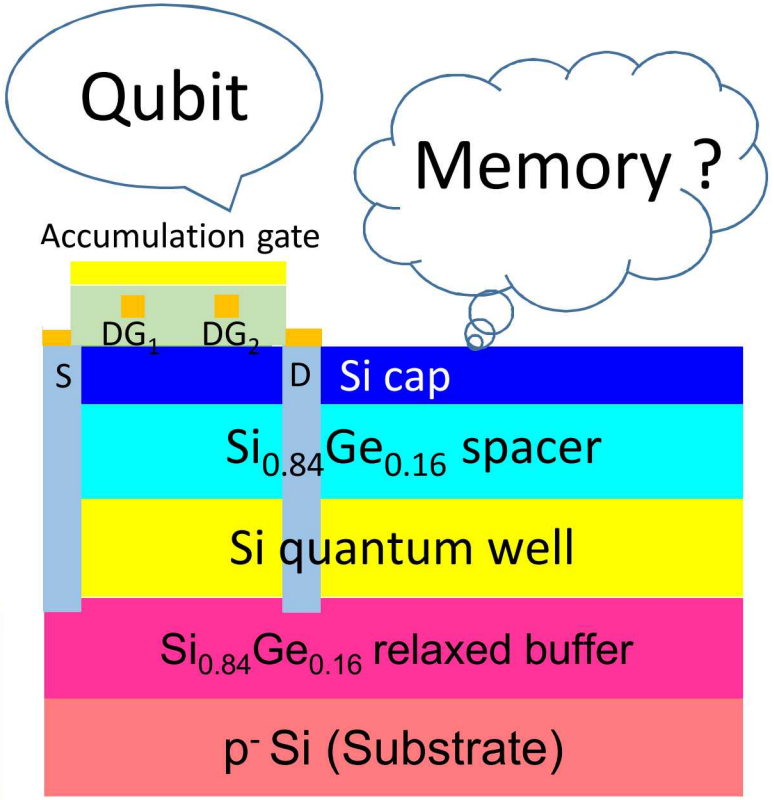


IMW (2018)

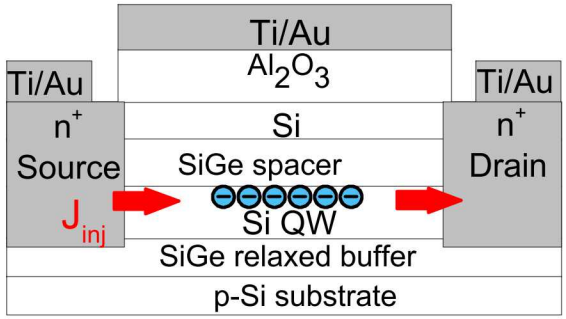
Motivation: Si/SiGe-Based Memory



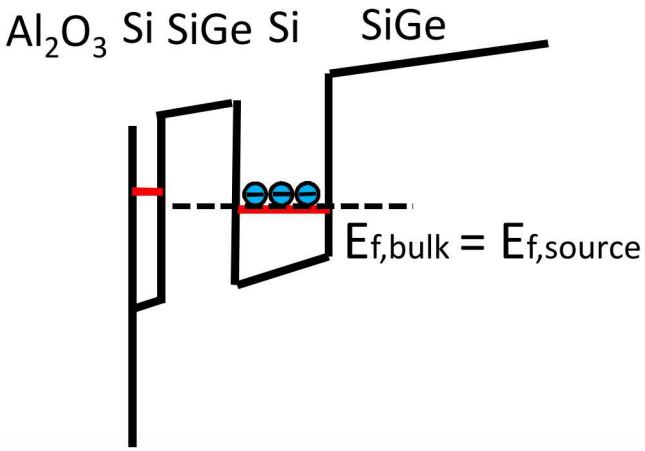


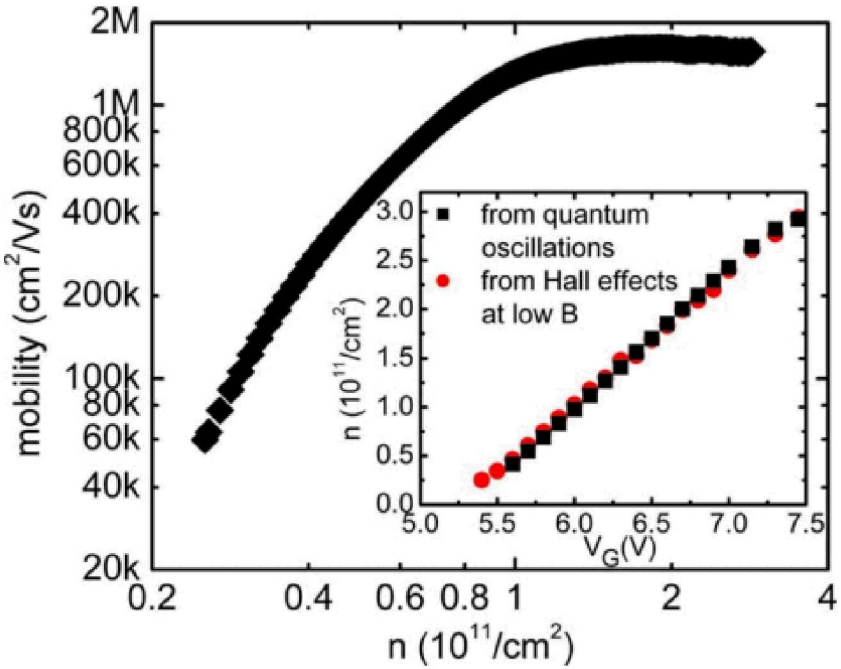


Prior Work: Surface Tunneling in Undoped Si/SiGe Heterostructures



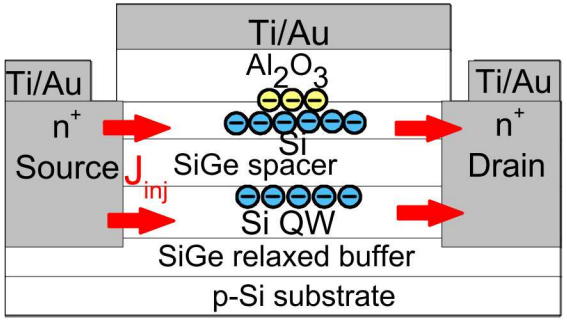
Mobile electrons

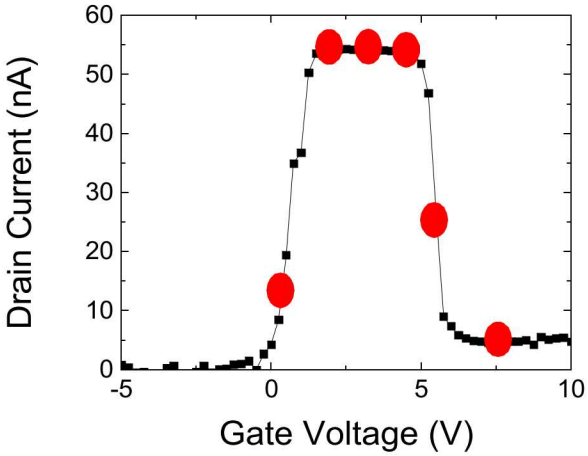


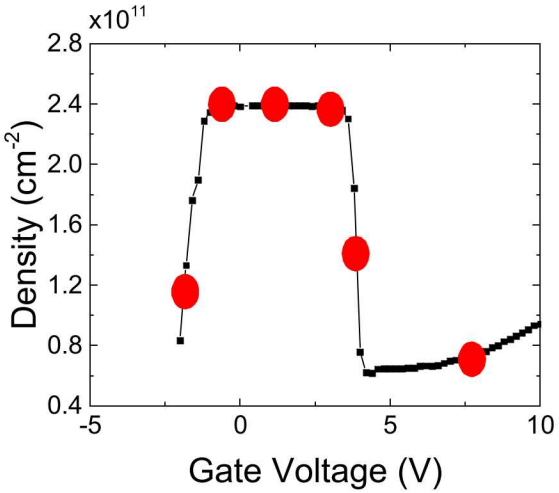


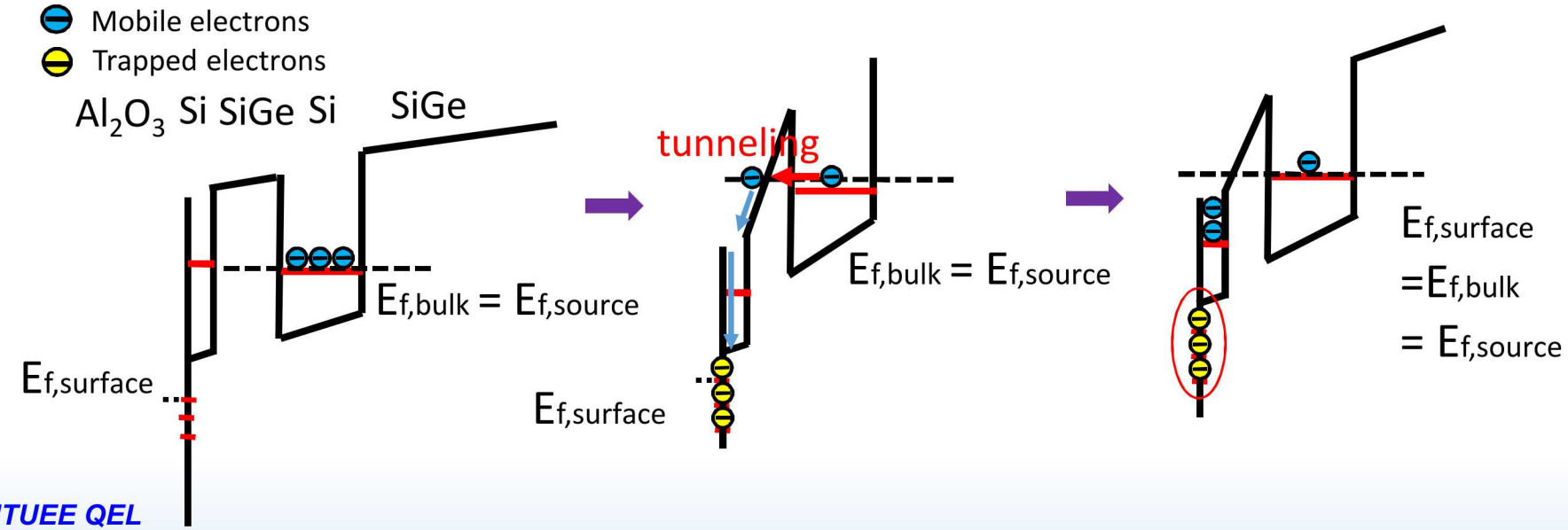
APL (2009)

Prior Work: Surface Tunneling in Undoped Si/SiGe Heterostructures

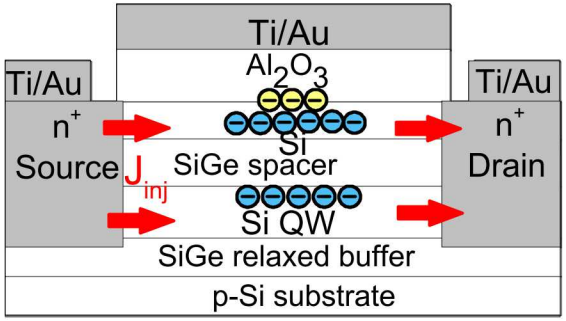


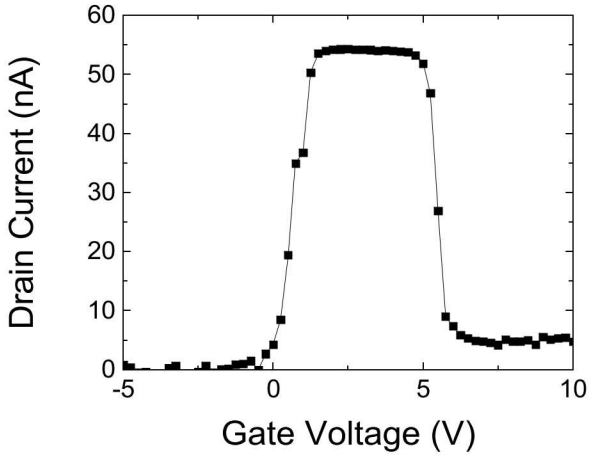


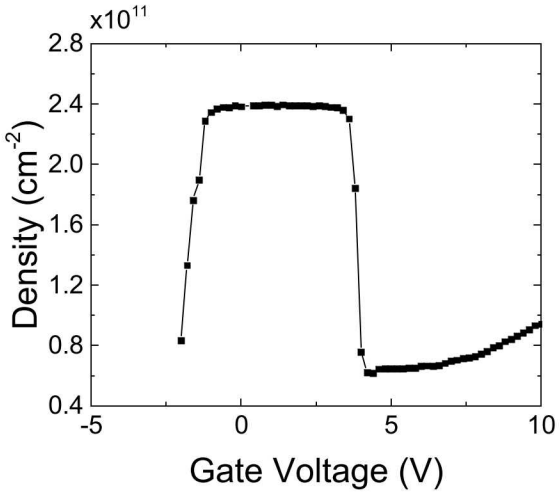


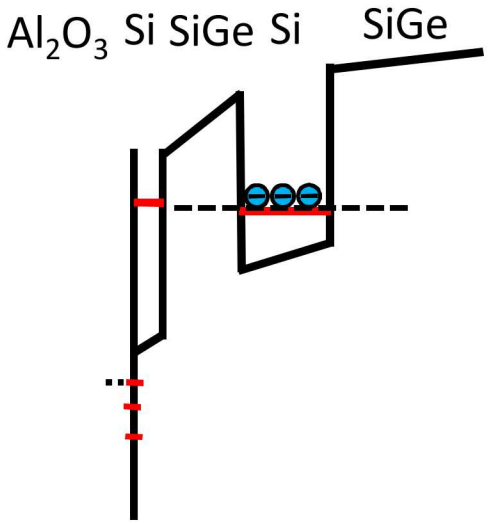


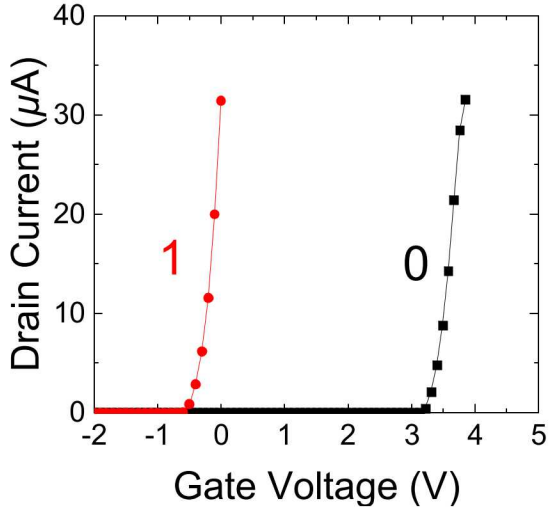
Prior Work: Surface Tunneling in Undoped Si/SiGe Heterostructures

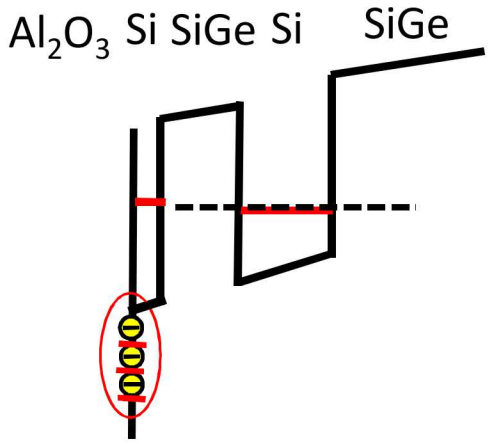






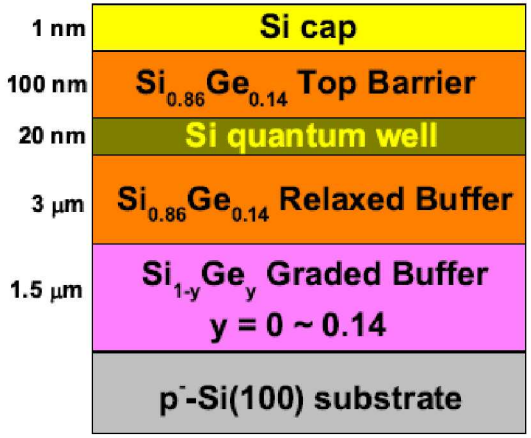


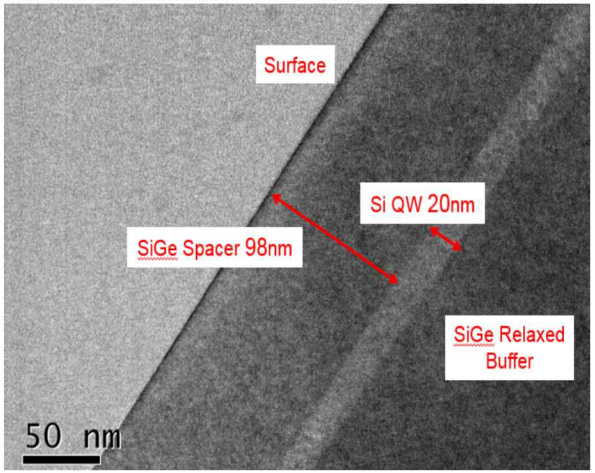


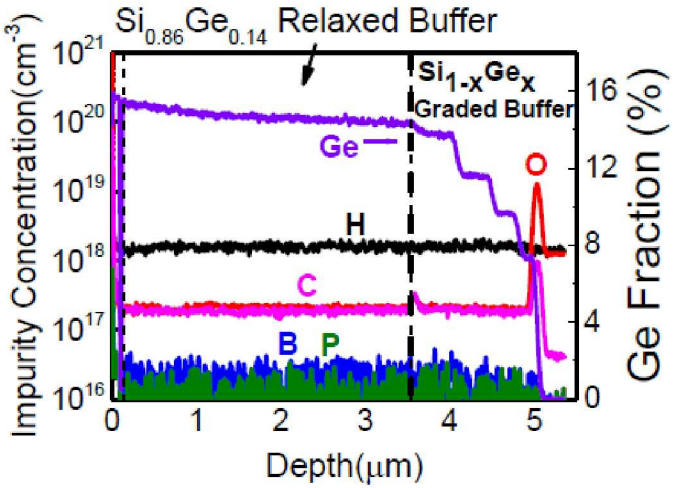


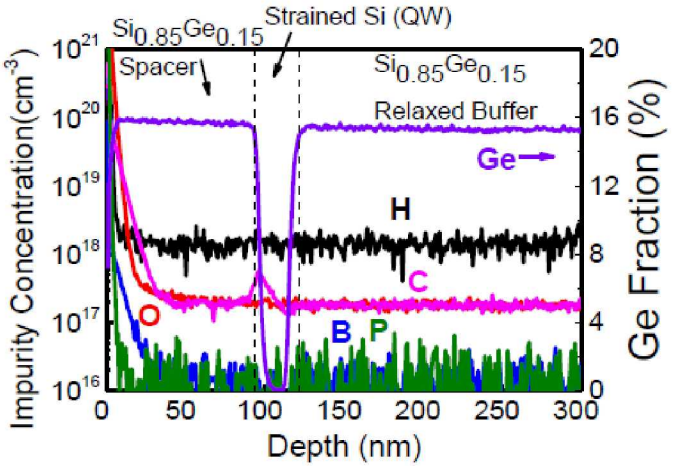
Charge ➡ ΔV_{th} ➡ Cryogenic Flash on Si/SiGe platform

Experiment: Epitaxy by Chemical Vapor Deposition



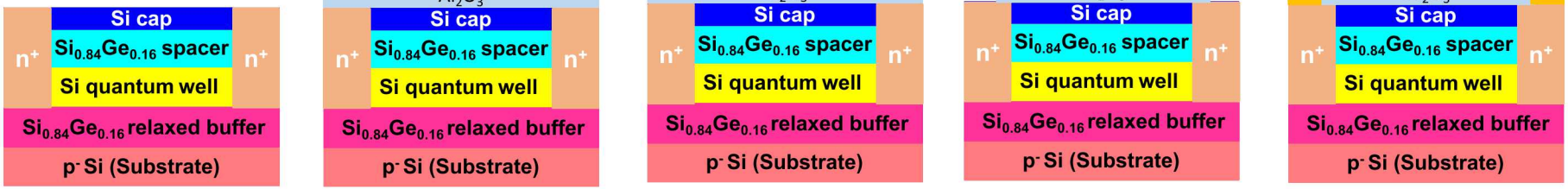






- Undoped Si/SiGe heterostructures grown by UHVCVD with SiH_4 and GeH_4 as precursors
- Low background impurity (C, O, B, P) levels

Device Fabrication



P^{31+} implant for S/D RTA 625°C 10 s for dopant activation

90-nm Al_2O_3 by ALD at 200°C

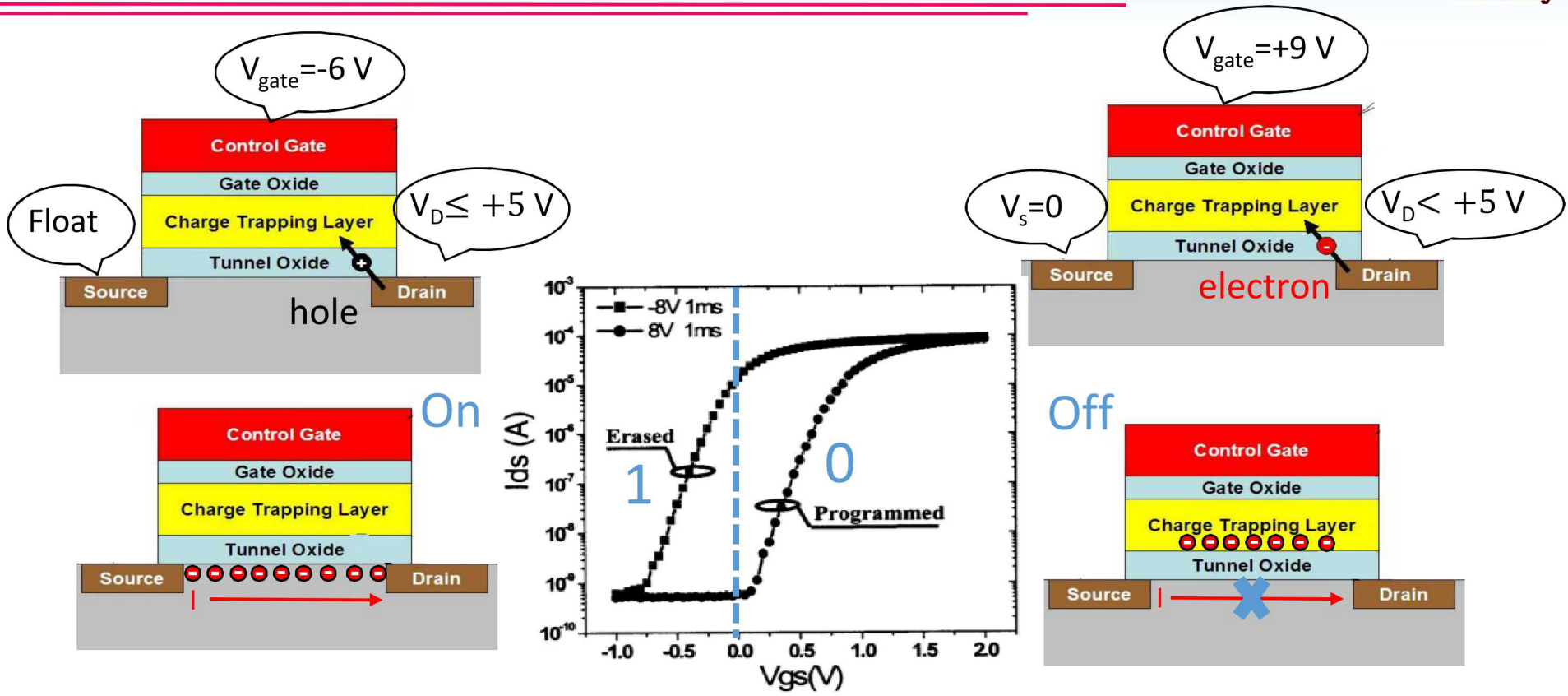
Ti/Au by e-beam evaporation as gate

Gate definition by ion mill

S/D contact window by BOE

Ti/Au by e-beam evaporation as contact

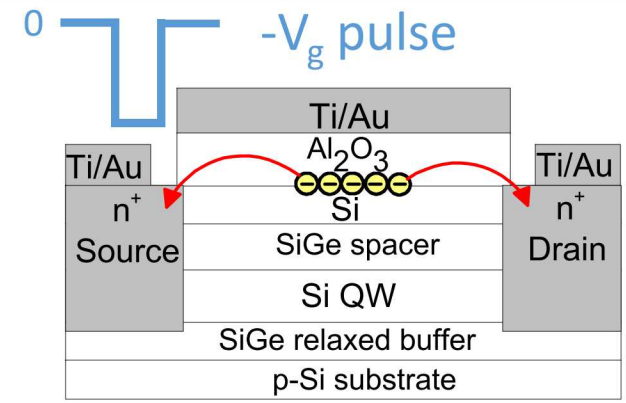
Operation Principle of Charge-Trapping Flash Memory

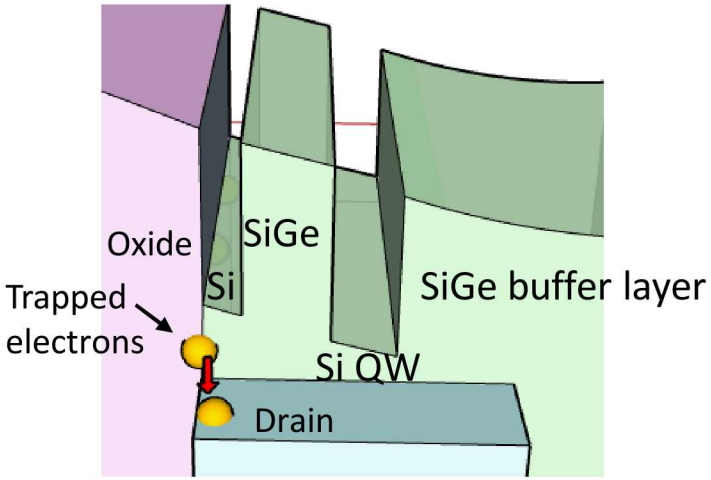


- Write '1' (Erase):
  Holes tunnel into CT layer, recombine with trapped electrons, V_{th} decreases.

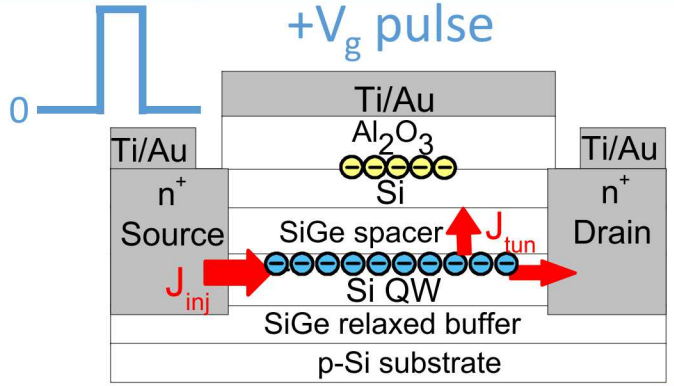
- Write '0' (Program):
  Electrons tunnel into and get trapped in the CT layer. V_{th} increases.

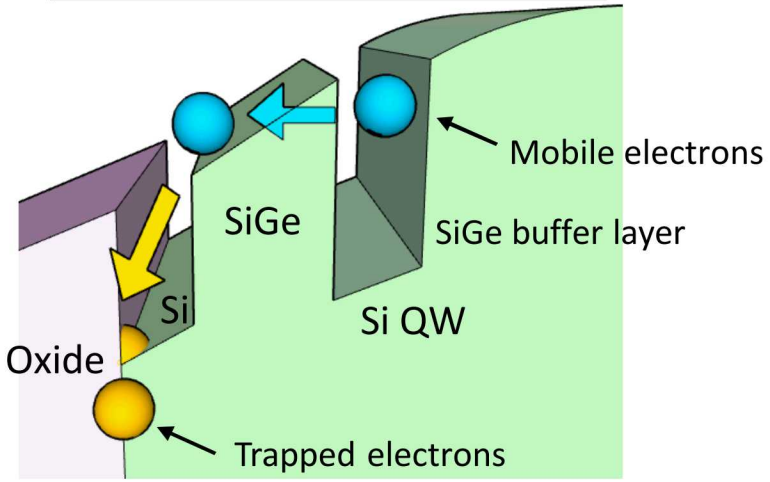
Operation Principle of Si/SiGe Flash Memory





- Write '1' (Erase):
  Electrons detrap from the interface states, V_{th} decreases.





- Write '0' (Program):
  Electrons tunnel to surface and be trapped at the Al_2O_3/Si interface states, V_{th} increases.

Operation Principle of Si/SiGe Flash Memory

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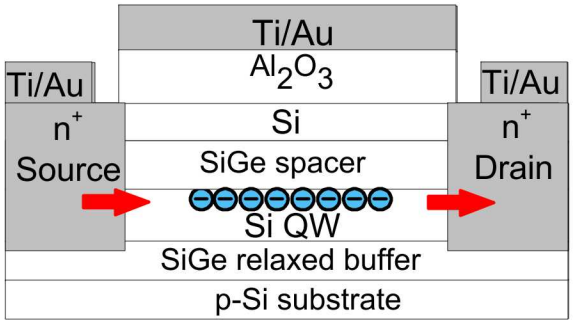
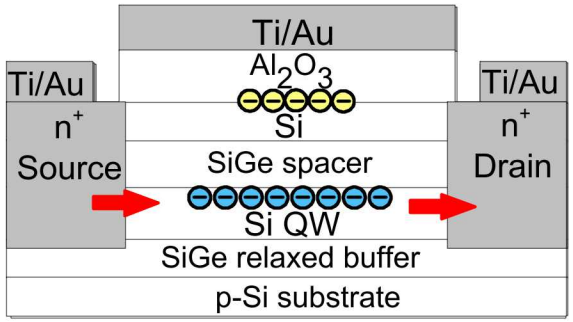
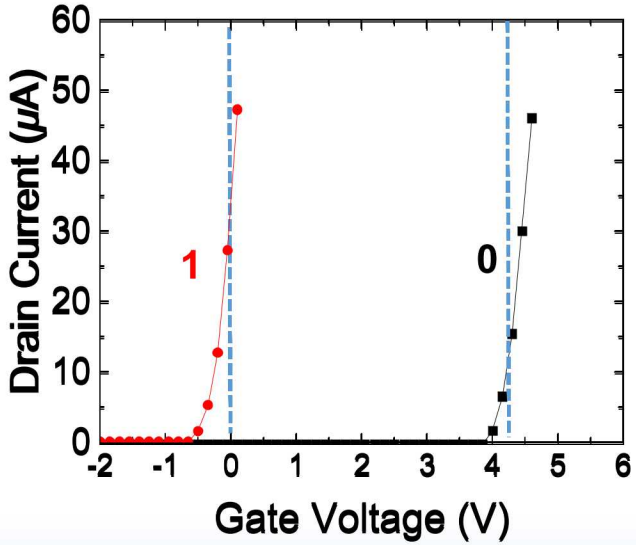
On



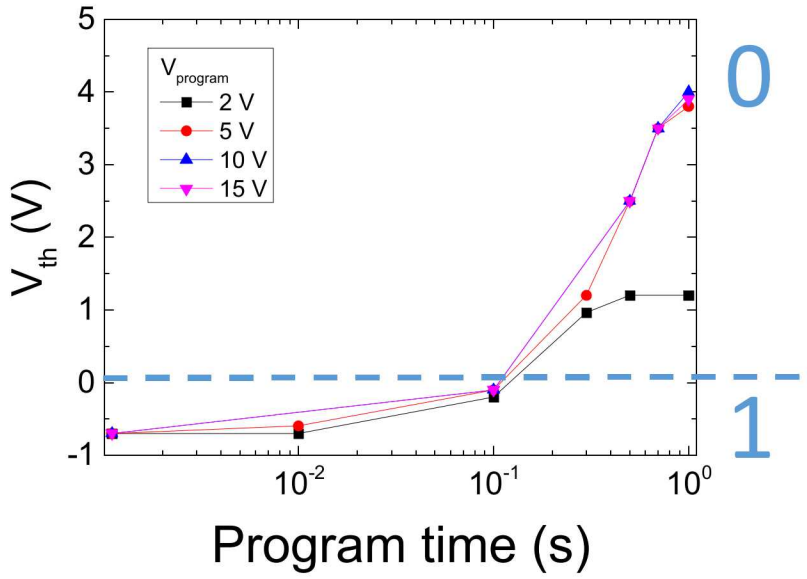
Off



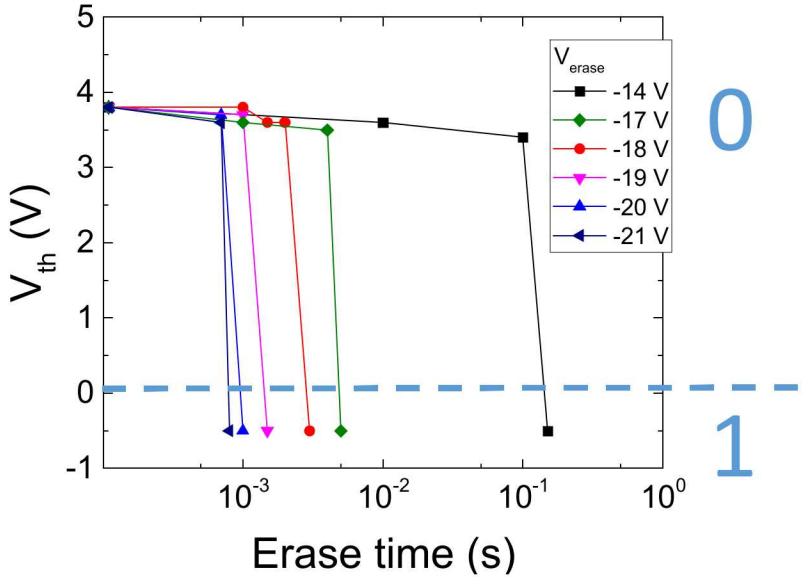


Device Characteristics

Program speed (Write 0)



Erase speed (Write 1)

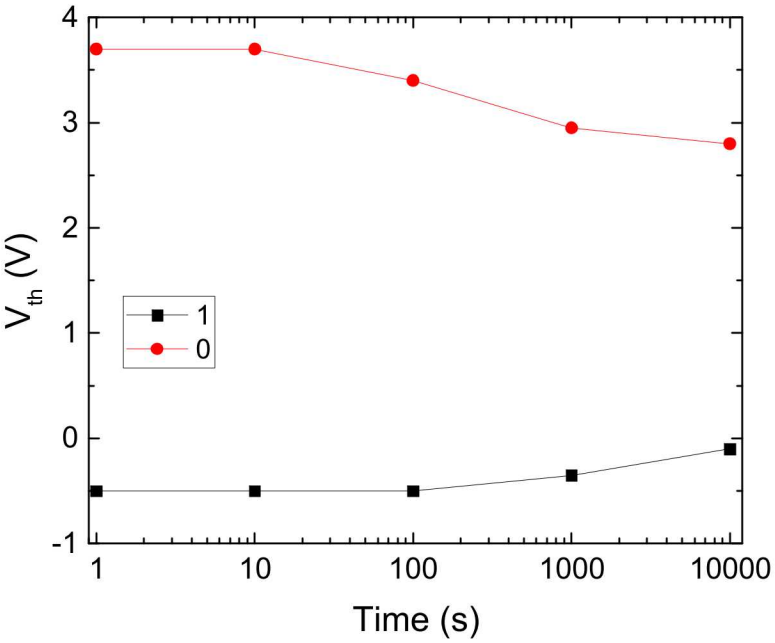


- The larger the erase voltage, the faster the erase speed.

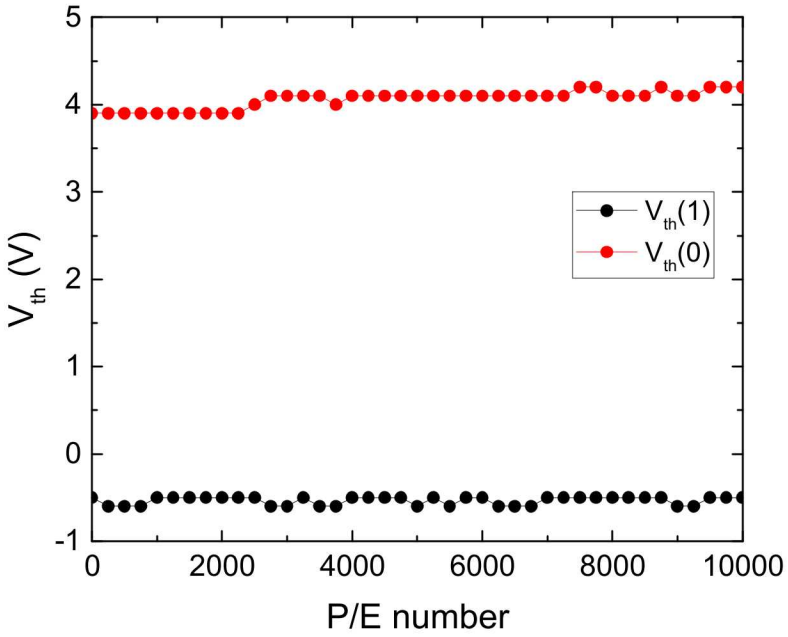
Device Characteristics

National Taiwan University

Retention



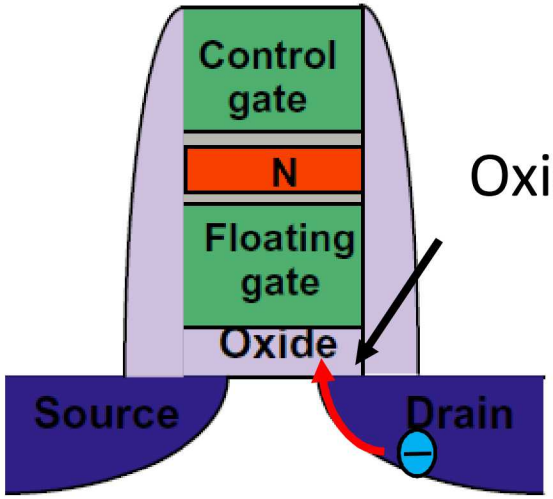
Endurance



- A large memory window (ΔV_T) of more than 4 V is obtained and retention is longer than 10,000 s.
- Endurance > 10,000 times without memory window degradation .

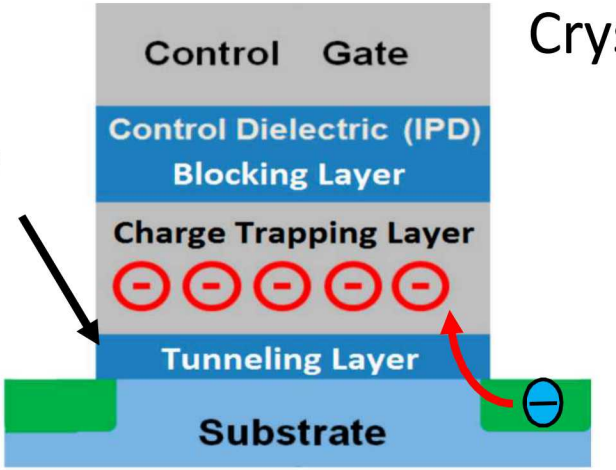
Comparison of Other Memories

Floating Gate Flash



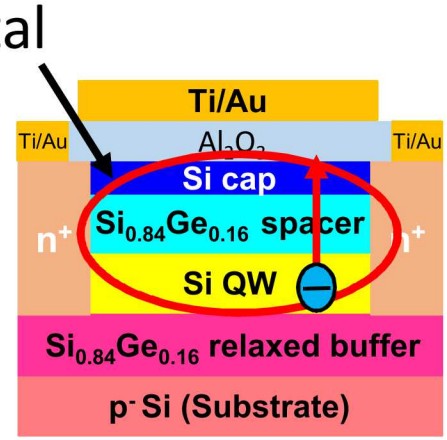
Microelectronic Engineering (2009)

Charge-Trapping Flash



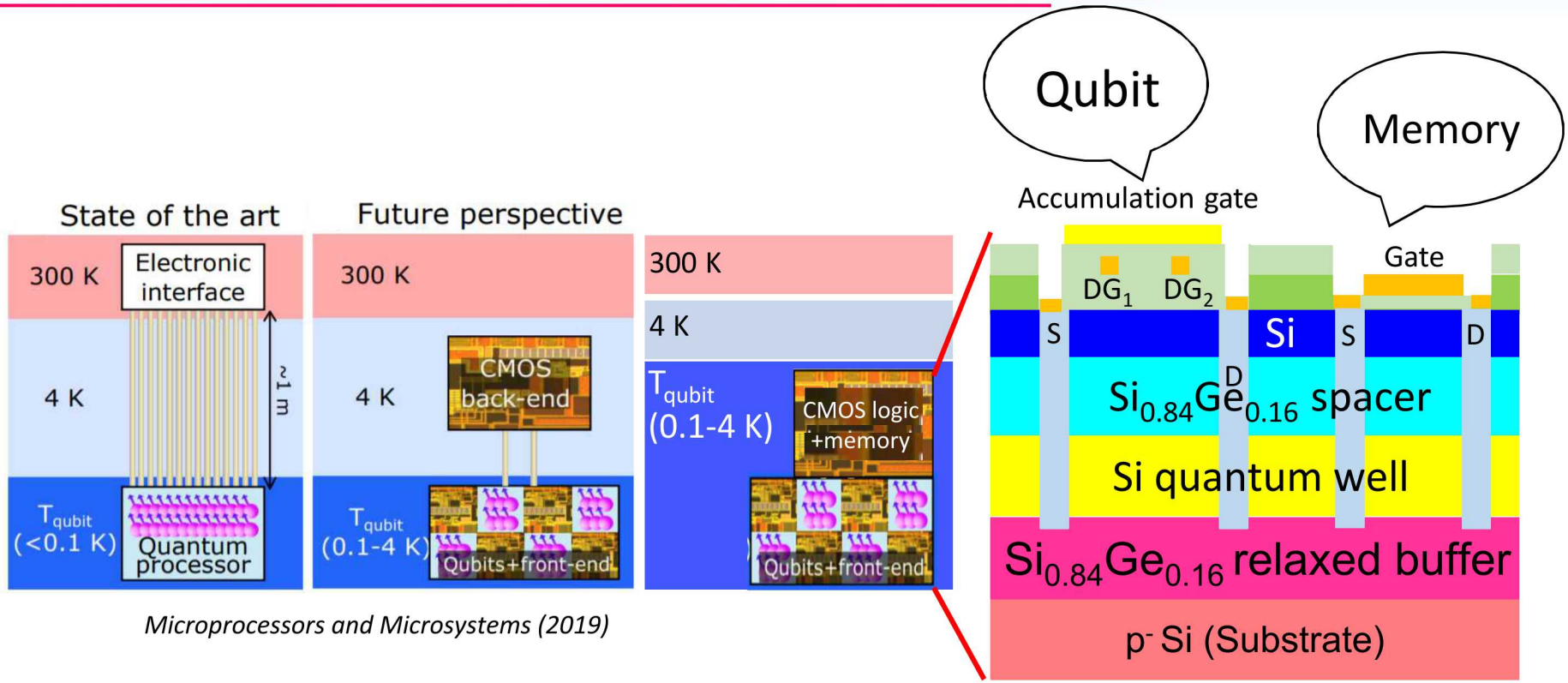
Materials 2014

Si/SiGe Flash



- Electrons tunnel through crystal SiGe instead of oxide
- No oxide breakdown issue ➡ Good endurance

Conclusions



Microprocessors and Microsystems (2019)

- Qubit and logic memory devices can be realized in Si/SiGe platform.

Summary

- Undoped Si/SiGe heterostructures insulated-gate FETs were fabricated and used as a cryogenic Flash memory.
- Electrons tunneled from buried QW to surface layer get trapped in the Al_2O_3/Si interface states, causing V_{th} shift.
- Endurance is tested by operating 10000 times without memory window degradation
- A large memory window (ΔVT) of more than 4 V is obtained and retention is longer than 10000 s.

Acknowledgement

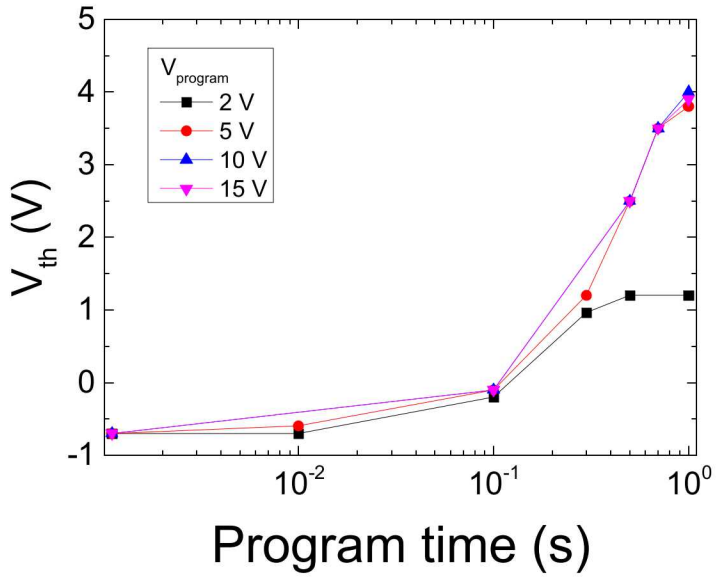
- This work at National Taiwan University has been support by the Ministry of Science and Technology.
- This work was performed, in part, at the Center for Integrated Nanotechnologies, a U.S. DOE, Office of Basic Energy Sciences, user facility. Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA-0003525. The views expressed in this presentation do not necessarily represent the views of the U.S. Department of Energy or the United States Government.

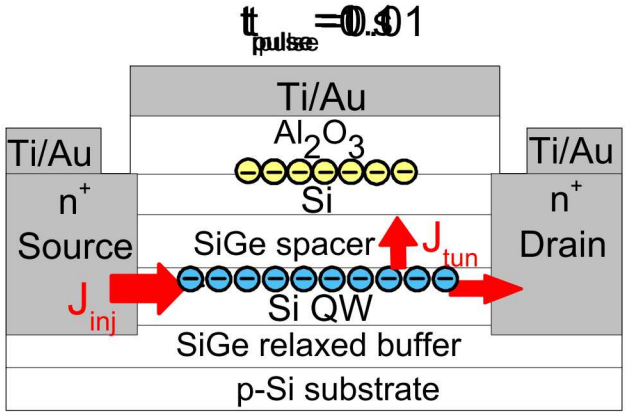
Thanks for your attentions

Back-up

Device Characteristics

Program speed

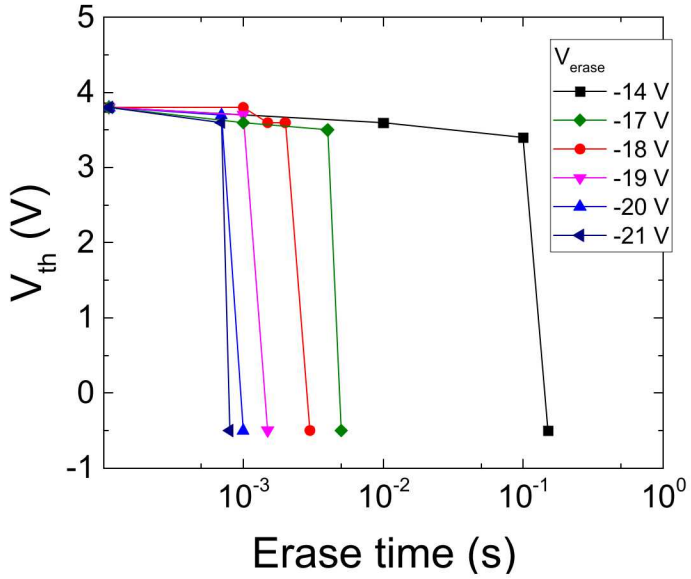


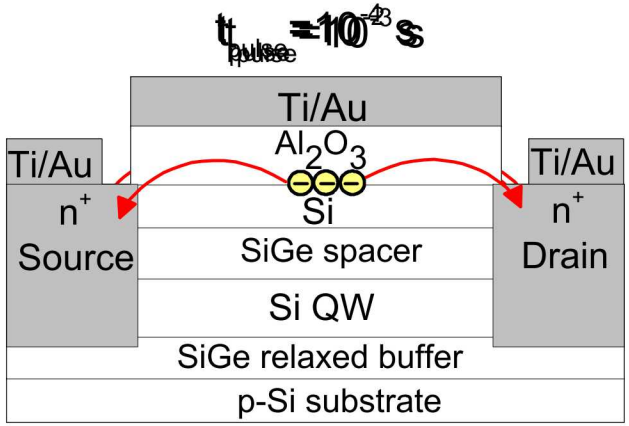


- The longer the program time, the bigger the ΔV_{th}.
- Program speed is not sensitive to program voltage.

Device Characteristics

Erase speed





- The longer the erase time, the bigger the ΔV_{th}.
- The larger the erase voltage, the faster the erase speed.

Temperature Dependence

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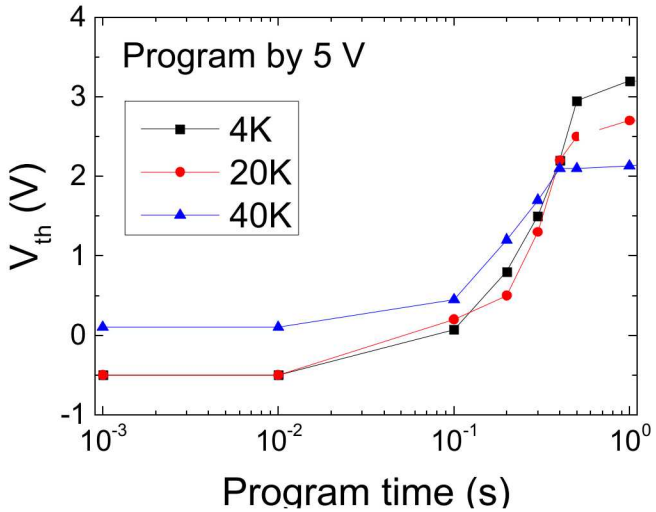
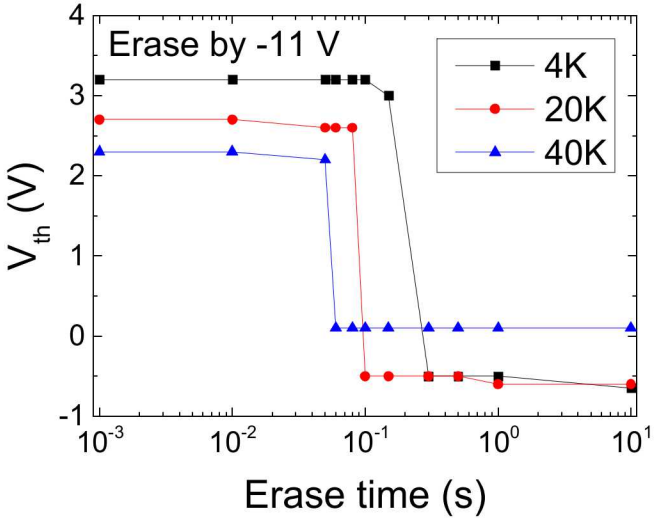
Program speed



Erase speed

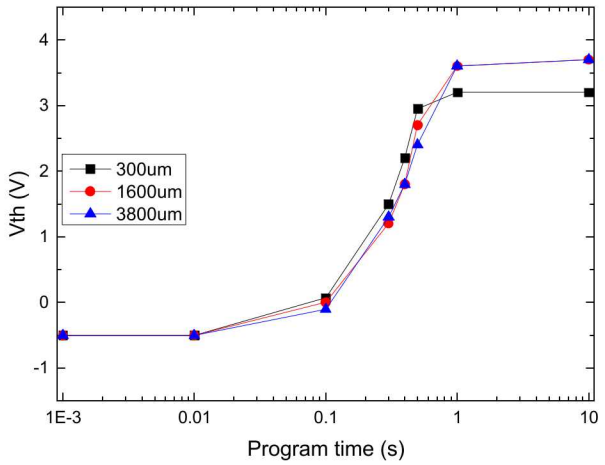


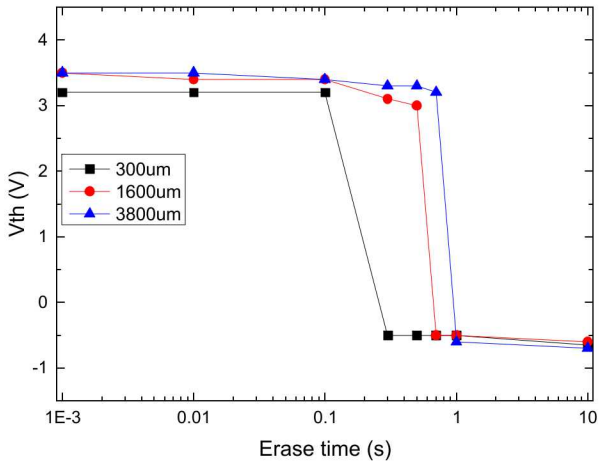
- Programming speed is insensitive to temperature
- Erasing speed increases with temperature

Write speed: Channel length effect

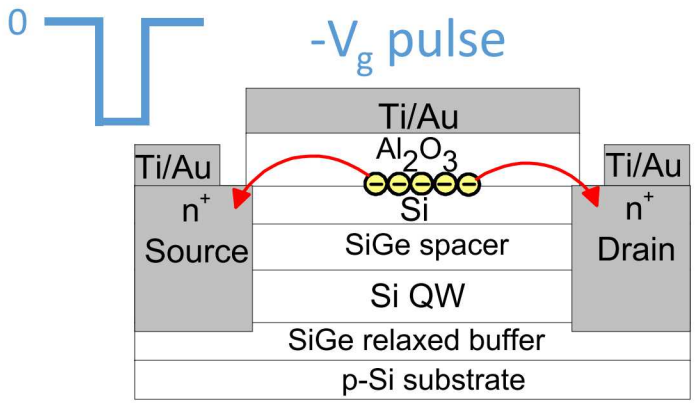
National Taiwan University

- Choose 5V as program voltage, pulse duration=1 s
  -11V as erase voltage, pulse duration= 1 s
- Program speed is not sensitive to channel length
- Erase speed is relevant to channel length:
  the shorter the channel, the faster the erase speed

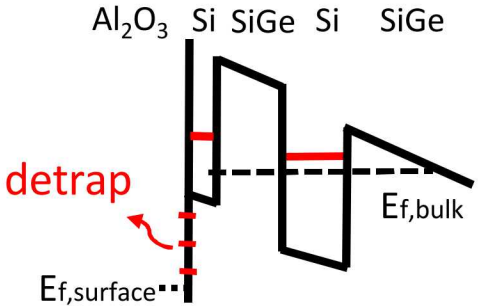


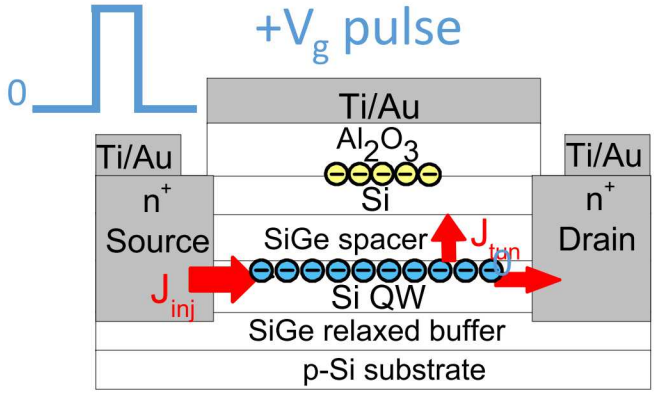


Operation principle of our device

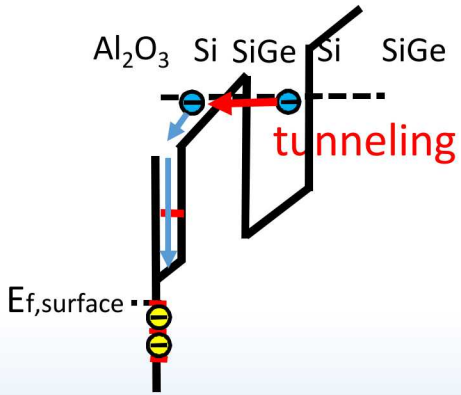


Write ‘1’ (Erase):
Electrons detrap from the interface states, V_{th} decreases.

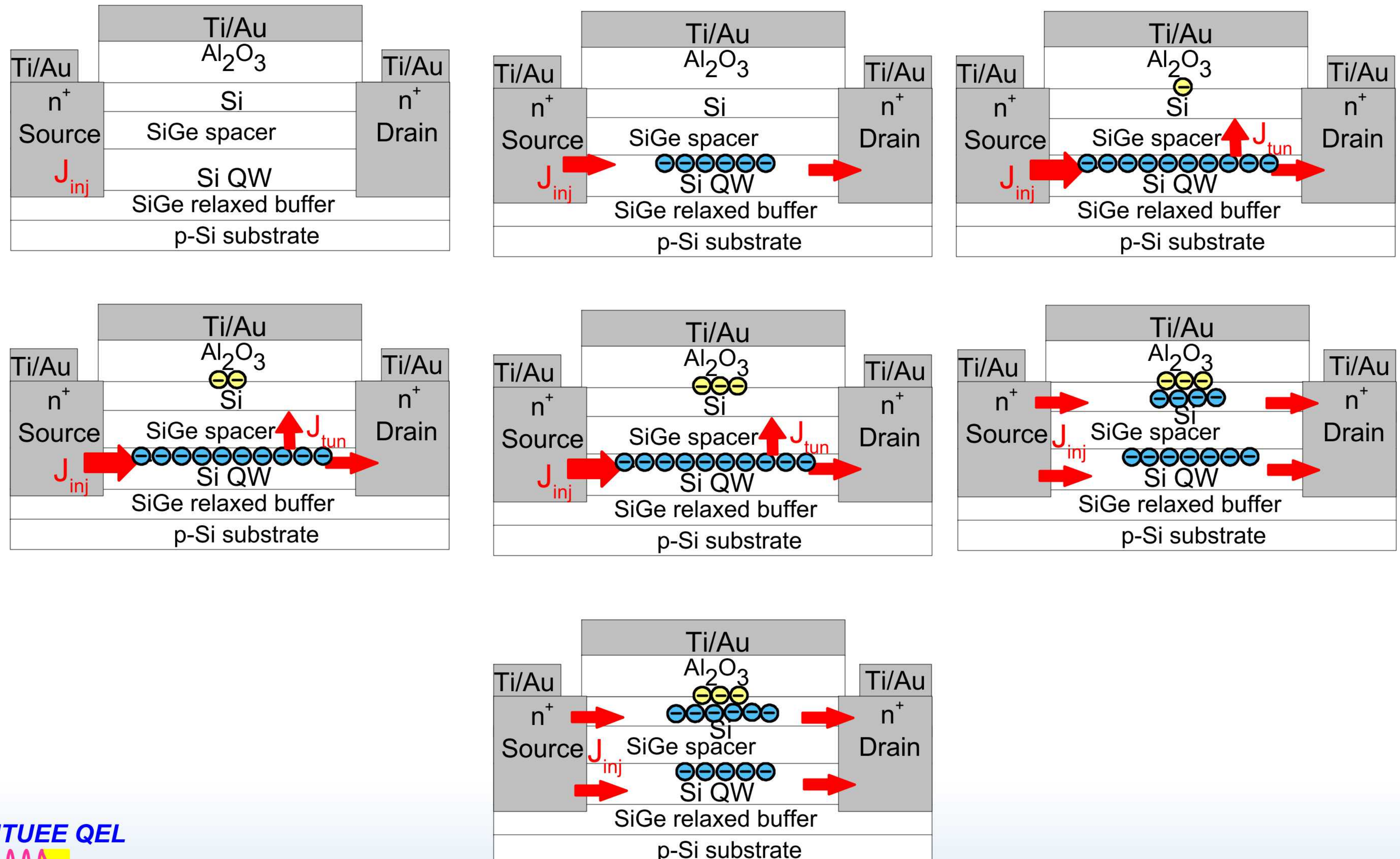




Write ‘0’ (Program):
Electrons tunnel to surface and be trapped at the Al_2O_3/Si interface states, V_{th} increases.



NTUEE QEL


Ti/Au
Al2O3
Ti/Au
Ti/Au
n+
Source
Si
SiGe spacer
n+
Drain
J inj
Si QW
SiGe relaxed buffer
p-Si substrate
Ti/Au
Al2O3
Ti/Au
Ti/Au
n+
Source
Si
SiGe spacer
n+
Drain
J inj
Si QW
SiGe relaxed buffer
p-Si substrate
Ti/Au
Al2O3
Ti/Au
Ti/Au
n+
Source
Si
SiGe spacer
J tun
n+
Drain
J inj
Si QW
SiGe relaxed buffer
p-Si substrate
Ti/Au
Al2O3
Ti/Au
Ti/Au
n+
Source
Si
SiGe spacer
J tun
n+
Drain
J inj
Si QW
SiGe relaxed buffer
p-Si substrate
Ti/Au
Al2O3
Ti/Au
Ti/Au
n+
Source
Si
SiGe spacer
J tun
n+
Drain
J inj
Si QW
SiGe relaxed buffer
p-Si substrate
Ti/Au
Al2O3
Ti/Au
Ti/Au
n+
Source
J inj
Si
SiGe spacer
n+
Drain
Si QW
SiGe relaxed buffer
p-Si substrate
Ti/Au
Al2O3
Ti/Au
Ti/Au
n+
Source
J inj
Si
SiGe spacer
n+
Drain
Si QW
SiGe relaxed buffer
p-Si substrate