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Sub-10µm Pitch Hybrid Direct Bond Interconnect Development for Die-to-Die Hybridization

John P. Mudrick, Jonatan A. Sierra-Suarez, Matthew B. Jordan, T.A. Friedmann, Robert Jarecki and M. David Henry

Sandia National Laboratories
Albuquerque, NM, USA

jmudric@sandia.gov

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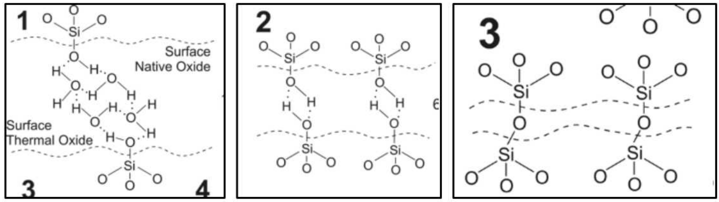
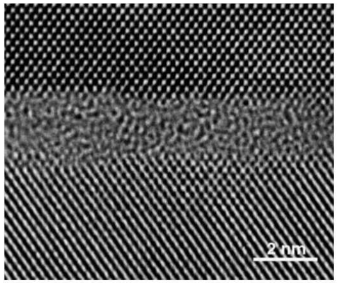
Direct bonding

- Homogeneous bonding
  - Hydrophobic (H-terminated) or hydrophilic (oxidized) surfaces
  - Attractive van der Waals interactions give way to covalent bond formation at moderate temperatures
  - Thermal requirements can be reduced with surface activation
- Hybrid bonding
  - 2 step bond formation
    - Homogeneous bond (above)
    - Post-bond anneal for interconnect formation



T. Plach et al., J. Appl. Phys. **113** (2013).
Goselle et al., *Semiconductor Wafer Bonding: Science and Technology* (1999).



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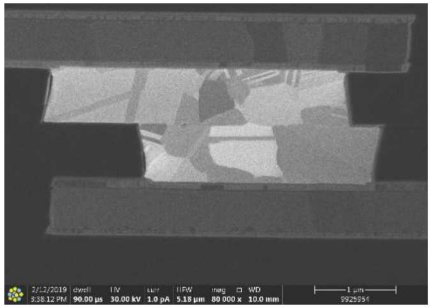
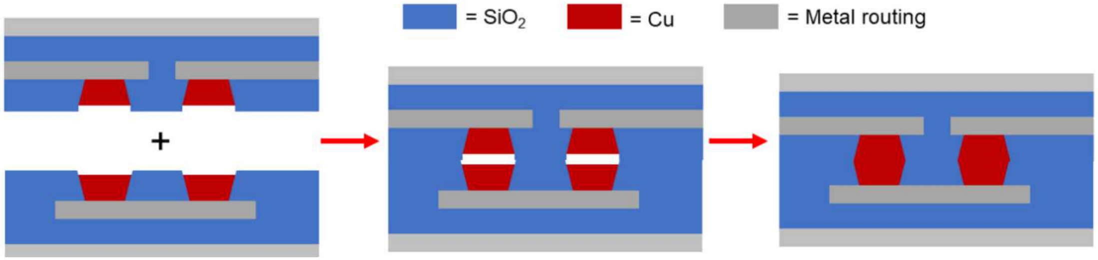
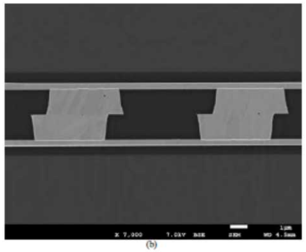
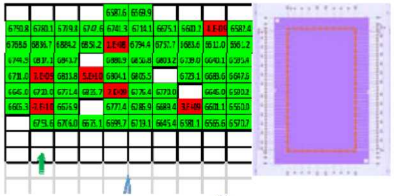




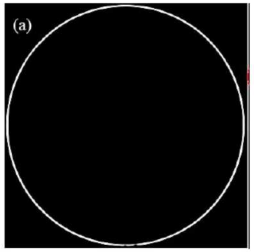
SiO_2/Cu interconnects: existing work

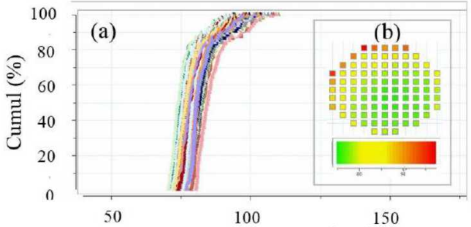
- Fine pitch, low defectivity, high reliability have been demonstrated





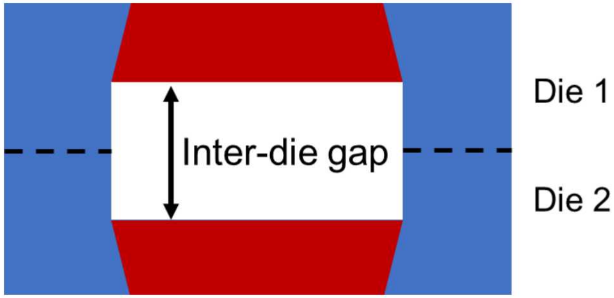
G. Gao et al., 2018 IEEE ECTC.

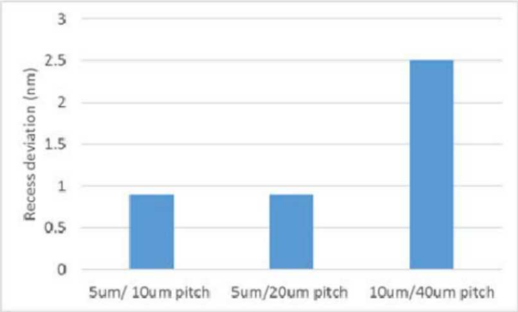




S. Lhostis et al., 2016 IEEE ECTC.

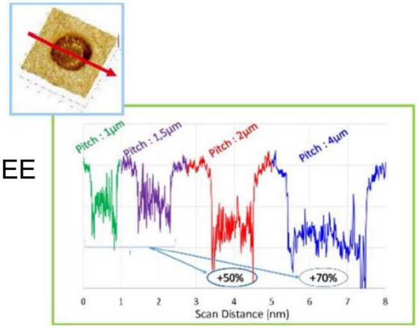
- Performance is reliant upon careful surface preparation
  - Low SiO_2 roughness and defectivity, uniform Cu recess depth

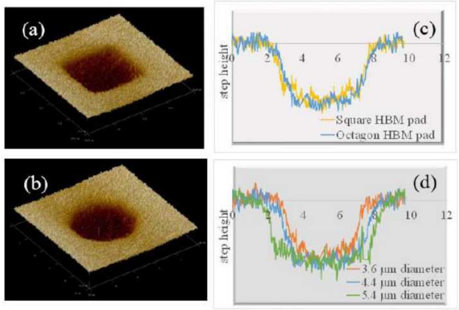




G. Gao et al., 2018 IEEE ECTC.

L. Arnaud et al., 2018 IEEE IRPS.

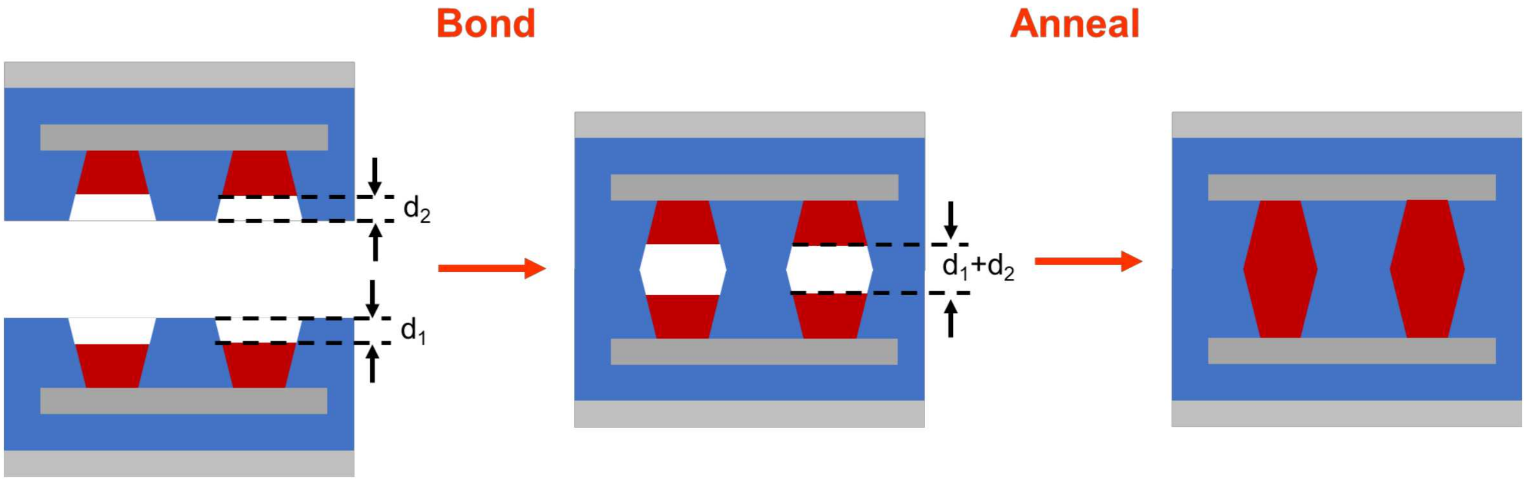




S. Lhostis et al., 2016 IEEE ECTC.

SiO_2/Cu interconnects: outstanding questions

- What range of inter-plug Cu gap heights leads to functional interconnects?
- Is there a dependence on post-bond anneal temperature?
- Goal: define process window
  - Key parameters: inter-die gap = $d_1 + d_2$, annealing temperature

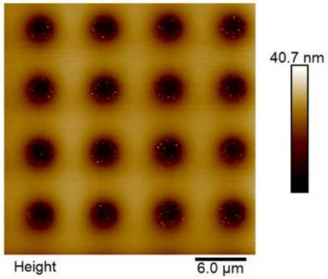


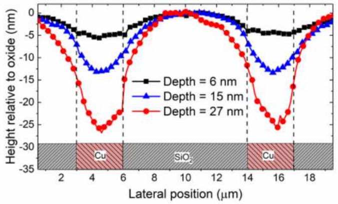
Outline of this work

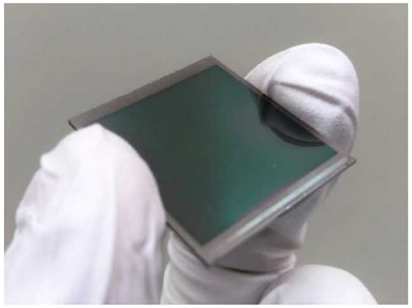
- Materials and process flow
- Direct bond surface preparation and metrology
- Test vehicle results
- Probing: physical and electrical
- Conclusion and paths forward

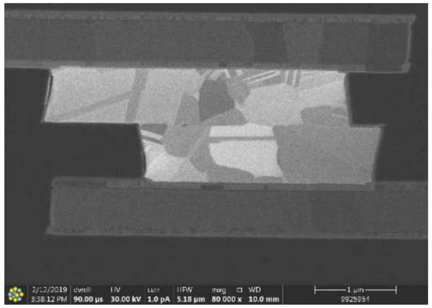
Acknowledgements

- Materials and process flow
  - **MESA Fab**
- Direct bond surface preparation and metrology
  - **Extensive AFM work: Lisa Caravello and Crystal Sennett (SNL)**
  - **Extensive CMP process development: Crystal Sennett**
- Test vehicle results
- Probing: physical and electrical
  - **FIB-SEM: Michael Rye (SNL)**
- Conclusion and paths forward









Outline

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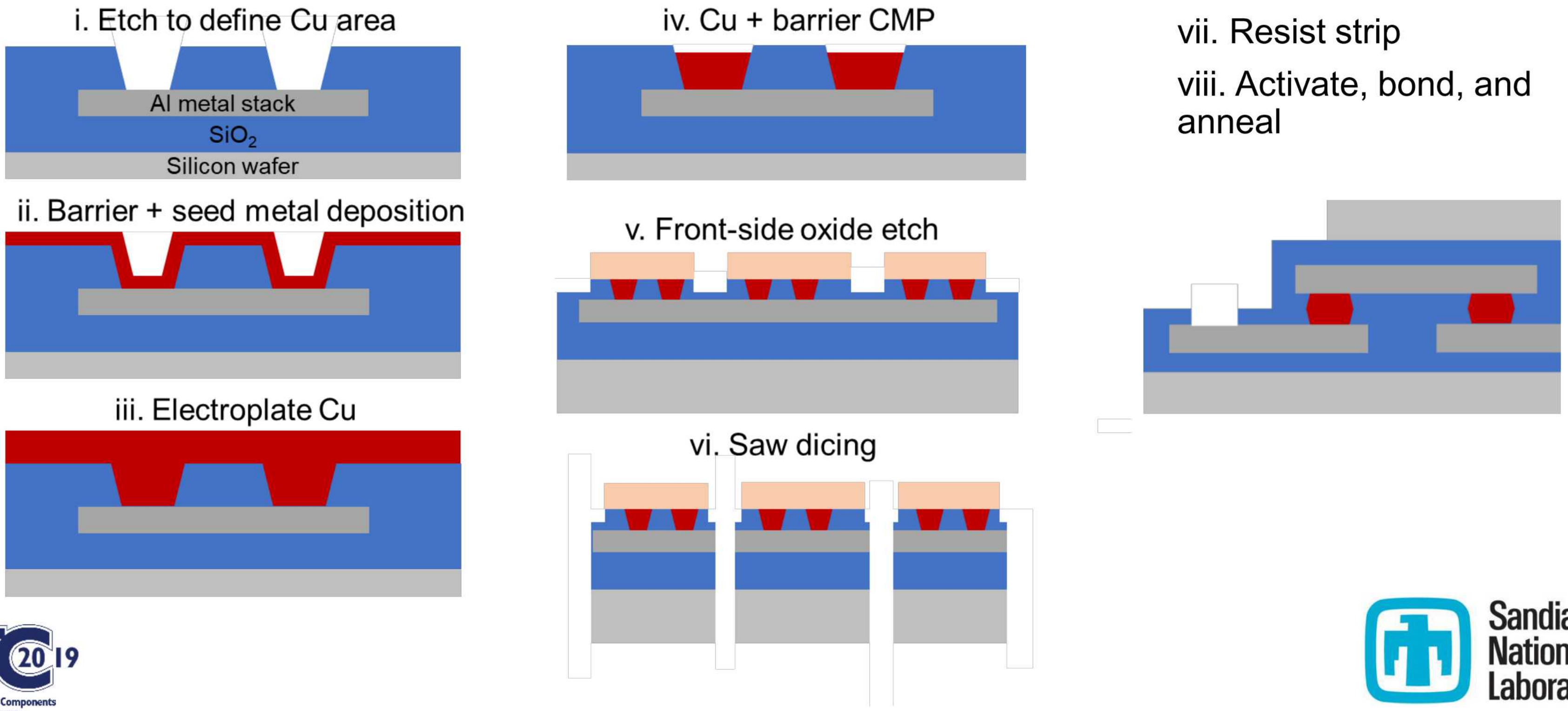
Materials and process flow

- Aluminum BEOL "starting material"
- Daisy chain structure with chain lengths up to 1.5 million
- Cu interconnect layer:
  - 3 μm diameter "plugs" on 7.5 μm pitch



i. Etch to define Cu area

ii. Barrier + seed metal deposition

iii. Electroplate Cu

iv. Cu + barrier CMP

v. Front-side oxide etch

vi. Saw dicing

vii. Resist strip

viii. Activate, bond, and anneal

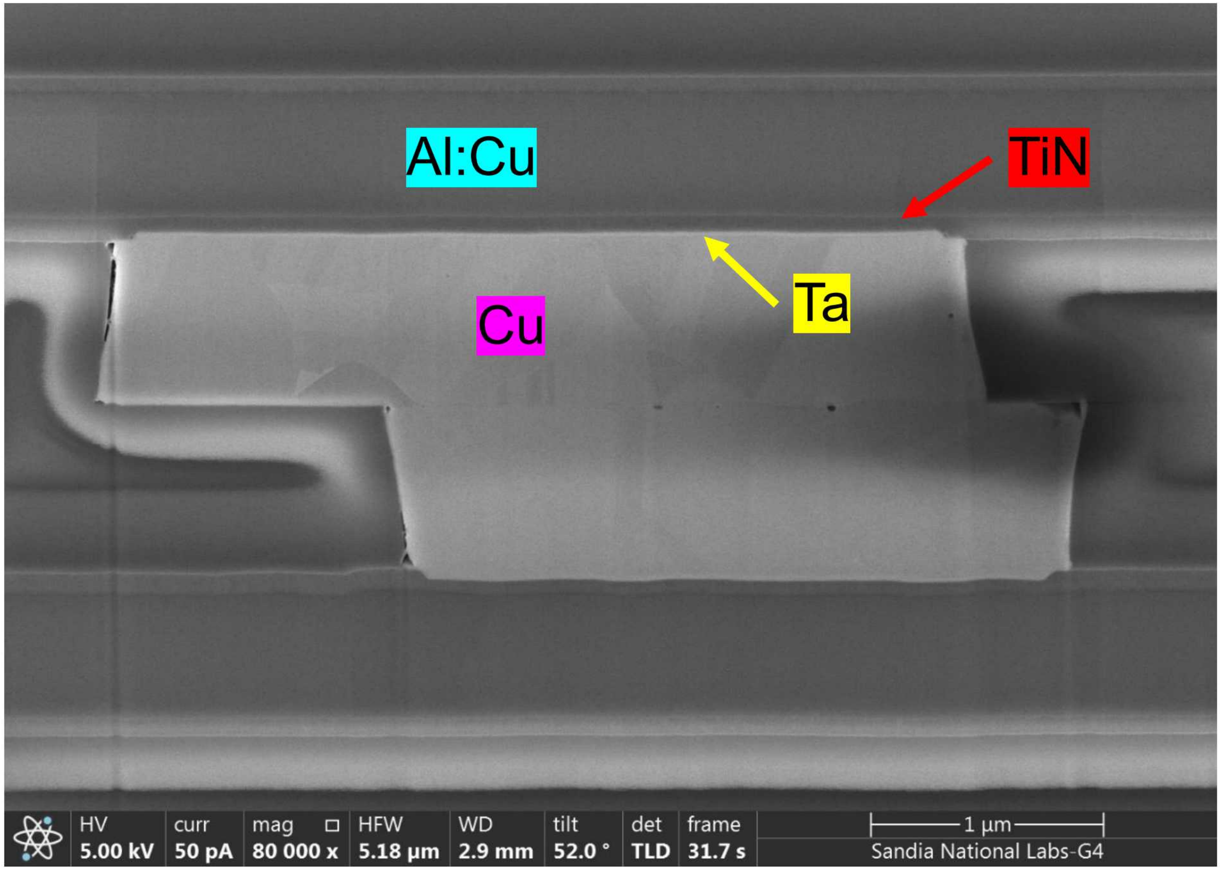
Materials and process flow

- Metal stack:

…

Al:Cu (1wt.%)
TiN (50-100 nm)
Ta (20 nm)
Cu (2 µm)
Ta (20 nm)
TiN (50-100 nm)
Al:Cu (1wt.%)

…



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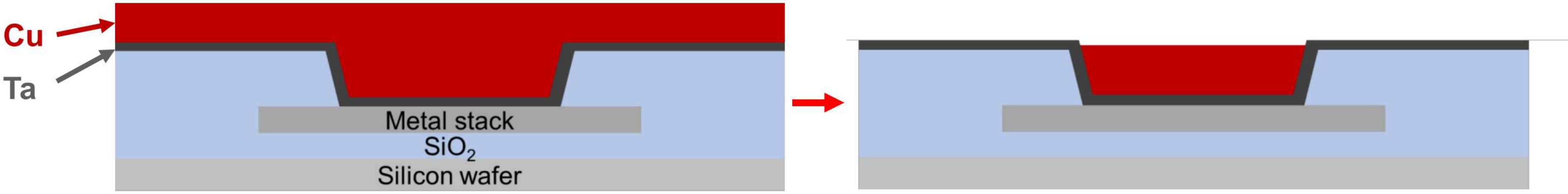
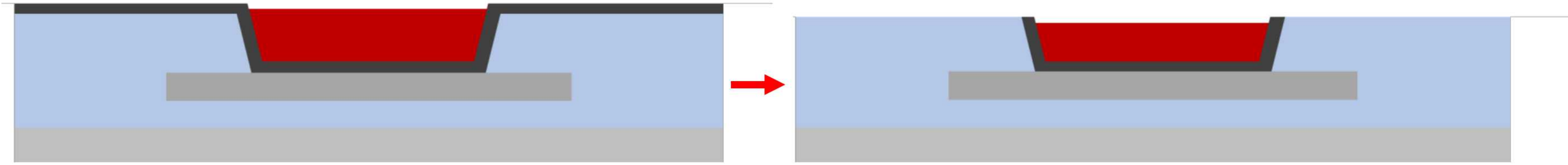
Surface preparation and metrology

- Two-step CMP process:
  - **Step 1**: remove Cu selectively over Ta (Cabot C8900 series slurry)



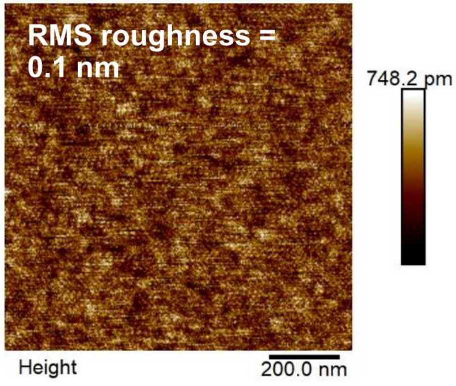
  - **Step 2**: non-selective Ta, Cu removal (Cabot B7000 series slurry)

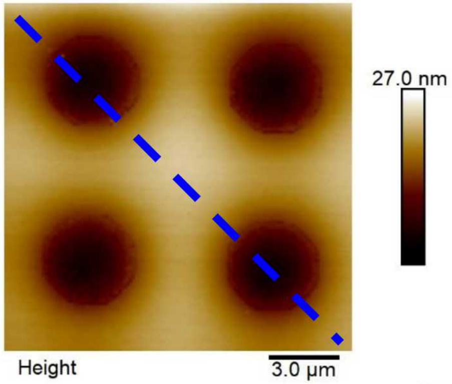


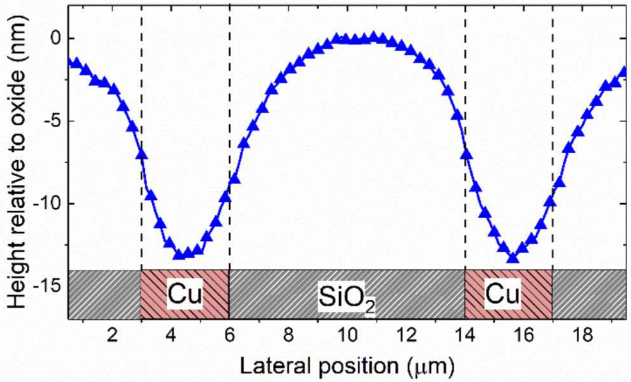
- **Cu recess depth is controlled by over-polish time in Step 1**

Surface preparation and metrology

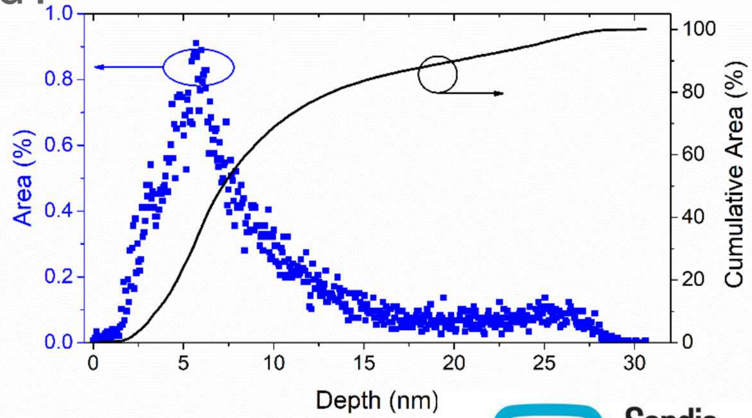
- AFM measurements: SiO_2 roughness and Cu recess depth







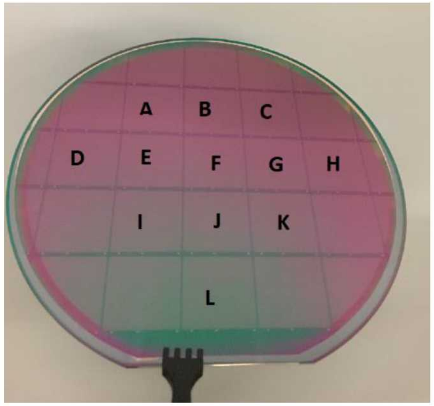
- Range of heights within SiO_2, Cu areas
  - How should Cu recess depth be defined?
  - "Top": crown of SiO_2 surface
  - "Bottom": depth encompassing 99% of the scan area



Surface preparation and metrology

Within-wafer variation

Example wafer:

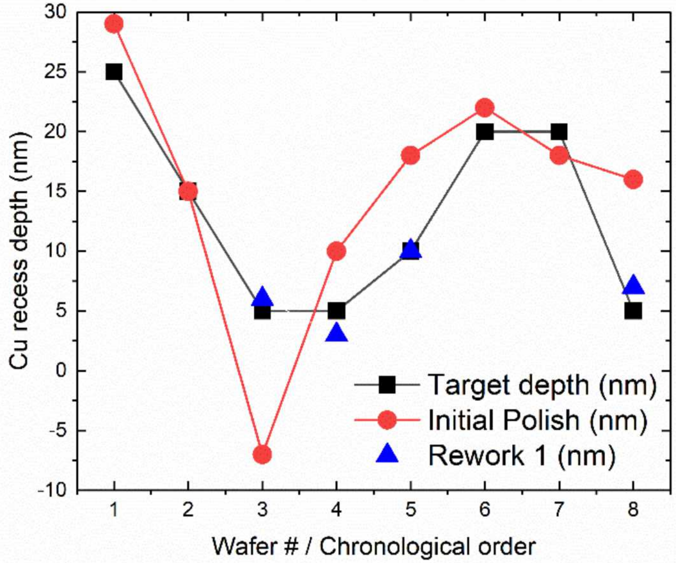


Die	Recess depth (nm)
A	12
B	12
C	13
D	14
E	13
F	13
G	14
H	15
I	13
J	13
K	15
L	13

Mean recess depth = 13.3 nm
Standard deviation = 1.0 nm

Depth targeting

- Create multiple inter-die gap heights by combining die from different parent wafers for multiple depth combinations



- Target depths are achieved with at most 1 rework step

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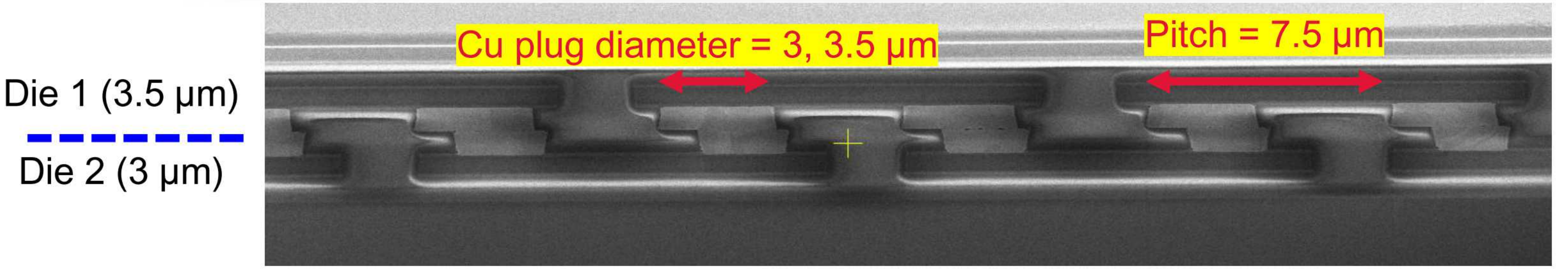
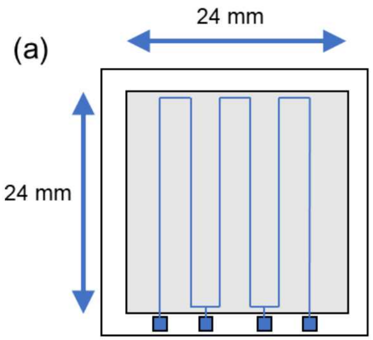
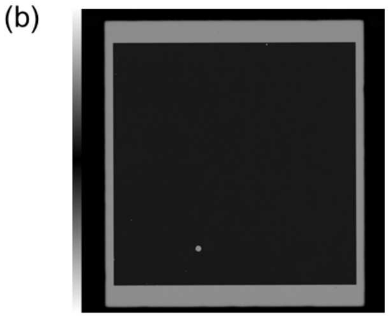
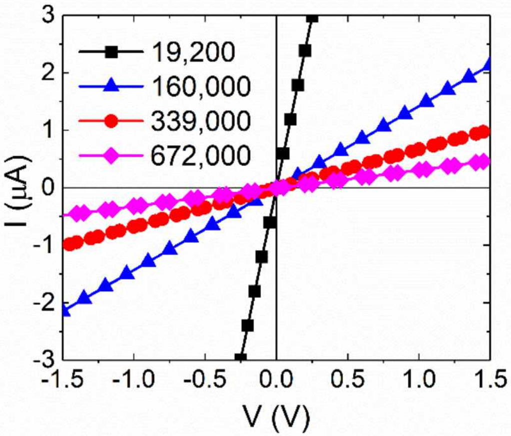
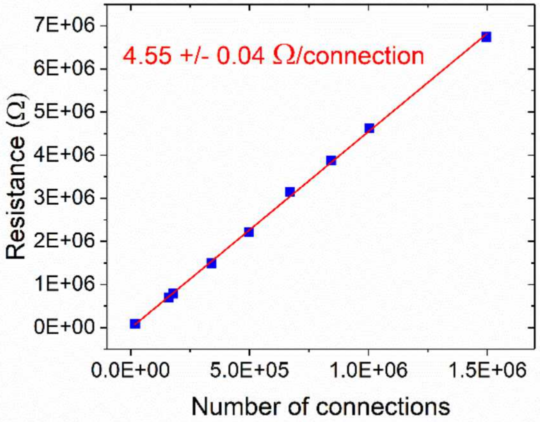
Test vehicle results: single inter-die gap





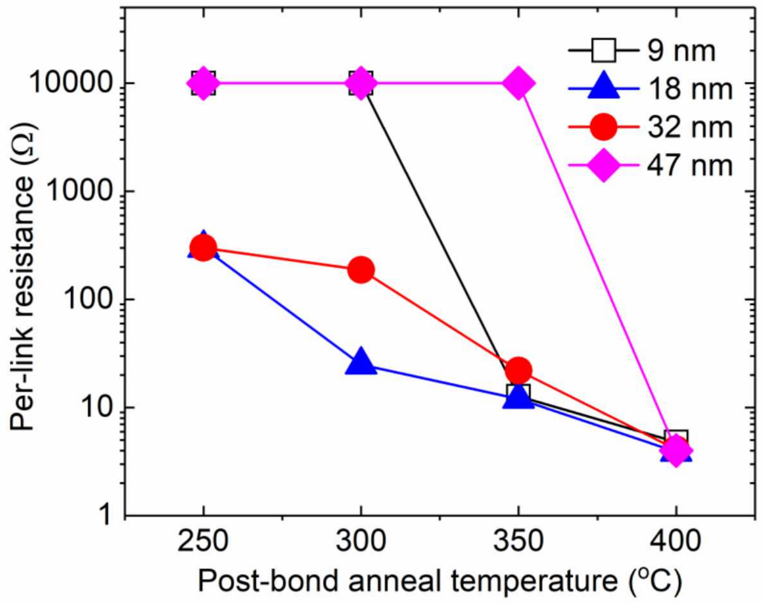






- Daisy chains span the entire ~1-inch die length
- Low bond void density
- Data shown for 9 nm-gap pair after 350 °C anneal
- Successful connections up to ~1.5M links

Test vehicle results: vary gap and temperature



Resistance after 400 ° C anneal	
Inter-die gap (± 2 nm)	Resistance (Ω/connection)
9	4.8 ± 0.2
18	3.9 ± 0.1
32	4.1 ± 0.1
47	4.0 ± 0.1

- General resistance drop is consistent with gap-closing mechanism
- Gap height trend is inconsistent: expect smallest gap to have lower resistance at low temperatures
- Ultimate resistance is consistent across all samples, yet higher than expected

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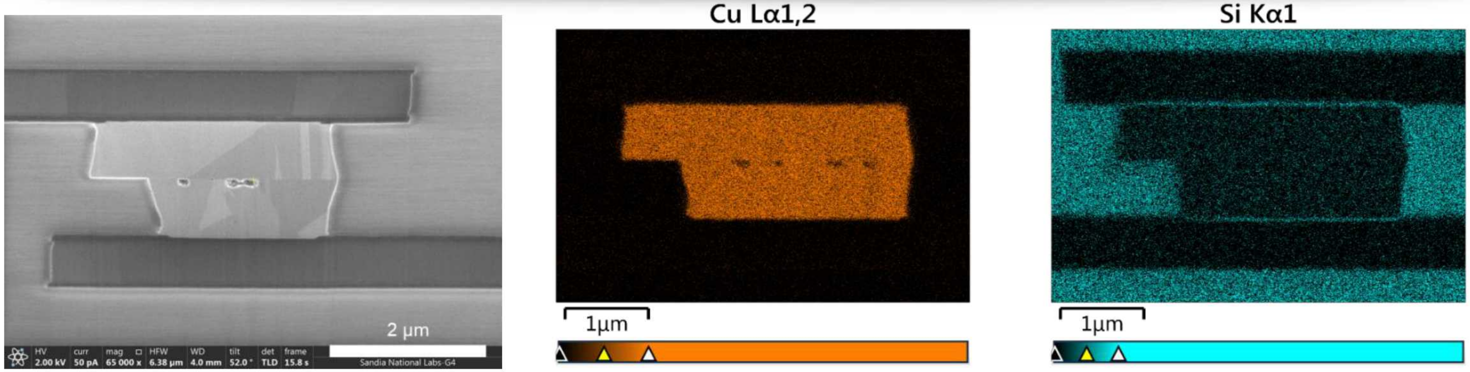
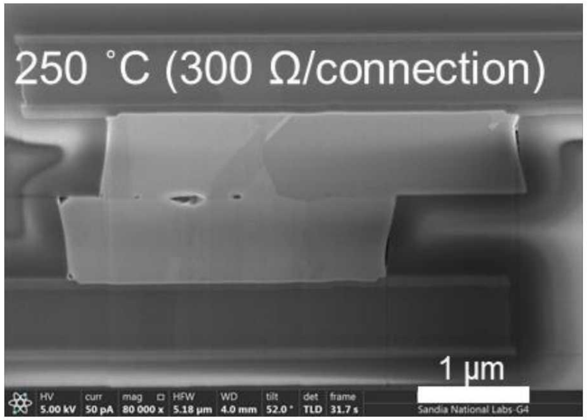
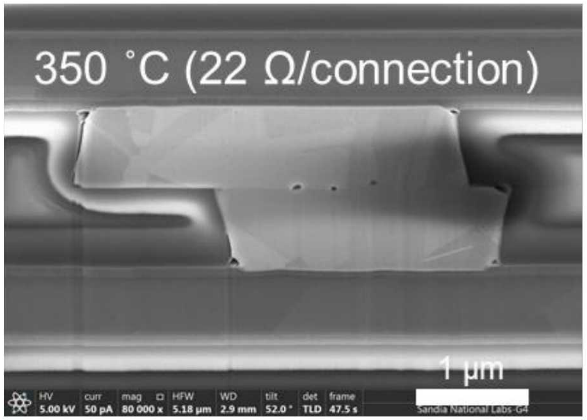
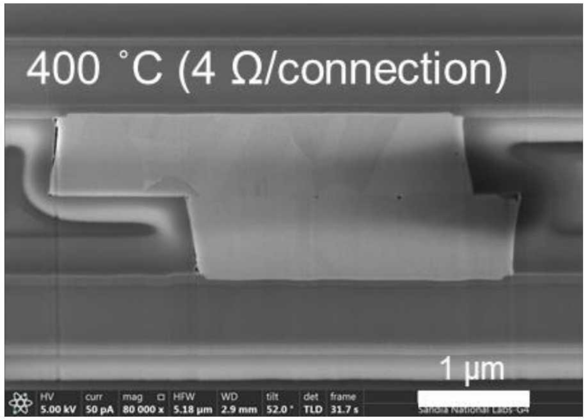
Probing: cross-section SEM



- Some interface voiding, but barrier metals are functional

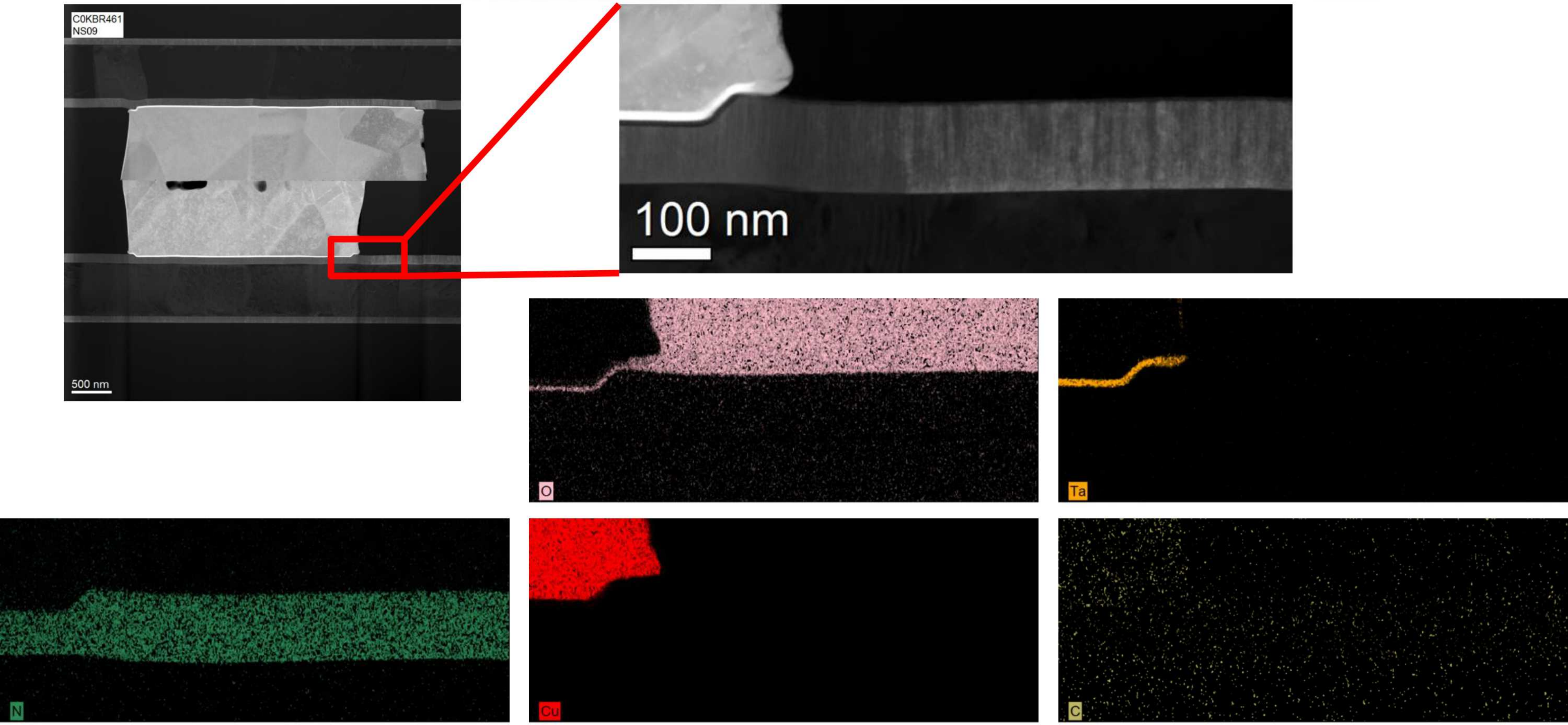






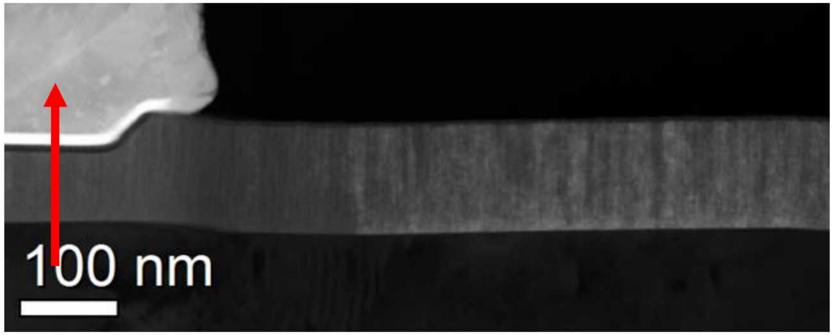
- Temperature evolution: resistance decrease does not correspond to significant microstructural evolution

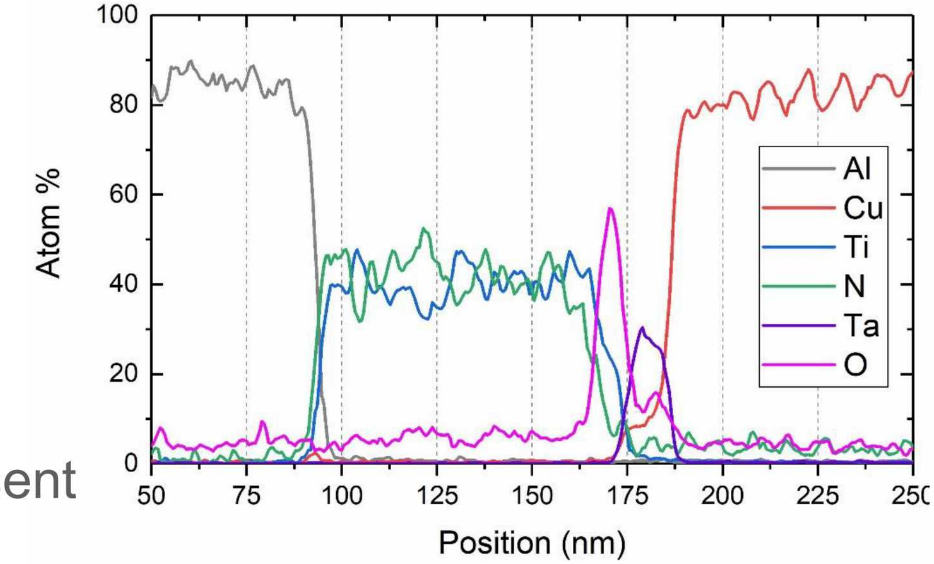
Probing: cross-section TEM



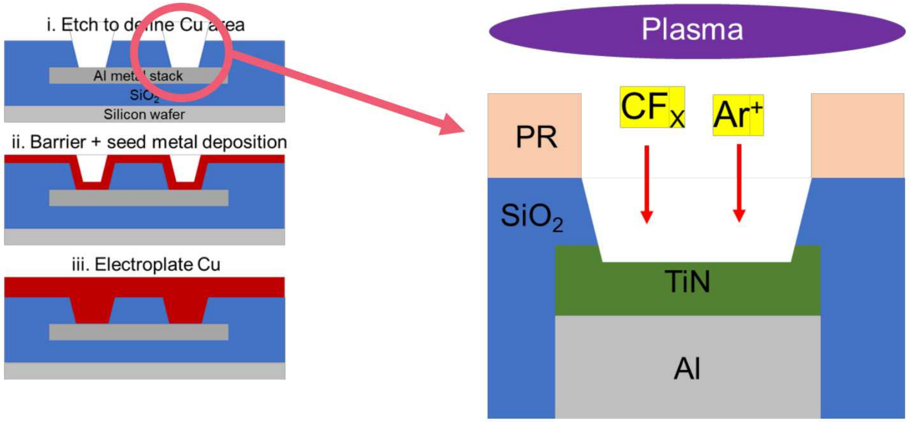
- Thin oxide layer is present between TiN and Ta layers

Probing: TEM-EDS linescan

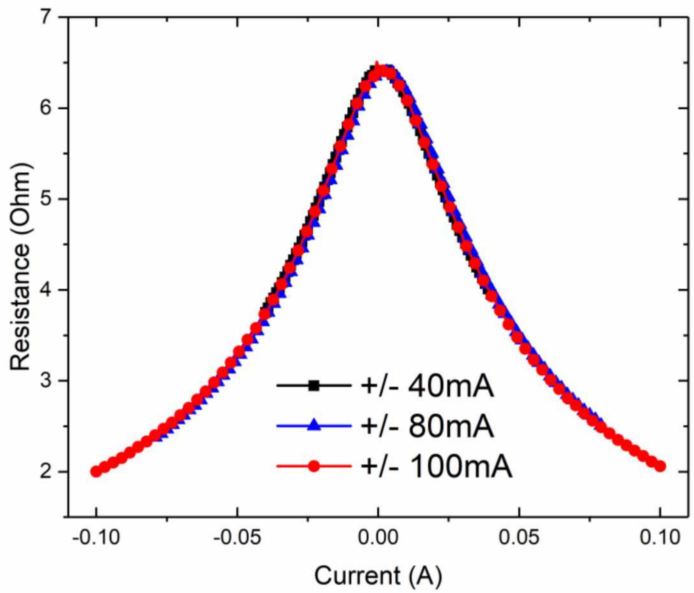


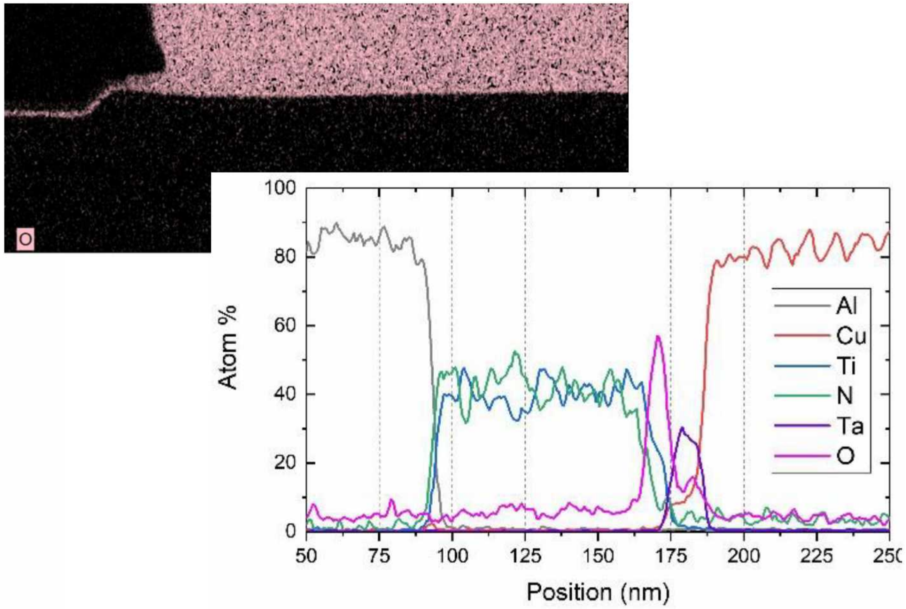


- EDS linescan: thin $TiNO_X$ layer present between TiN and Ta films
- TiN etching during SiO_2/Cu pattern step, followed by air exposure:



Probing: TCR





- Resistance decrease with increasing current indicates a Schottky barrier
- We suggest that this is correlated to the oxidized TiN surface
- Processing that leads to $TiNO_X$ layer was identical for all wafers/die, so similar ultimate resistance is likely limited by this layer

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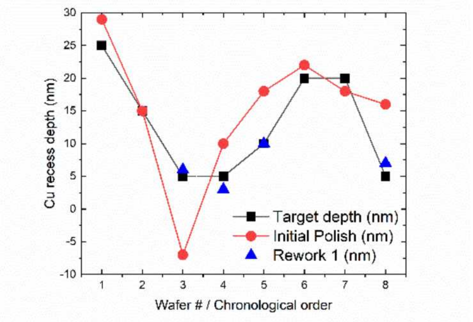
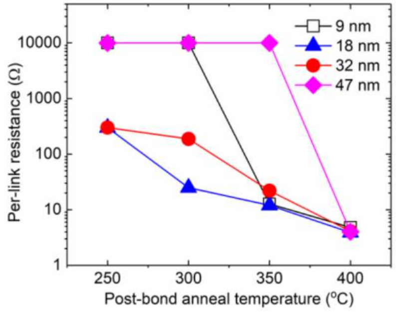
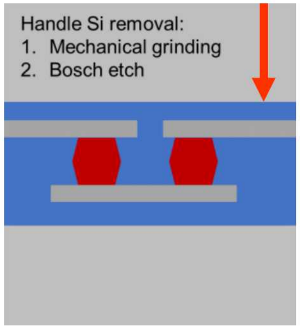
Conclusion

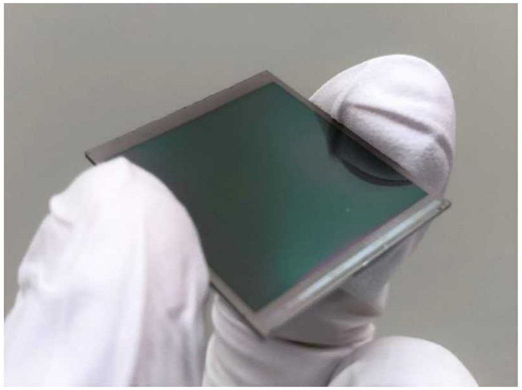
- Demonstrated two-step CMP process that generates bondable surfaces with controlled Cu recess depth
- Inter-die gaps of 9, 18, 32, and 47 nm had similar resistance after annealing at 400 °C
  - Intermediate temperatures had non-straightforward dependence
- Demonstration: bond is resilient to aggressive downstream processing

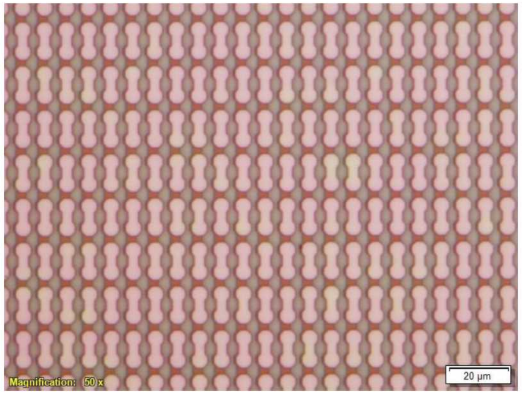






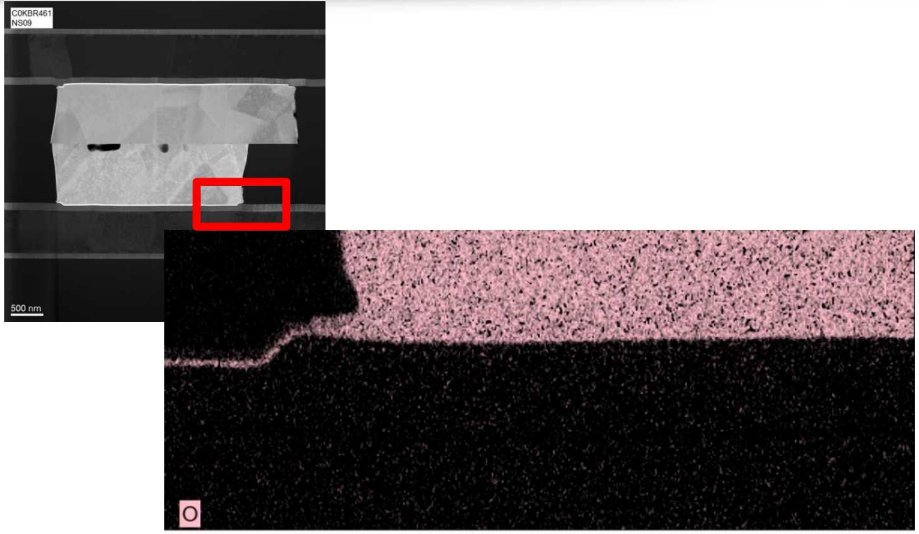
Handle Si removal:
1. Mechanical grinding
2. Bosch etch

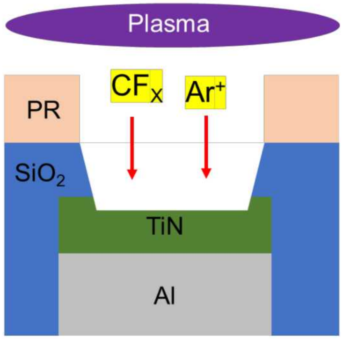


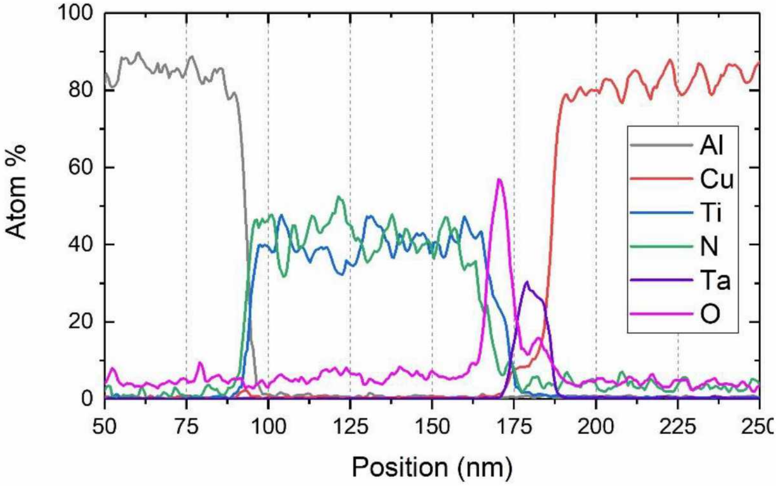


Conclusion and next steps

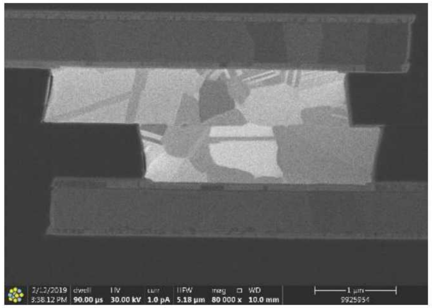
- Failure analysis: insulating $TiNO_X$ layer present between Al routing and Ta barrier likely responsible for high resistance, present across all samples
- Next steps: native TiN oxide removal prior to Ta deposition
  - Wet chemistry with timing spec
  - Preferred: in-situ sputter

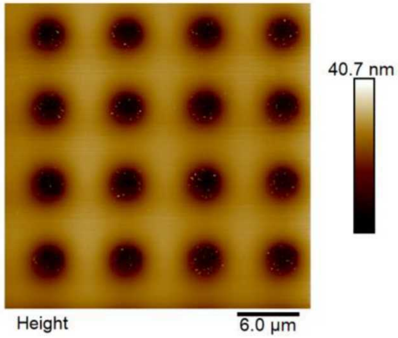


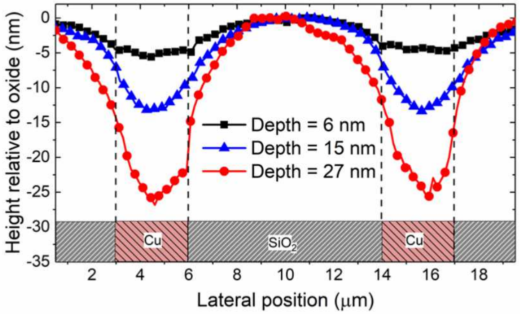




Questions and discussion







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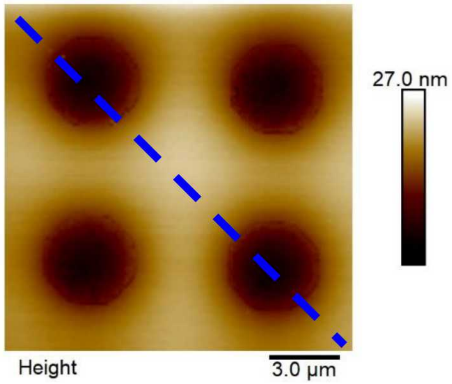
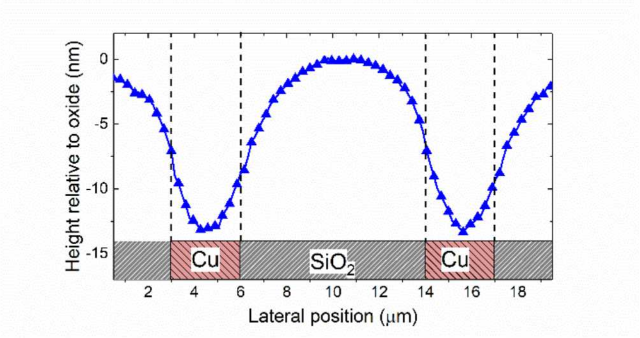
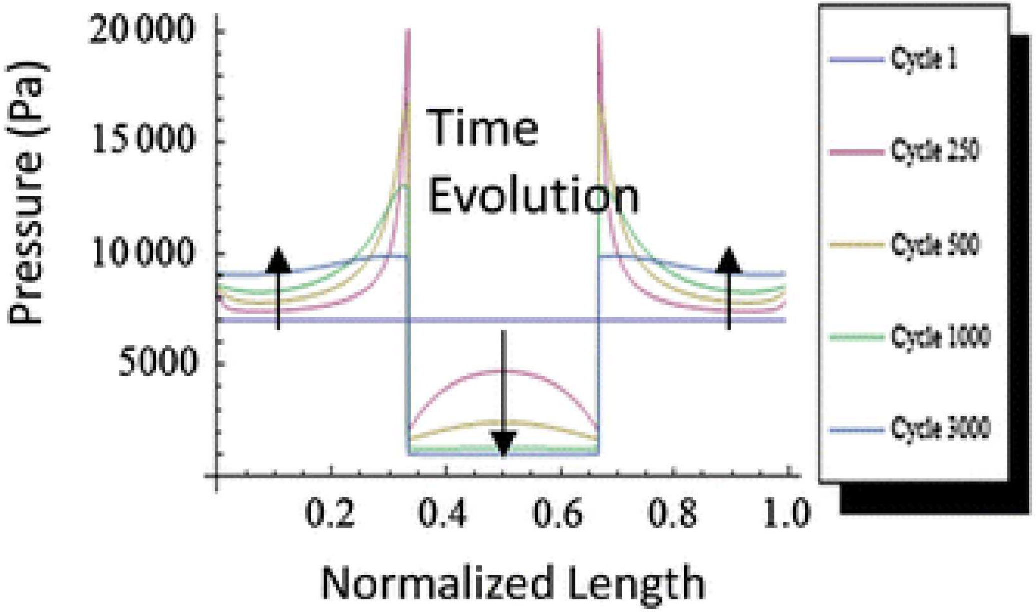
Extra slides

SiO_2 topography mechanism

- Higher local pressure in areas nearest Cu recess

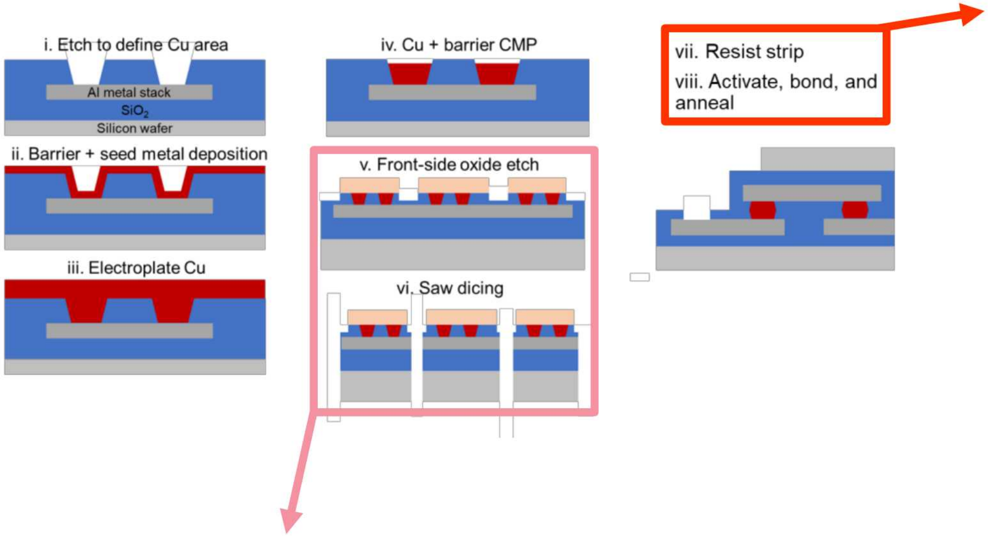




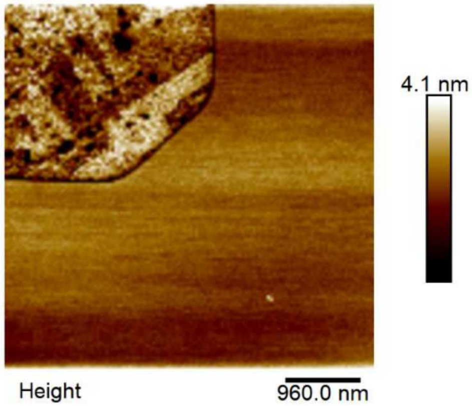


J. A. Sierra Suarez et al. *Trib. Lett.* ***59*** *(2015).*

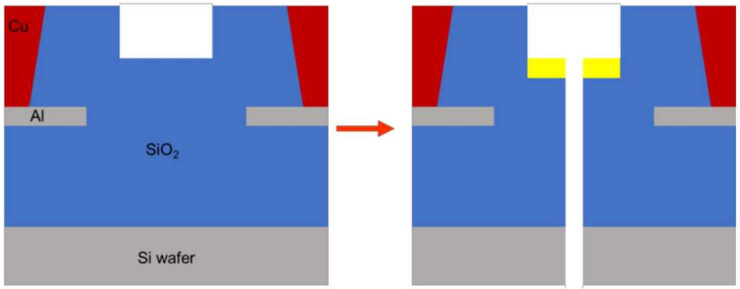
Process flow detail

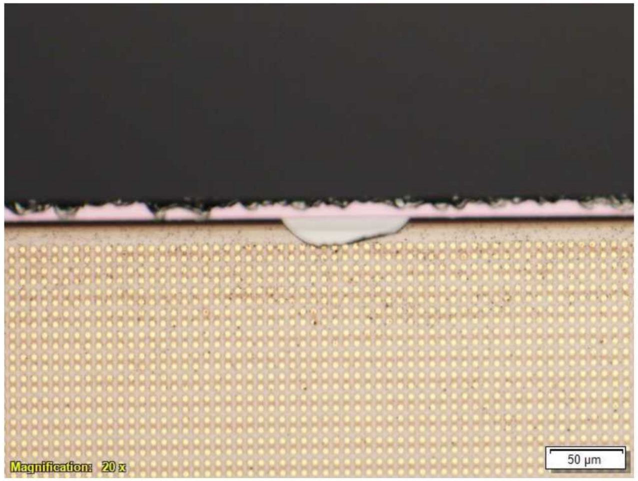


Soft PR bake (125C x 3 min) and gentle strip chemistry (Acetone/IPA) preserves SiO_2 smoothness:

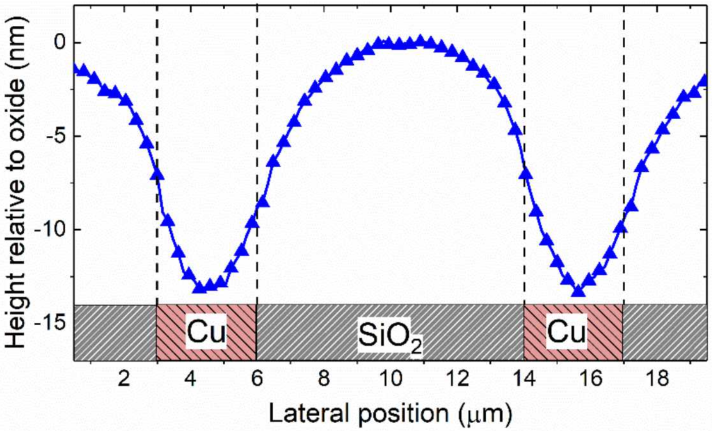


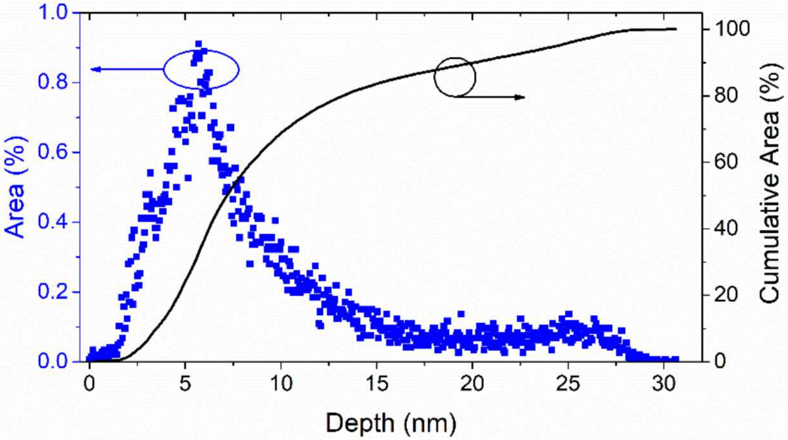
Cracks in SiO_2 are isolated from the bonding surface

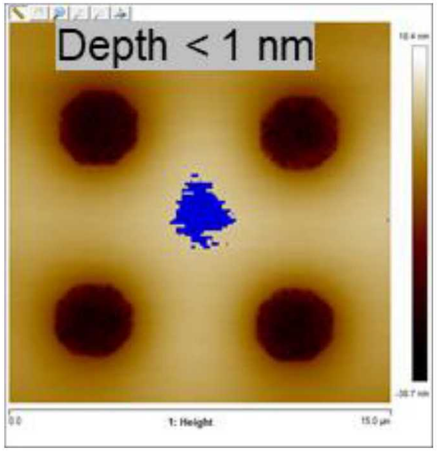


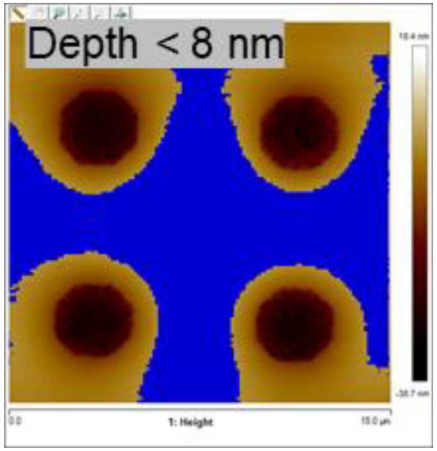


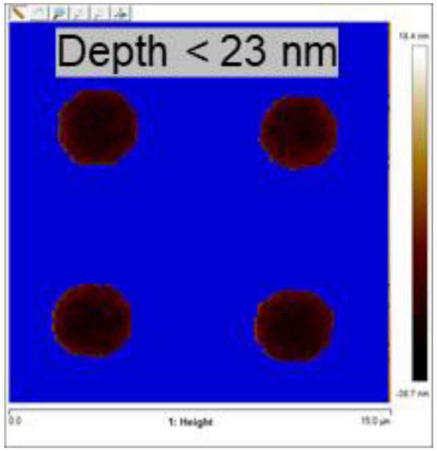
Surface metrology: bearing analysis

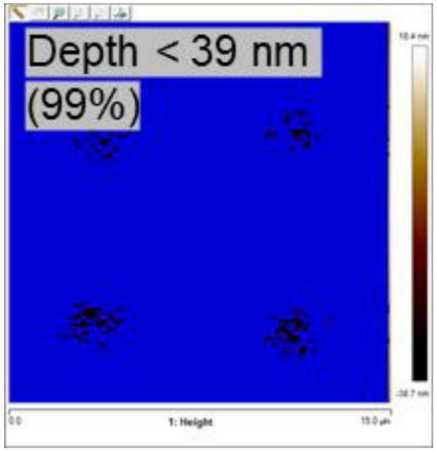




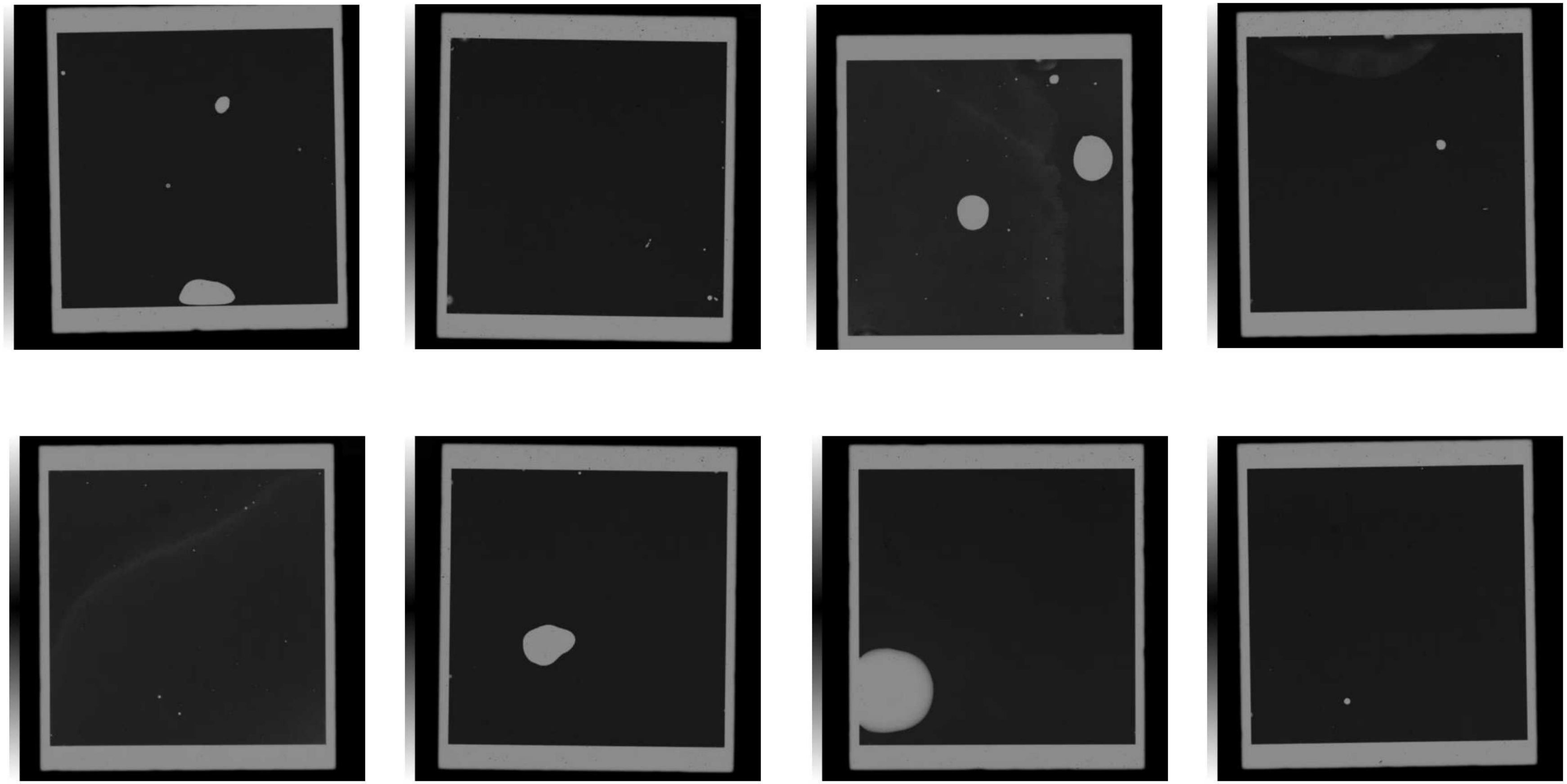






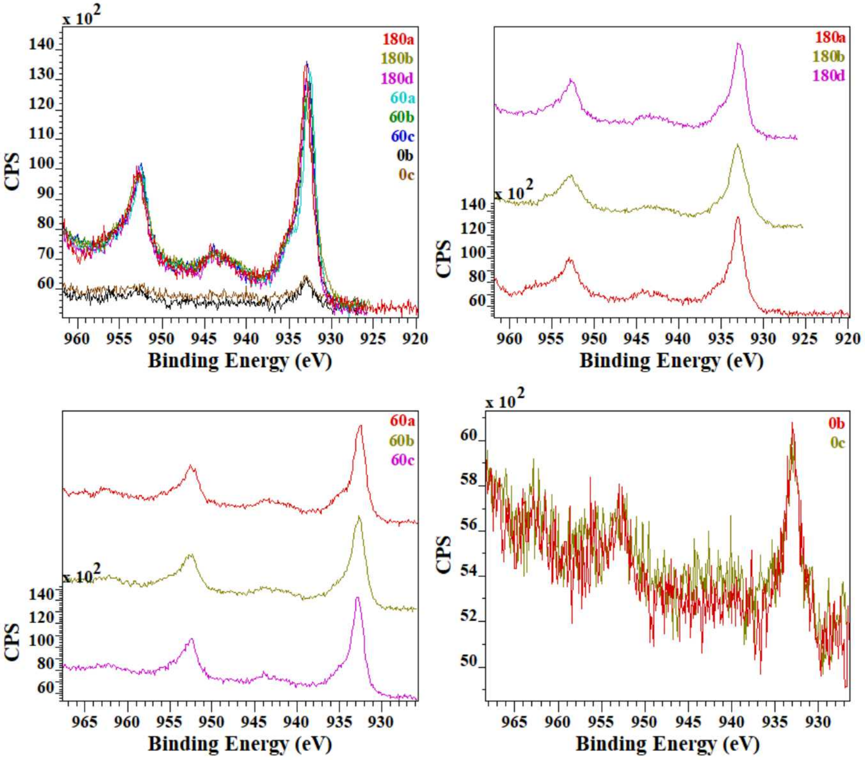


CSAM images

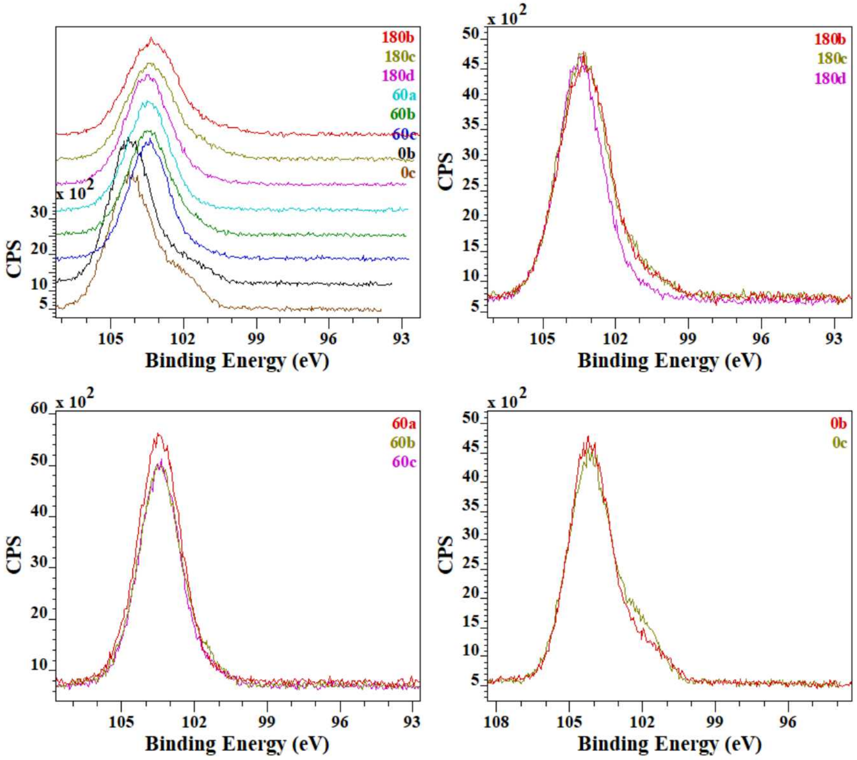


XPS: Cu/SiO$_2$ surface chemistry

Cu 2p



Si 2p



TEM-EDS: Cu/Cu interface