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Formation of Ohmic Contacts to n-GaAs at Temperatures Compatible with Indium Flip-Chip Bonding

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***Abstract*—We demonstrate the formation of low resistivity Pd/Ge/Au ohmic contacts to n-GaAs through long annealing at temperatures as low as 140 °C. This annealing temperature is compatible with flip-chip bonding processes including In bump bonding and epoxy underfill.**

Heterogenous integration of III-V photodetectors with Si readout circuitry is an enabling technology for applications including focal plane arrays [1] and concentrating solar cells [2, 3]. Typical integration schemes include low temperature flip-chip bonding using indium (In) bump bonds, followed by epoxy underfill, and mechanical and/or chemical removal of the III-V substrate to expose the epitaxially grown detector layers [1].

For maximum flexibility in device design and processing, it is desirable to be able to form low resistance illumination-side contacts to either p-type or n-type layers after flip-chip bonding. Formation of non-alloyed contacts to p-GaAs is relatively straightforward and can be readily implemented after flip-chip bonding [4]. Conventional contacts to n-GaAs are formed by evaporation of Ge/Au/Ni followed by a rapid thermal annealing step at 400 °C [4], considerably above the 156 °C melting point of In and above the degradation temperature of many standard underfill epoxies. Several groups have studied the formation of ohmic contacts to n-GaAs through low temperature annealing of Pd/Ge/Au metal stacks [3, 5, 6], however all reports to date have used annealing temperatures near or above the melting point of In.

In this work, we report the formation of ohmic contacts with a specific contact resistivity as low as 5.6×10^{-6} Ω-cm^2 after annealing at a temperature of 140 °C, significantly below the In melting point. Figures 1 and 2 show experimental results of transfer line method (TLM) test structures measured on an epitaxially grown 800 nm thick, $1x10^{18}$ cm^{-3} n-GaAs layer with 7 nm Pd/ 50 nm Ge/ 200 nm Au contacts patterned with photolithography and evaporation. The samples were annealed in an oven with a N_2 ambient and measured repeatedly throughout the annealing process. We observe a transition from Schottky to ohmic behavior after 10 hours of annealing followed by a steady decrease in resistance for annealing times out to 48 hours. A companion sample that had been flip-chip bonded with In bumps and underfilled with Epotek 301 epoxy showed no degradation after annealing. The black line in Fig. 1 is provided as a reference of the measured specific contact resistivity of a standard Ge/Au/Ni/Au metal stack deposited on the same n-GaAs layer after a 30 second, 400 °C anneal.

The creation of low-resistance ohmic contacts to n-GaAs at this low temperature is an enabling technology for III-V heterogeneous integration efforts with a wide array of temperature-sensitive materials such as In, epoxies, photoresists, and plastics.

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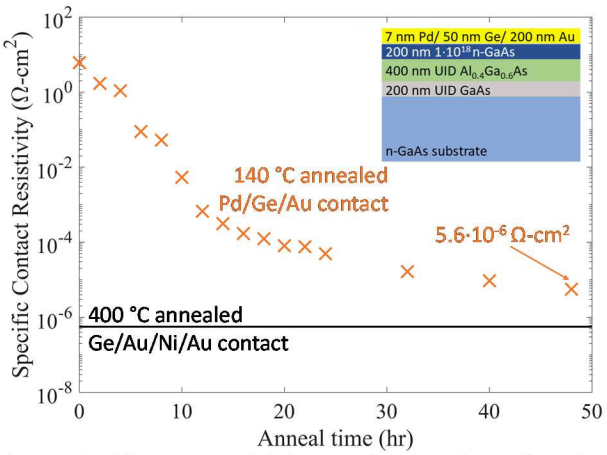

Fig. 1. Specific contact resistivity as a function of annealing time. The material stack is provided in the inset.

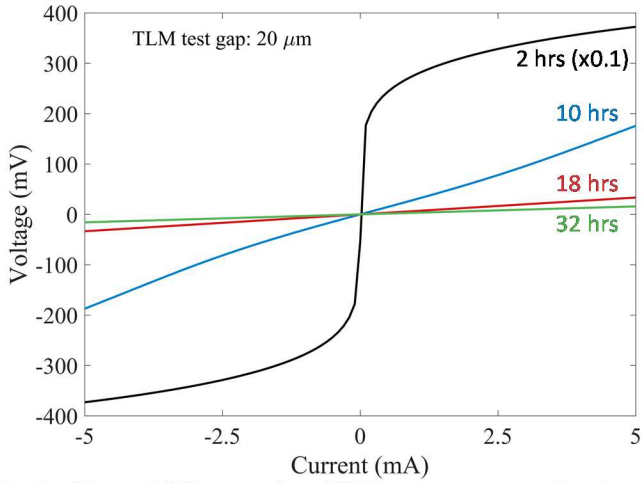

Fig. 2. Measured I-V curves from TLM test structure as a function of annealing time at 140 °C.