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Formation of Si Nanowires and Quantum Dots via Ge Diffusion During Oxidation of Si/SiGe Heterostructures

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Sandia National Laboratories

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SWAMP Research Group

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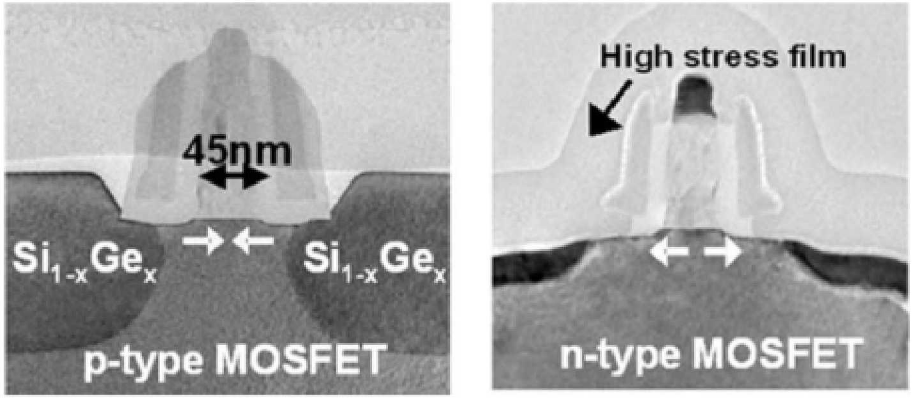
Outline

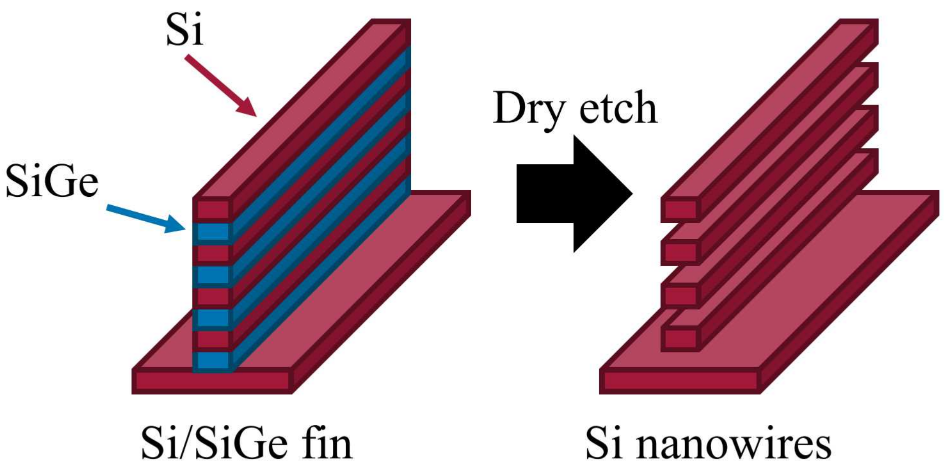
- Introduction
  - *Si and SiGe materials system*
  - *Enhanced diffusion of Ge along Si/SiO_2 interface*
- Oxidation of Si/SiGe pillar structures
  - *Characterization challenges*
  - *Si QD formation after oxidation*
- Conclusions

Si and SiGe materials system

- Scaling limits to Si planar transistors
- SiGe has gained interest for transistor and nanowire fabrication
- Desire to fabricate 0-D structures
  - Quantum computing
  - Challenges in scalable fabrication
- SiGe and Si interactions must be well understood
  - Oxidation of Si and SiGe
  - Diffusion in Si/SiGe materials system



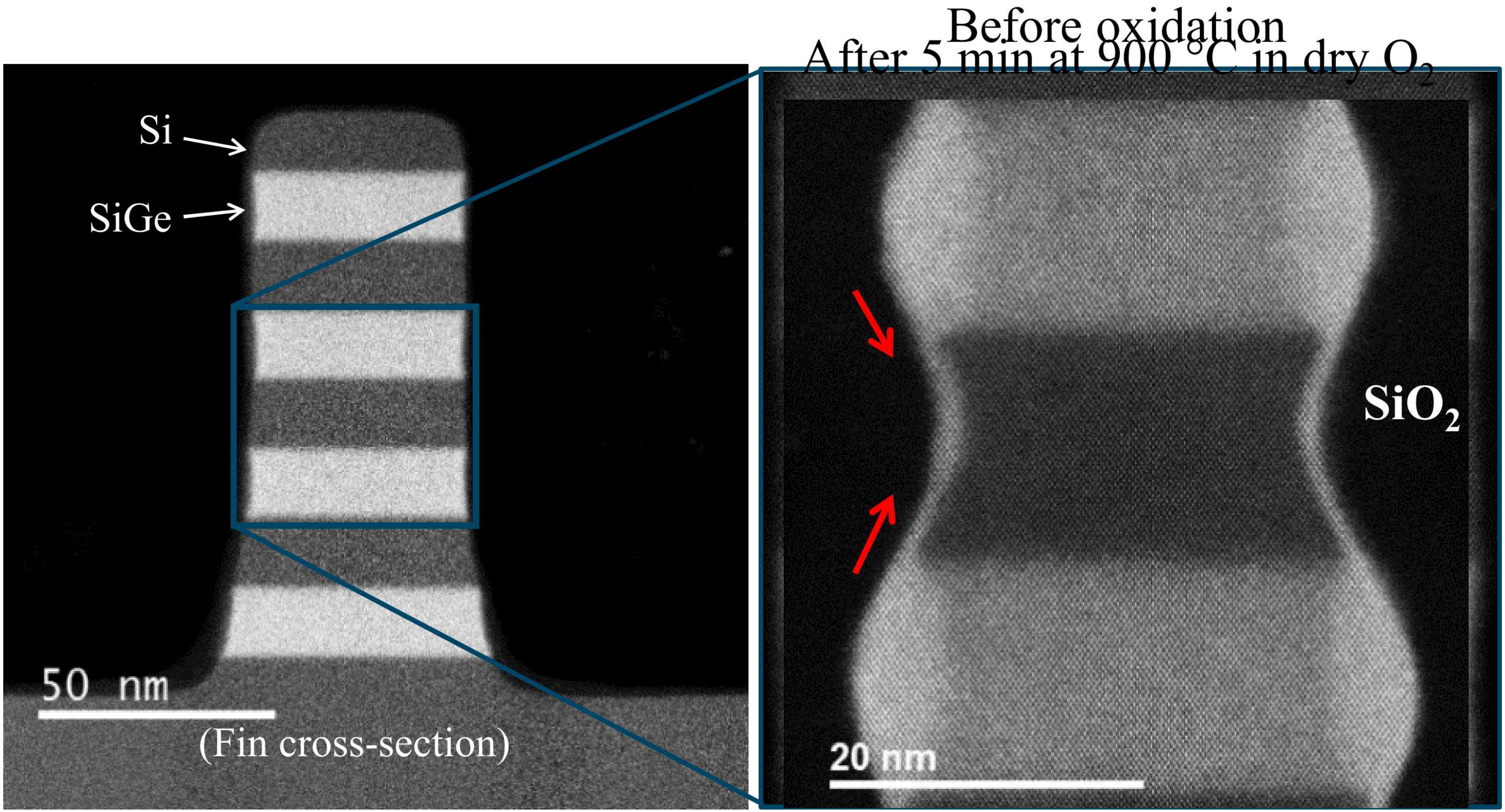
Cross-sectional TEM images of 45 nm p-type and n-type MOSFET. White arrows indicate compressively strained p-type channel (left).



Thompson, S. E. *et al.* A logic nanotechnology featuring strained-silicon. *IEEE Electron Device Lett.* **25,** 191–193 (2004).

Figure courtesy of Will Brewer

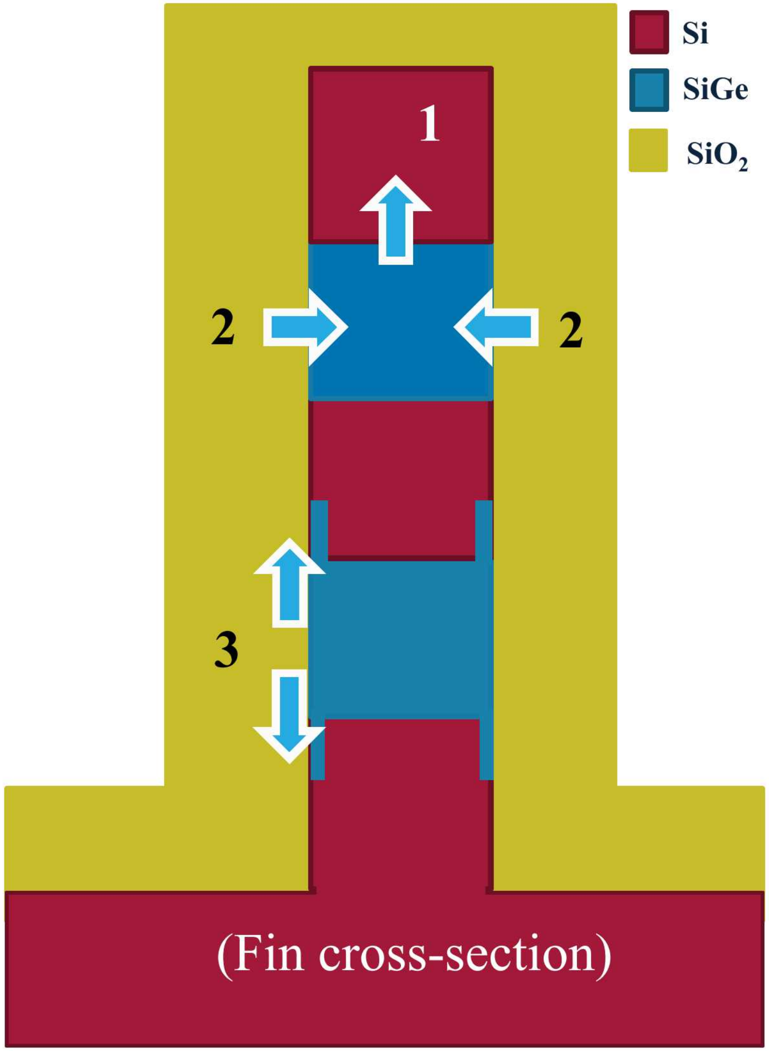
Enhanced diffusion of Ge along Si/SiO_2 interface



Brewer, W. M. *et al.* Lateral Ge Diffusion During Oxidation of Si/SiGe Fins. *Nano Lett.* **17,** 2159–2164 (2017).

Competing Ge diffusion mechanisms

- Diffusion of SiGe/Si structures
  1. Diffusion of Ge into bulk Si
  2. Segregation of Ge during bulk SiGe oxidation
  3. Enhanced diffusion of Ge along Si/SiO_2 interface



Competing Ge diffusion mechanisms

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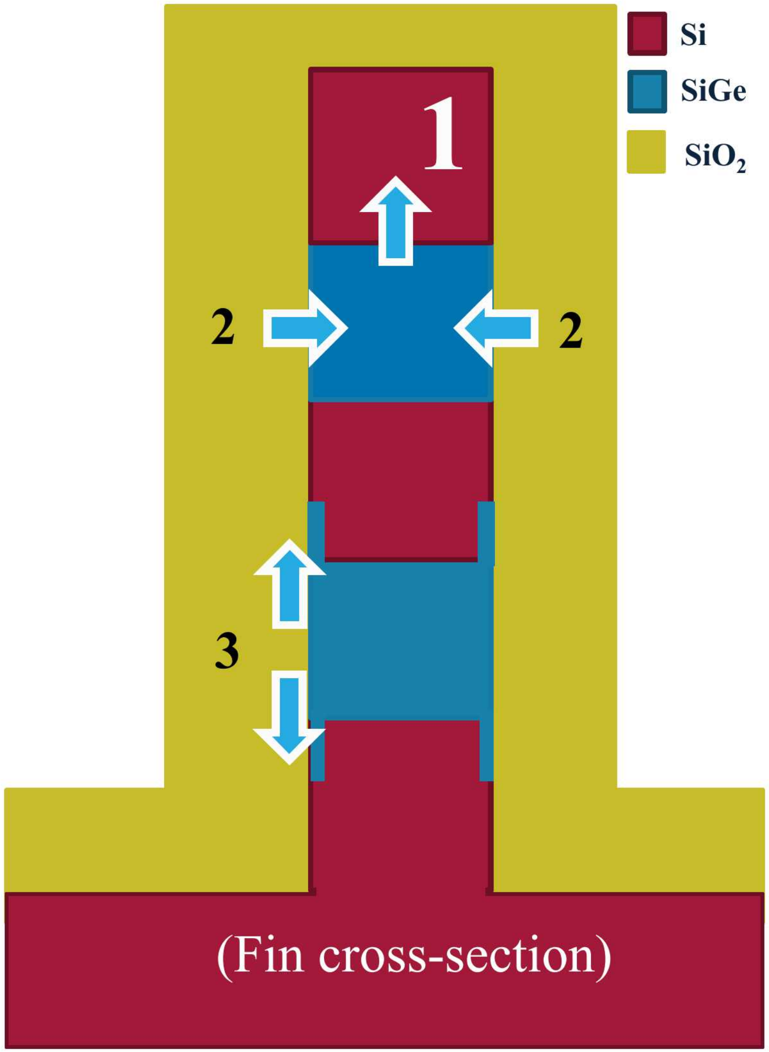

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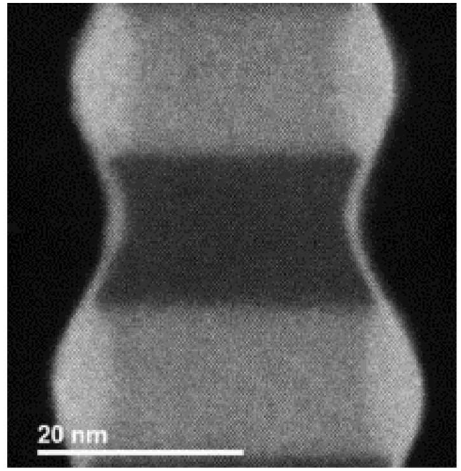
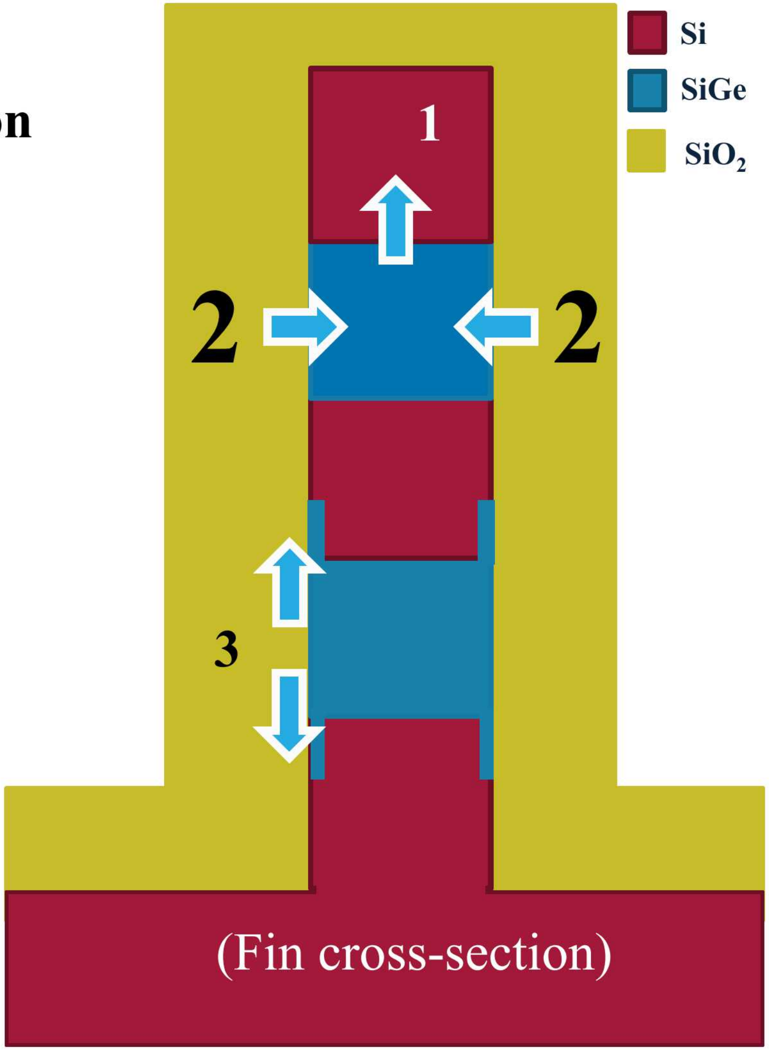
Competing Ge diffusion mechanisms

- Diffusion of SiGe/Si structures
  1. Diffusion of Ge into bulk Si
  2. **Segregation of Ge during bulk SiGe oxidation**
  3. Enhanced diffusion of Ge along Si/SiO_2 interface
- Bulk diffusion of Ge in Si
- SiGe oxidation and subsequent Ge rejection

After 5 min at 900 °C in dry O_2

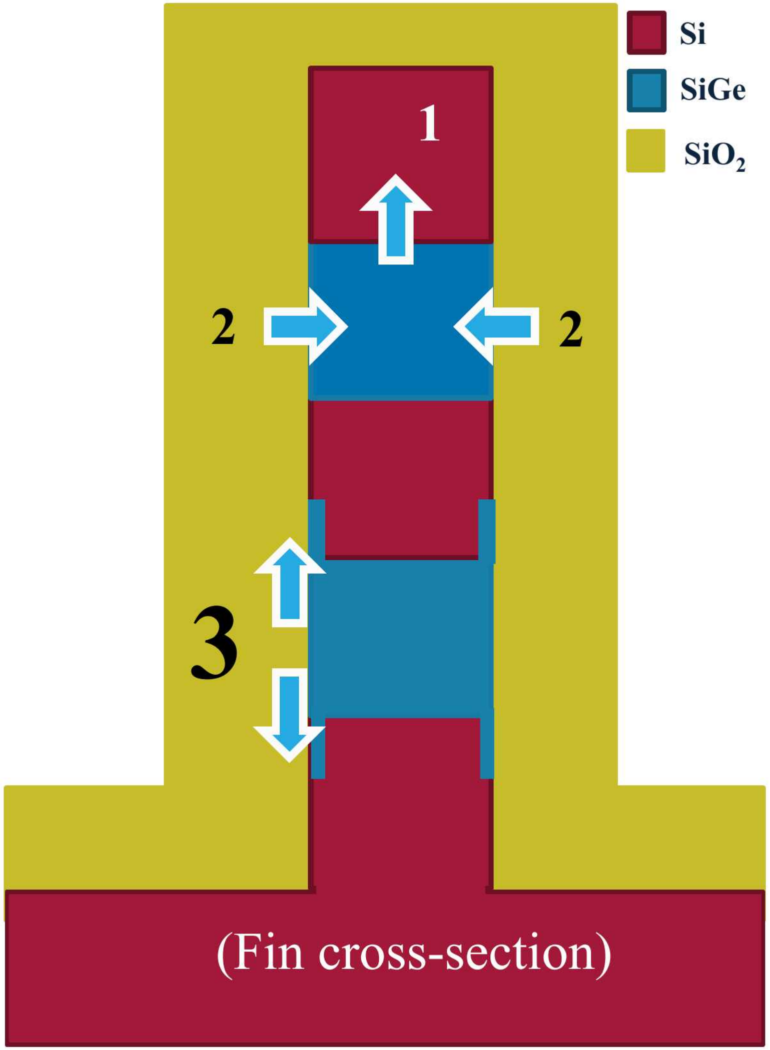




Margalit, S., Bar-Lev, A., Kuper, A. B., Aharoni, H. & Neugroschel, A. Oxidation of silicon-germanium alloys. *J. Cryst. Growth* **17,** 288–297 (1972).

Competing Ge diffusion mechanisms

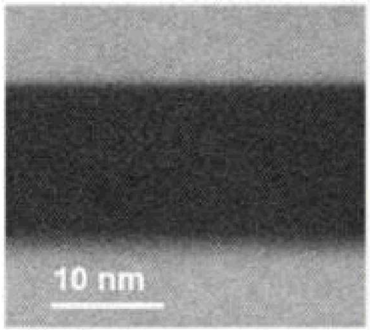
- Diffusion of SiGe/Si structures
  1. Diffusion of Ge into bulk Si
  2. Segregation of Ge during bulk SiGe oxidation
  3. **Enhanced diffusion of Ge along Si/SiO_2 interface**
- Bulk diffusion of Ge in Si
- SiGe oxidation and subsequent Ge rejection
- During high temperature oxidation, Ge rapidly diffuses along Si/SiO_2 interface
  - Newly formed SiGe layer pseudomorphic, remains single crystal
  - Possible new fabrication method!



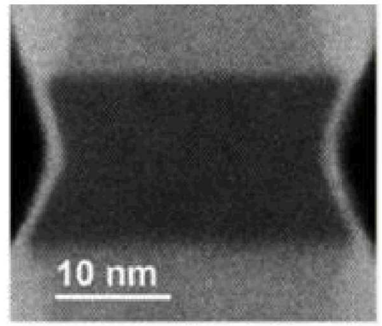
Brewer, W. M. *et al.* Lateral Ge Diffusion During Oxidation of Si/SiGe Fins. *Nano Lett.* **17,** 2159–2164 (2017).

Si nanowire formation during 900 ˚C oxidizing anneal

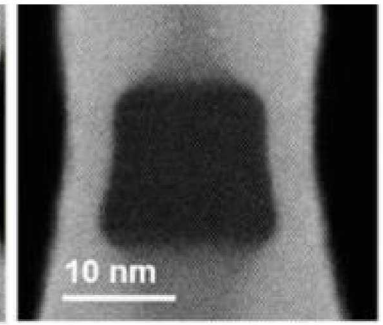
- Fin cross section during oxidation at 900 ˚C in O_2



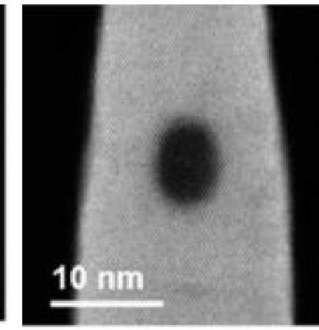
Before oxidation



5 minutes

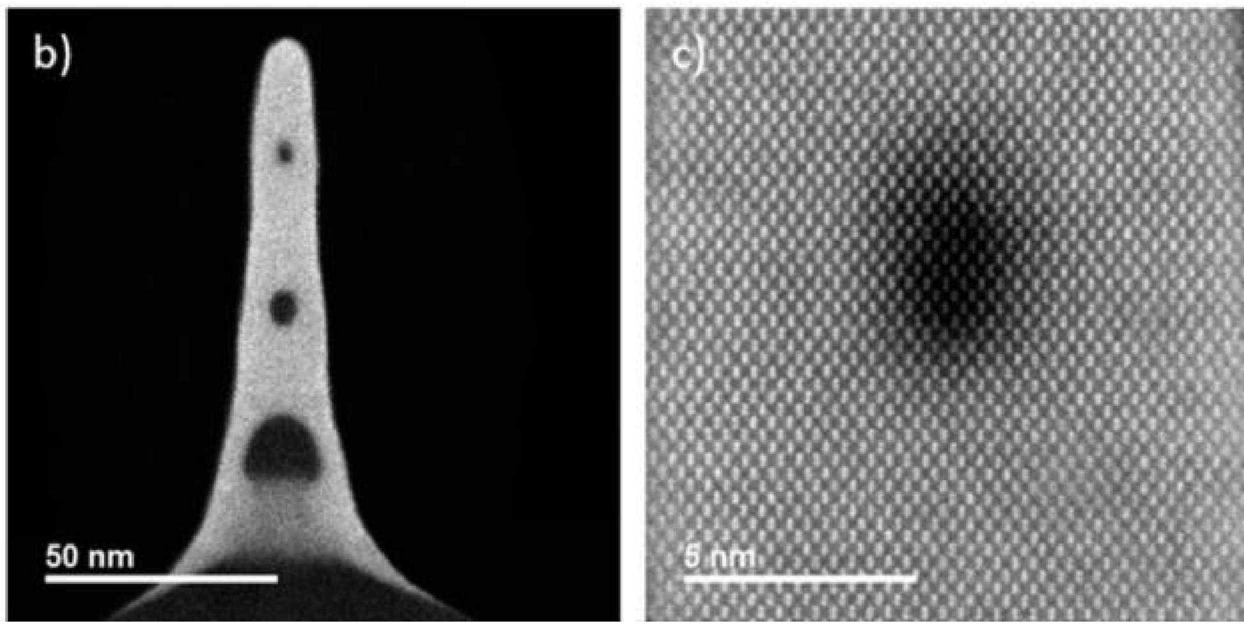


20 minutes



45 minutes

- Unexpected formation of lateral Si nanowires down to 2 nm in diameter!

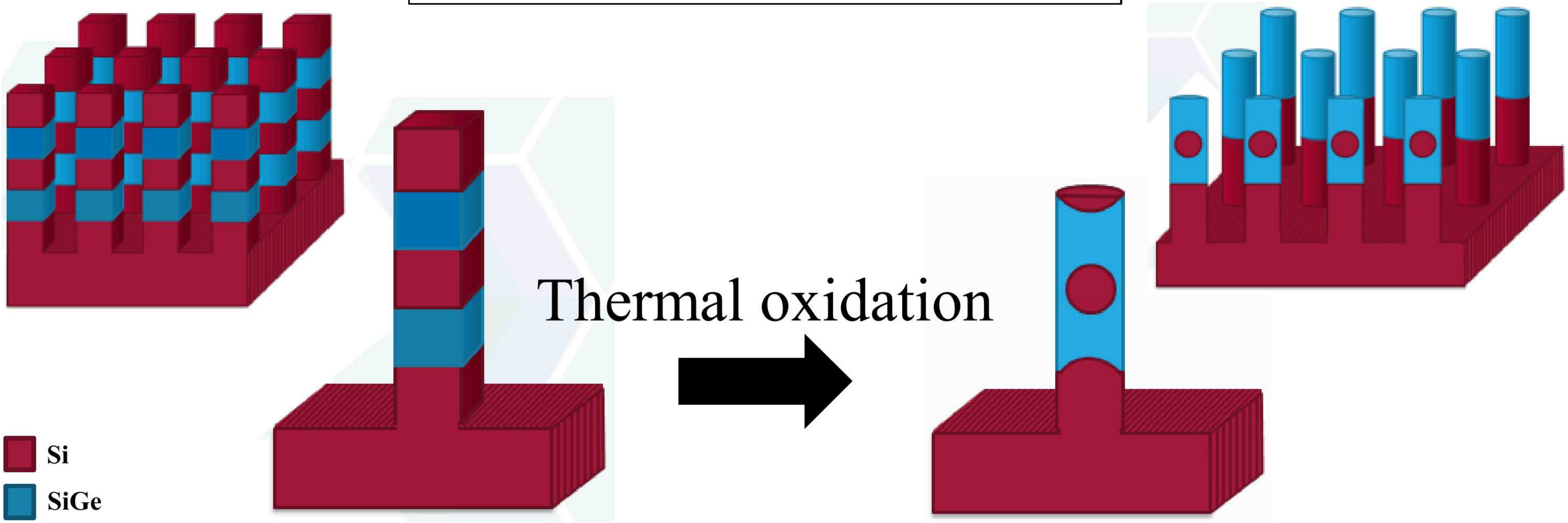


Brewer, W. M. *et al.* Lateral Ge Diffusion During Oxidation of Si/SiGe Fins. *Nano Lett.* **17,** 2159–2164 (2017).

Enhanced Ge diffusion for novel fabrication method

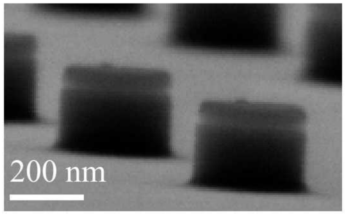
- Need scalable methods for on-chip Si nanostructures with dimensions <10nm
- Can we extend the use of this enhanced Ge diffusion process to create 0D structures (quantum dots)?

Next step: Si/SiGe pillars



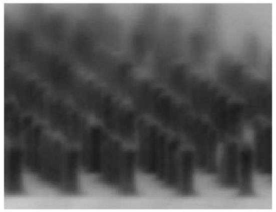
Vertical Si/SiGe pillars

- Fabricate pillars via e-beam lithography and plasma etch
- Oxidize pillars at 900 C in dry O2 for a range of times
- Characterize using cross sectional S/TEM
- Focused ion beam sample preparation
    1. Protect lamella area from ion beam damage
    2. Remove lamella by milling out two trenches, attaching slice to omniprobe
    3. Attach lamella to TEM grid and thin until electron transparent (<150nm)



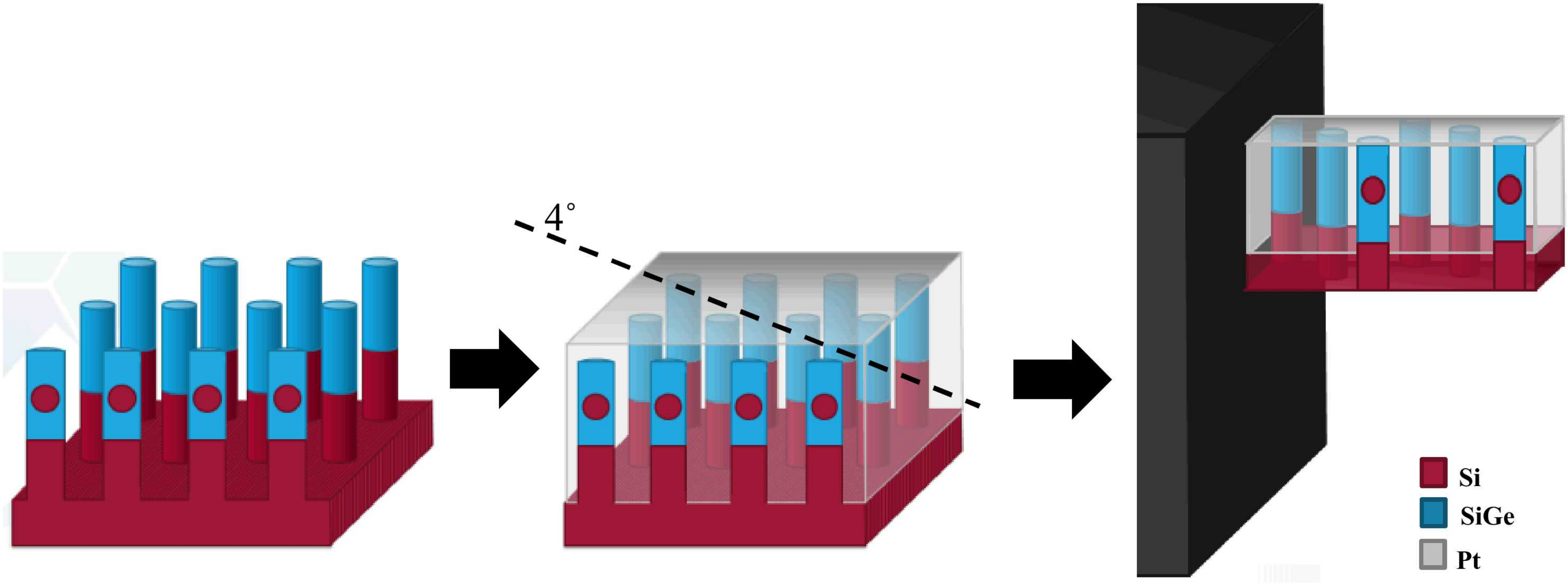
167 nm diameter

100 nm diameter



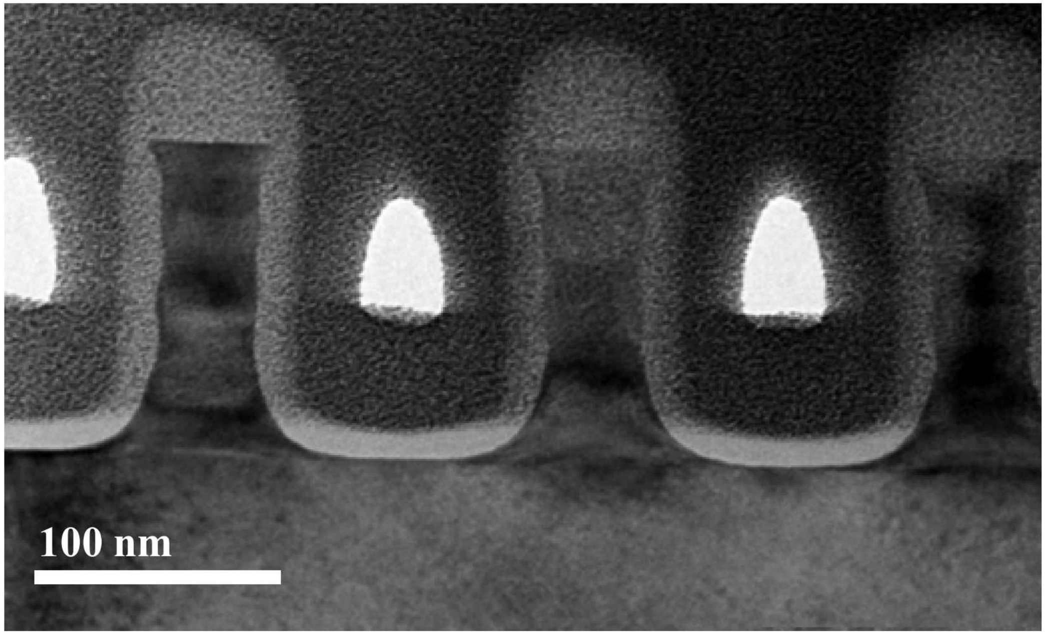
37 nm diameter

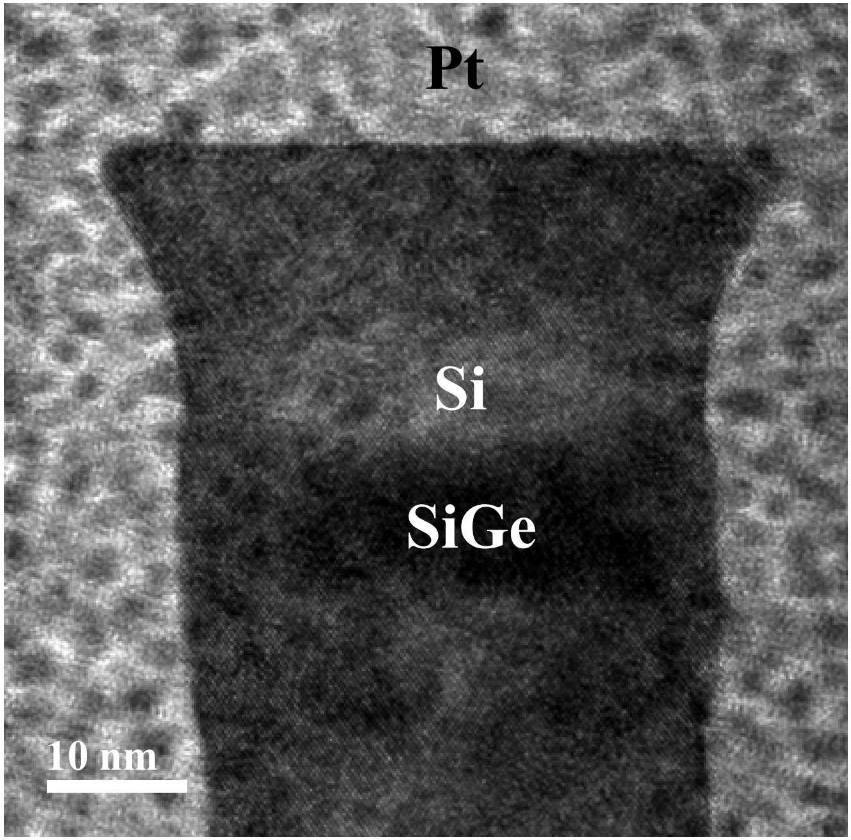
Typical FIB process for XTEM



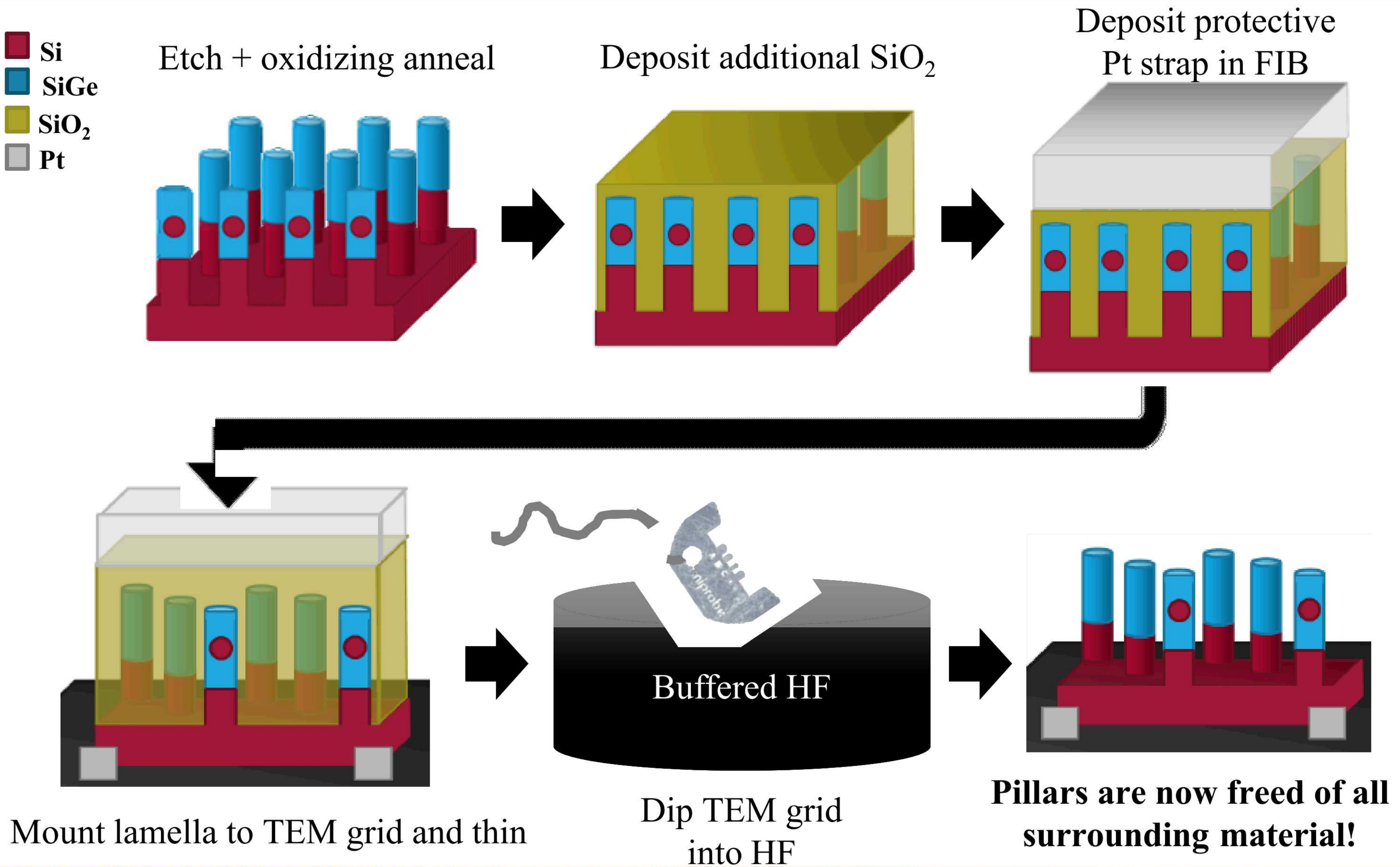
HR TEM images of Si/SiGe pillars

- Cross section of 37nm pillars after a 5 minute anneal at 900 ˚C in O_2
- Platinum protective layer added in FIB obscures Si/SiGe pillar



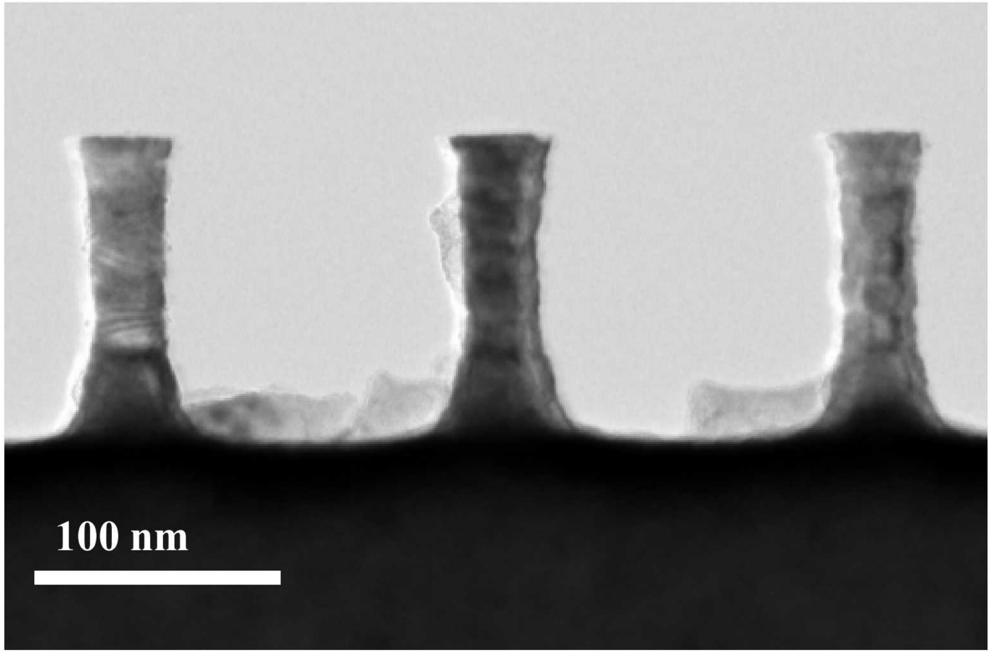


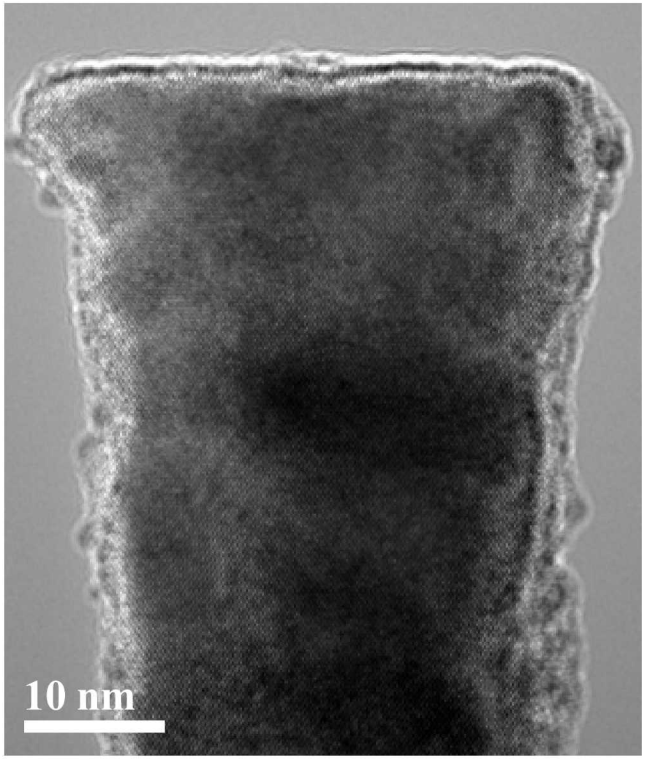
Etch-release method for XTEM



TEM of Si/SiGe pillars after HF dip

- Cross section of 37nm pillars after a 5 minute anneal at 900 ˚C in O_2

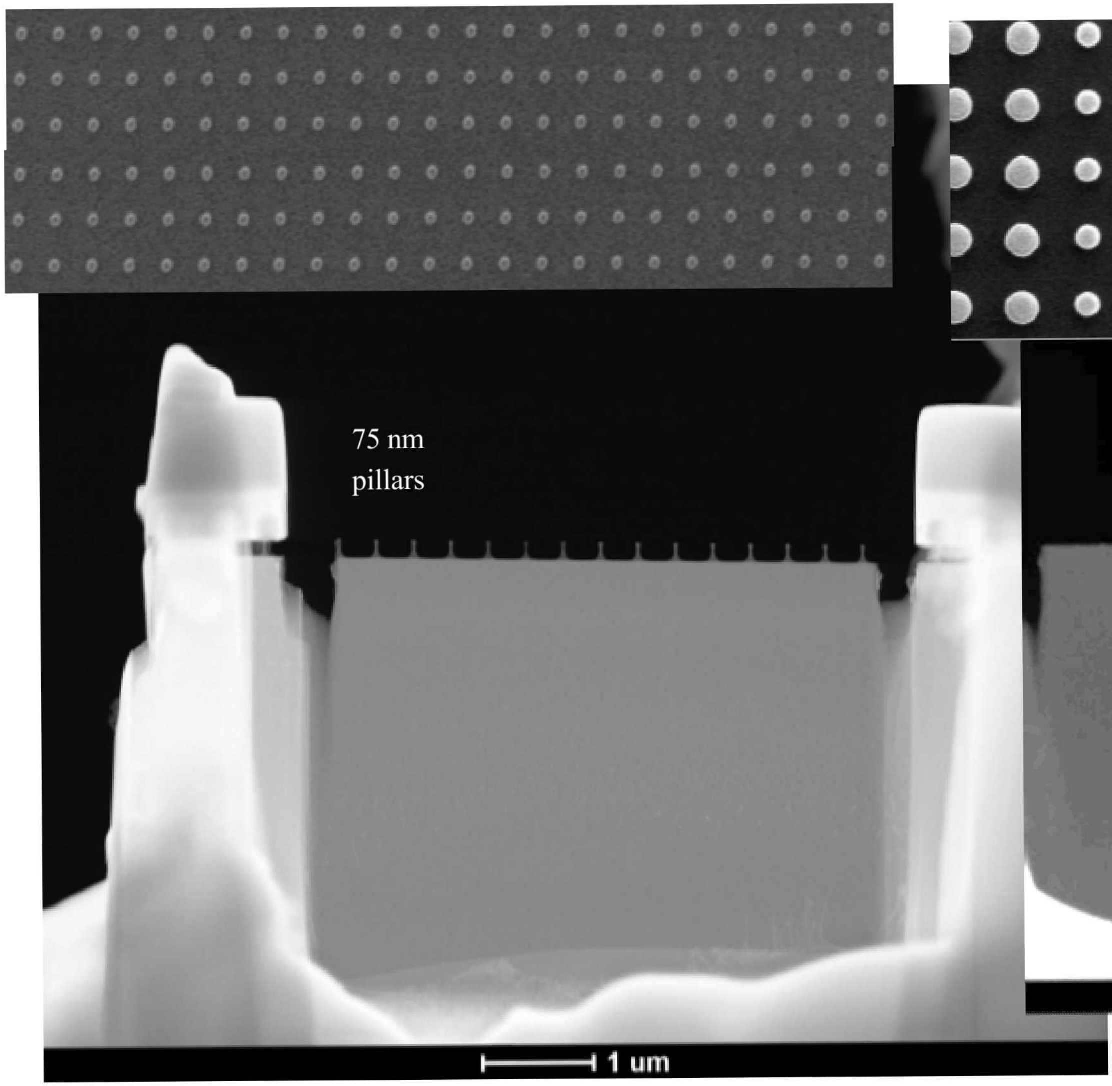


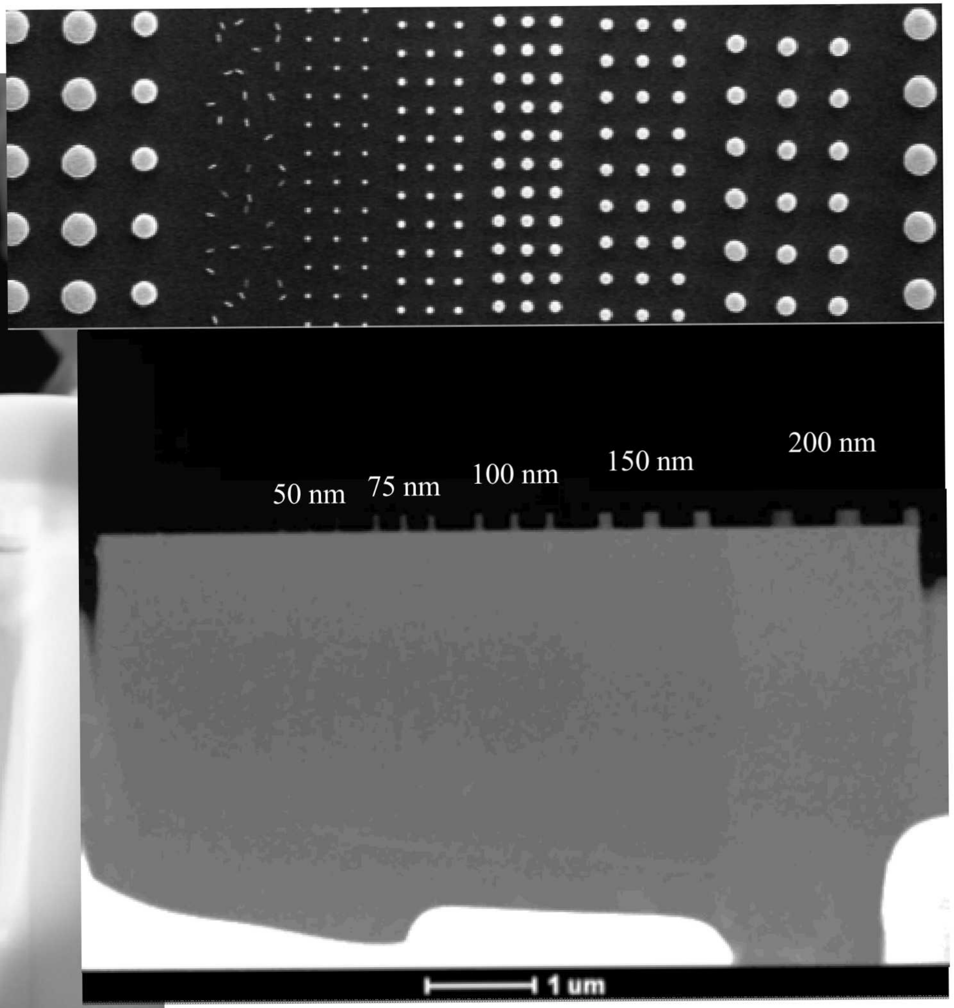


STEM of Si/SiGe pillars after HF dip

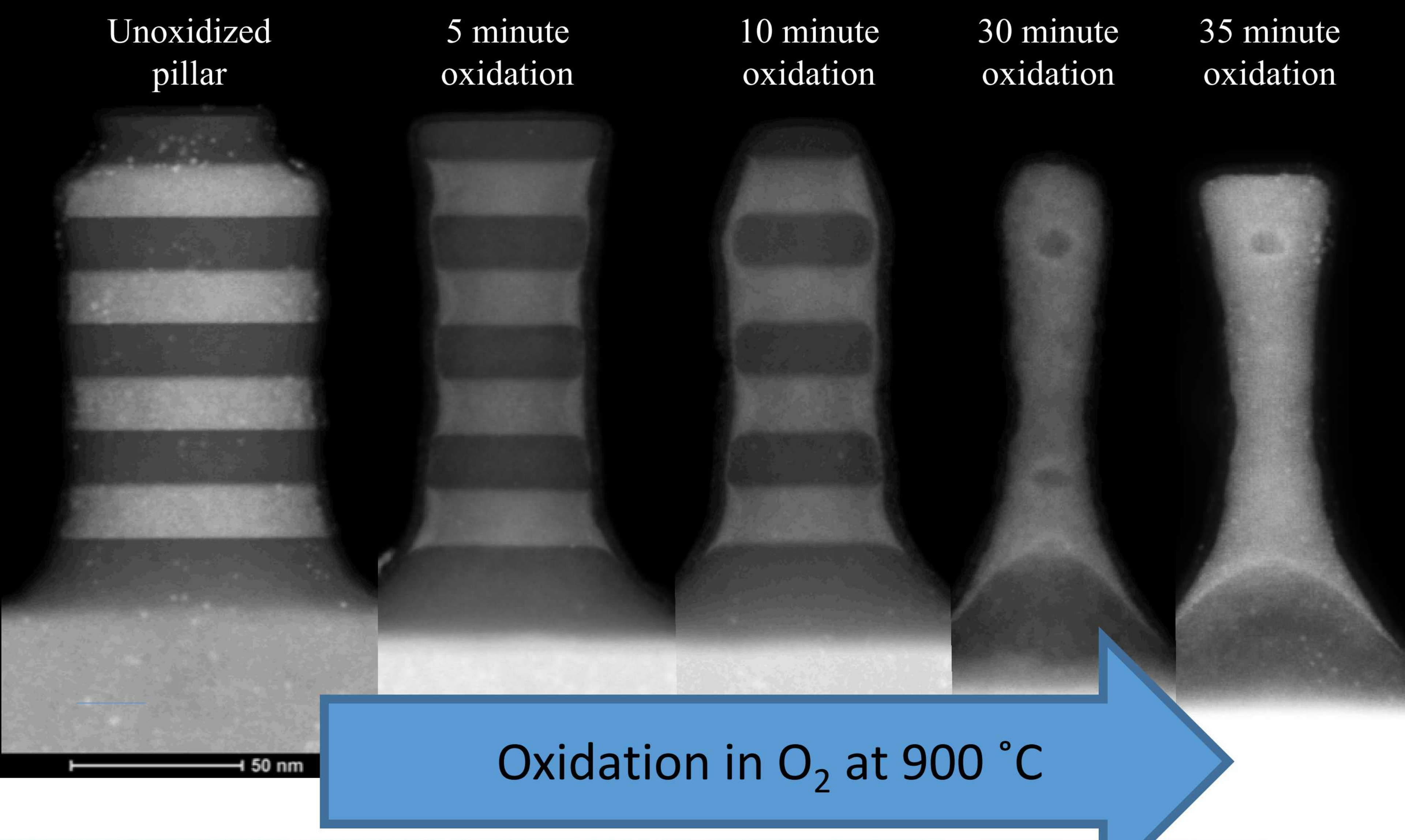
- [STEM images of 37 nm pillars]

Etch-release method for XTEM



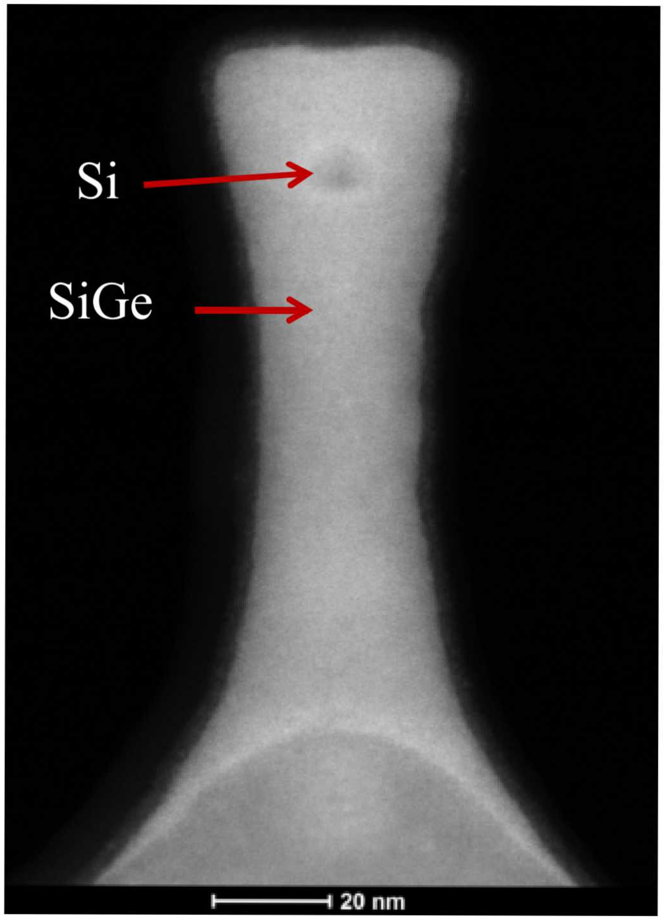


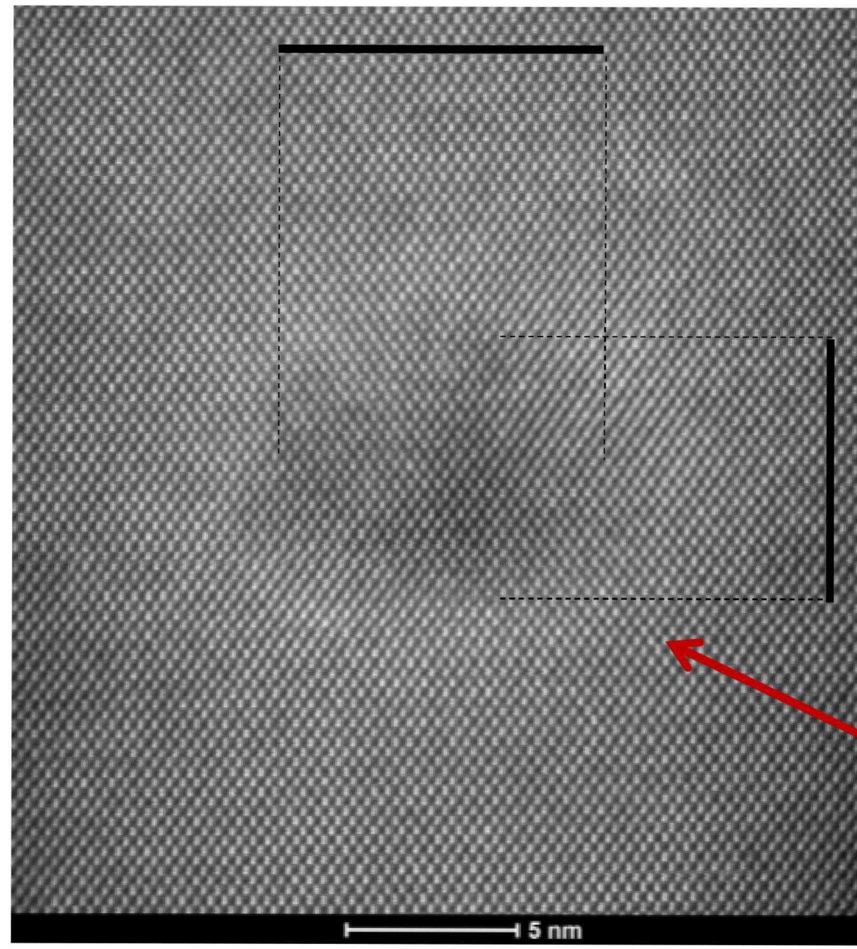
Evolution of 75 nm pillar



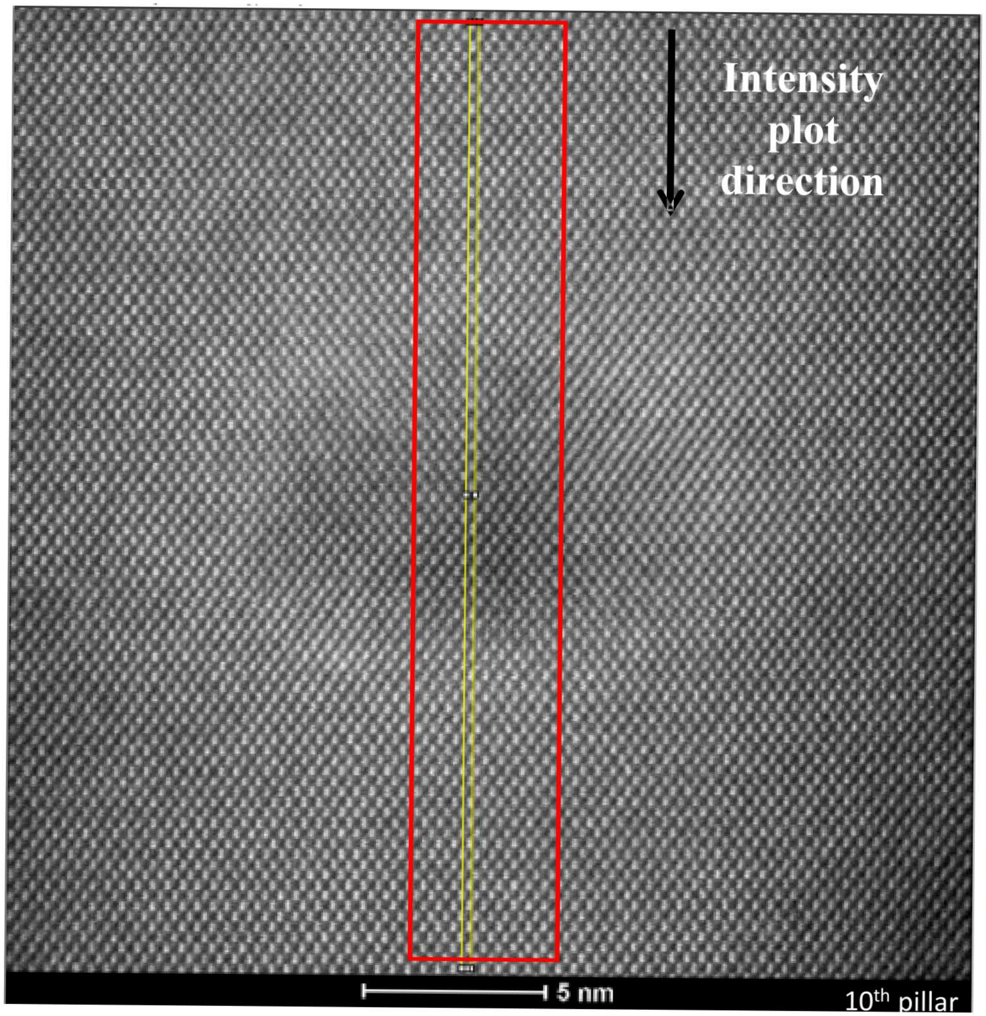
STEM of encapsulated Si dot in SiGe

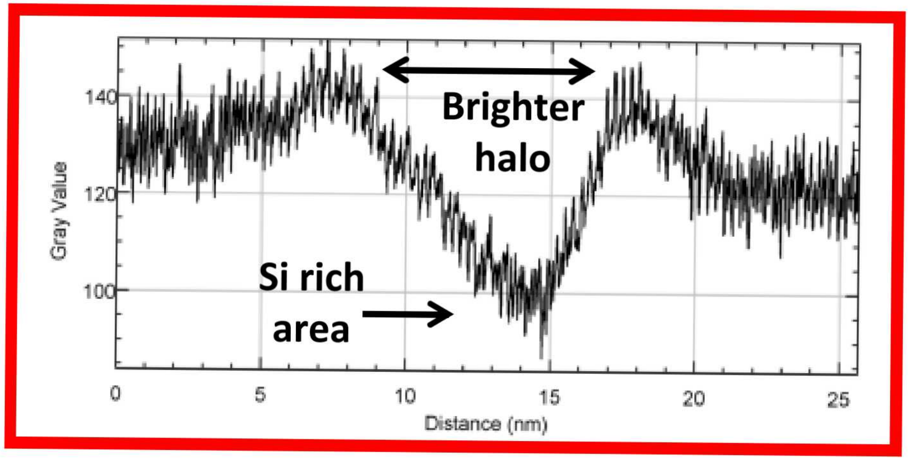
- Si layers fully encapsulated by single crystal SiGe after 35 minute oxidation at 900 ˚C in O_2

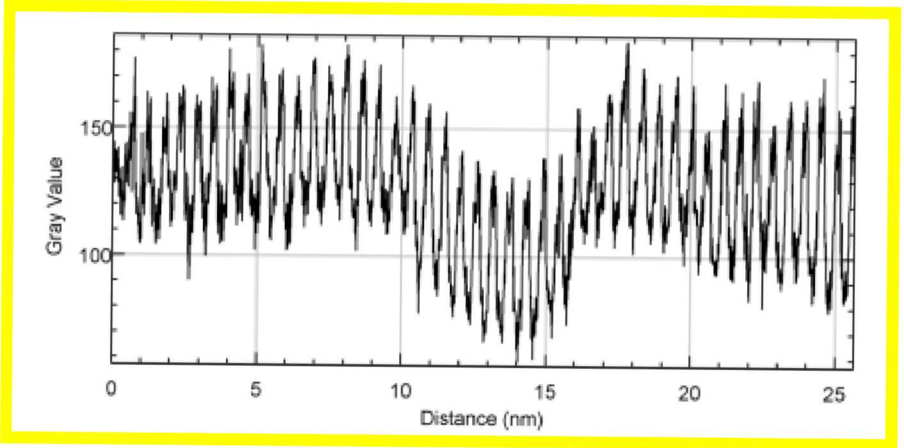




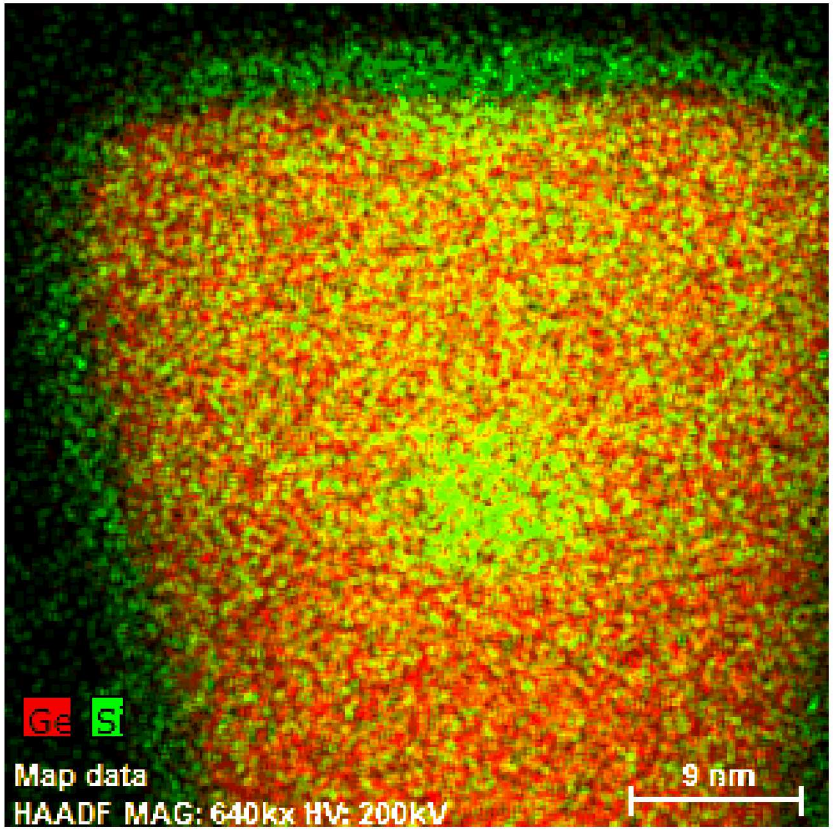
Greyscale intensity plots for 75 nm pillar after 35 minute oxidation at 900 °C

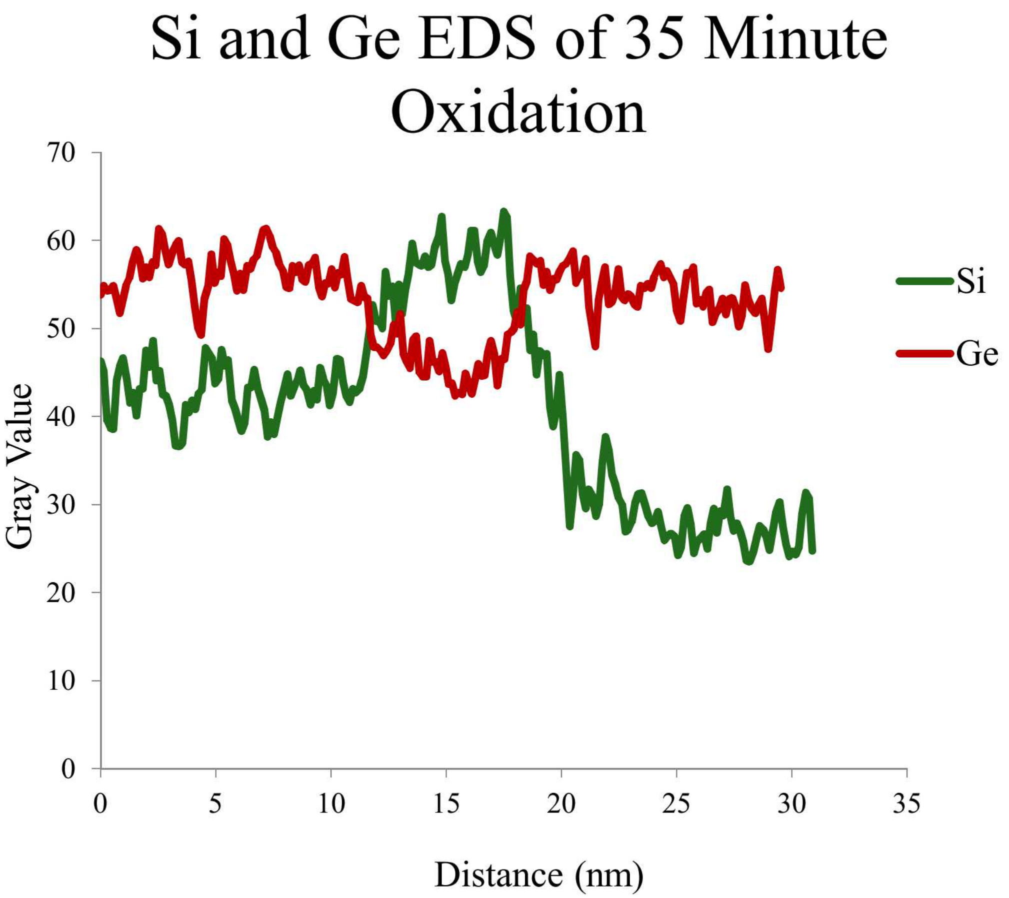






EDS of Si dot encapsulated in SiGe





Conclusions

- Understanding SiGe and Si interactions and oxidation is key to continued progress in many microelectronics applications
- Novel Ge diffusion also observed in Si/SiGe pillar structures
- Continued oxidation forms encapsulated Si QDs!
- Enhanced Ge diffusion could pave the way to formation of novel Si (and SiGe) structures for future electronics applications

Acknowledgments

- Sandia National Laboratories
  - CINT
  - Dr. George Wang
- Dr. Kevin Jones
- SWAMP Group

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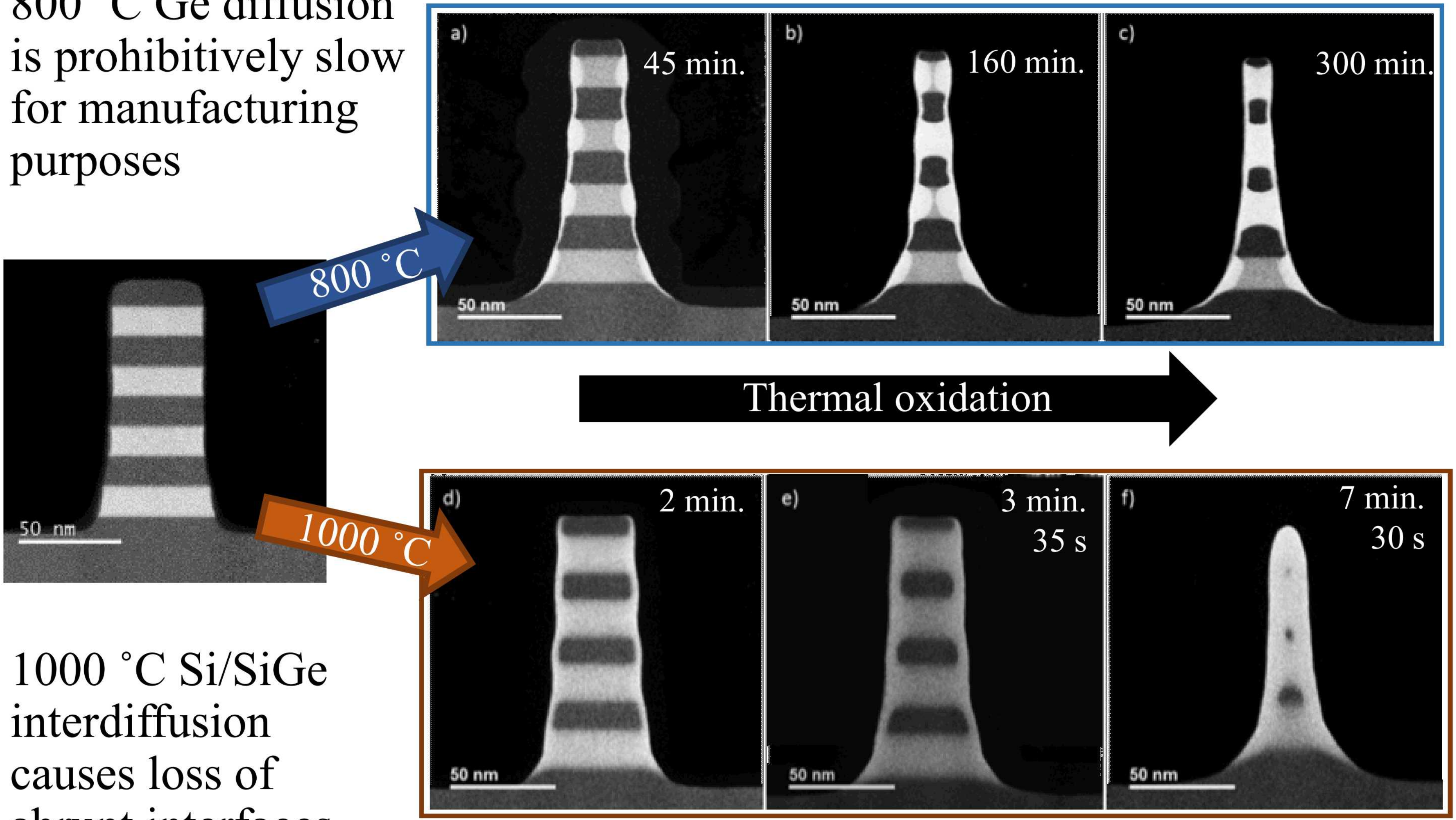
Additional slides

Temperature studies of fin structures

- 800 ˚C Ge diffusion is prohibitively slow for manufacturing purposes

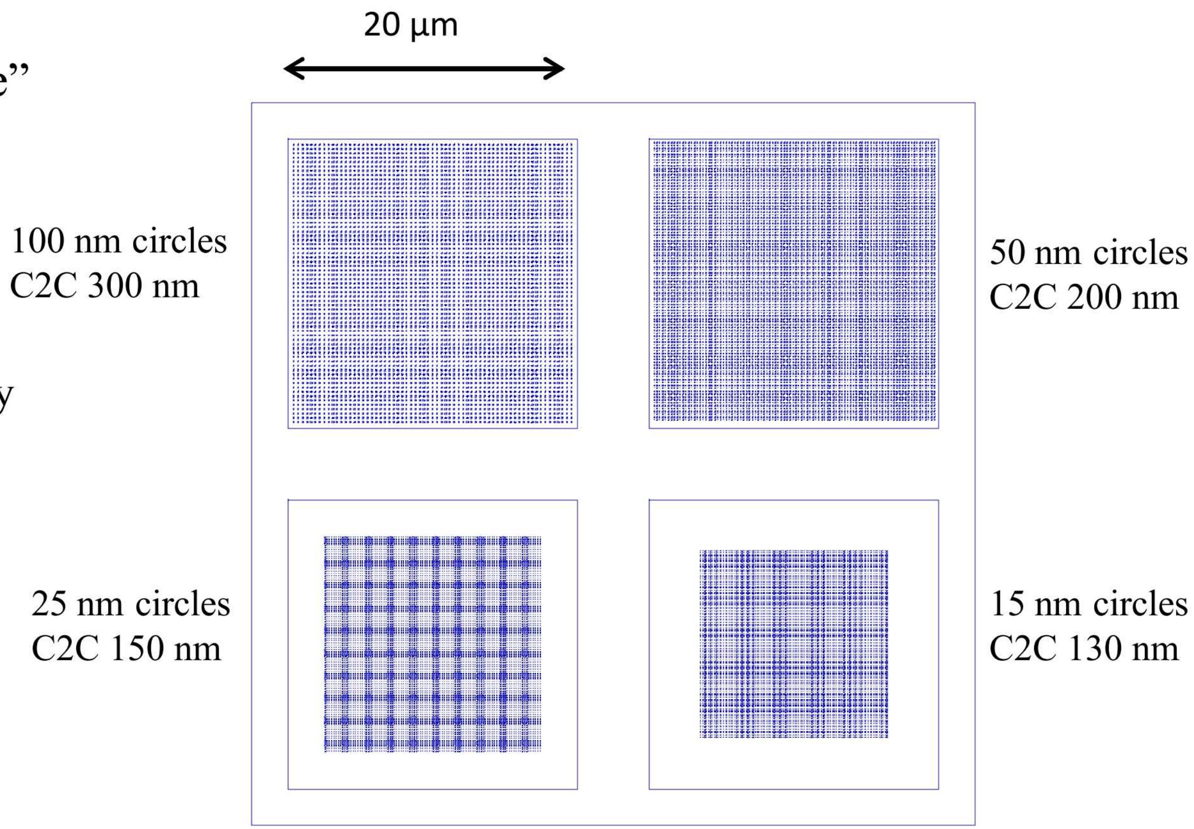


- 1000 ˚C Si/SiGe interdiffusion causes loss of abrupt interfaces

Brewer, W. M. *et al.* Lateral Ge Diffusion During Oxidation of Si/SiGe Fins. *Nano Lett.* **17,** 2159–2164 (2017).

Fabrication challenges of nanopillars

- Pillar pattern considerations
  - E beam lithography time consuming for large arrays
  - Must optimize e-beam "dose" seen by each feature
    - Too much dose results in larger features and overexposure of places between features
    - Too little dose fails to fully crosschain the polymer, causing features to be removed when developed after e-beam exposure
  - Must leave enough space between pillars to allow for uninhibited oxide growth
- Want pillars close enough together to capture several in a single FIB cross section

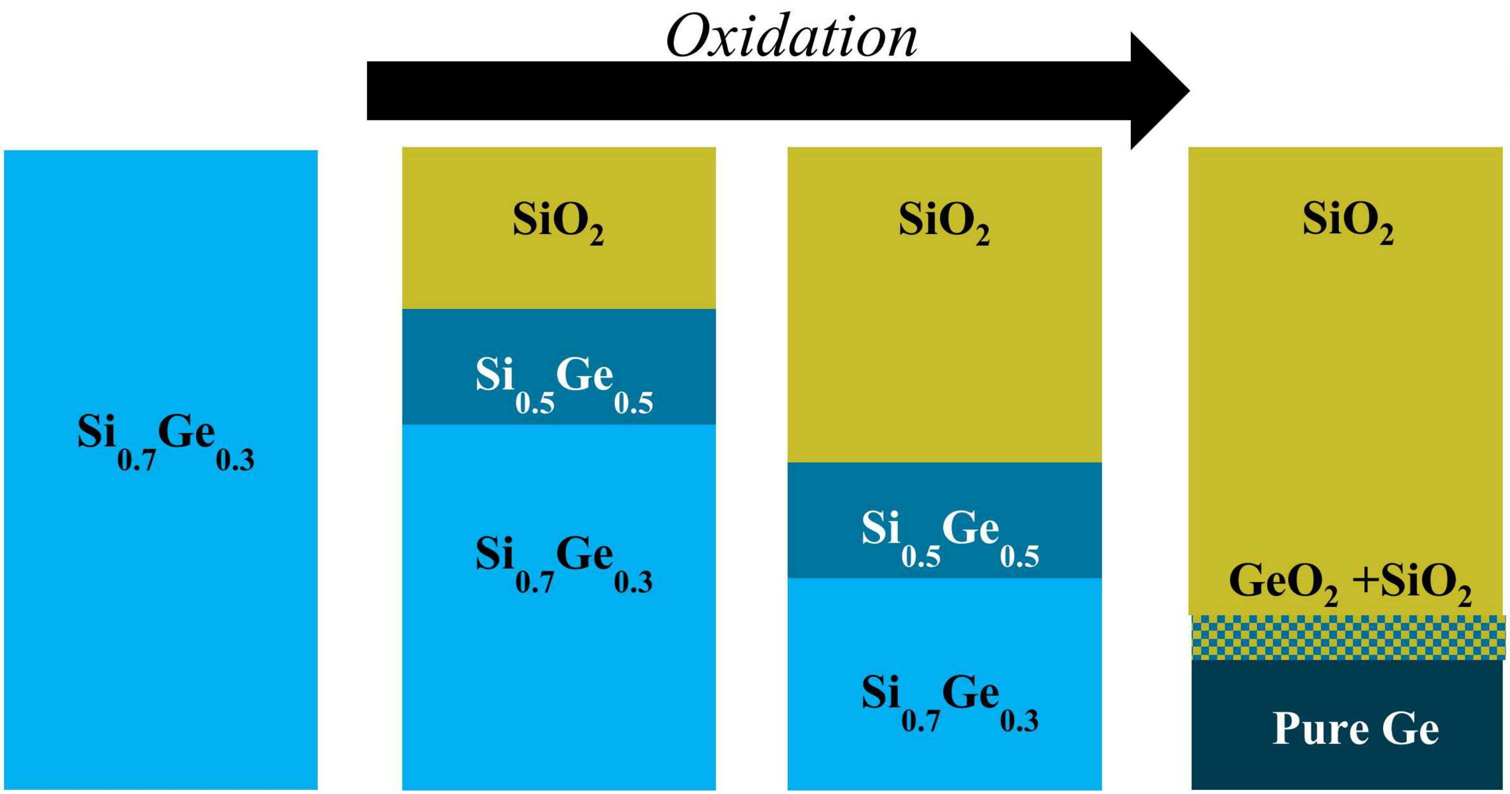


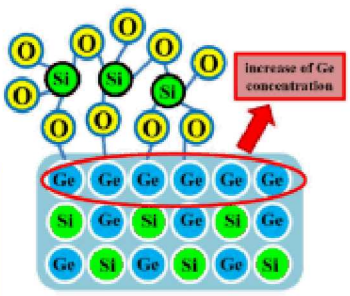
Fabrication challenges of nanopillars

- Plasma etch considerations
  - Want pillars tall enough to allow uninhibited Ge diffusion down sidewalls
  - Need pillars to maintain structural integrity during subsequent processing steps
- Protective layer for FIB work considerations
  - Need layer of protective material to avoid implant damage from FIB while making cross section
  - Need to be able to find pillar array on sample after protective layer is in place
  - Protective layer must not obscure nanostructures during S/TEM imaging

Oxidation of SiGe and subsequent Ge pileup

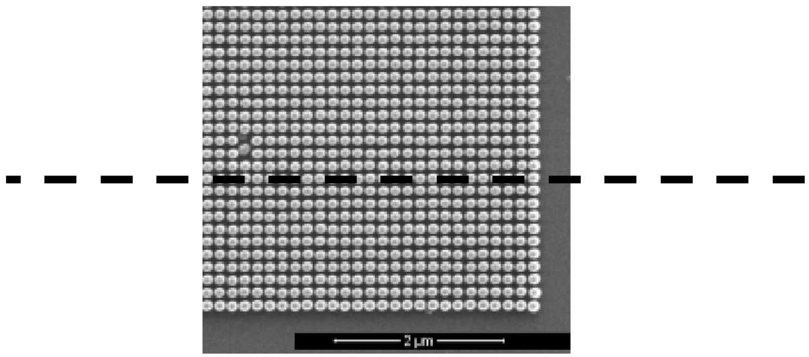
- Selective Si oxidation and Ge pileup in the SiGe layer at the oxidizing interface
- SiO_2 growth now also dependent on Ge concentration at $SiGe/SiO_2$ interface



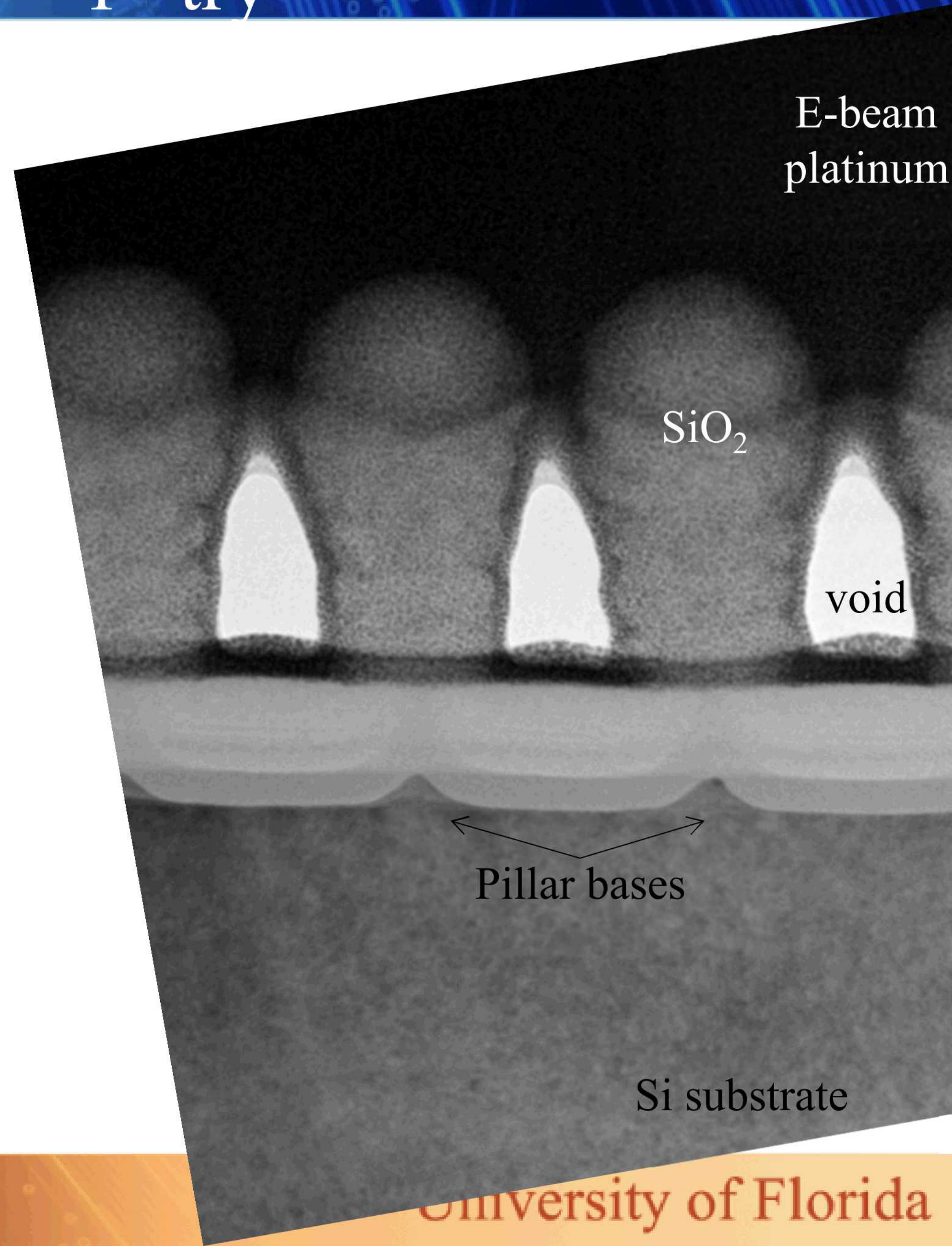


37 nm pillar HR-TEM images of 20 min anneal at 900°C – 1st try

- Cross section of 37 nm pillars using FIB
  - Carbon coater used (instead of sharpie)
  - E-beam platinum used (instead of I-beam)
- Took cross section aligned with pillar rows:

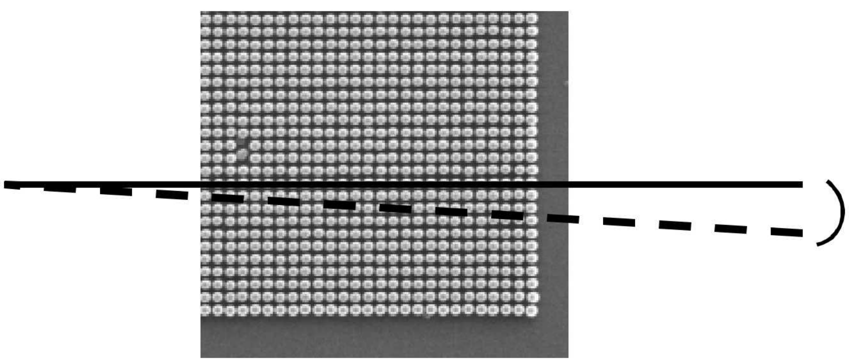


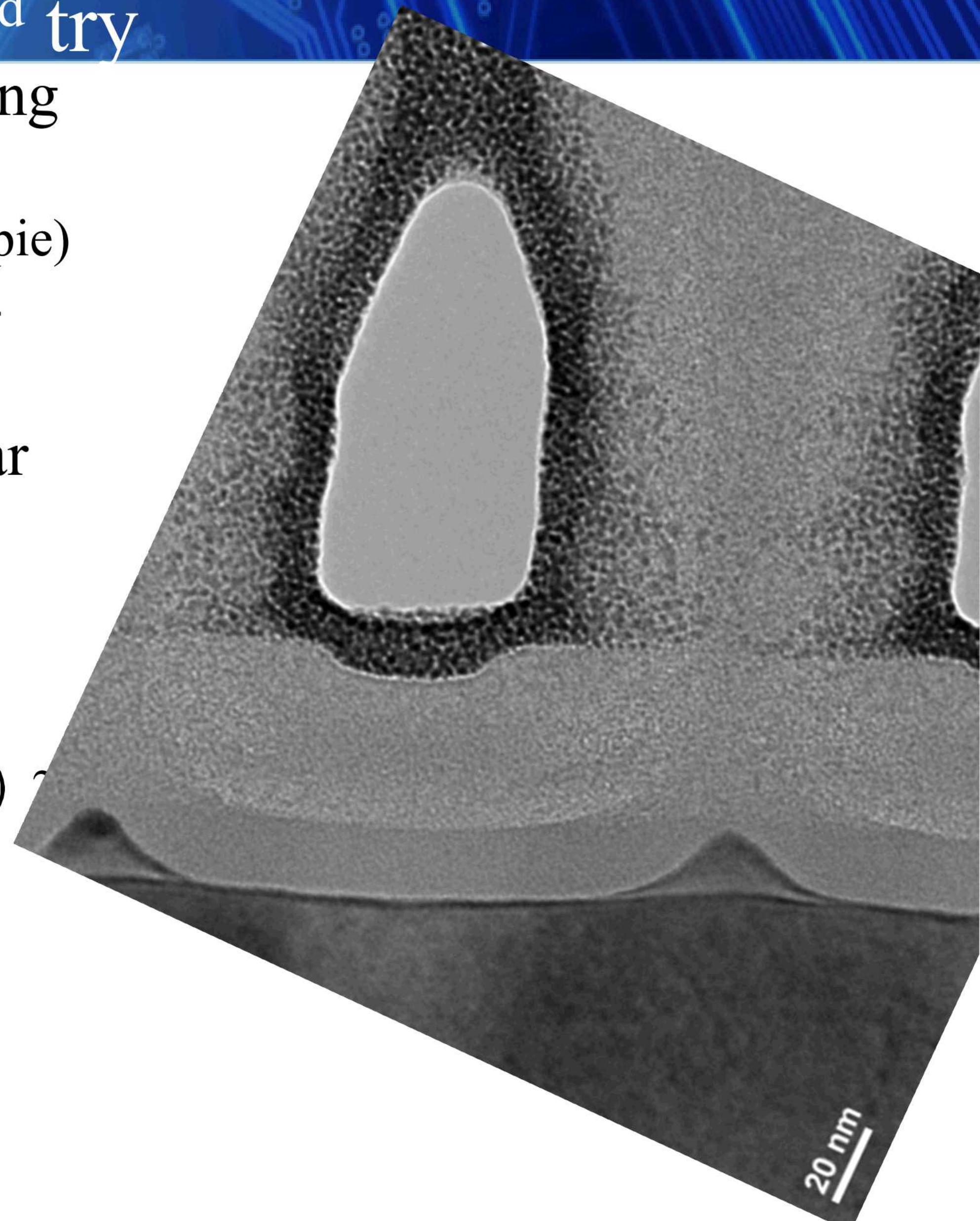
- Captured bottom of pillars in cross section
- Next, try making cross section at an angle



37 nm pillar TEM images of 20 min anneal at 900˚C – 2nd try

- Cross section of 37 nm pillars using FIB
  - Carbon coater used (instead of sharpie)
  - E-beam platinum used (instead of I-beam)
- Took cross section ~2˚ off of pillar rows

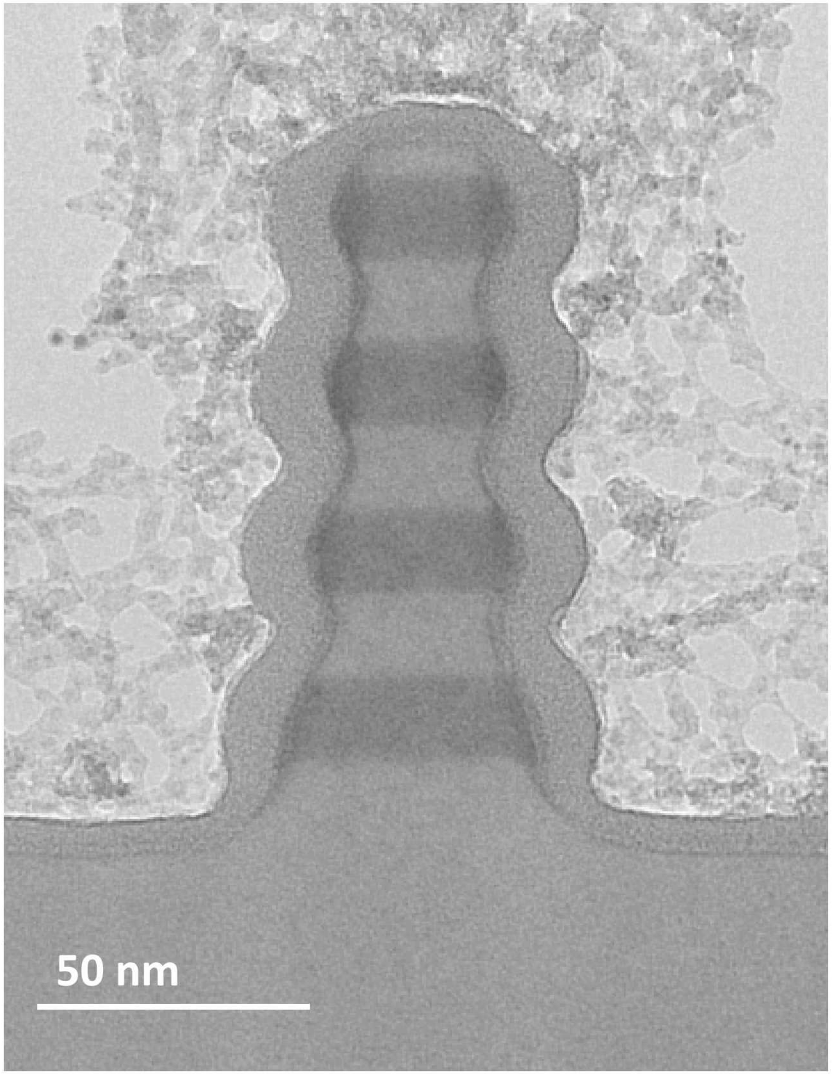




- Again captured bottom of pillars

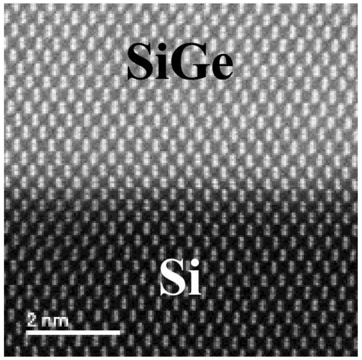
SiO_2 growth during oxidation of fins

- Cross section of Si/SiGe fin after oxidation at 900 ˚C



Analytical Techniques

- Cross-sectional HAADF STEM
- Gives high resolution, excellent Z contrast
- Ideal for observing:
  - Initial Ge movement along Si/SiO_2 interface
  - Differences in SiGe concentration



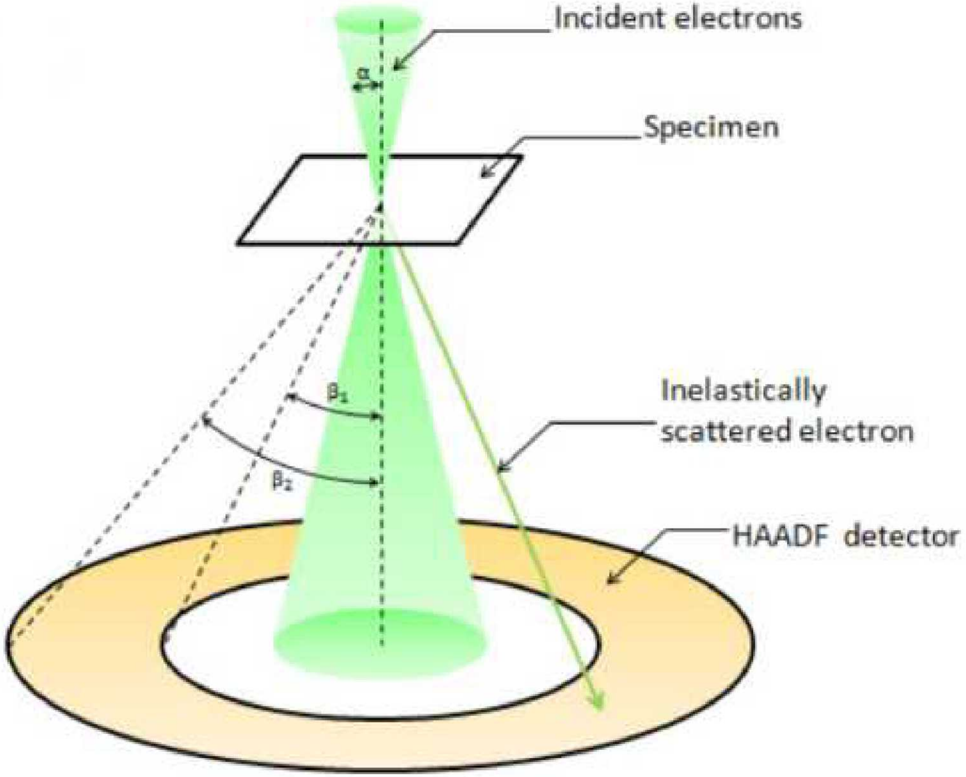
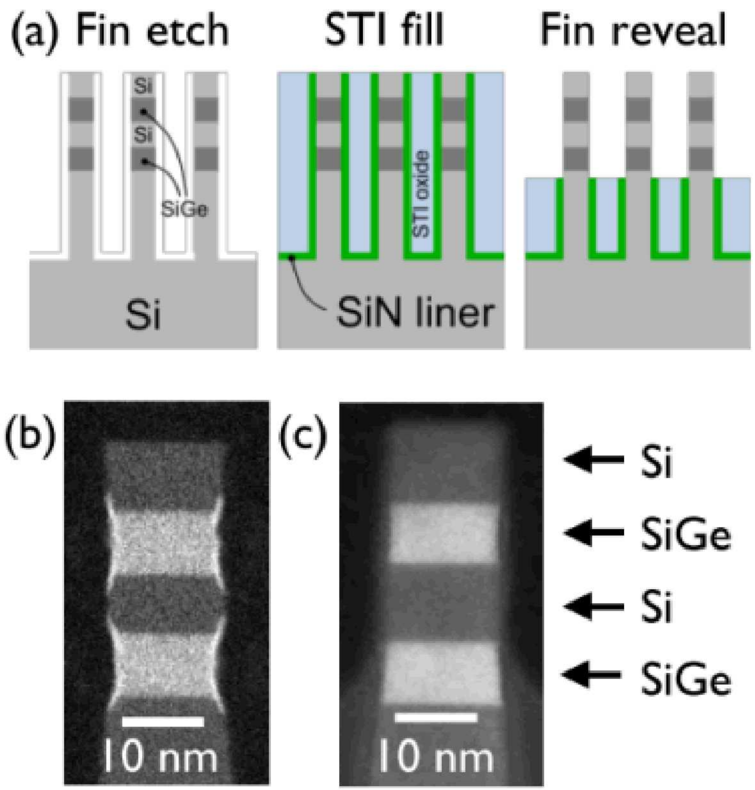


Figure courtesy of JEOL

Brewer, W. M. *et al.* Lateral Ge Diffusion During Oxidation of Si/SiGe Fins. *Nano Lett.* **17**, 2159–2164 (2017).

Si/SiGe heterostructures



(a) Schematics of fin structures after fin etch, shallow trench isolation (STI) fill, and fin reveal. (b) and (c) STEM images of fins after STI fill (b) w/o and (c) w/ SiN liner, revealing better preserved fin shape w/ SiN liner.

Thermodynamics of the oxidation

- In pure O_2, oxidation of silicon and germanium forming SiO_2 and GeO_2:
  - $Si + O_2 \rightarrow SiO_2$ with free energy change $G_1\Delta = -732$ kJ/mol O_2
  - $Ge + O_2 \rightarrow GeO_2$ $G_2\Delta = -376$ kJ/mol O_2
  - $Si + GeO_2 \rightarrow SiO_2 + Ge$ $G_2\Delta = -356$ kJ/mol O_2
  - The free energy values are obtained for the reactions at 1000 K (726 ˚C)

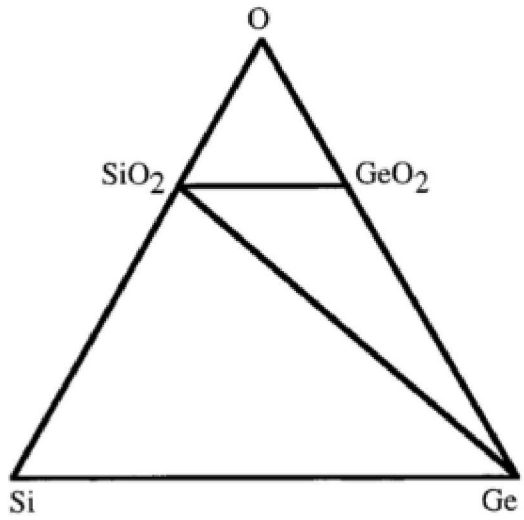
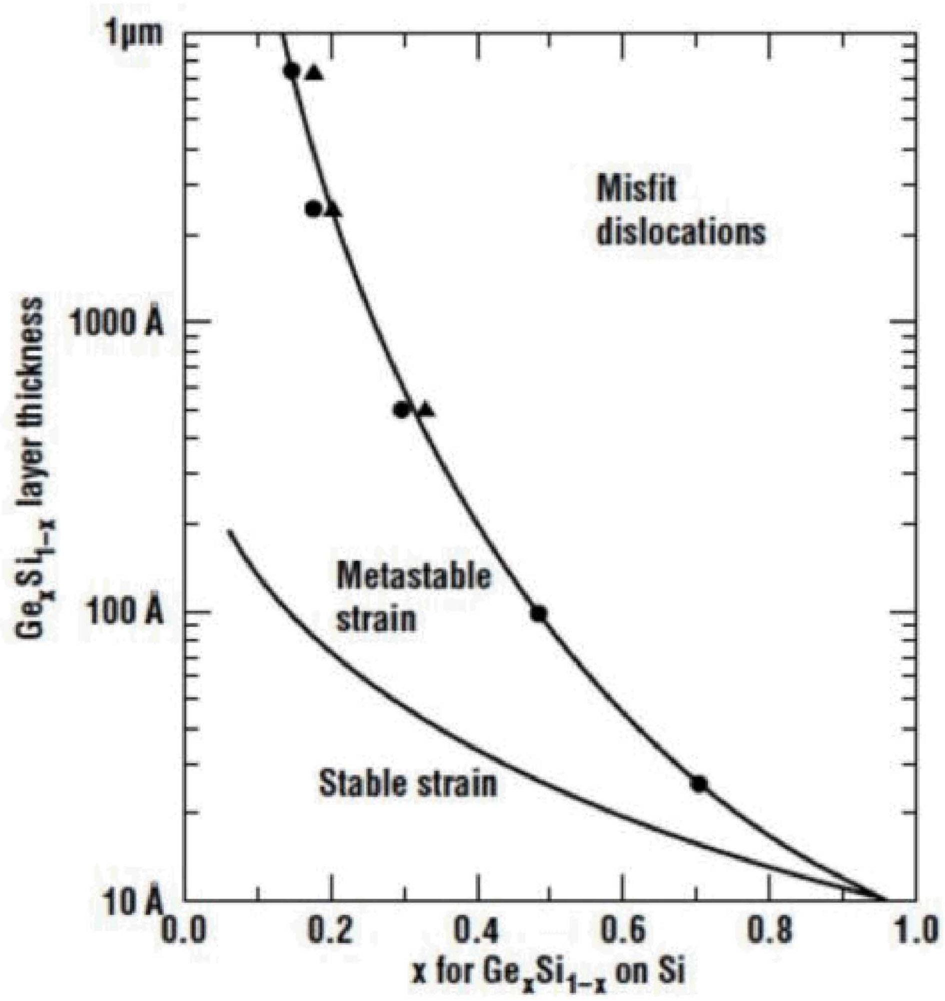


FIG. 1. Ternary phase diagram for the Si–Ge–O system at 1000 K and 1 bar, calculated based on the thermochemical data. The tie line linking SiO2 and Ge indicates that SiO2 is stable in the presence of germanium and that the equilibrium silicon concentration below which GeO2 begins to form approaches zero on the order of 10^{-19}.

3. Hellberg, P.-E., Zhang, S.-L., d'Heurle, F. M. & Petersson, C. S. Oxidation of silicon–germanium alloys. II. A mathematical model. *J. Appl. Phys.* (1997).

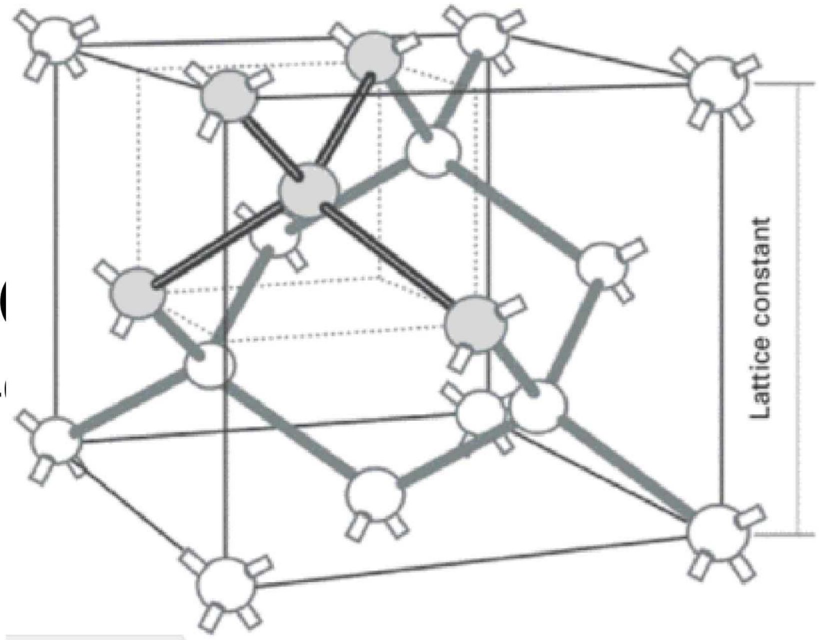
Strain vs SiGe layer thickness



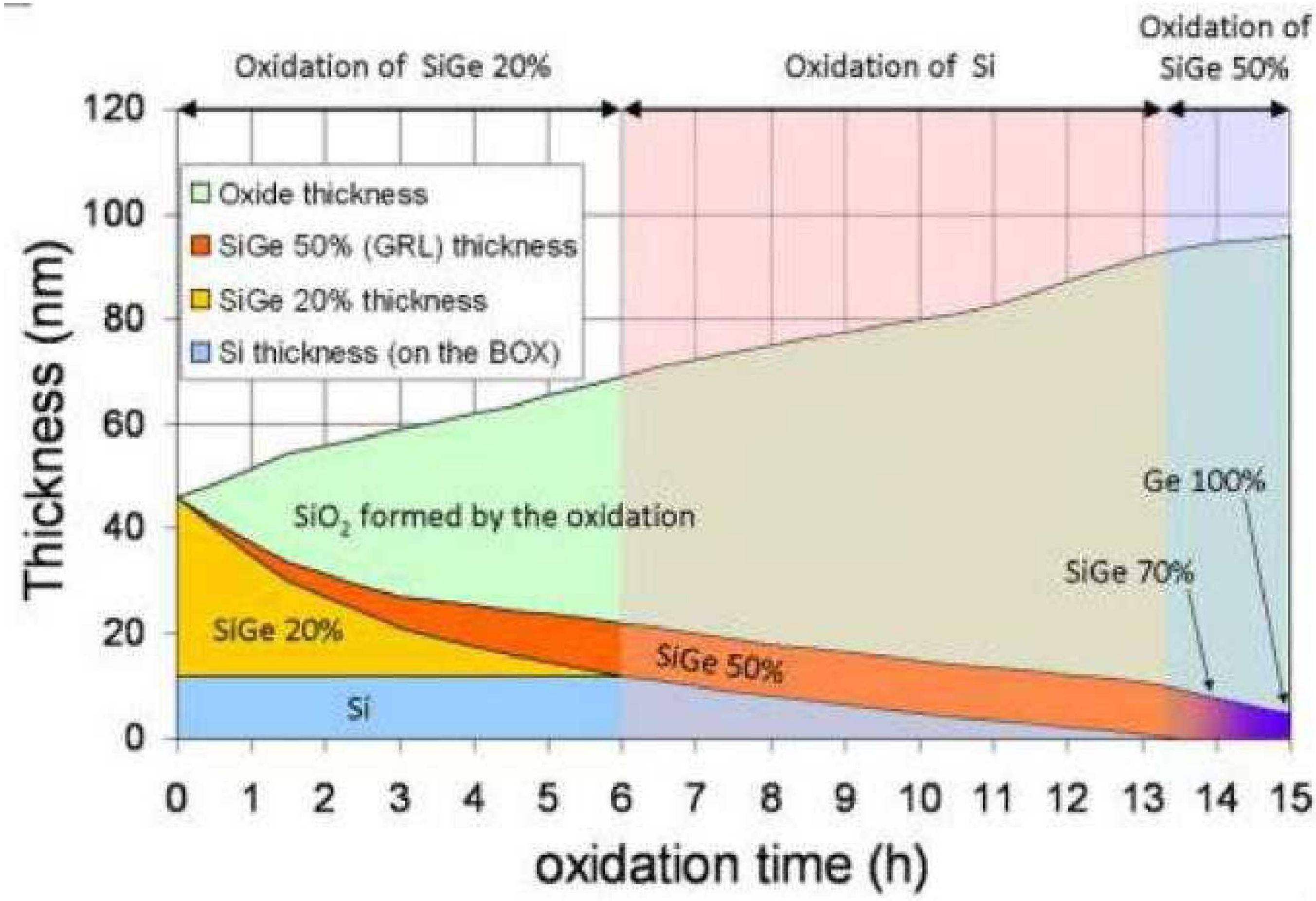
Campbell, S. A. Fabrication Engineering at the Micro- and Nanoscale. (Oxford University Press, USA, 2012)

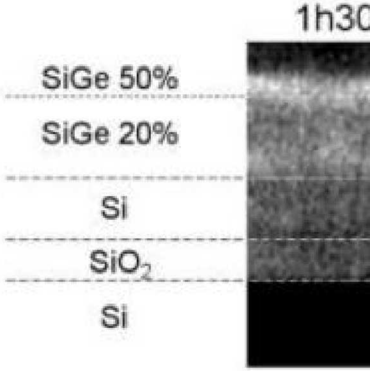
SiGe/Si Materials System

- Si and Ge completely miscible, forming $Si_{1-x}Ge_x$ diamond lattice
- Space group 0h–Fd3m, cubic unit cell with 8 atoms
- Non-primitive, covalently bonded
- Ge lattice constant = 5.658 A
- Si lattice constant = 5.431 A
  - Follows Vegard's law: $a_{A_{(1-x)}B_x} = ($
    - Small negative deviation with max of -



SiGe Oxidation

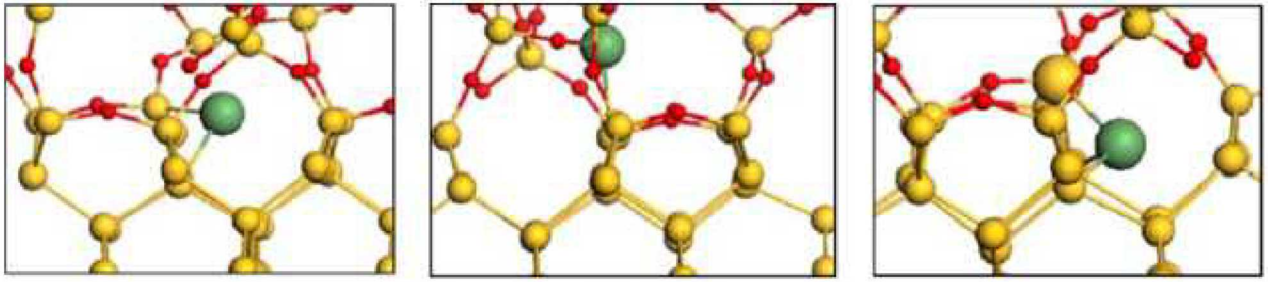




David, T. *et al. J. Phys. Chem. C* **119,** 24606–24613 (2015).

DFT calculations on Ge at the Si/SiO2 interface

- DFT calculations show that the interstitial Ge at the Si/SiO2 interface is more stable than in bulk Si
- **Ge interstitial would undergo thermally activated site exchange with a lattice Si atom in the Si part near the Si/SiO2 interface.**
- Ge atoms introduced into the Si/SiO2 system will be segregated in the Si region, preferentially near the strained Si/SiO2 interface



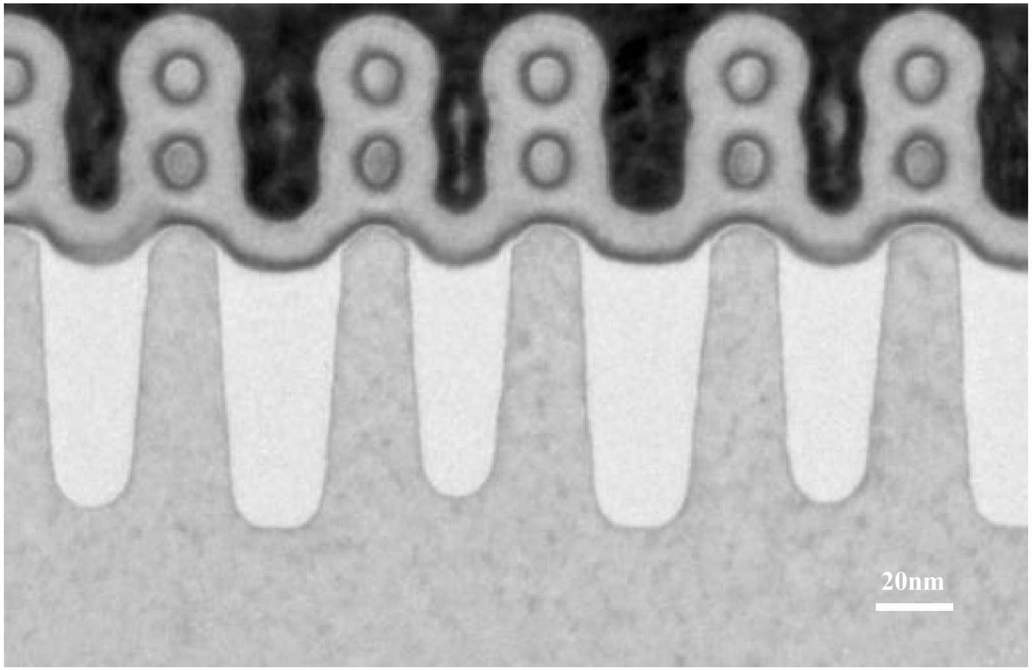
(a) (b) (c)

Figure 4. (Color online) Optimized configurations for interstitial Ge at the Si(001)/a-SiO_2 interface. (a) Si–Si BC (b) (111)-split, and (c) Si–O BC. Big dark gray (green), gray (yellow), and small darker gray (red) indicate Ge, Si, and O atoms, respectively.

Yu, D. & Hwang, G. S. Structure and Dynamics of Ge in the Si–SiO2 System: Implications for Oxide-Embedded Ge Nanoparticle Formation. *Electrochem. Solid-State Lett.* **11,** 17–19 (2008).

Current SiGe fabrication technology

- SiGe/Si superlattice material currently being used to manufacture Si horizontal nanowire transistors



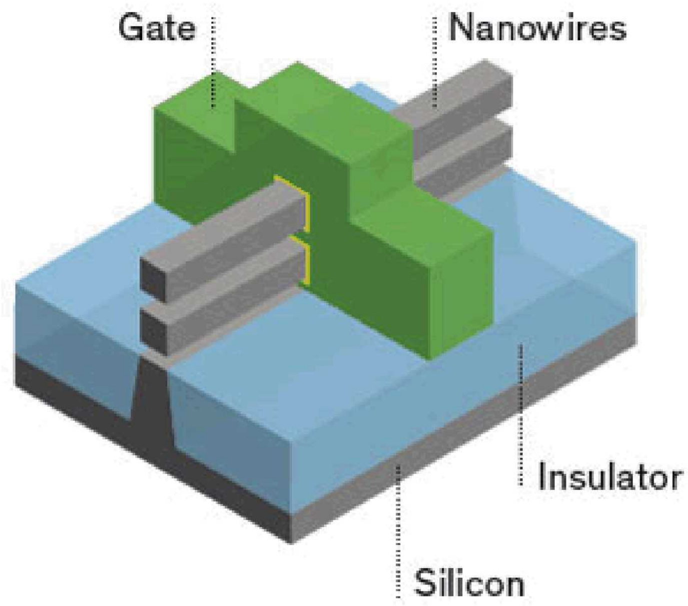
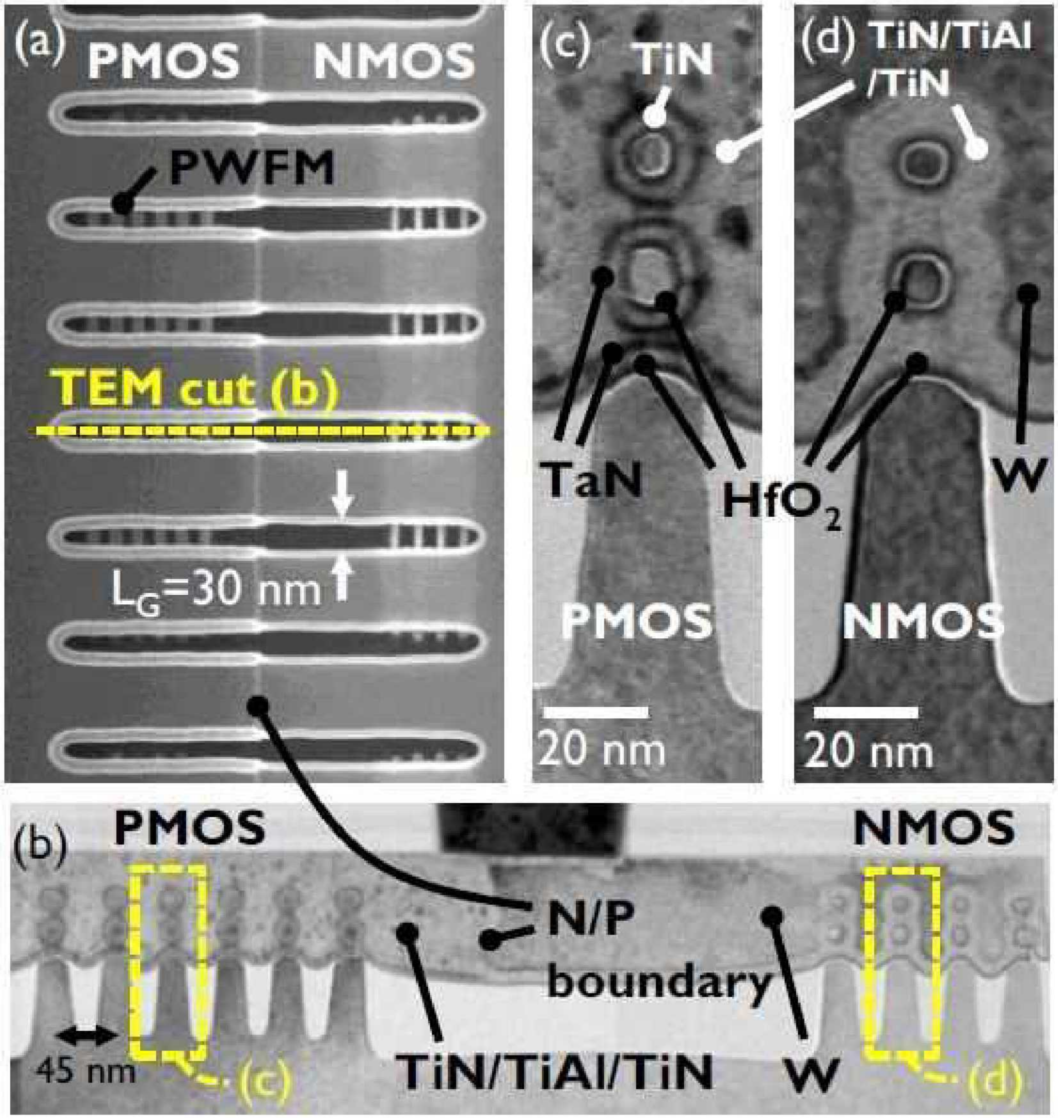


Illustration: Erik Vrielink

GAA NW transistors

- Imec (2016)

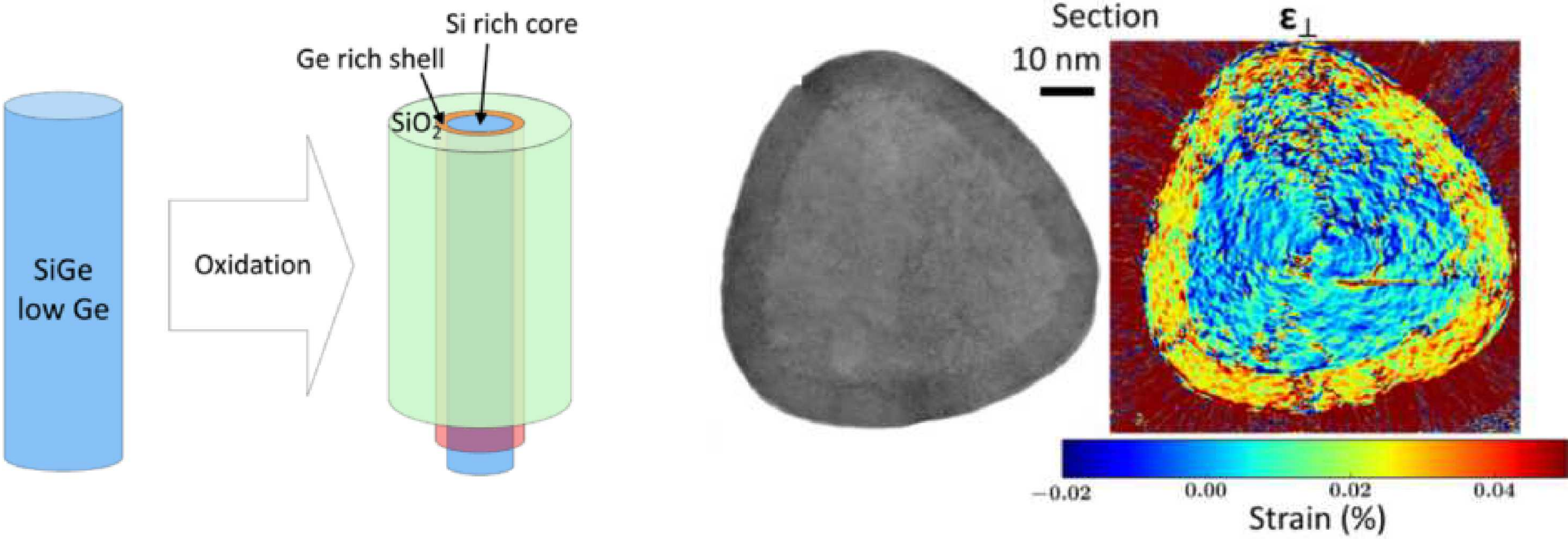


International Technology Roadmap for Semiconductors

YEAR OF PRODUCTION	2015	2017	2019	2021	2024	2027	2030
Logic device technology naming	P70M56	P48M36	P42M24	P32M20	P24M12G1	P24M12G2	P24M12G3
Logic industry "Node Range" Labeling (nm)	"16/14"	"11/10"	"8/7"	"6/5"	"4/3"	"3/2.5"	"2/1.5"
Logic device structure options	FinFET	FinFET	FinFET	FinFET	VGAA,	VGAA,	VGAA,
Footprint drive efficiency - lateral GAA, 3x NWs stacked			2.4	2.8	START	OF 3D	DOMAIN
Vertical GAA Lateral Half-pitch (nm)				10.0	6.0	6.0	6.0
Vertical GAA Diameter (nm)				6.0	5.0	5.0	5.0
Footprint drive efficiency - vertical GAA, 3x NWs stacked				2.8	3.9	3.9	3.9
Device effective width - [nm]	92.0	90.0	56.5	56.5	56.5	56.5	56.5
Device lateral half pitch (nm)	21.0	18.0	12.0	10.0	6.0	6.0	6.0
Device width or diameter (nm)	8.0	6.0	6.0	6.0	5.0	5.0	5.0

International Technology Roadmap for Semiconductors 2.0. 1–79 (2015).

- Core-shell SiGe vertical nanowire transistors[1]
  - Initial SiGe nanowires grown via vapor-liquid-solid growth
  - Difficult to scale this fabrication method



SiGe nanowires grown by VLS method and oxidized at 750 ˚C for 30-60 minutes. Resulting core-shell nanowires experienced 2% homogeneous strain.

[1]David, T. *et al.* Tailoring Strain and Morphology of Core − Shell SiGe Nanowires by Low-Temperature Ge Condensation. *Nanoletters* **17,** 7299–7305 (2017).