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A Novel Triple Inverter Design for CMOS Clocks and Oscillators

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***Abstract*—Single inverter gate CMOS oscillator designs have been used for decades based on the CMOS technology of the time. While a single inverter gate can deliver very good performance dependent on the application, it presents design limitations due to parameter trade-offs of transconductance, output impedance, and bias current. This paper introduces a novel CMOS sustaining amplifier design that significantly increases the design flexibility beyond what a single inverter can provide. It uses a three-stage inverter with the center inverter incorporating negative feedback to allow for a wide range of transconductance with wide operational bandwidth. High transconductance can provide operation for high-resistance resonators and or resonators that have significant activity dips [1]. This design is resistant to parasitic oscillations seen with high transconductance sustaining amplifiers. An equation and model describing the circuit transconductance is derived and accurately determines the circuit gain using a small number of circuit parameters. Given a desired transconductance, this new amplifier operates with lower power and higher output impedance than an equivalent single inverter. Engineers at Sandia National Laboratories have fabricated and implemented this type of design with approximately 20 mS of transconductance at frequencies of 50 MHz and has been applied to frequencies up to 100 MHz.**

Keywords— Pierce oscillator; CMOS; amplifier; inverter; transistor

I. INTRODUCTION: THE CMOS INVERTER

Traditional CMOS oscillator design, based on the classic inverter, single P and N device, is typically self-biased with a large-value feedback resistor. This design has been used with a wide variety of resonator types and frequencies for clock oscillator applications. Fig. 1 shows the schematic and symbol for a CMOS inverter used ubiquitously for Pierce oscillator designs.

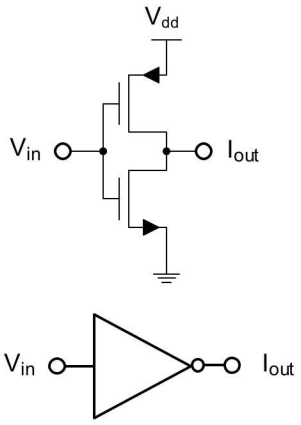

Fig. 1. CMOS inverter.

This basic design is simple and elegant as a sustaining amplifier for low- and high-frequency Pierce clock oscillator designs. The amplifier self-biases with a large-value resistor connected across its input and output [2, 3]. The inverter is a transconductance amplifier that can be modeled as a voltage-to-current converter with input and output impedances. Fig. 2 shows the schematic of the transconductance circuit model.

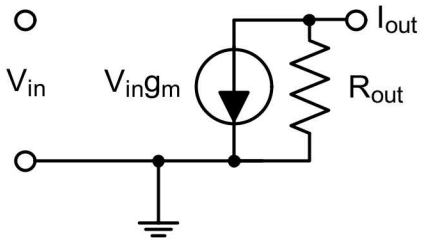

Fig. 2. Transconductance model.

The CMOS inverter is an inverting transconductance circuit. The value of g_m is the sum of the N and P transistor g_m values, and MOS g_m is a function of device dimensions, process parameters, and bias current. In this model, the CMOS inverter R_{out} is a function of bias current and transistor, λ. The value of R_{out} is the parallel combination of the output resistances of the P and N devices.

A single inverter used as a sustaining amplifier in a Pierce configuration has limitations in design flexibility in that gain,

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g_m, and output impedance, R_{out}, can be in opposition and both are dependent on bias current [4]. Designing an oscillator to operate over a range of simultaneous constraints, such as power supply voltage variability, temperature and process variations, resonator loss, and even oscillator start-up time, may require a larger transconductance.

Multi-stage (three) inverters, as shown in Fig. 3, offer an option for designing a sustaining amplifier with improved parameter flexibility; however, the transconductance of this type of circuit is extremely large and poorly controlled. It will typically exhibit strong free-running parasitic frequency modes which can result in an unreliable operation.

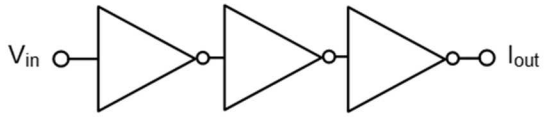

Fig. 3. CMOS triple inverter.

II. Development of a Novel CMOS Architecture

We have developed a much-improved triple inverter-based sustaining amplifier that uses unique intra-circuit feedback configuration (patent #US7183868B1). It can be used for Pierce oscillator applications or any other type of oscillator where large inverting transconductance is desired. This triple inverter with center feedback (TICF) is shown in Fig. 4.

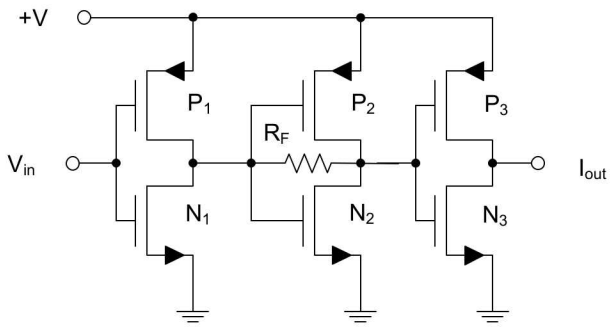

Fig. 4. Triple inverter with center feedback.

This triple inverter design uses negative feedback in the center inverter by using a resistor, RF, from input to output to control the gain and phase characteristics of the overall amplifier. The first two stages control the overall transconductance while simultaneously reducing the impedance between the stages. The last stage provides transconductance and drives the resonator network. This new circuit allows wide control of transconductance and output impedance as well as bias currents with less inter-parameter dependency than a single inverter while allowing high-frequency operation. To derive the total transconductance of the TICF, the center stage with feedback must be characterized for input impedance and voltage gain to formulate the total g_m of the TCIF. Fig. 5 is a simplified schematic/model of the center stage that combines the two transistors N_2 and P_2 into one, NP_2, with the equivalent parameters.

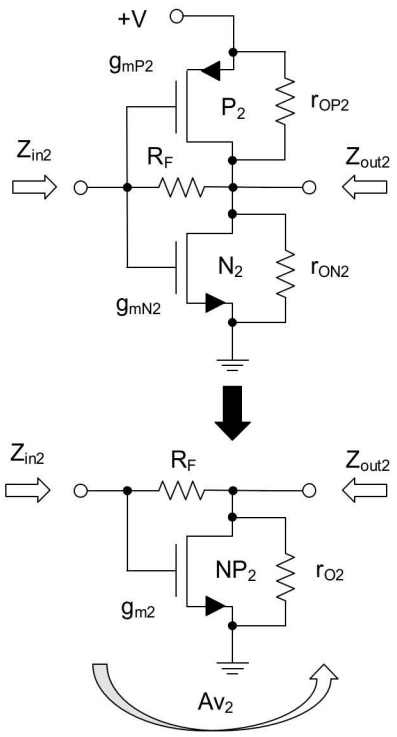

Fig. 5. TICF center stage schematic and model.

Equations (1) and (2) are the equivalent model of the second stage converted to a single transistor model.

$$g_{m2} = g_{mP2} + g_{mN2} \tag{1}$$

$$r_{02} = \left(\frac{r_{OP2} r_{ON2}}{r_{OP2} + r_{ON2}}\right) \tag{2}$$

The input impedance, Zin_2, is as follows, assuming the feedback term dominates the impedance:

$$Zin_2 \approx \frac{1}{g_{m2}} \left(\frac{r_{O2} + R_f}{r_{O2}}\right) \tag{3}$$

The gain of the second inverter, Av_2, is:

$$Av_2 = (1/R_F - g_{m2})\left(\frac{R_F r_{O2}}{R_F + r_{O2}}\right) \tag{4}$$

The total TICF transconductance can be calculated from these parameters and the combined g_m of the inverter pairs of the first and last stages, g_{m1} and g_{m3}, where:

$$g_{m1} = g_{mP1} + g_{mN1} \tag{5}$$

$$g_{m3} = g_{mP3} + g_{mN3} \tag{6}$$

Fig. 6 is the model used to formulate the total transconductance of the TICF circuit, inverter stages I_1, I_2 I_3.

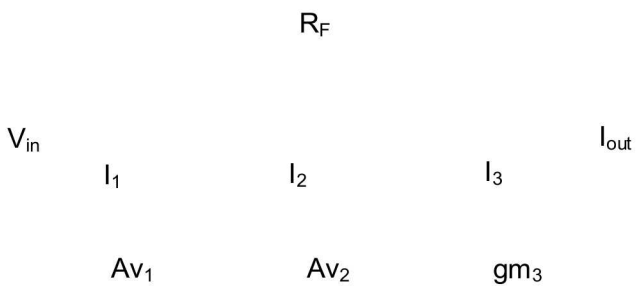

Fig. 6. Circuit model for formulating total TICF transconductance.

For this design, the inverters used in I_1 and I_2 are identical devices. The gain Av_1 is formulated assuming that the net output impedance of inverter I_1, r_{O1}, is much larger than Zin_2, which is a very good assumption in this design.

$$Av_1 \approx g_{m1} Zin_2 \qquad \text{where } r_{O1} > Zin_2 \tag{7}$$

Substituting Zin_2 from equation (3).

$$Av_1 \approx -g_{m1}\left(\frac{1}{g_{m2}}\left(\frac{r_{O2}+R_f}{r_{O2}}\right)\right) \tag{8}$$

If transistors of I_1 are identical to those in I_2 then $g_{m1} = g_{m2}$,

$$Av_1 \approx -\left(\frac{r_{O2}+R_f}{r_{O2}}\right). \tag{9}$$

Equation (9) shows that if $R_f < r_{O2}$, which is easily the case when R_f is chosen to be in the unity kilo-ohm range, then Av_1 will be approximately -1. Because it is undesirable to have this gain be less than one, this design is typically made with equal transconductances for I_1 and I_2. To have gain greater than one either compromises the function of I_2 due to decreased g_m or forces the first stage to use more current, both of which are not overwhelmingly desirable. The total g_m of the TCIF is

$$g_{mt} \approx (Av_1)(Av_2) g_{m3} \tag{10}$$

$$g_{mt} \approx \left(-\frac{r_{O2}+R_F}{r_{O2}}\right)\left((1/R_F - g_{m2})\left(\frac{R_F r_{O2}}{R_F + r_{O2}}\right)\right) g_{m3} \tag{11}$$

This simplifies to:

$$g_{mt} \approx (1 - g_{m2} R_F) g_{m3} \tag{12}$$

These equations assume the first and second stages are identical transistors. The third stage uses the same L/W ratio transistors as stages one and two, but they are M times larger, depending on the drive and gain desired. The TICF output impedance, R_{out}, is equal to the parallel output impedances of P_3 and N_3, equation (13). This impedance is required to model the TCIF used in the Pierce oscillator configuration.

$$R_{out} = r_{O3} = \left(\frac{r_{OP3} r_{ON3}}{r_{OP3} + r_{ON3}}\right) \tag{13}$$

Due to the high-gain and high-frequency capability of the TICF, the addition of a small capacitor, C_F, across the feedback resistor, R_F, is used to decrease g_{mt} as a function of frequency. This helps eliminate high-frequency parasitic oscillations due to resonator lead inductance. This capacitor is chosen to be small enough to have a minimal impact on g_{mt} phase at the desired operating frequency.

Fig. 7 shows this addition to the design with symbol containing the total TICF circuit and its use in a Pierce oscillator configuration.

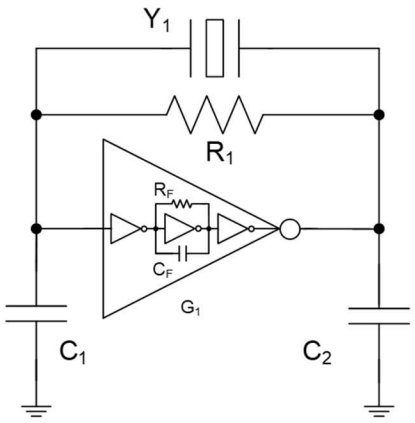

Fig. 7. TICF sustaining amplifier in a Pierce configuration.

III. Oscillator Design and Simulation

A TICF and single inverter were designed and simulated in the Sandia 350 nm CMOS technology. The design parameters for the two circuits are shown in Table 1. The W/L of the transistors are all identical. In the TICF, the multipliers (M) are 1, 1, and 3, while the single inverter has a multiplier of 16. This illustrates the potential area savings using the TICF. The output resistance is 5.67 kΩ. For the single inverter (of equal g_m), the output resistance is 1.17 kΩ.

TABLE I. Design Parameters for TICF and Single Inverter Used in This Paper

Parameter	TICF	Single Inverter
W/L, NMOS	10/1	
W/L, PMOS	16/1	
Multiplier(s)	1, 1, 3	16
R_F	5 kΩ	N/A
C_F	120 fF	N/A
R_1	50 kΩ	

In addition, we simulated the TICF with the center feedback removed. Fig. 8 shows the simulated transconductance as a function of frequency for the TICF and single inverter; by design, both have g_m = 21 mS at 50 MHz. Without the center feedback, the triple inverter has g_m = 1.8 S at 50 MHz; this is almost 100 times the g_m of the other two circuits, and the phase is very frequency dependent. These attributes suggest that using this type of triple inverter oscillator will result in strong parasitic oscillation conditions.

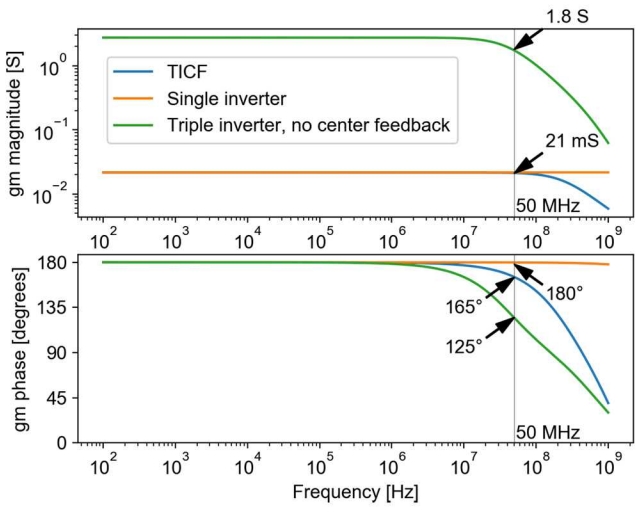

Fig. 8. Simulated g_m over frequency for TICF, single inverter, and triple inverter without center feedback. The g_m at 50 MHz is about 21 mS for the TICF and single inverter and 1.8 S for the triple inverter.

For the TICF in this simulation, g_{m1} and g_{m2} are equal at 1.3 mS, r_{o1} and r_{o2} are 17 kΩ each, and g_{m3} is 3.9 mS, with R_F chosen to be 5 kΩ. Using equation (9), the gain of the first stage is Av1 ≈ -1.29 V/V; using equation (4), the gain of the second stage is Av2 = -4.25 V/V; and using equation (12), the value of g_{mt} is 21 mS, as confirmed by simulation. For comparison, this would equate to a bipolar transistor transconductance at 0.52 mA of emitter current, a significant transconductance and much larger than the individual inverter stages used in this design.

Fig. 9 shows the total TICF circuit and its use in a Pierce oscillator/clock configuration with nodes labeled. The resonator has a load capacitance of 8 pF for 50 MHz operation. To operate the resonator at a moderate drive level, we chose $C_1 = 2C_2$, resulting in C_1 = 24 pF and C_2 = 12 pF.

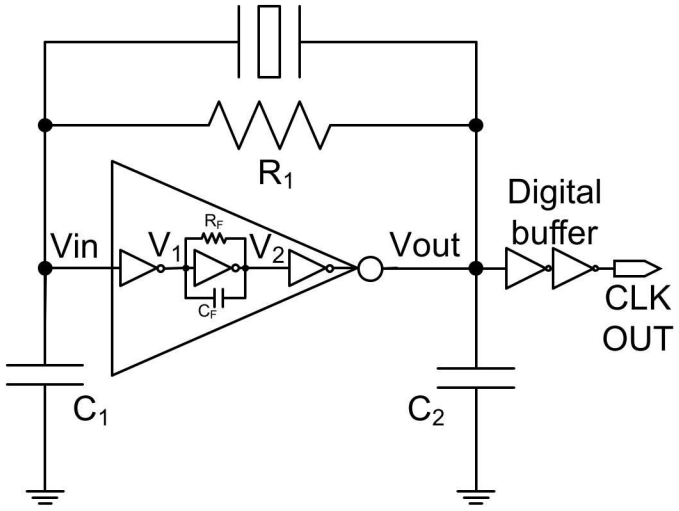

Fig. 9. TICF sustaining amplifier in a Pierce configuration, with an output buffer for clock applications.

Fig. 10 shows the simulated loop gain magnitude and phase of the oscillator using a TCIF and the same triple inverters without the center feedback circuit. This simulation shows that the TCIF has a single mode of oscillation at the crystal frequency (50 MHz), whereas the triple inverter, no center feedback has both a crystal and high frequency parasitic oscillation mode.

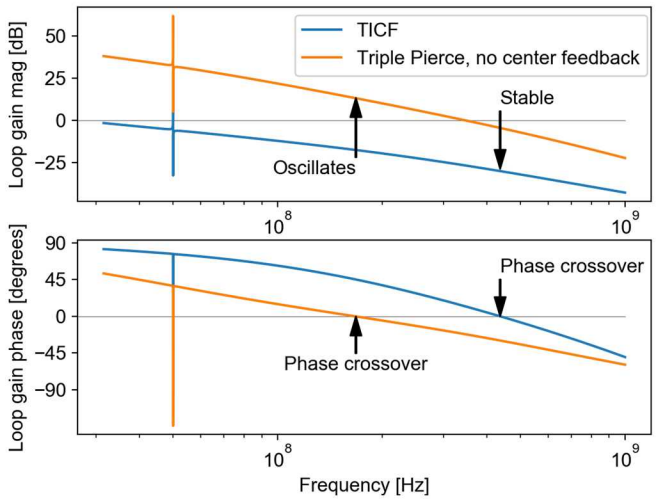

Fig. 10. Loop gain of triple-inverter oscillator (no center feedback resistor R_{mid}) and TICF oscillator, showing the suppression of a parasitic oscillation condition with the use of the center feedback resistor. Frequency range is 30 MHz to 1 GHz.

Fig. 11 shows the simulated steady-state oscillations of the nodes in the TICF oscillator of Fig. 9. This shows rail-to-rail output (V_{out}), with V_{in} at half that amplitude due to the ratio of C_1 and C_2. The power consumption of this circuit is 4.5 mW in steady-state oscillation.

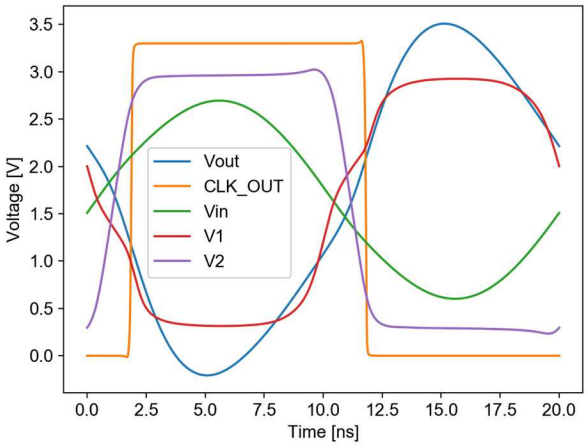

Fig. 11. TICF oscillator steady-state waveforms for one period of oscillation.

Fig. 12 shows the simulated steady-state oscillations of the single-inverter Pierce oscillator, using the same resonator and pillar capacitances as the TICF oscillator. It shows a less sinusoidal drive across the crystal compared to that of the TICF oscillator. The steady-state power consumption of this circuit is 9.7 mW. Compared to the 4.5 mW of the TICF, the single-inverter Pierce oscillator has a lower g_m/I_D efficiency.

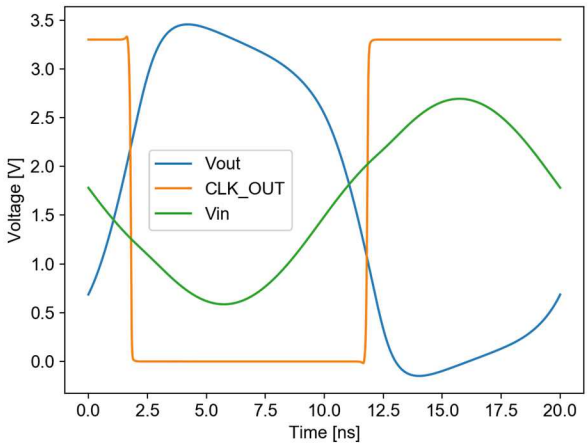

Fig. 12. Single-inverter Pierce oscillator steady-state waveforms for one period of oscillation.

The TICF is more robust against variations in resonator losses than the single-inverter because of its higher output resistance. For example, for a half-rail amplitude at Vout, the motional resistance of the resonator, can be as high as 330 Ω for the TICF (Q > 1700), whereas the motional resistance for the single-inverter must be less than 230 Ω (Q > 2500) for half-rail amplitude.

The simulated phase noise at 1 kHz offset of the TICF oscillator is -135 dBc/Hz, while that of the single-inverter oscillator is -142 dBc/Hz. This is most likely due to the TICF's multiple stages, where the first stage contributes noise while not contributing gain.

Fig. 13 shows the simulated transient output waveform of a triple-inverter Pierce oscillator without any center feedback network. After starting up rapidly at its parasitic oscillation frequency (left inset), the crystal oscillation eventually takes over (middle and right insets). The middle inset of Fig. 13 shows the superposition of the two oscillation modes, while the right inset shows the waveform after the crystal takes over, showing perturbations from the parasitic mode. Parasitic oscillations can cause phase-noise and start-up anomalies. The power consumption after the crystal oscillation takes over is 7.8 mW, higher than that of the TICF.

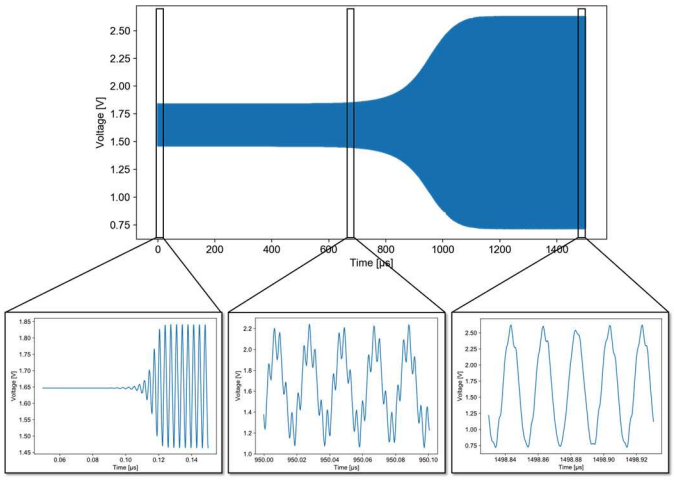

Fig. 13. Simulated transients for the triple-inverter Pierce oscillator (no center feedback) at node Vout. The three insets have the same 100 ns time window. The left inset shows the 288 MHz parasitic oscillation starting up almost immediately. The crystal oscillation frequency eventually starts (middle inset) and takes over (right inset), but the parasitic mode compromises the oscillator performance as well as increases the power consumption.

Table II summarizes the results discussed in this section, comparing the single-inverter Pierce oscillator with the TICF and the triple-inverter without center feedback.

TABLE II. SUMMARY OF SIMULATED OSCILLATOR RESULTS

	Single Inverter	**TICF**	**Triple Inverter, No R_F**
Transistor Multipliers	16	1, 1, 3	1, 1, 3
g_m at 50 MHz	21 mS	21 mS	~1.8 S
R_{out}	1.17 kΩ	5.67 kΩ	5.67 kΩ
Max resonator Rm for ½-rail Transients	230 Ω	330 Ω	
Phase noise at 1 kHz offset	-142 dBc/Hz	-135 dBc/Hz	
Idle Power	12.2 mW	6.9 mW	8.4 mW
Steady-state Power	9.7 mW	4.5 mW	7.8 mW

The benefit of adding the C_F in parallel with R_F in the TICF is the protection against resonator lead inductance. Fig. 14 shows the effect of a 25 nH inductance in series with the resonator for TICF oscillators with and without the 120 fF C_F. The C_F moves the potential parasitic phase crossover to a lower frequency than the resonance between the inductance and the resonator, thus avoiding a parasitic oscillation.

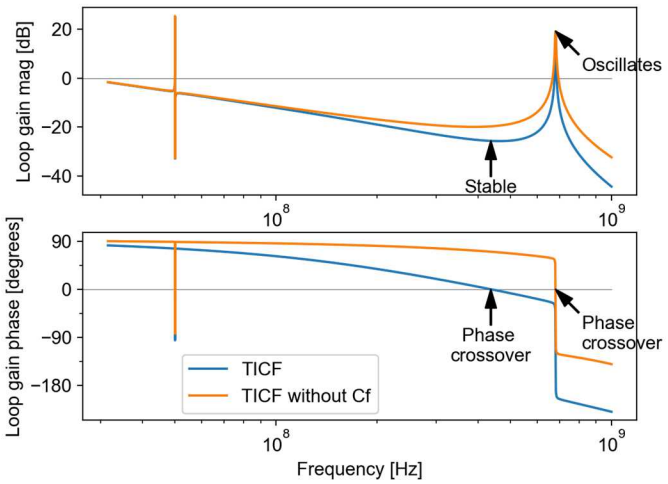

Fig. 14. Loop gain of TICF oscillator with 25nH lead inductance with and without 120 fF C_F in the center feedback, showing that parasitic oscillation can result from not having C_F.

IV. Measured Results

We designed and fabricated a 50 MHz clock/oscillator in our Sandia CMOS foundry using a TICF inverter of a similar design to that of the previous section. It worked as intended and measured very close to the simulations and design goals. Fig. 15 shows the measured waveforms at the TICF input and output nodes.

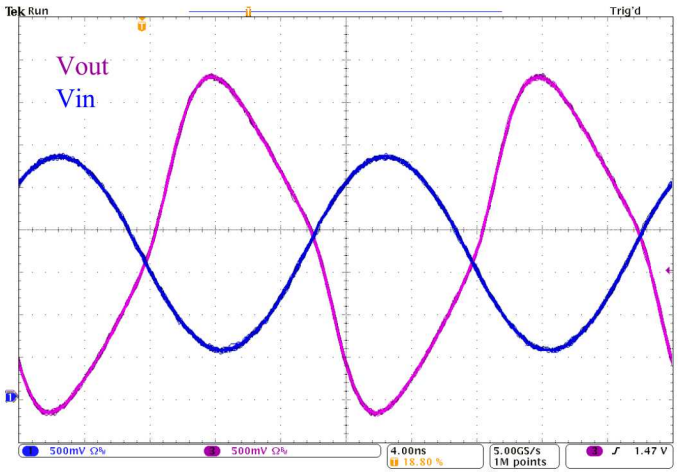

Fig. 15. Measured steady-state waveforms of the fabricated TICF oscillator

Due to parasitic capacitances degrading phase, the measurements for g_m were conducted at 25 MHz. Tables III and IV show the experiment's design goals and measurements. The modeled, measured, and calculated transconductances are in good agreement. The calculated g_{mt} is higher than the model due to the use of switches in the P device sources, not taken into account in equation (12). The measured versus calculated R_{out} values show a significant difference likely due to process variations from the model. The transconductance is far less dependent upon this parameter.

TABLE III. TICF Transconductance Design and Measurements

g_{mt} Design Goal 50 MHz @25°C Nominal	**Simulation 25 MHz**	**Measured 25 MHz**	**Calculated Baseline**
30 mS–15 mS	25 mS	20 mS	29 mS Eq (12)
Phase > 160°	173°	167°	N/A

TABLE IV. TICF Output Resistance

R_{out} Calculated from SPICE Model	**Measured R_{out}**
7 kΩ Eq (13)	20 kΩ

V. Conclusions

A new CMOS oscillator architecture that allows high transconductance with improved design flexibility over a single inverter has been presented. These simulations and data show how a triple inverter can be utilized with feedback in the center stage to have a very high transconductance while operating in a well-controlled manner, free of parasitic oscillations. The TCIF operation strongly agrees with the simulations conducted on all parameters. This design has advantages over a large area single-inverter in both physical size and circuit performance such as power consumption and circuit parameters such as output-impedance when designed for an equivalent transconductance. The TICF has been implemented and patented, we have used it reliably in multiple applications and frequencies. This design also may have advantages in MEMS or low-frequency tuning-fork resonator applications.

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