SAND2019-3928C

A Novel Triple Inverter Design for CMOS Clocks and Oscillators

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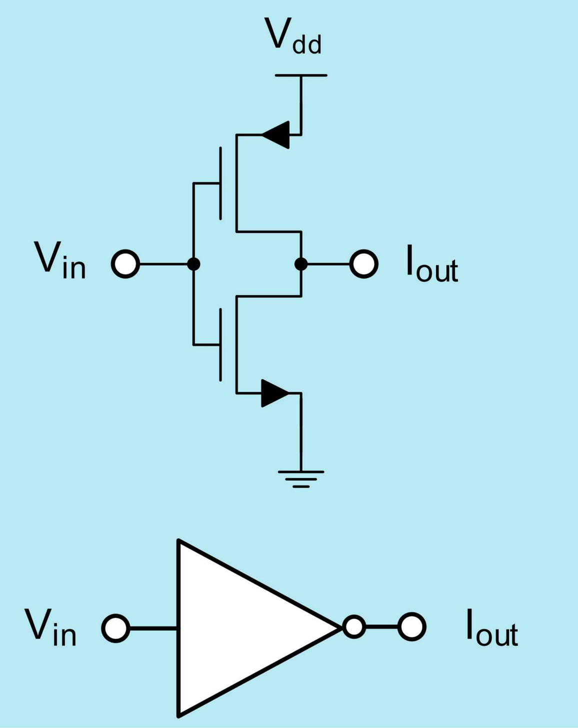
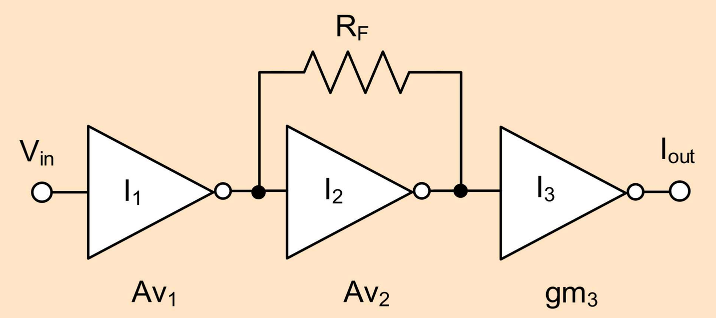
CMOS Inverter



TICF Design Equations



$$Zin_2 \approx \frac{1}{g_{m2}}\left(\frac{r_{O2}+R_f}{r_{O2}}\right)$$

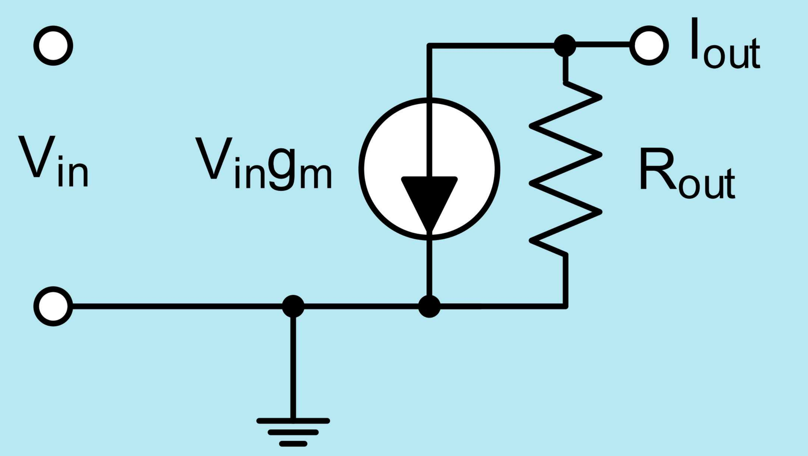
$$Av_2 = (1/R_F - g_{m2})\left(\frac{R_F r_{O2}}{R_F + r_{O2}}\right)$$

$$Av_1 \approx -\left(\frac{r_{O2}+R_f}{r_{O2}}\right) \approx -1$$

$$g_{mt} \approx (1 - g_{m2}R_F)g_{m3}$$

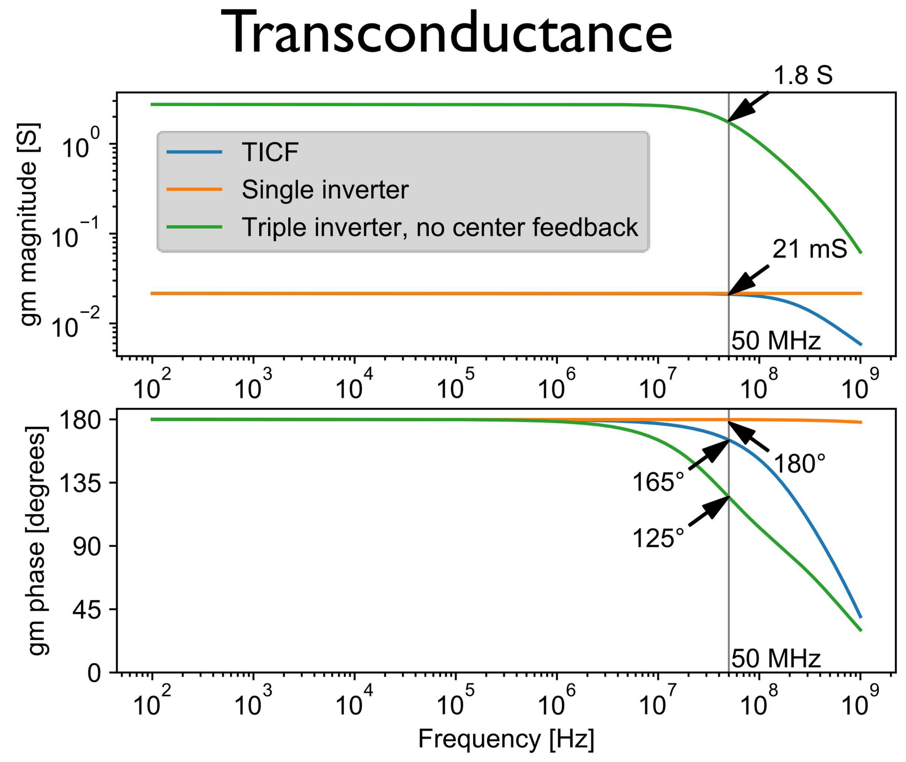
- Allows well controlled high g_m with wide operational BW
- Flexible control of sustaining amplifier design parameters
- Low current operation due to cascaded gain
- High in and out impedance

Transconductance Model

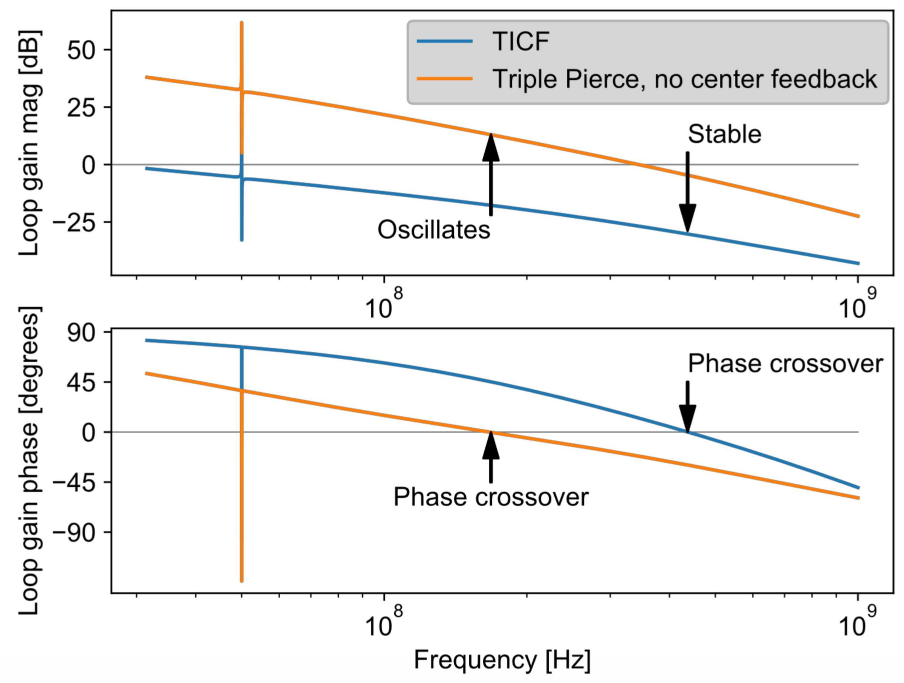


- Inverting voltage to current amplifier
- High in and out impedance

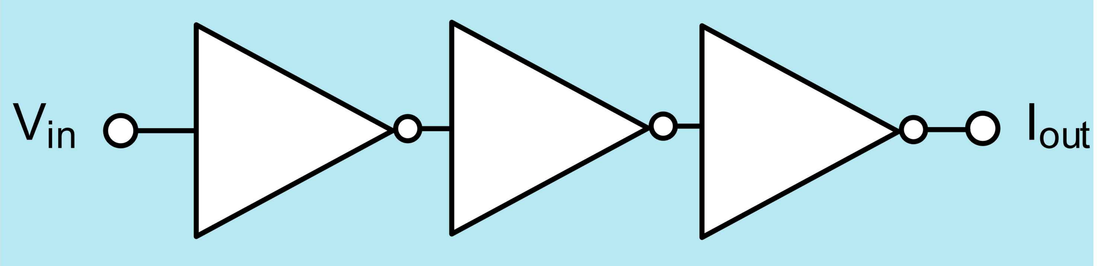
Transconductance



Oscillator Loop Gain



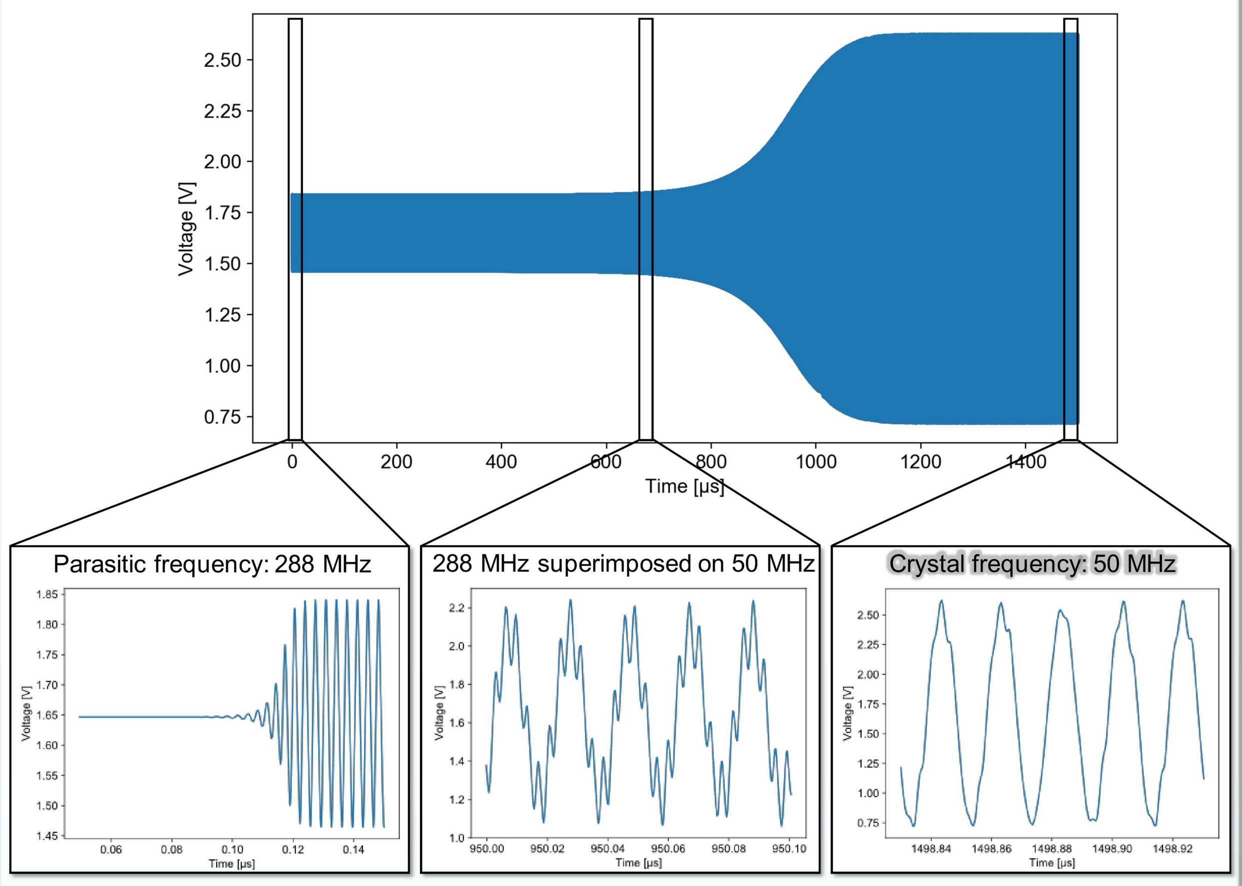
Triple Inverter to Increase g_m



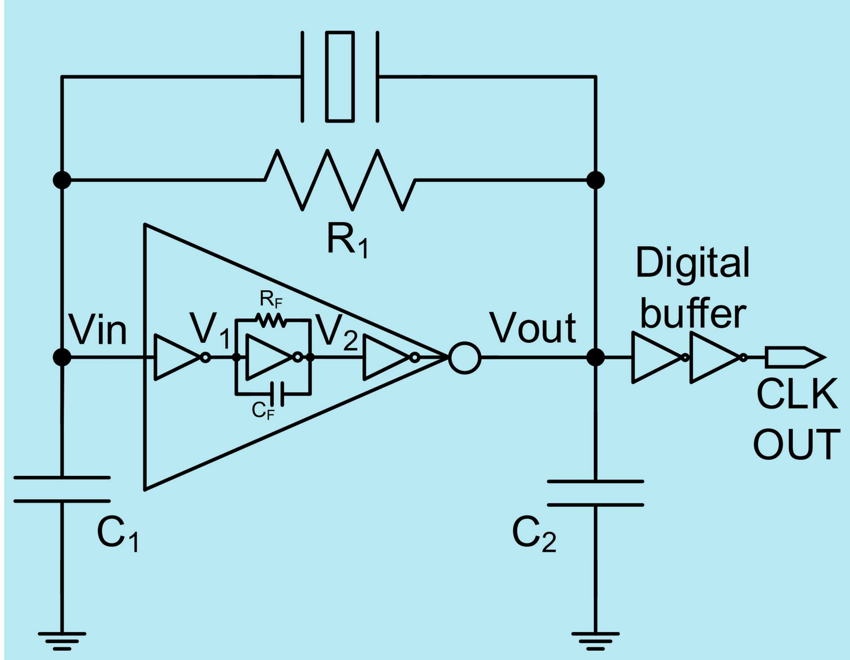
- Huge effective g_m at a cost:
- Poor operational bandwidth
- Strong parasitic oscillation
- Unreliable operation, "loose canon"

Simulation	Single inverter	TICF	3 inverter, no middle R
Transistor multipliers	16	1, 1, 3	1, 1, 3
g_m at 50 MHz	21 mS	21 mS	~1.8 S But has gain at parasitic frequency
R_{out}	1.17 kΩ	5.67 kΩ	5.67 kΩ
Max resonator Rm for ½-rail transients	230 Ω	330 Ω	
Phase noise at 1 kHz offset	-142 dBc/Hz	-135 dBc/Hz	
Idle power	12.2 mW	6.9 mW	8.4 mW
Steady-state power	9.7 mW	4.5 mW	7.8 mW

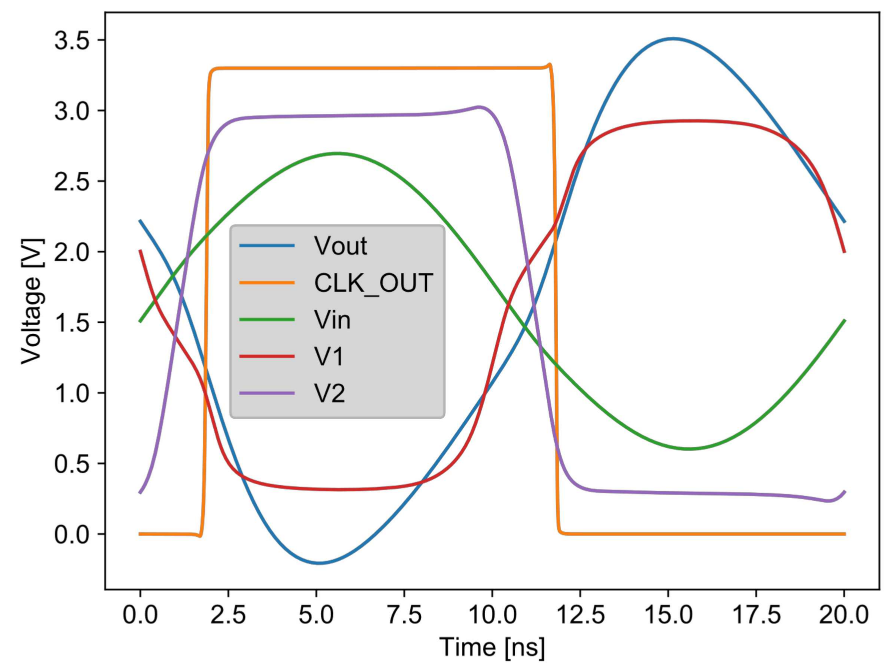
Triple-inverter Pierce without center feedback



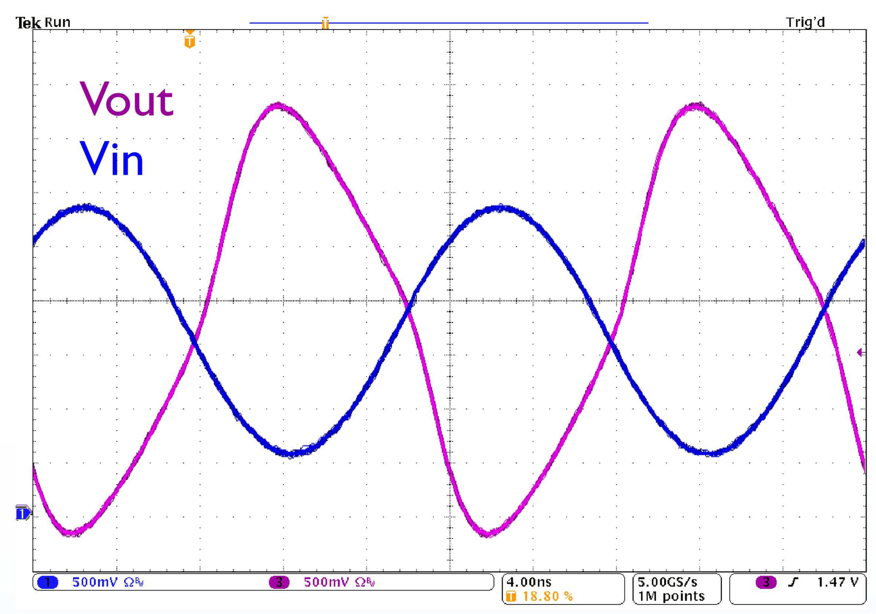
TICF Design Practical Pierce Oscillator



TICF Pierce Steady-State Waveforms



Measured TICF Pierce Steady-State Waveforms



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