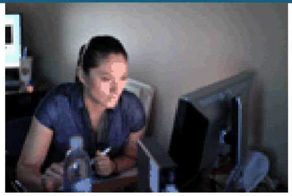
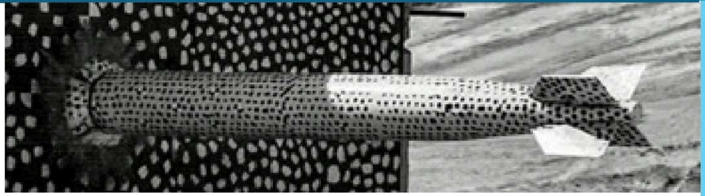
SAND2019-3599C

Die Level Microbumping and Flip Chip Bonding for MPW Die





PRESENTED BY

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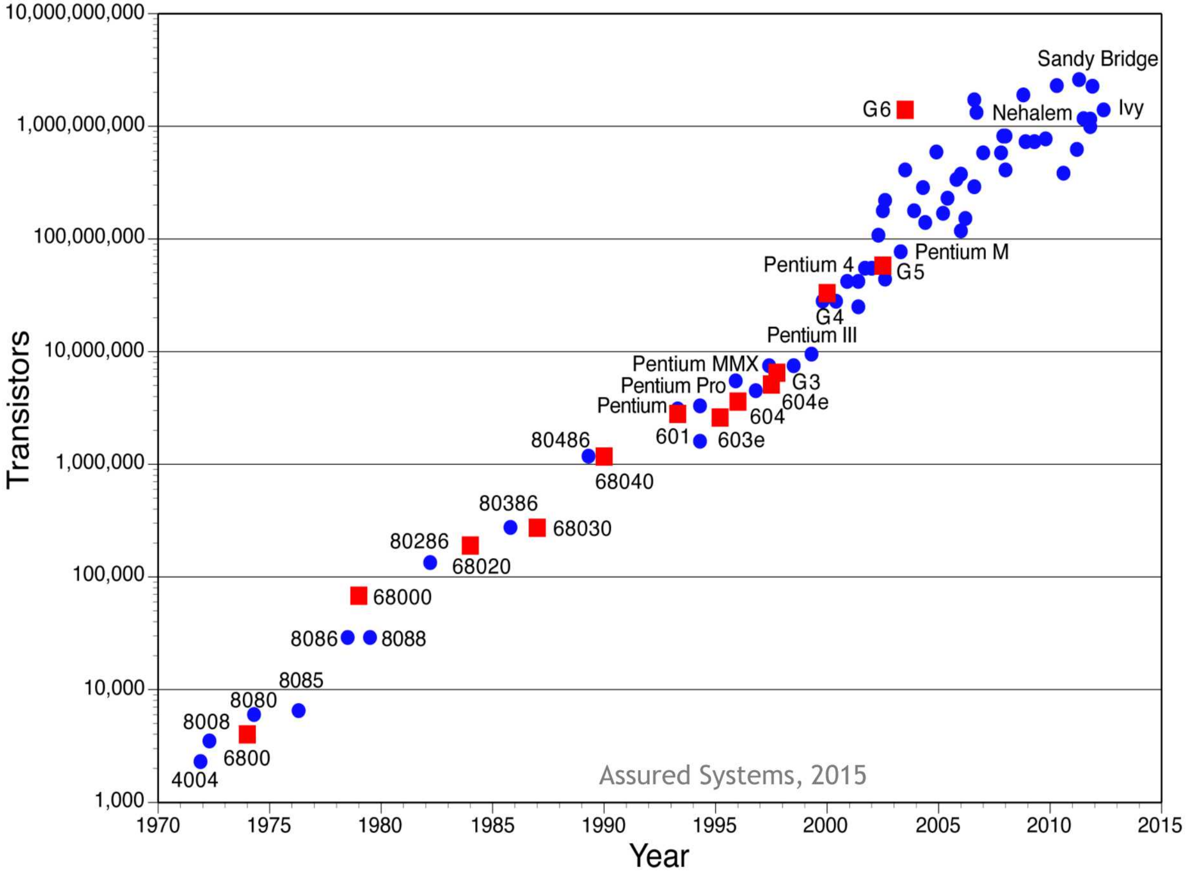
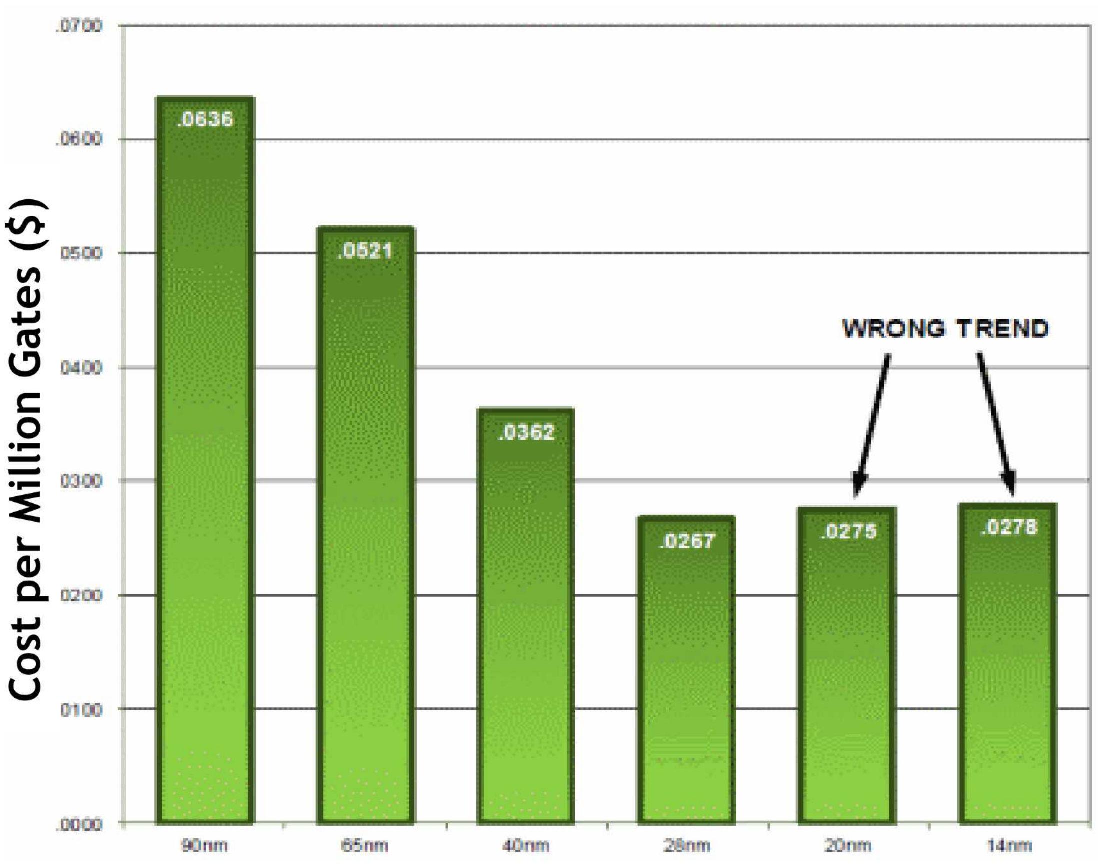
Moore's Law - Continued Scaling

Transistor density continues to increase



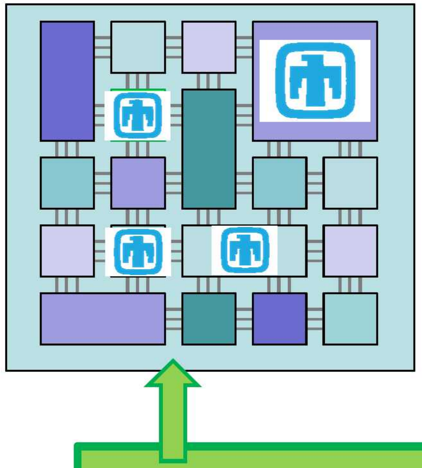
Cost per transistor is increasing

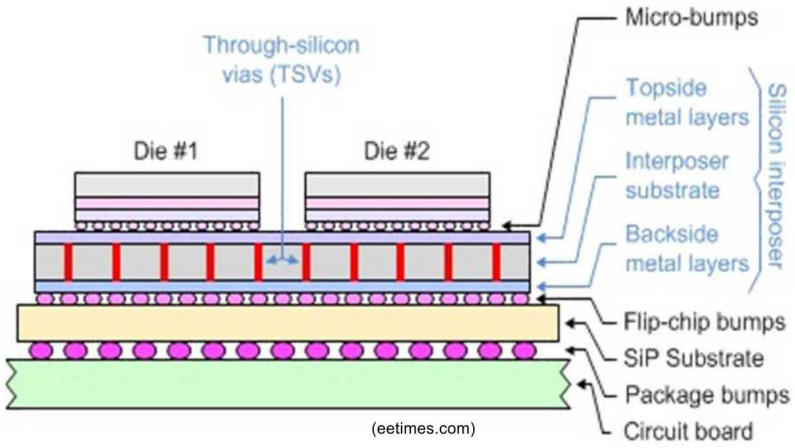


Handel Jones, IBS 2012

2.5D/3D Heterogeneously Integrated Microsystems

2.5D "System in Package"





Flexible Interconnect Fabric

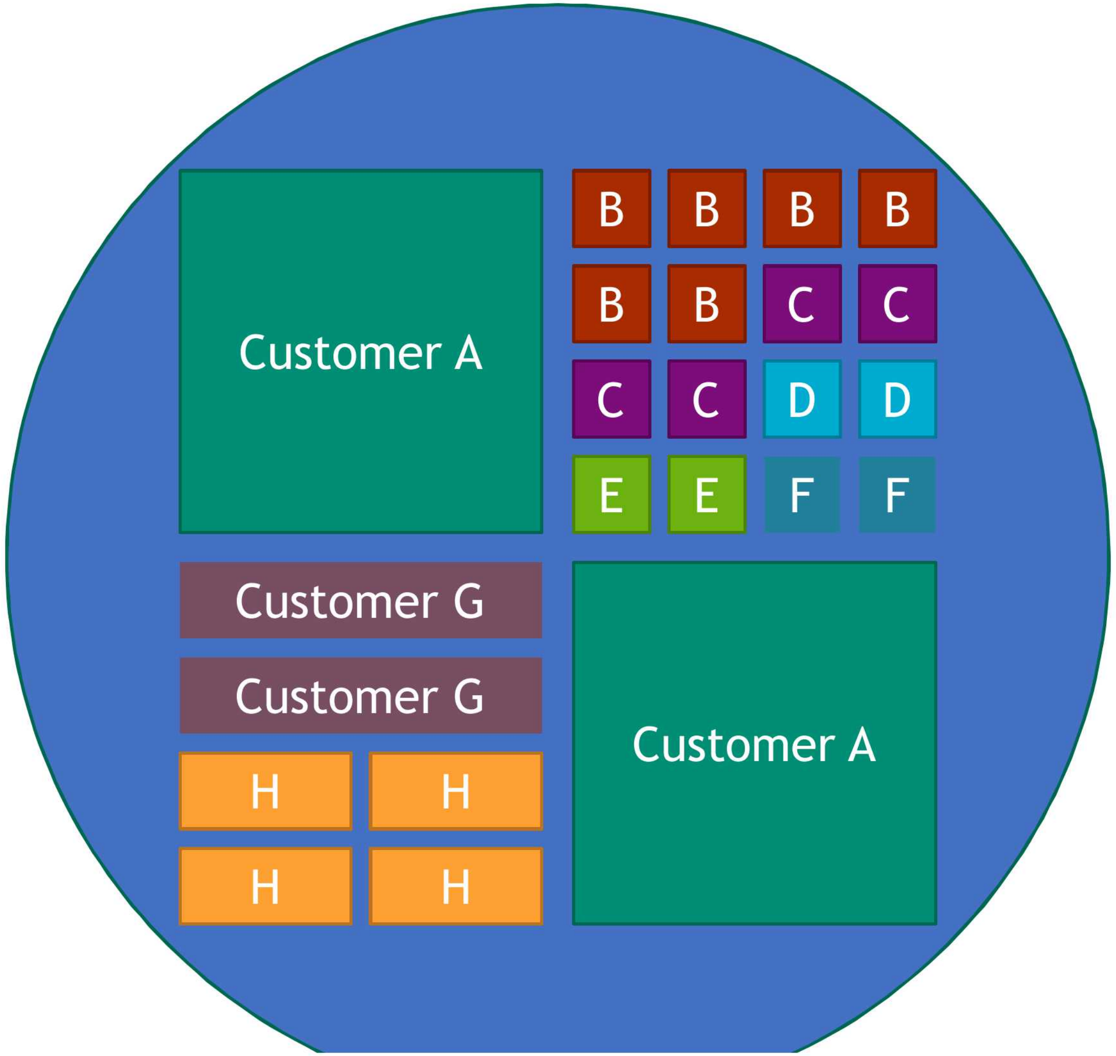
→ Multi layer high density routing
→ Massively parallel I/O for future functions (performance, rad-hard/trust functions)
→ Low latency, low packaging parasitics

- 2.5D Integration on Interposer
  - Use Sandia tech, COTS, MPW die, partner die, etc. in low volumes
  - Partially disentangle issues of performance, radiation hardness, etc.
  - Standardized digital/analog/power buses
  - Limited BEOL processing for interconnect (no TSVs thru function die, limit process incompatibilities)
  - Pre-build active device blocks
- Heterogeneous Integration
  - High-value functions in custom technologies
  - Unlock performance of disparate technologies
  - Internal and external tech: III/Vs, MEMS, photonics, etc.

Challenge: Microbumping for low-volume USG applications (DOE, DOD, etc.)
Current options: High Labor Cost - or - High Fab Cost

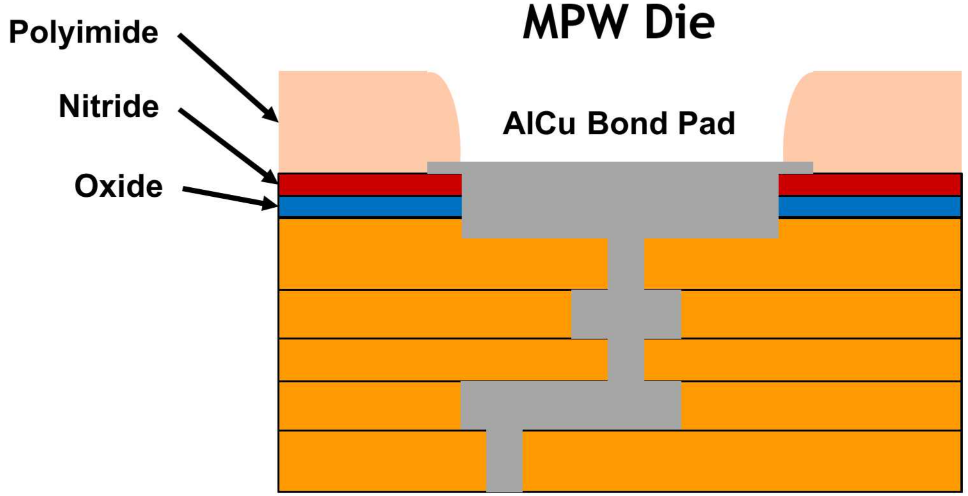
Multi-Project Wafers (MPW)

MPW Wafers

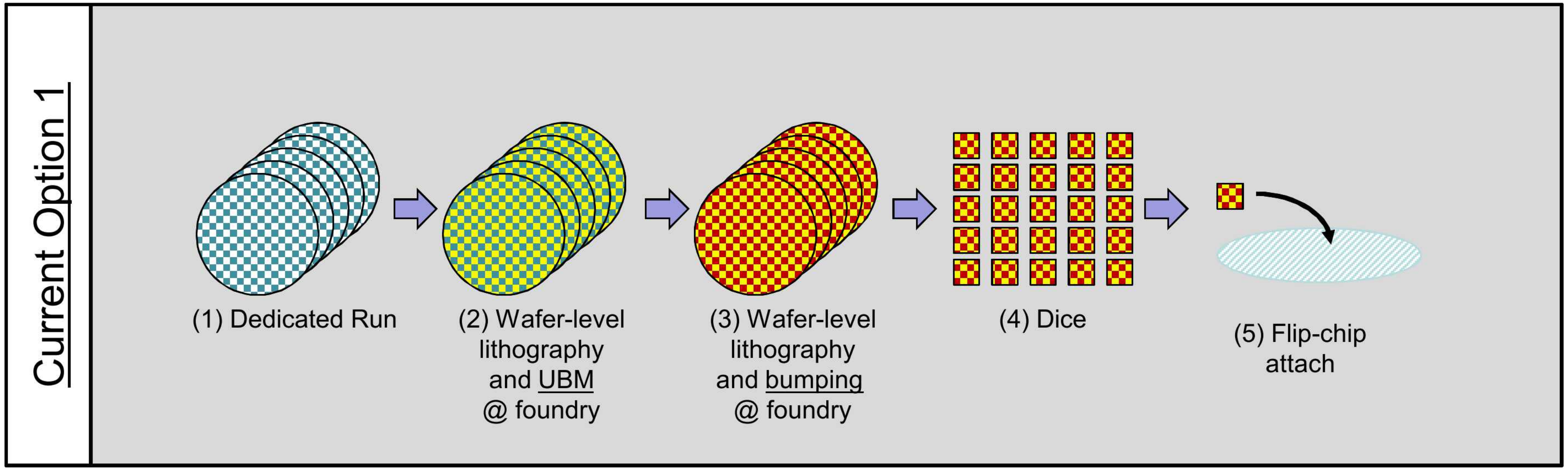


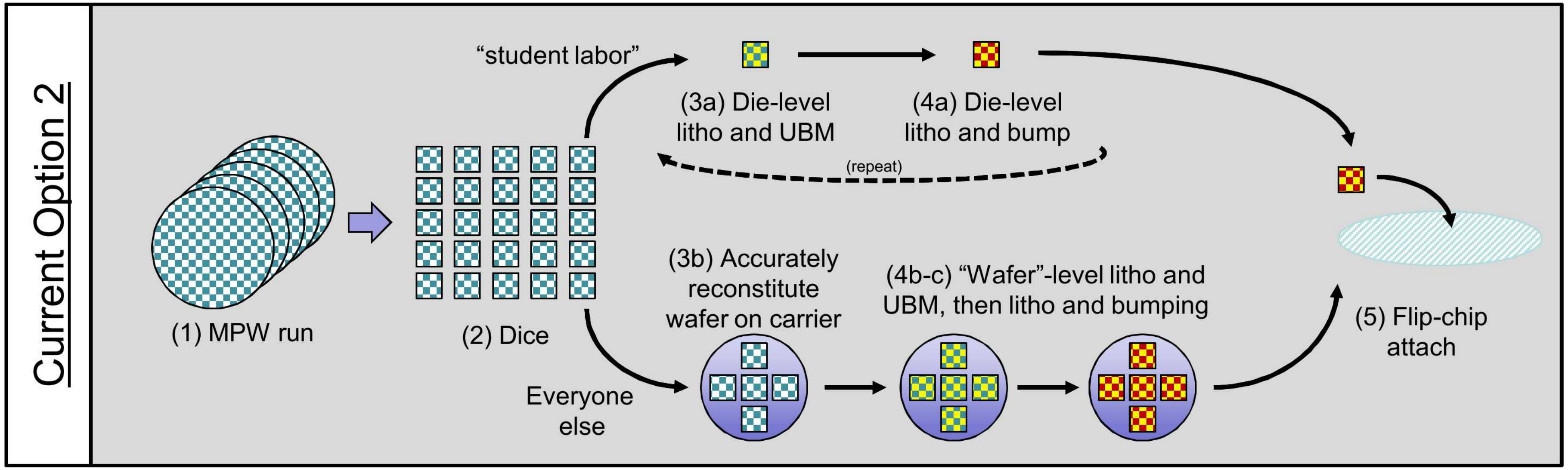
- Costs of a run are distributed across many different customers (10s-100s k$)
- Access to high performance technology nodes
- Must follow standard process flow and design rules
- Die ready for flip chip bonding isn't always an option

MPW Die



Challenges with MPW Die: Foundry CMOS + Advanced 2.5D

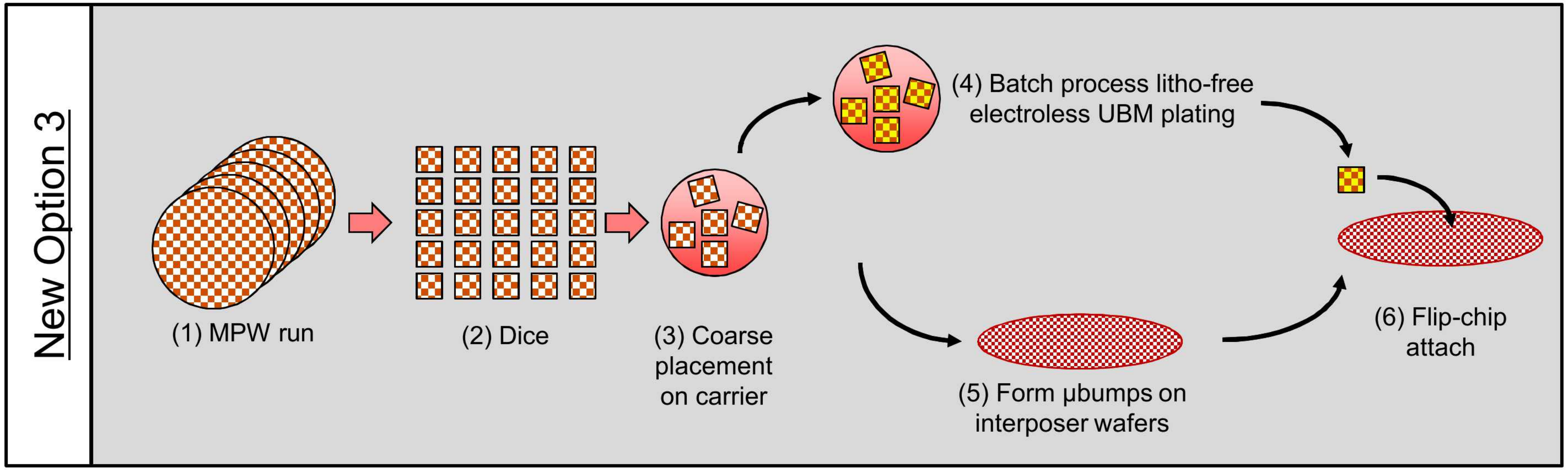




Challenges with Low Volume, High Value 2.5D Integration

Very Low Volume ≈ 1 - 100 die	Low Volume ≈ 100 - 1000s of die	Mid-high volume ≈ > 1000s die
Use interns/students/postdocs Feasible for demonstrations and development	Utilize interns, students, postdocs… (but they hate you) Make a wafer-like substitute at OSAT $$$ Spend lots of $$$ and purchase full wafers from a foundry	Buy a dedicated run at an advanced foundry

Proposed Solution: Lithography Free Batch Level Processing



Benefits:

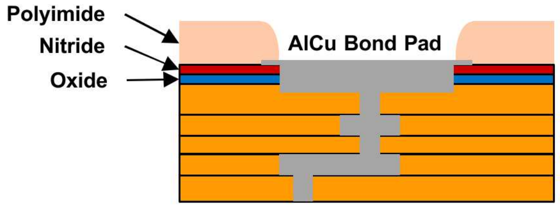
- Massive cost savings through MPW runs
- Batch process with no fine alignment
- Lithography "free"
- Wafer-level interposer bumping @ legacy fab

What you'll see today:

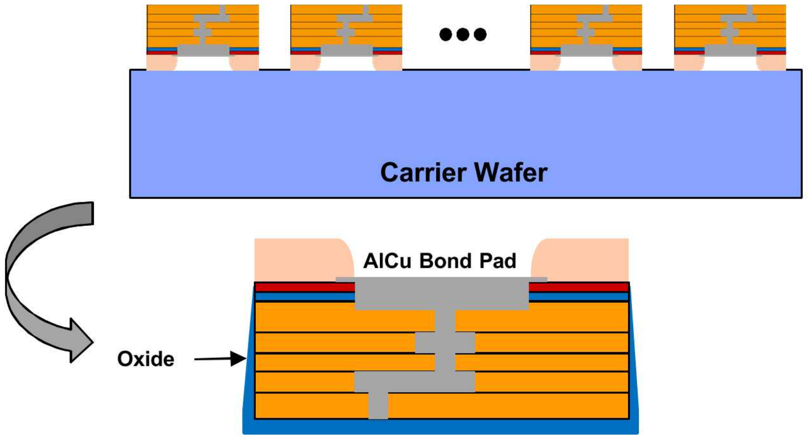
- Proposed process
- Batch-level UBM preparation for singulated die
- Two flip chip approaches and µ-bump development

Die Level UBM Preparation

1. As received MPW die with AlCu bond pads

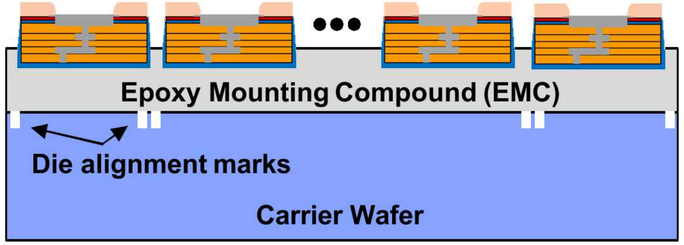


2. Flip die upside down onto carrier wafer and deposit 1 µm CVD TEOS to passivate exposed Si

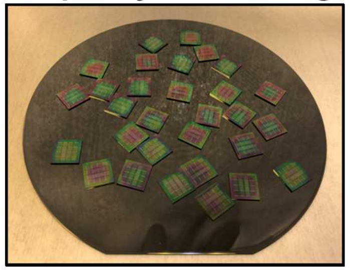


- Exposed Si disrupts ENEPIG/ENIG electroless deposition and must be passivated
- 10% thickness coverage on sidewall
- No temporary bonding media necessary

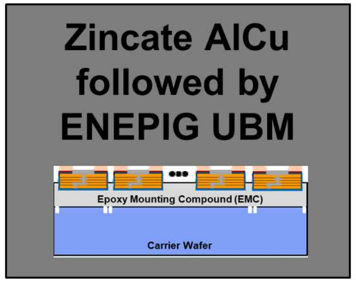
3. A temporary epoxy mounting compound (EMC) used for batch level UBM deposition



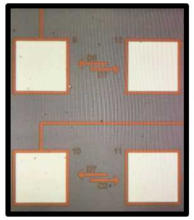
Temporary Die Bonding



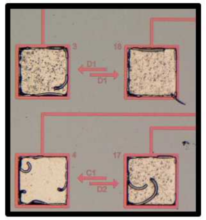
4. Batch electroless UBM deposition.
ENEPIG = electroless Ni, electroless Pd, immersion Au.



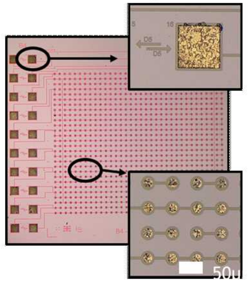
AlCu Pads



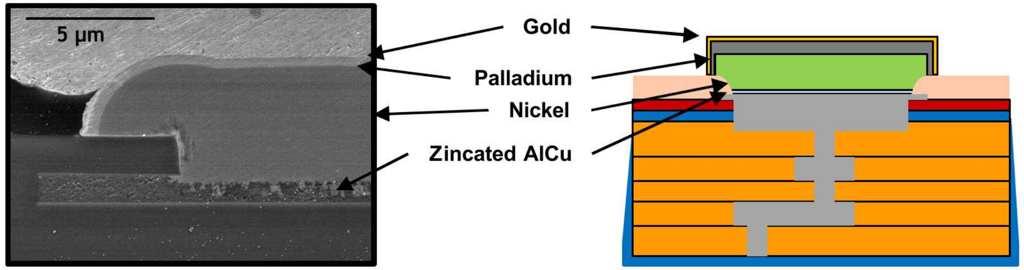
Zn + Ni



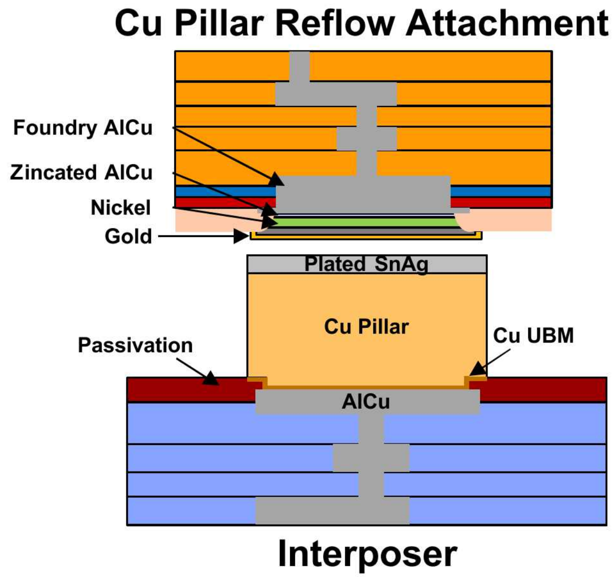
ENEPIG

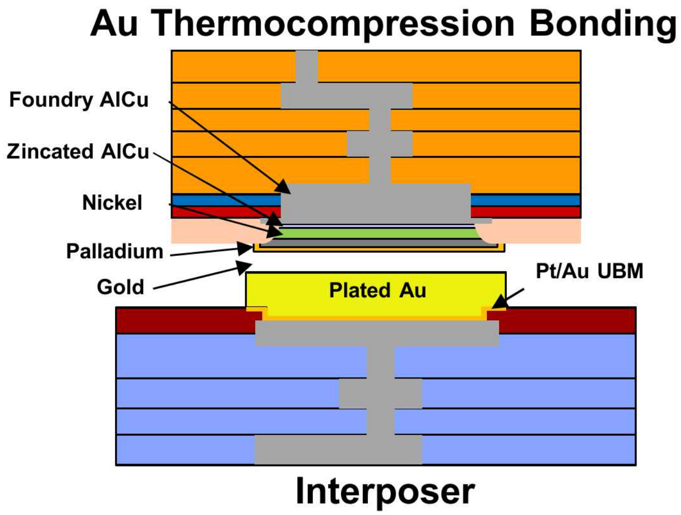


5. Solvent release die from EMC and die are ready for flip chip bonding



Micro-bumped Interposers

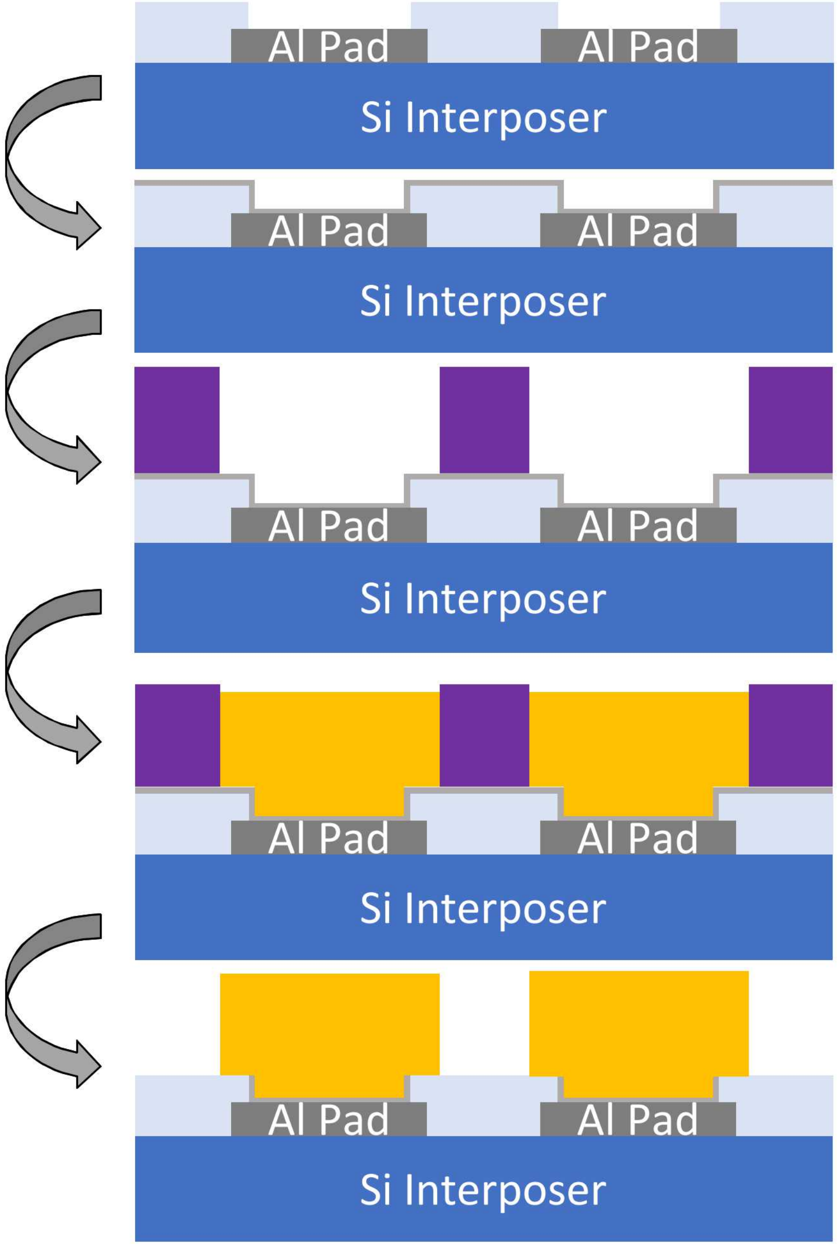




- Reflow solder attachment
- Wide-spread industry adoption
- Intermetallic formation concerns
- Height determined by Cu pillar
- Pd not necessary
- Rigidity has potential mechanical reliability concerns
- SnAg defines temperature constraints (challenging integration with TSV thinning)

- Thercompression bonding (TCB)
- Less reactive, more ductile than Cu
- TCB usually has thick Au on both sides
- Au to ENEPIG bonding needs to be evaluated
- TCB force may damage low-k dielectrics
- Potentially compatible with TSV thinning and TSV pad formation processes

Interposer Preparation



Recipe Conditions

Coat Recipe:

- # 762-JMC PLATING TEST
  - AZ 40xT Coat
    - 1200 RPM
  - Soft Bake
    - 125°C/120 sec d@ 1.27 mm
    - 125°C/120 sec @ 0.63 mm
    - 125°C/180 sec @ 0.00 mm

EBR Recipe

- #763 JMC 40XT EBR
  - 7mm edge bead

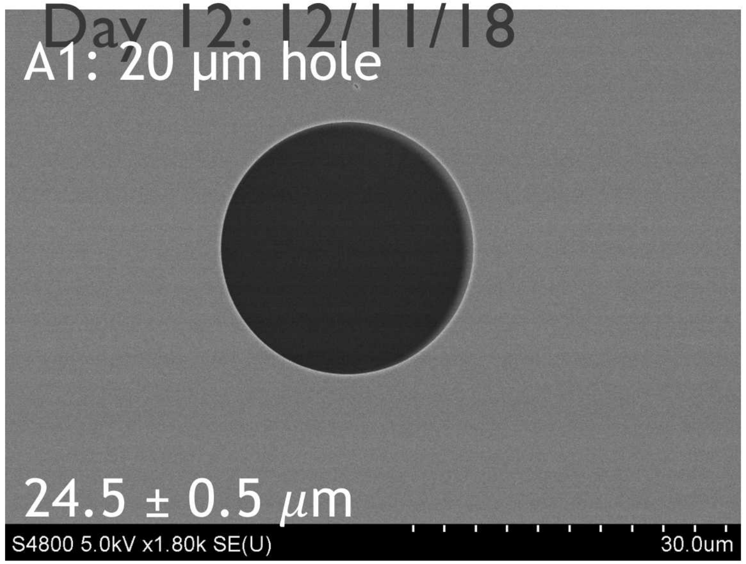
Exposure

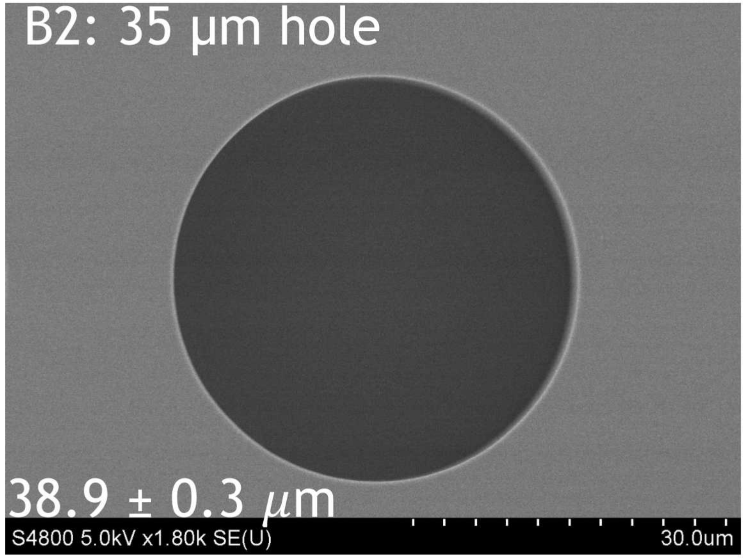
- Hard contact (0.3 Bar WEC), 36s exposure energy

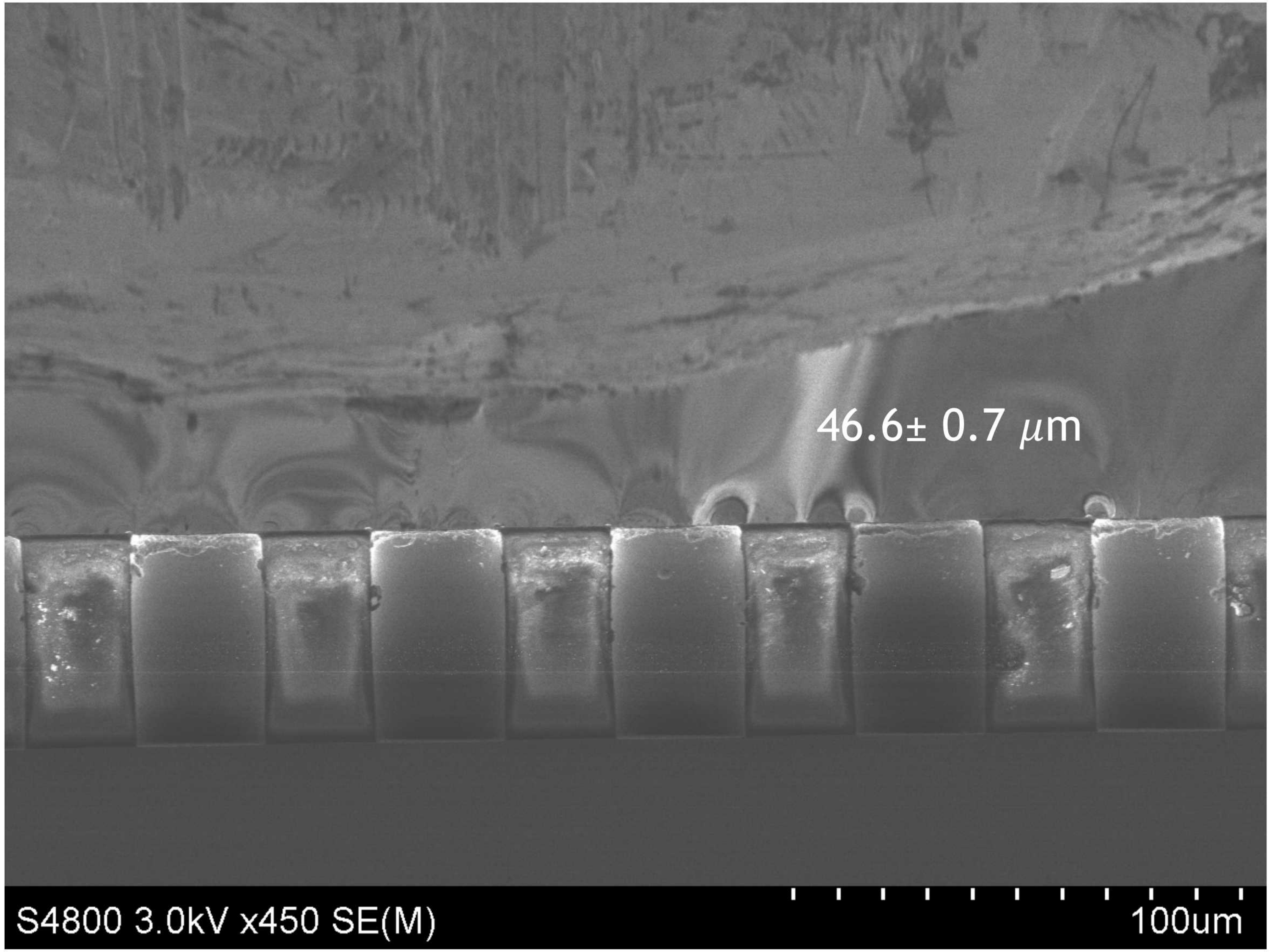
PEB and Develop

- #764 JMC PEB 40XT
  - PEB
    - 110°C/10sec @ 1.3mm
    - 110°C/10 sec @ 0.6 mm
    - 110°C/ 80 sec @ 0.0 mm
  - Developer
    - MIF 30s puddle x 6

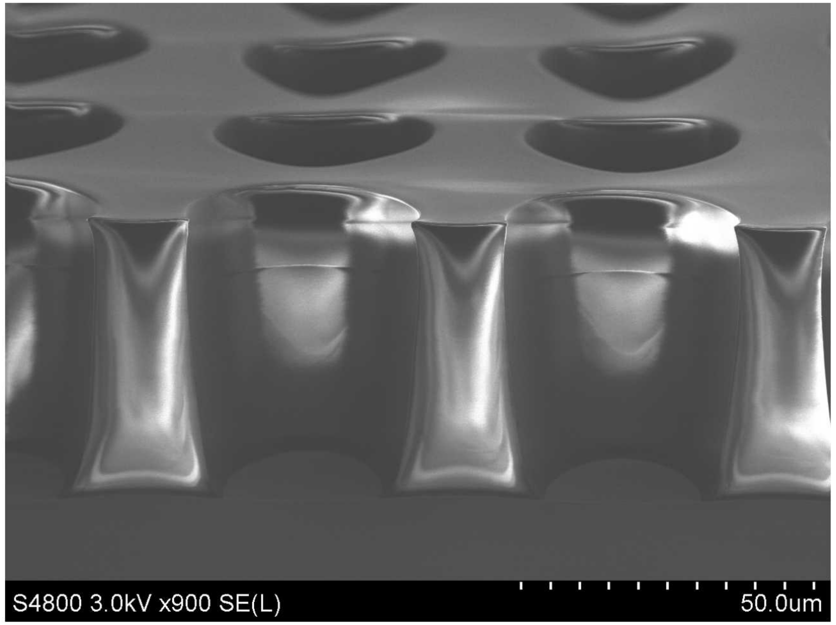
Day 12: 12/11/18



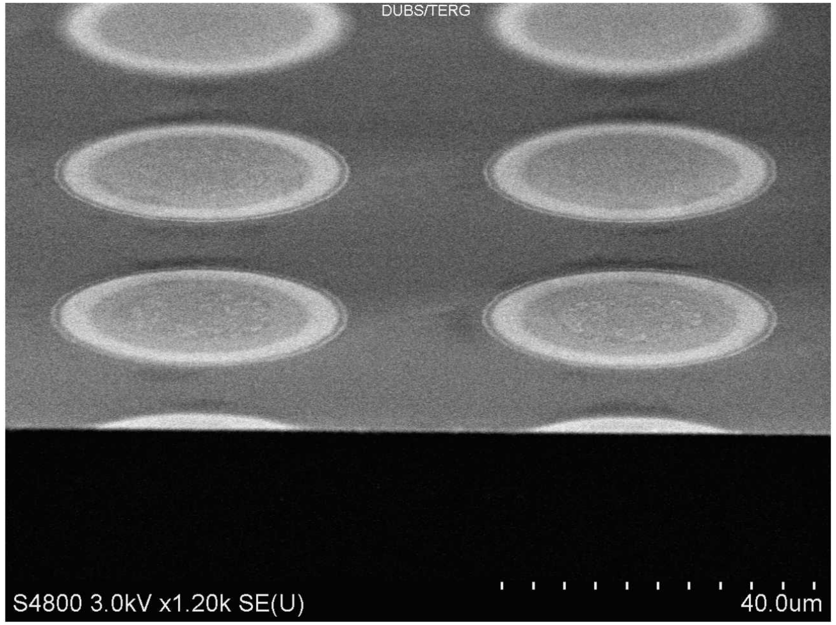




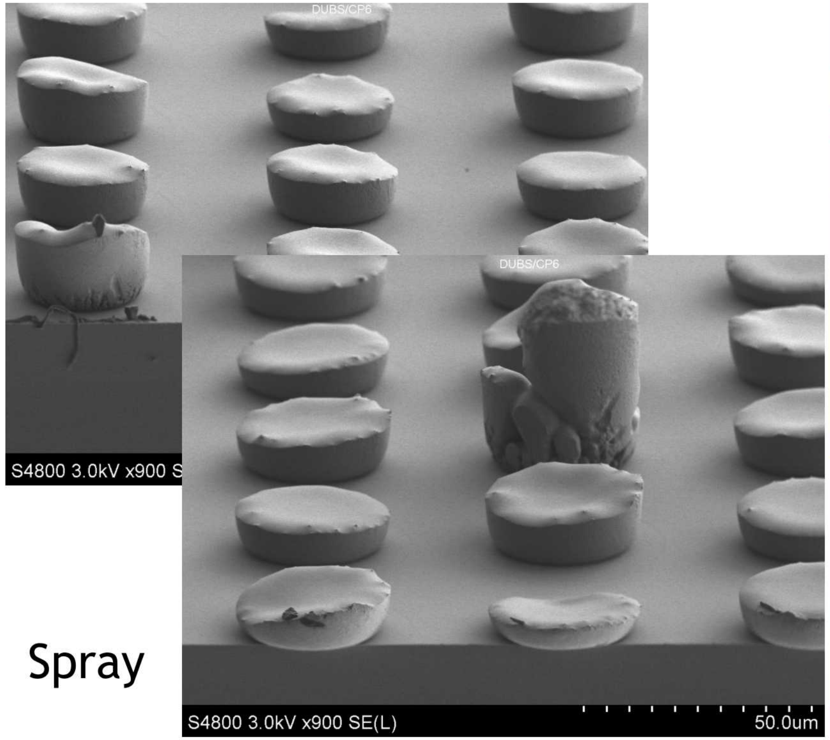
Copper Pillar Bump Development – Prewet conditions



No Prewet



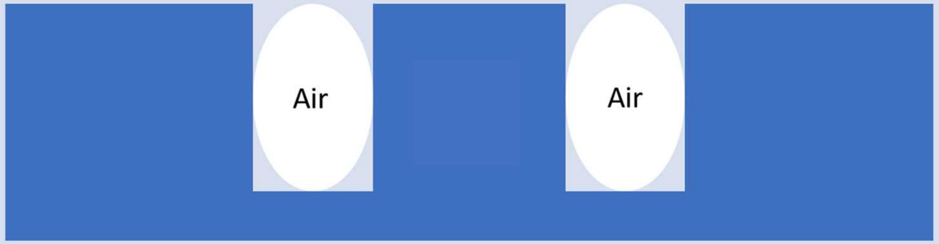
Tergitol



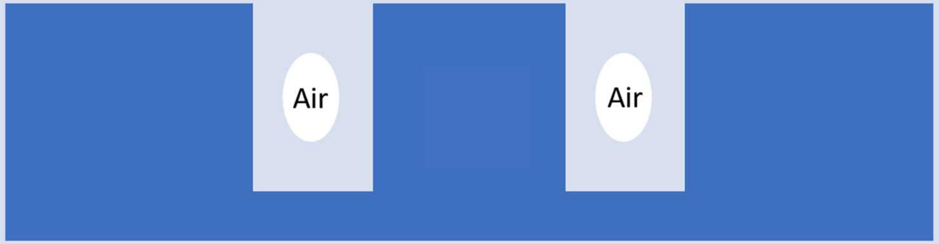
Spray

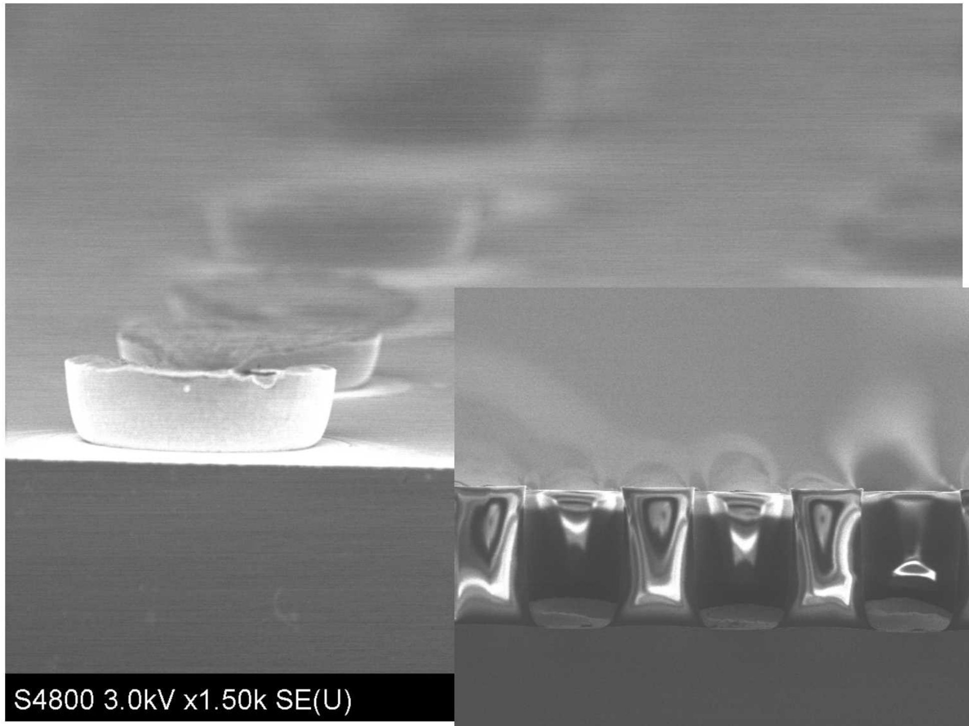
Copper Pillar Bump Development - Vacuum Prewet

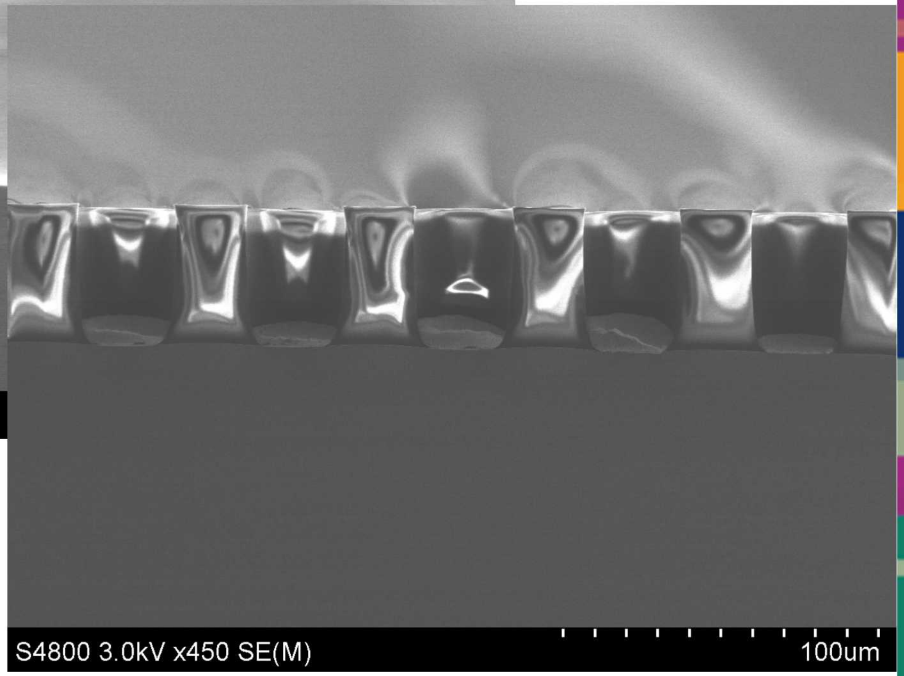
Air bubbles can become trapped
in high aspect ratio features



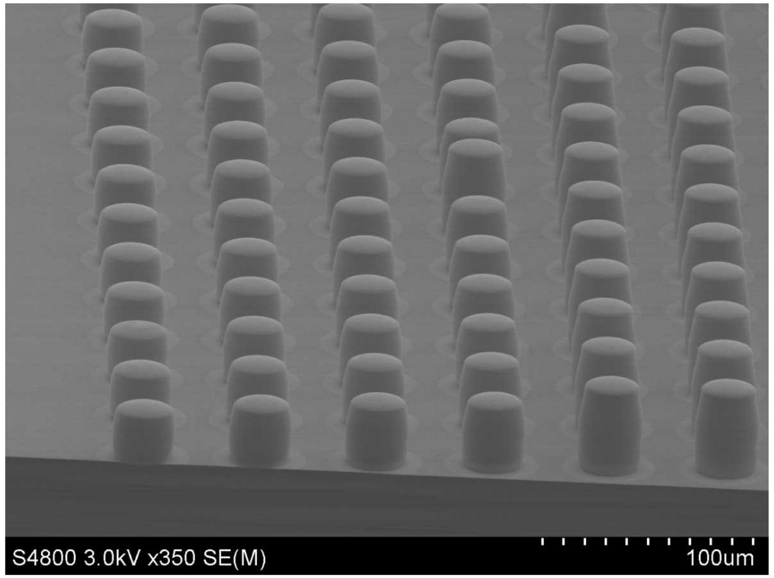
Applying a vacuum before wetting
reduces the volume of the bubbles
Allowing them to escape when returned to atmosphere

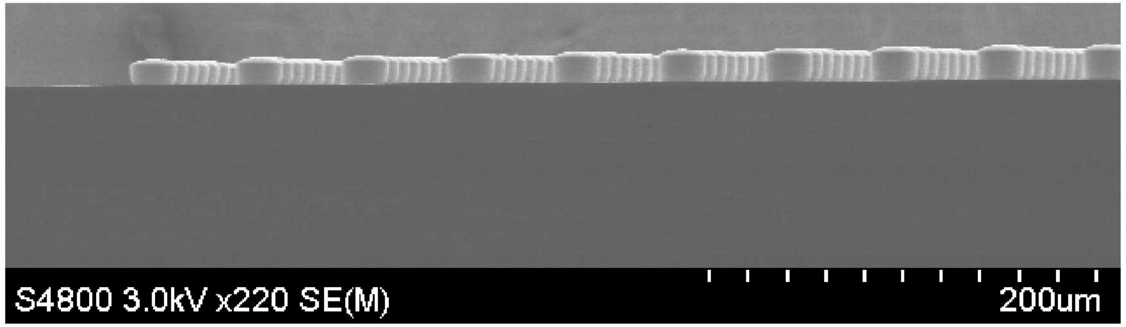






Problem Statement





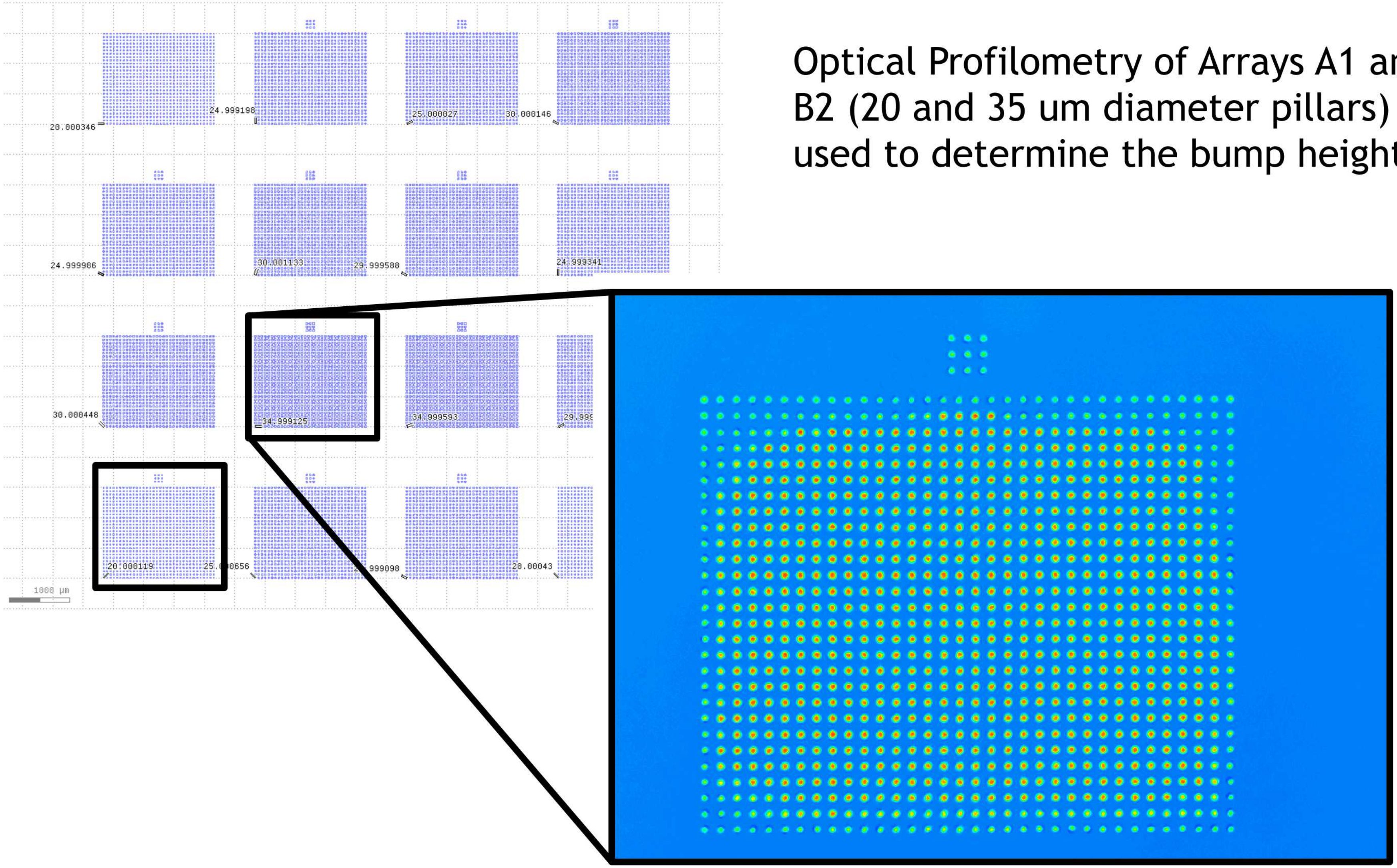
There's a height difference of the pillars towards the edge of the array.

Trackable Data

Keyence

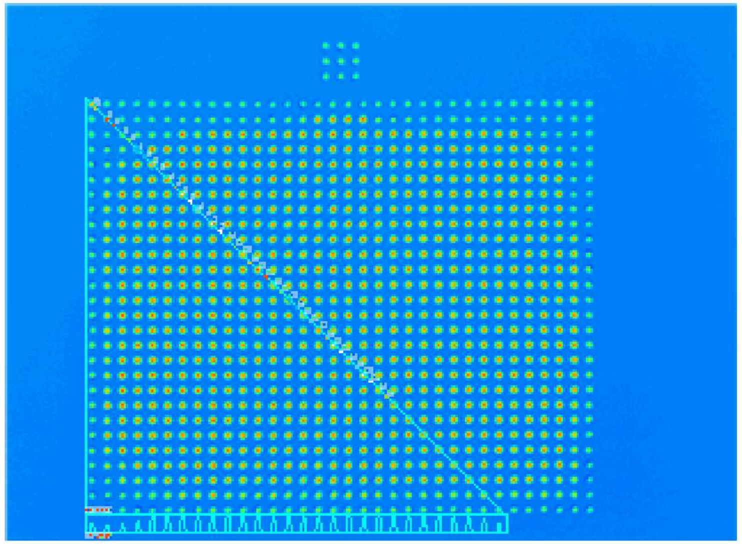
SEM

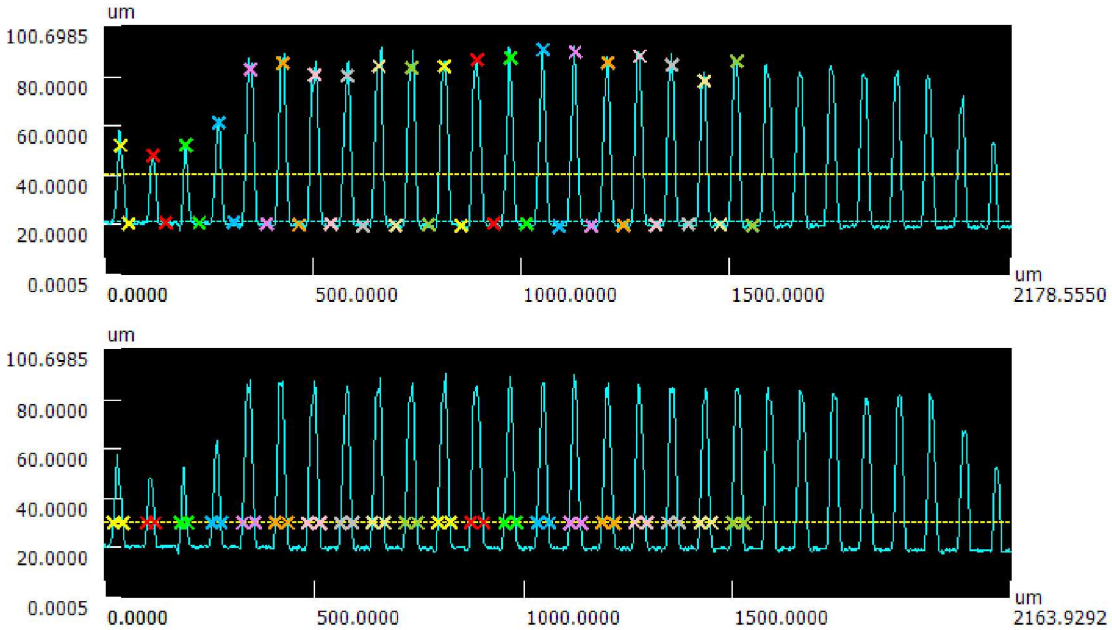
Experiment – Results Methodology



Optical Profilometry of Arrays A1 and B2 (20 and 35 um diameter pillars) was used to determine the bump heights

Experiment – Results Methodology





- Two Diagonal profiles are used (top left -> bottom right and top right -> bottom left)
- 20 measurements per profile give the heights of the bumps (center floor to center top) and the widths (determined near the bottom)

- Note: Widths are not 100% accurate due to method of measurement. Can compare widths within the same run but not well run to run.

Experiment

DC plating experiments

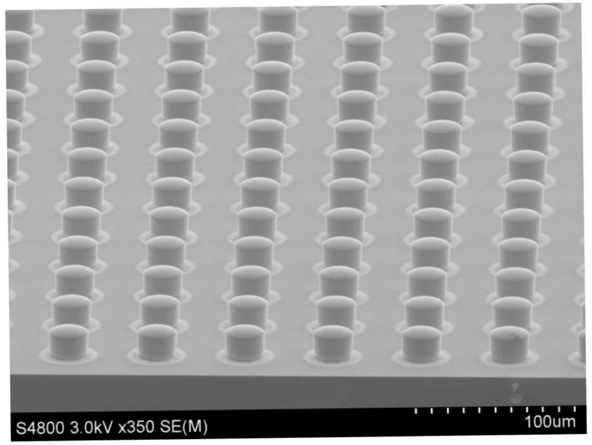
Just rotation rate

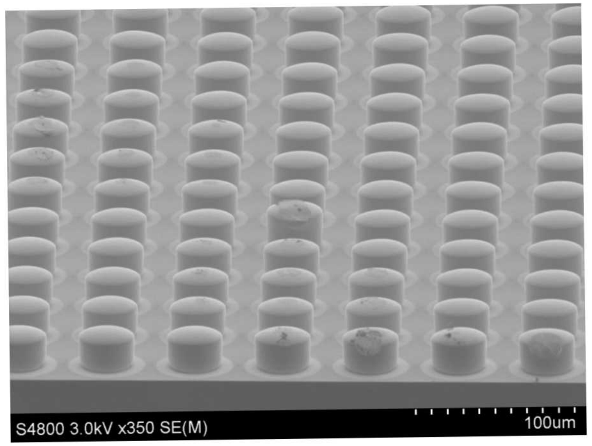
Full Factor DOE on rotation and reverse plating

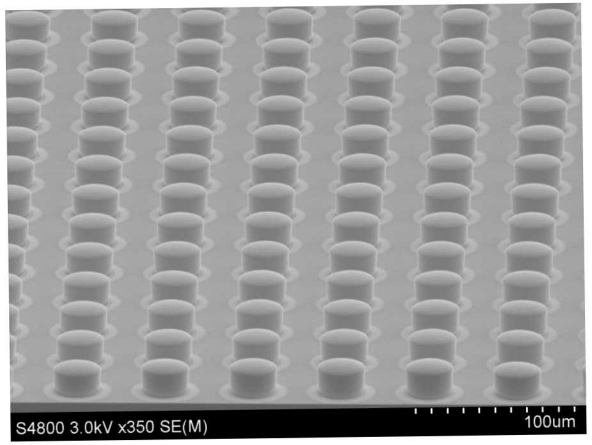
Run	Spin	Reverse Pulse (ms)	Reverse Current (mA)	Rest time
1	40	0	0	0
2	200	0	0	0
3	200	0	0	1
4	40	1	7	1
5	40	1	15	1
6	40	10	7	1
~~7~~	~~40~~	~~10~~	~~15~~	~~1~~
8	200	1	7	1
9	200	1	15	1
10	200	10	7	1
~~11~~	~~200~~	~~10~~	~~15~~	~~1~~

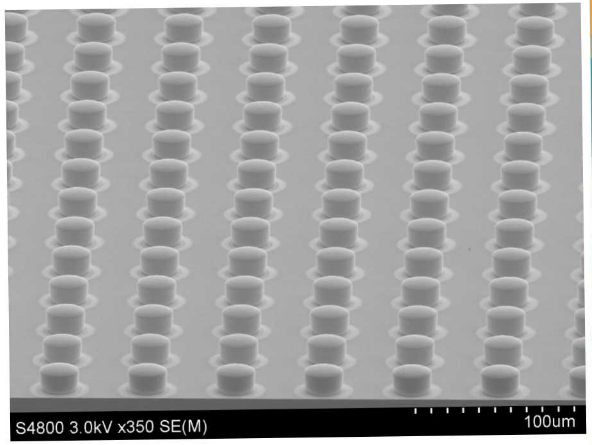
Note that 15 mA for 10 ms is more than the forward charge… Not running numbers 7 and 11

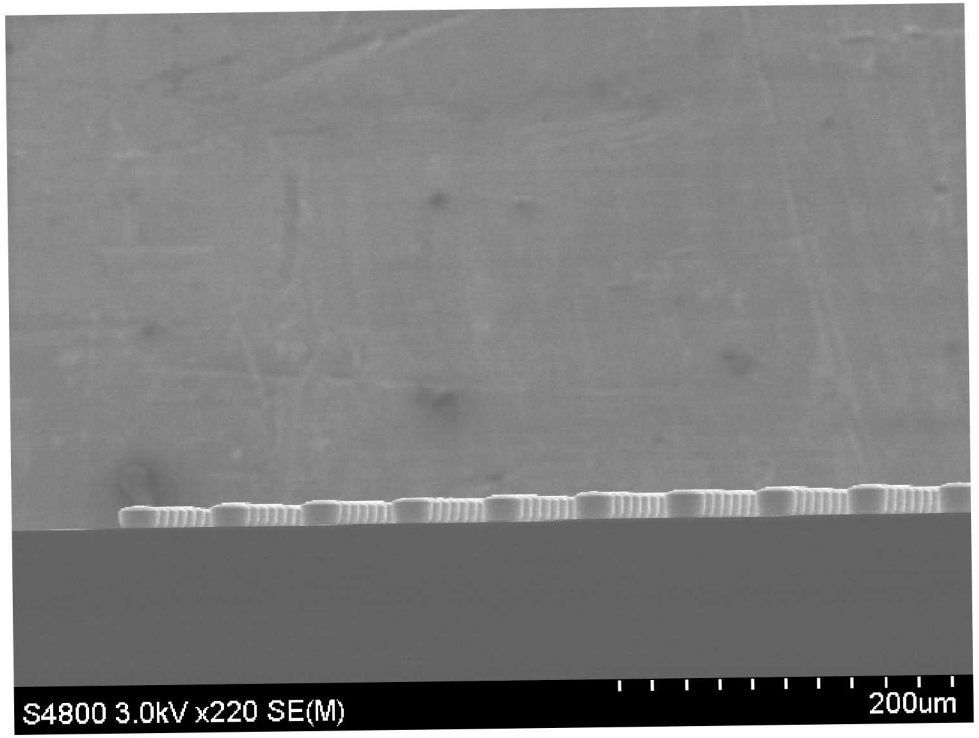
Copper Bump Development – Tune Additives and Current Density

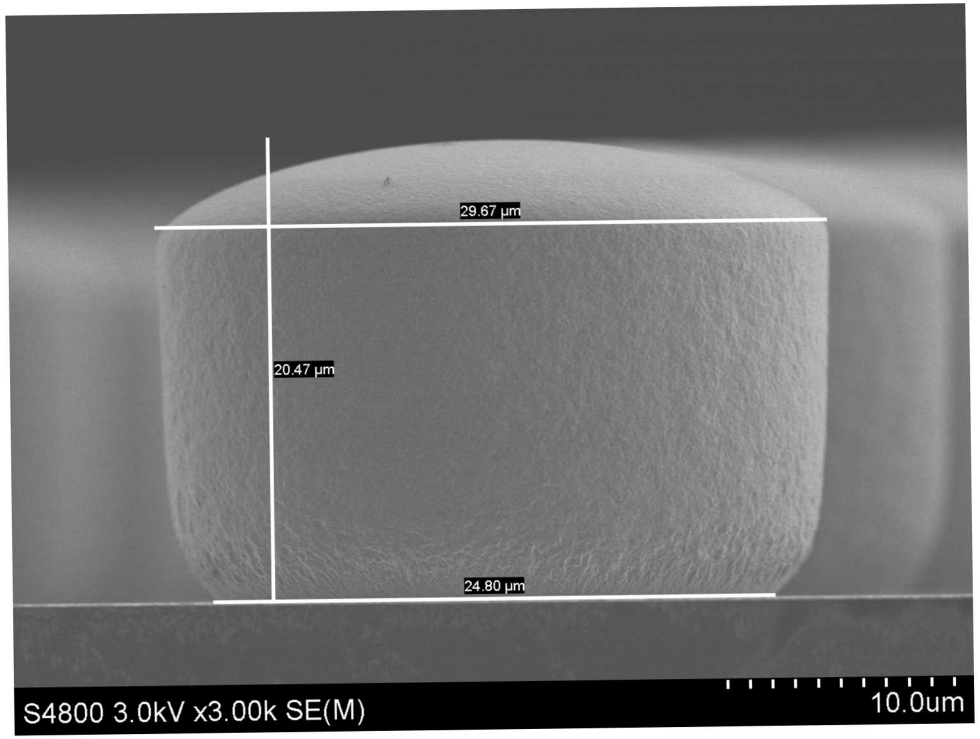




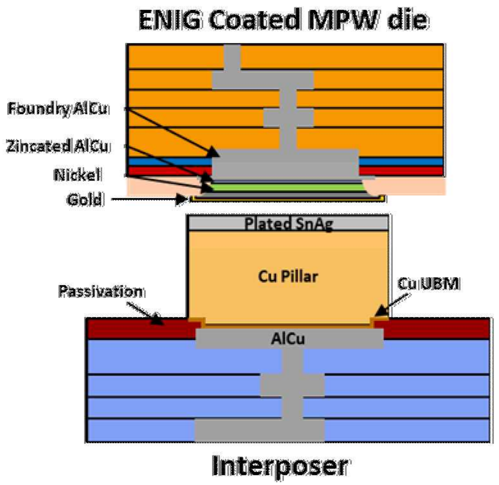




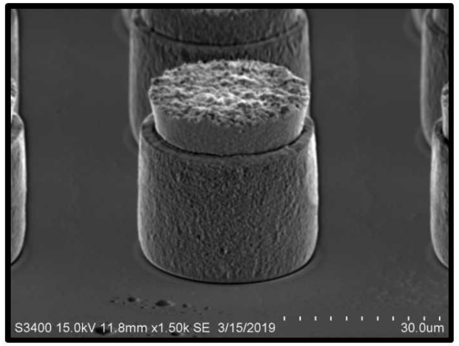




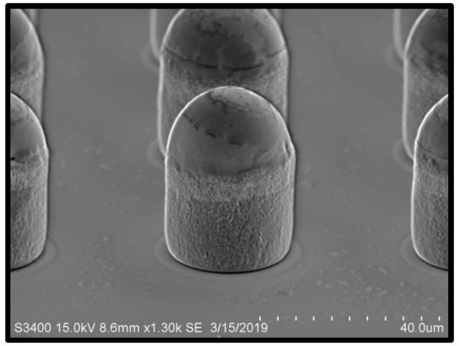
Cu Pillar Development



SnAg Capped Cu Pillar

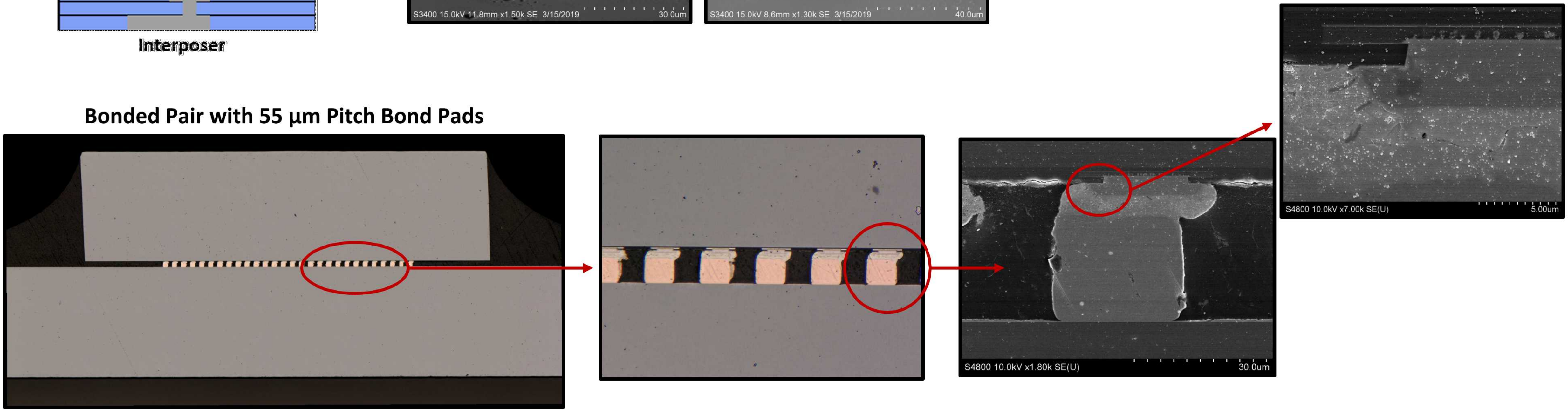


SnAg Reflow

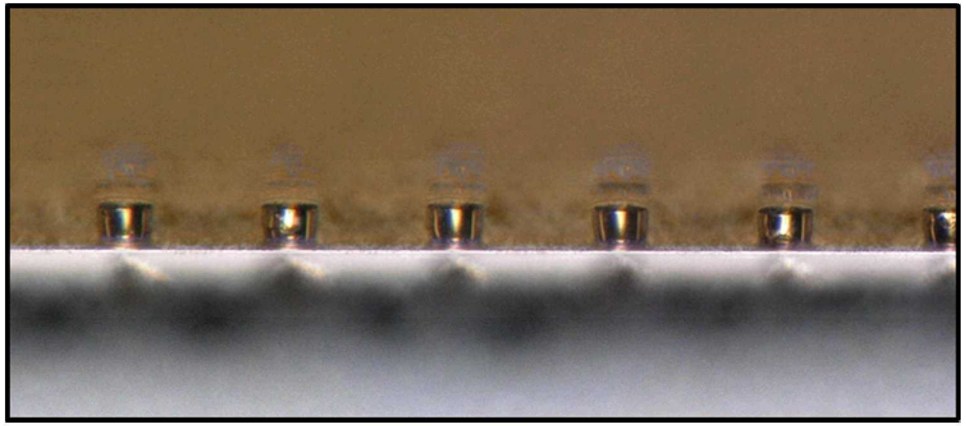


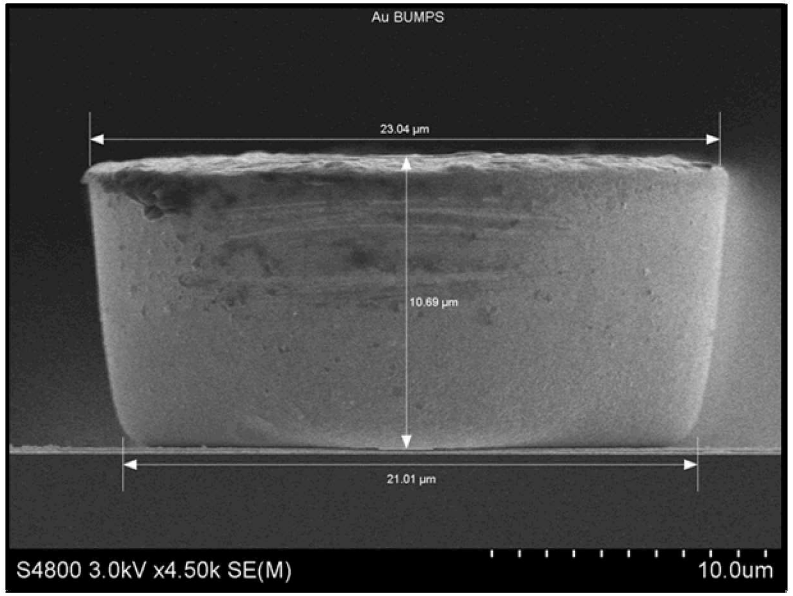
- **Electroplated (ECD) Cu pillars**
- **Cap pillars with ECD SnAg solder**
- **Reflow solder attachment**
- **55 µm pitch demonstrated, smaller pitch possible**

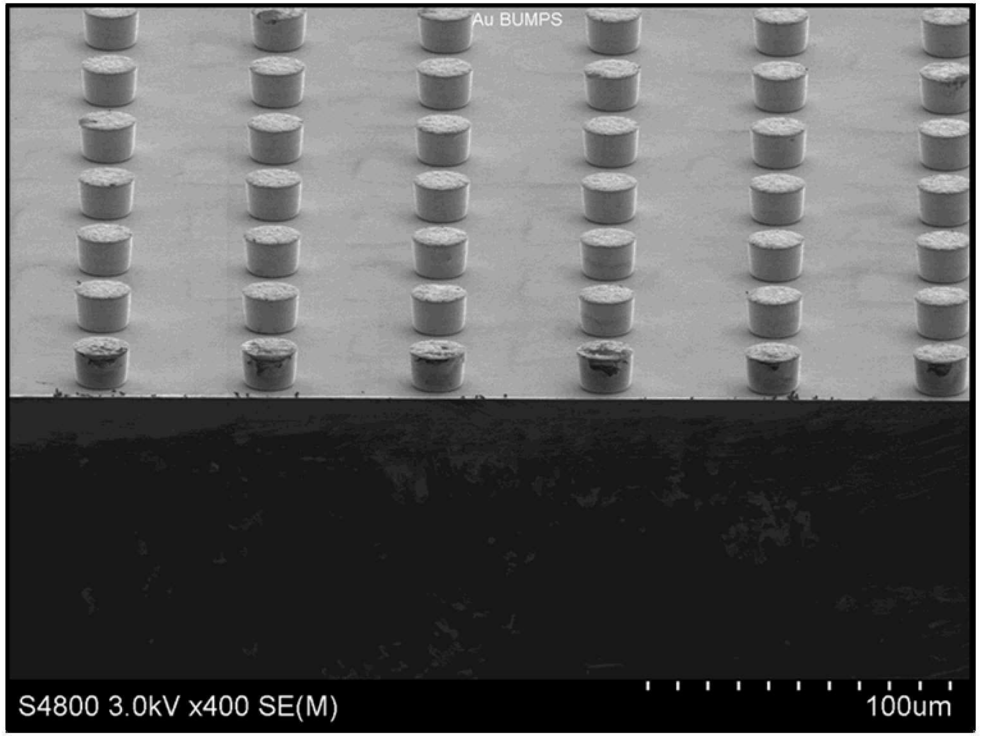
Bonded Pair with 55 µm Pitch Bond Pads

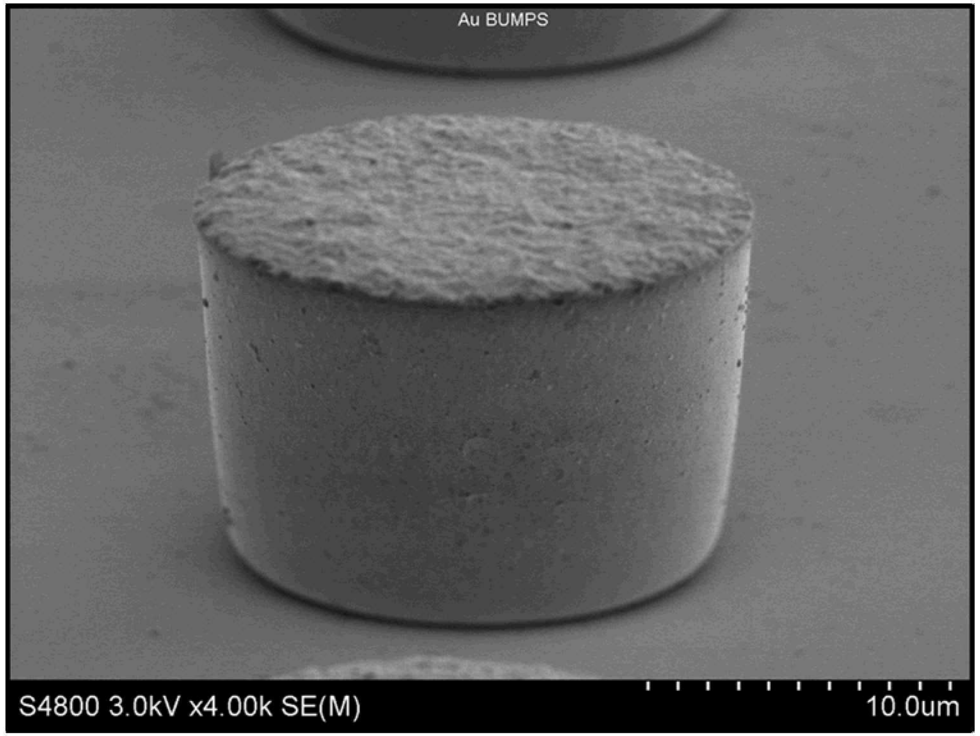


Gold Bump Development



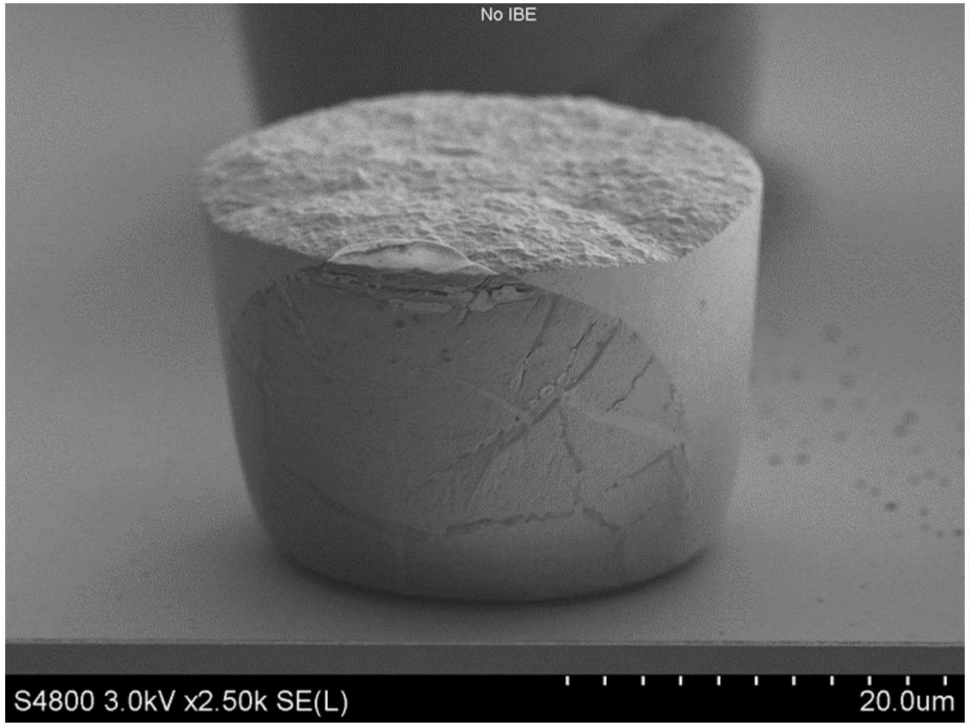




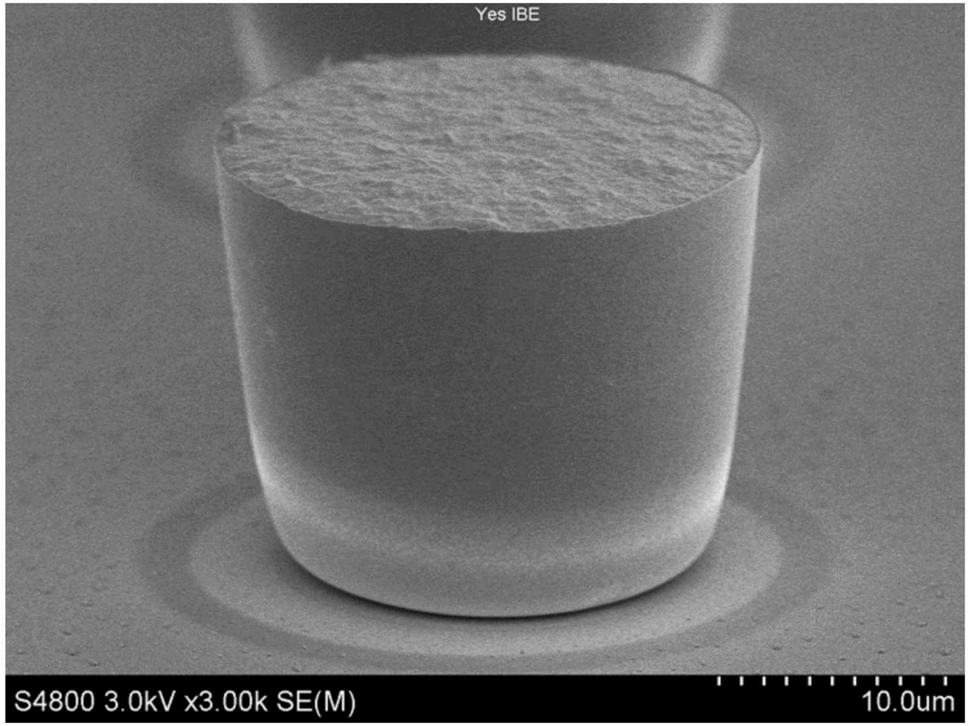


Gold Bump Development – Seed and UBM Removal

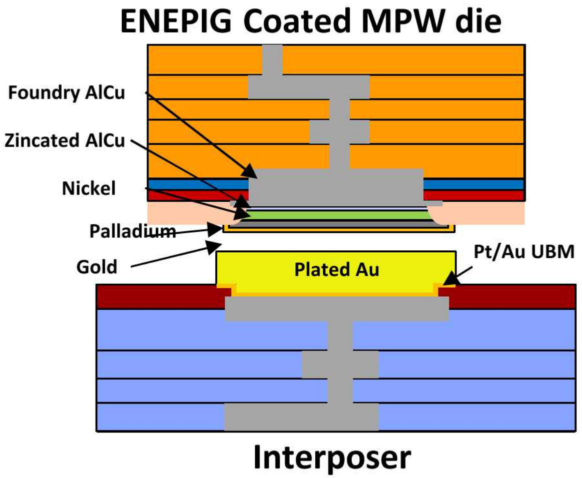
Pre seed removal



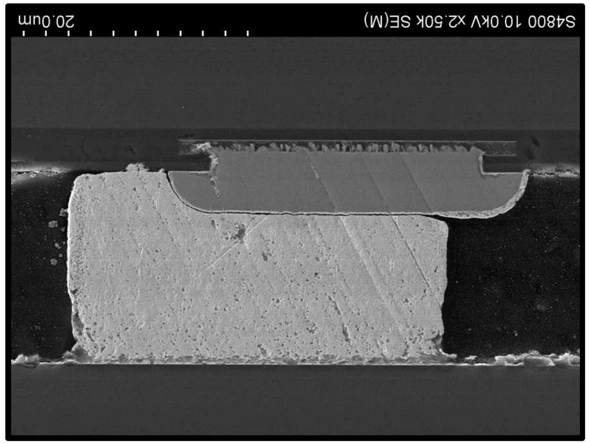
Post seed removal



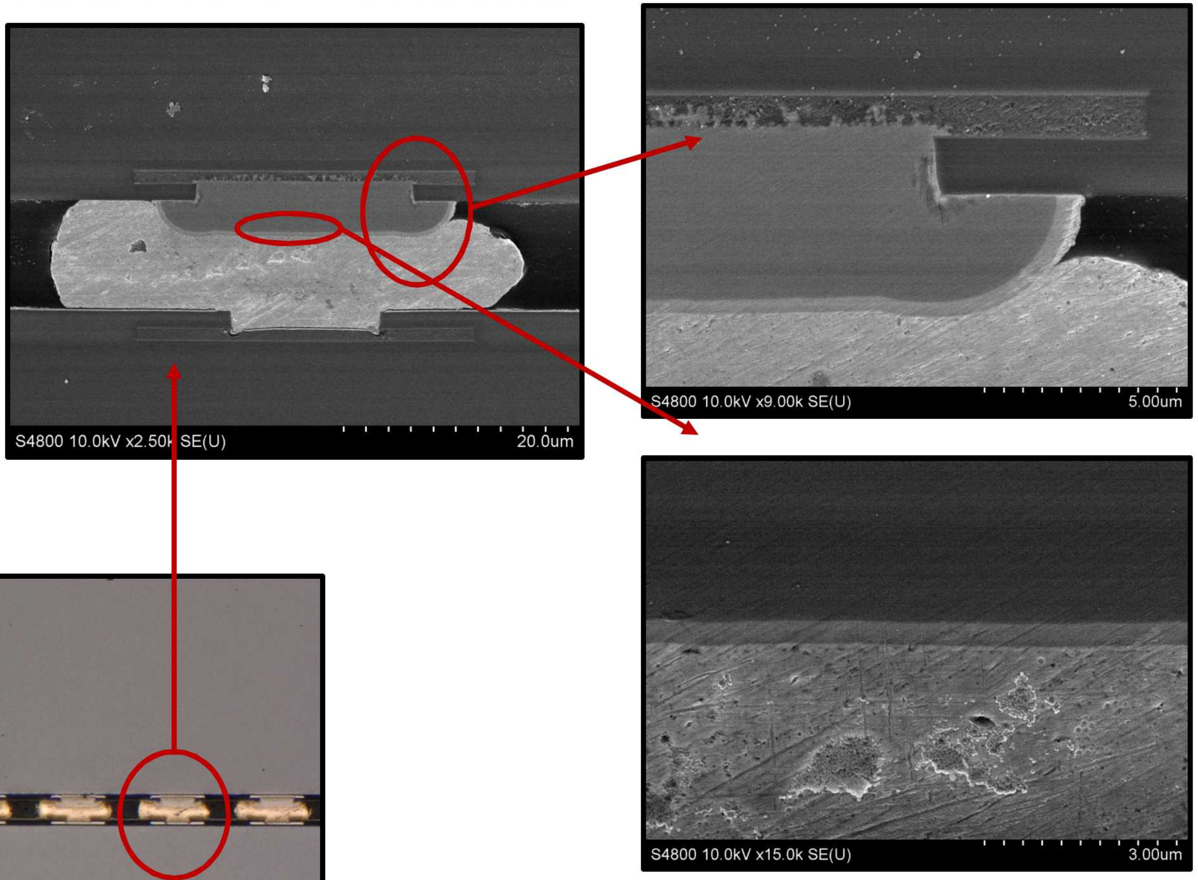
Au Microbump Development



Au to ENIG -> Poor Bond

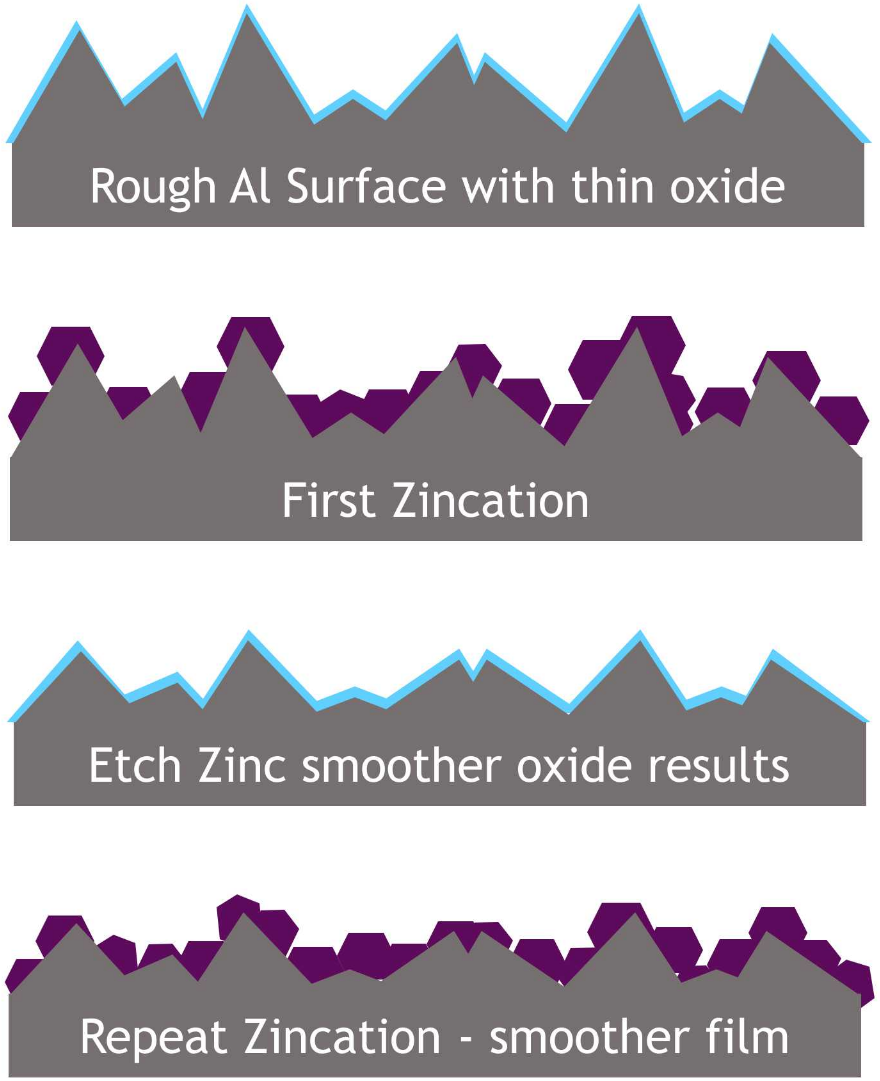


Au to ENEPIG -> Good Bond



Thank you – Questions?

Zincation Process



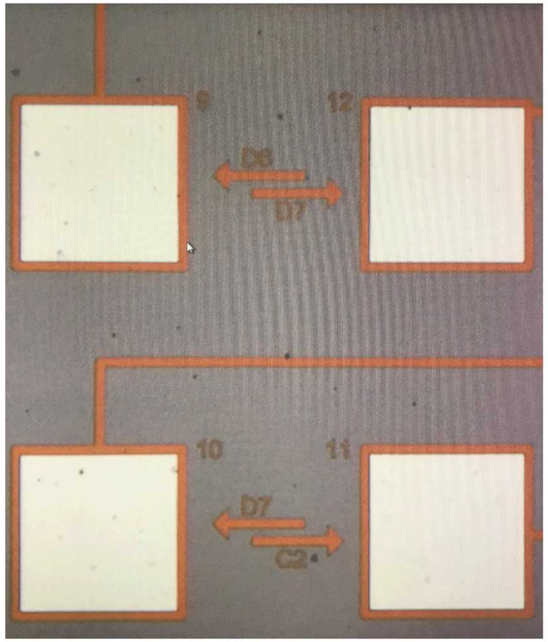
Process

- Zinc complexes exchange in solution with Aluminum resulting in Zn deposition and Al etching
- Grow zinc crystallites for 30-60 seconds
- Quickly dissolve zinc in HNO_3 and repeat

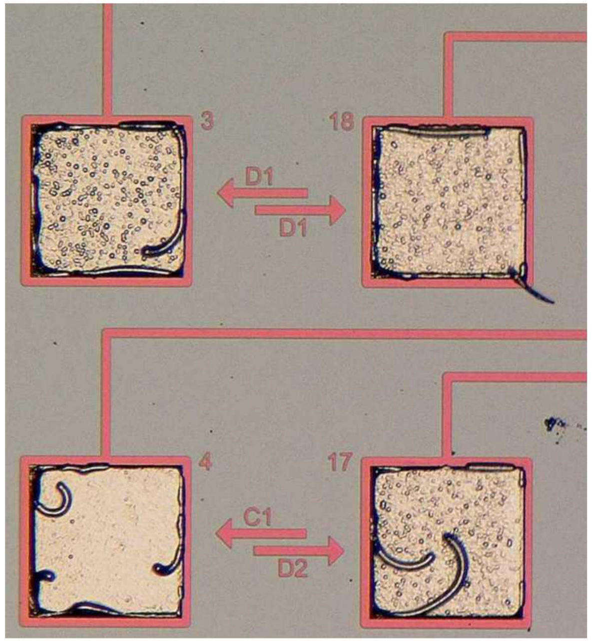
Zincation Formula

- 100:1:10:500 ZnO/$FeCl_3$/Rochelle salt/NaOH
- ZnO is Zn source
- $FeCl_3$ and tartrate ions enhance adhesion of Zn deposits
- Sodium nitrate limits the thickness of Zn deposits

Zincation Results



Al bond pads



After Zincation
and Electroless Ni

ENIG Coated Pads