

# JEOL JBX 6300-FS

A Tool Specific Photonics Application

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- Introduction
- Changes to Data Prep
- Resist Process
- Substrate Holders/Mounting
- Pre-Alignment/Alignment
- Jobdeck Setup
- Results
- Summary

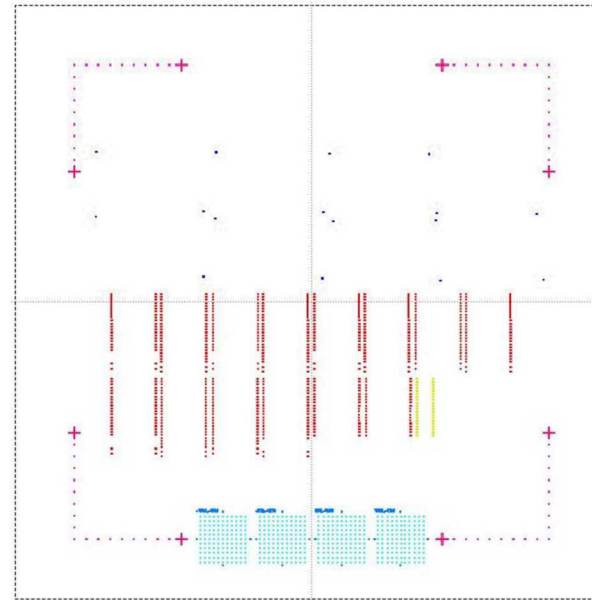




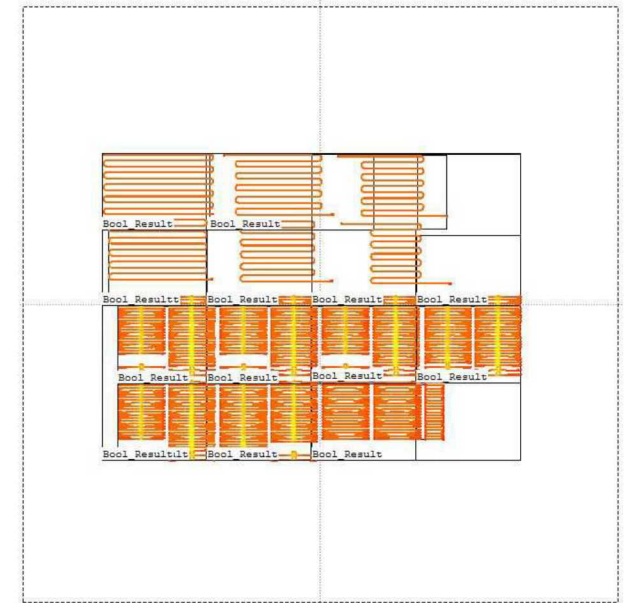


- JEOL JBX-6300FS (Installed 2009)
- 25-50-100kV Accelerating Voltage
  - CINT tool is kept at 100kV.
  - 2 “Modes” available at each voltage.
    - Mode 3: 500 x 500 micron write field
    - Mode 6: 62.5 x 62.5 micron write field
- Scan Speed 250Hz to 12MHz
- Field write area: 500um<sup>2</sup>/4um<sup>2</sup> or 62.5um<sup>2</sup>/0.5um<sup>2</sup>
- Stitching accuracy is +/-20nm
- Focal Plane +/-100um
- Focus Strategy: Manual, Auto, Static
- 50pA to 20nA Beam Currents
- No Stage (Theta) rotation.
- SEM-only alignment
- Nanowire fabrication, meta-materials, gratings, biological.

- CINT uses software produced by GenlSys to aid image conversion, write preparation, and metrology.
  - BEAMER – File Prep
  - TRACER – Monte Carlo Simulation
  - ProSEM – SEM evaluation
- The original pattern comprised of two layers:
  - Gratings and Markers
  - Waveguides
- The configuration of the cross marks within the Gratings Layer are not traditional for the JEOL.



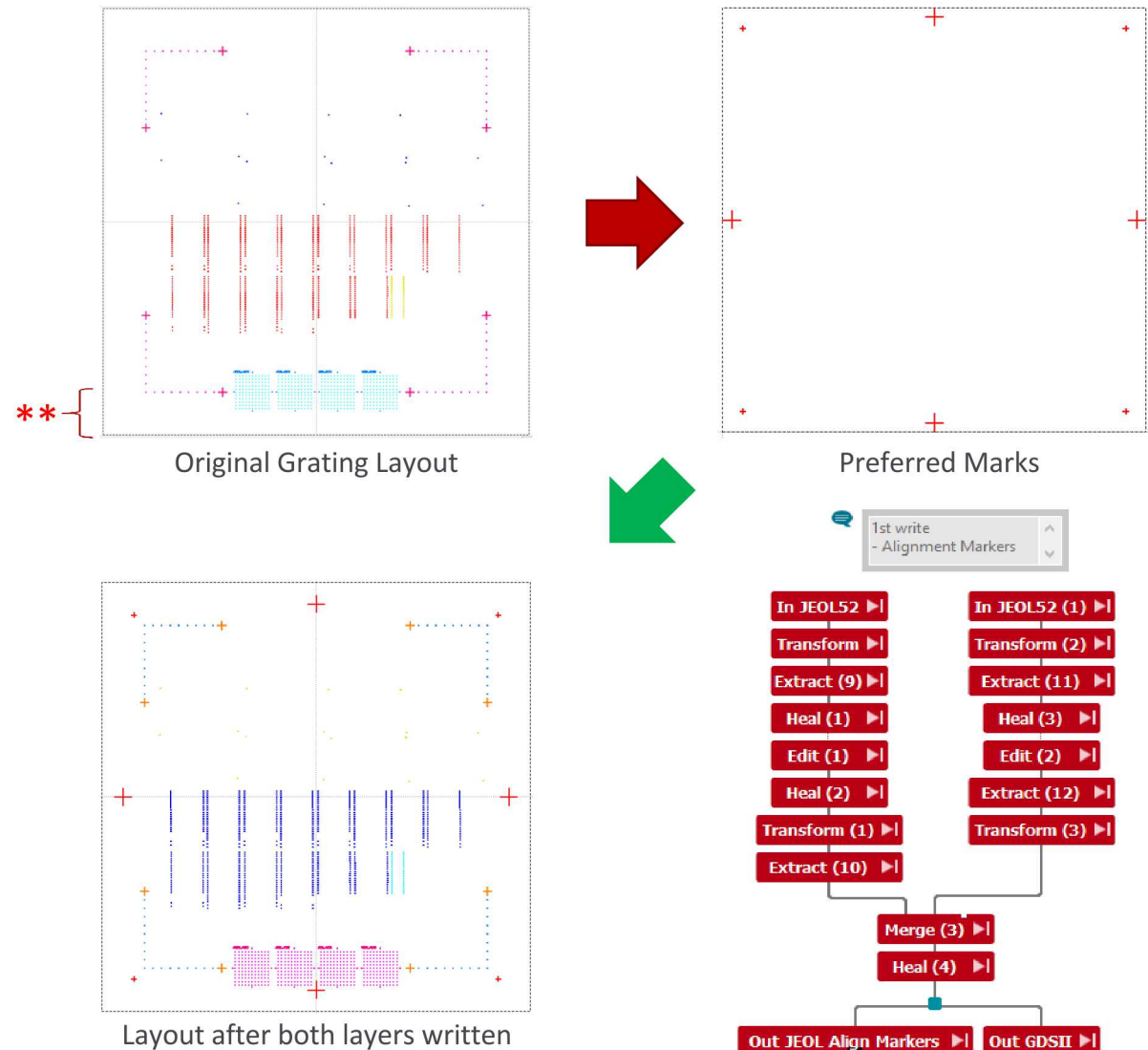
Original Grating Layout



Original Waveguide Layout

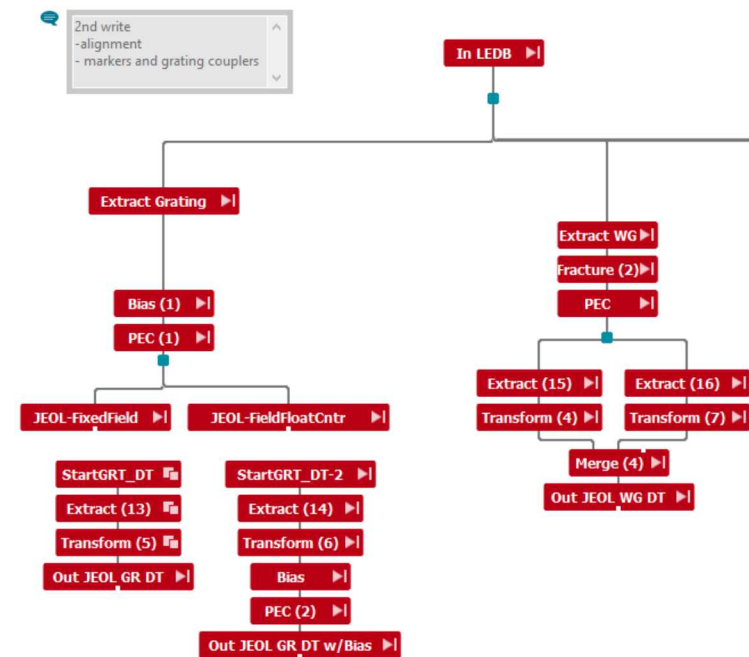
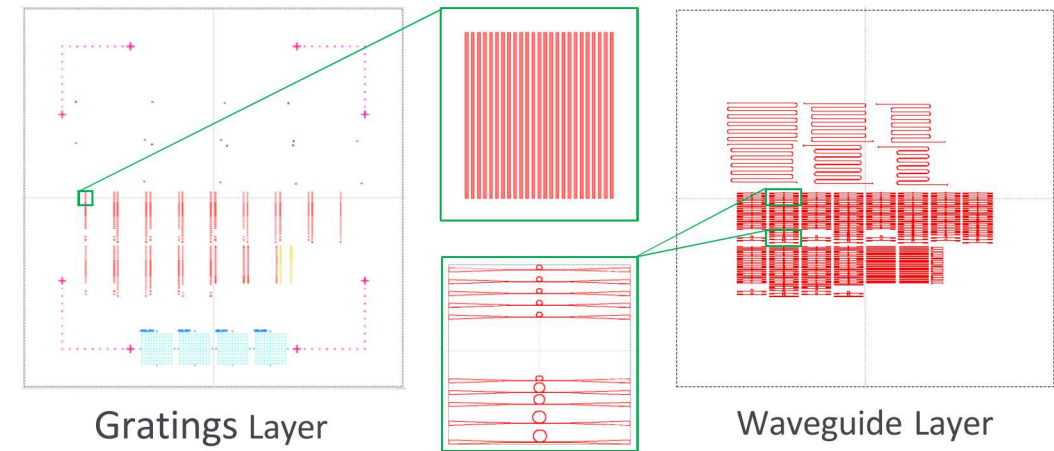


- The JEOL system requires a different format for Global and Chip Marks.
- The system is flexible enough to possibly use existing marks, however the patterns extend beyond the boundaries\*\*, which is a source for potential write error or system errors.
- New marks were added, and written prior to the original marks and grating pattern.



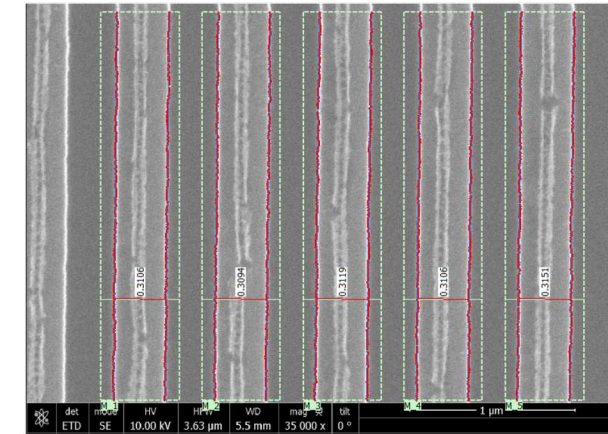


- Conversion flows are started for the full patterns to use as references.
- Prior to exposing the bulk pattern, small regions are clipped from the original pattern to use in dose tests.
  - Look for regions or features that represent critical dimensions.
  - Clip out the regions/features and create “new” dose test patterns.
    - Reduces overall time to find the process window(s).
- Use the same expose and post processing that would be applied to the bulk pattern to process the dose test patterns.
- Identify a specific dose or dose range that generates the necessary quality from the completed test.
- Evaluate write field positioning and how it effected the final exposure.

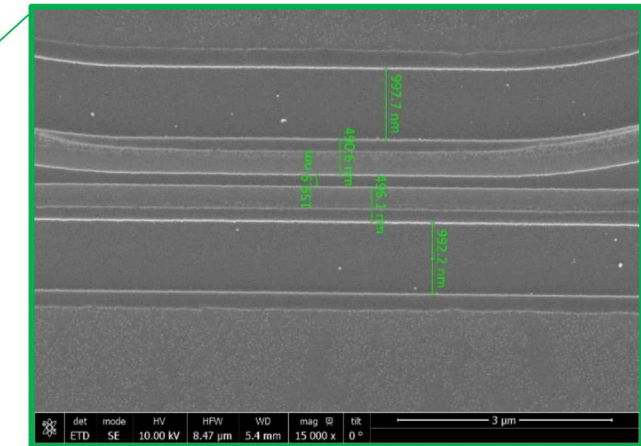
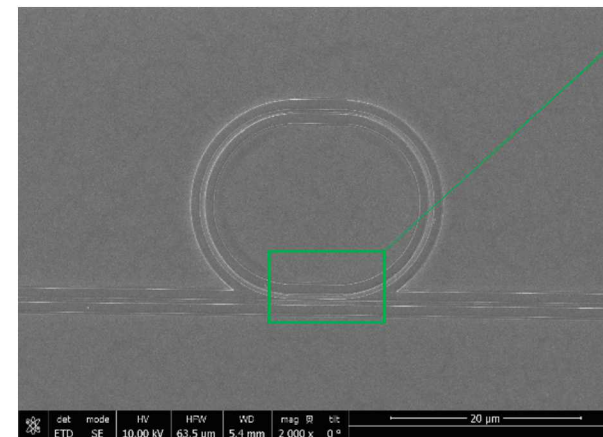




- The cut-out/dose test patterns for gratings and waveguides are exposed and etched.
  - Use the results to evaluate durability of resist in addition to dimension and edge roughness.
- Following the etch, process the samples through an O<sub>2</sub> plasma ash.
  - Piranha clean and 100:1 HF may be options to further clean away polymer veils.
- Dimensions are checked against the design, and the total dose is determined for the cd region.
  - Example:
    - Dose for cd region in PEC is 1.5190 (for 1.1X normal).
    - Base dose is 170uC/cm<sup>2</sup>.
    - The total dose which produced the desired outcome of the targeted features is 258uC/cm<sup>2</sup>.



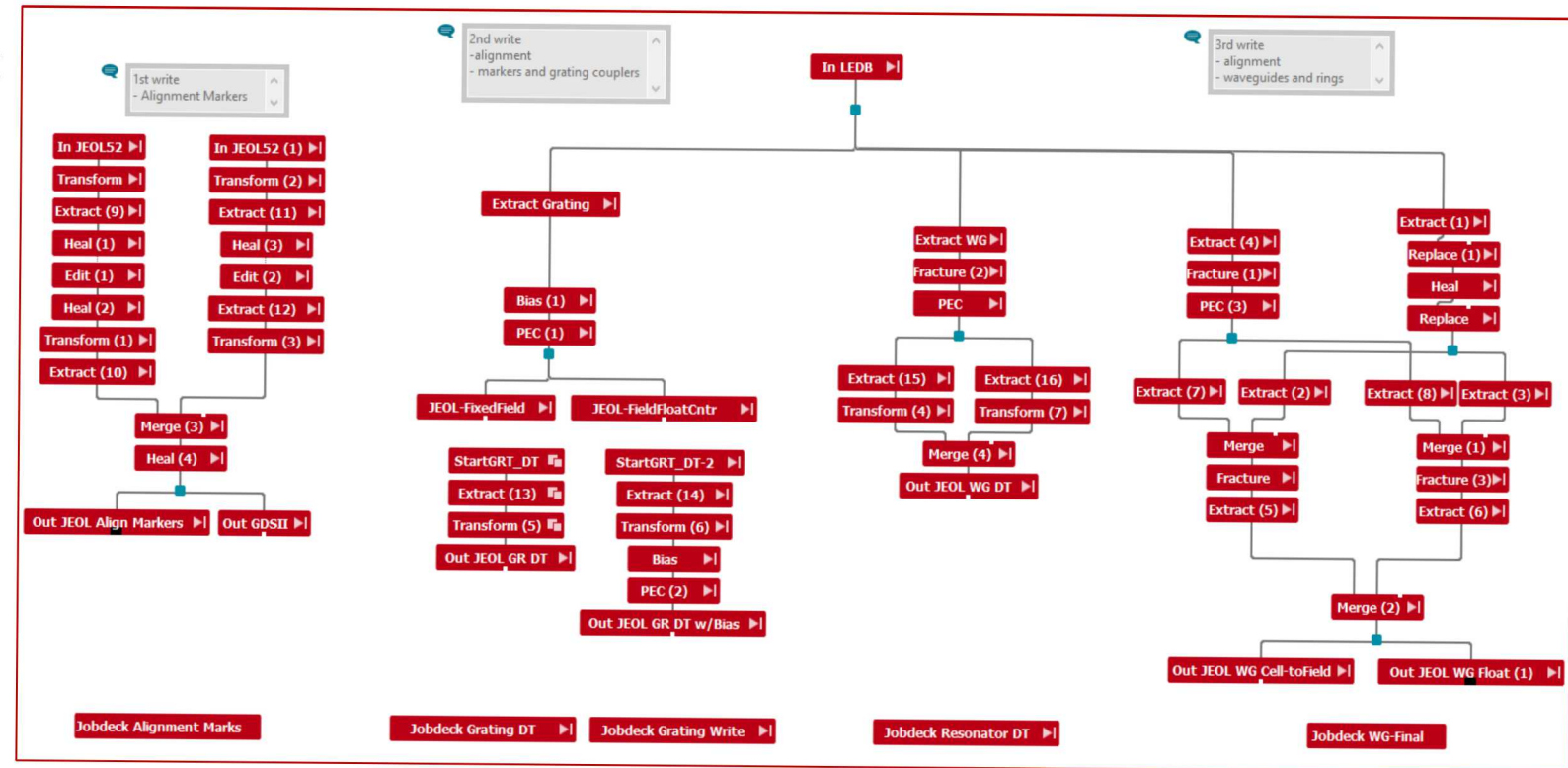
Post Grating Etch



Post Waveguide Etch



- Make final adjustments to the full pattern flows, if needed, based on the dose test results.
- Establish final write sequence.
  - Alignment Marks
    - “Mask” write – no alignment
    - Dual Layer PMMA
    - Metal Deposition
    - Liftoff
  - Gratings Layer
    - Aligned write
    - ZEP 520a resist
    - Etch
    - Strip resist
  - Waveguide Layer
    - Aligned write
    - ZEP 520a resist
    - Etch
    - Strip resist

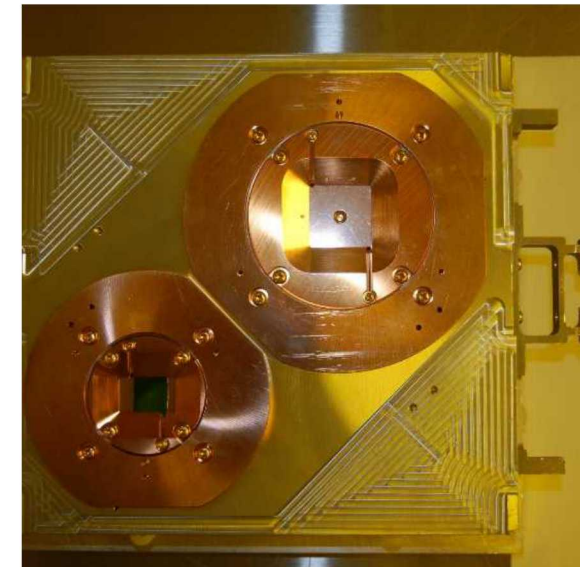
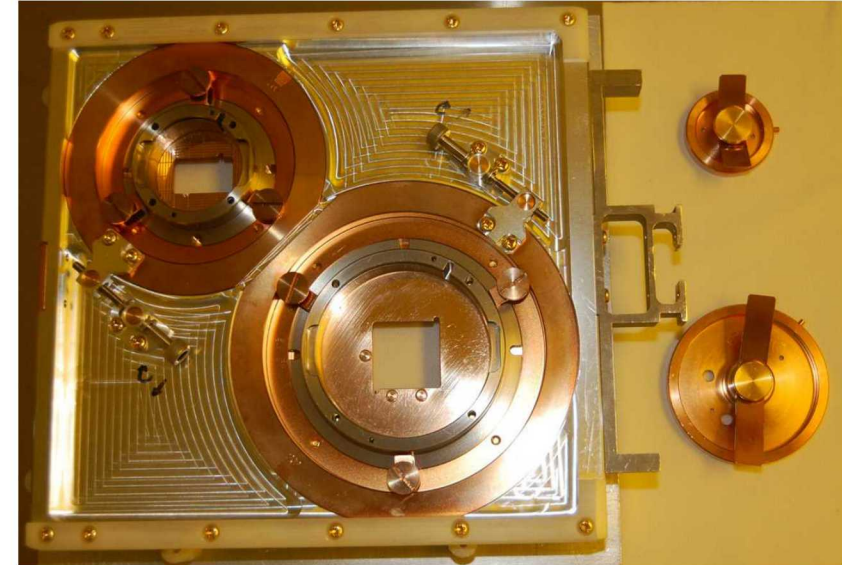






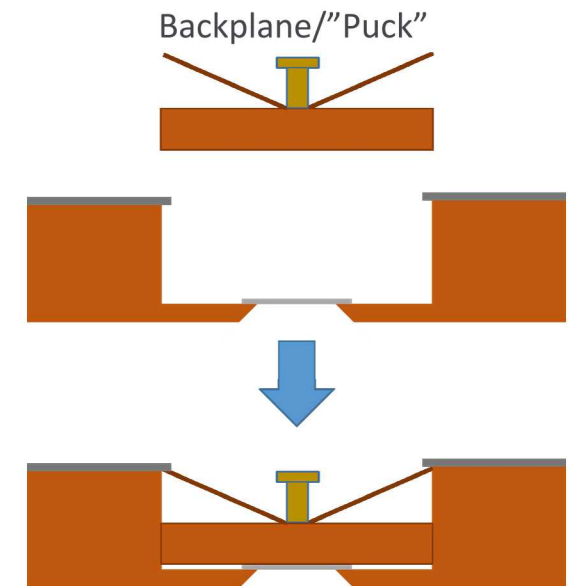
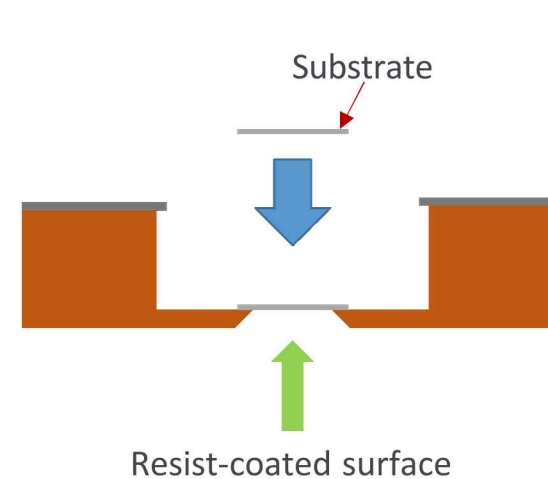
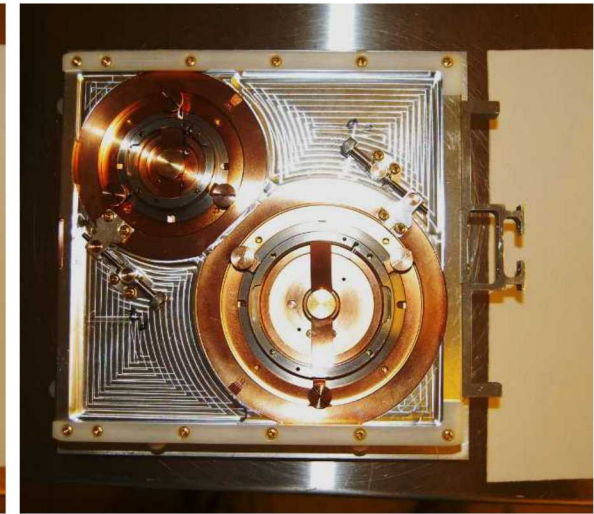
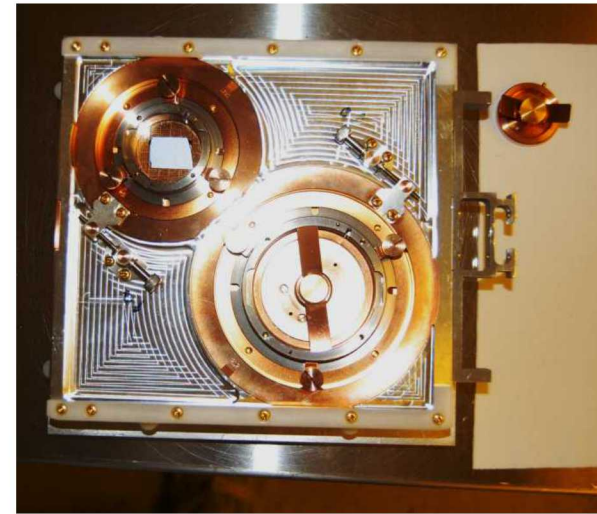
- Headway Research Spin Coaters were used for resist deposition.
  - Programs are simple 1-step processes: Ramp to 3000rpm at 3000rpm/s, dwell for 30s.
- A new, “prime” Si wafer was coated with AZ4330 resist and then baked at 90°C for 60 seconds.
  - After coat, the wafer was cleaved.
    - Dicing is preferred.
  - Soak the substrate in acetone (60-120s), then rinse with acetone (2-5s), IPA (2-5s), dry, and process with an O<sub>2</sub> plasma (ash).
  - Following the clean, the piece should be inspected under a microscope; dark field viewing mode.
  - For the Alignment Mark Layer – a PMMA A4 bi-layer resist stack is used.
    - PMMA 495 A4 spun, baked 170°C for 120s.
    - PMMA 950 A4 spun, baked 170°C for 120s
    - Develop in 1:3 MIBK:IPA for 60s, room temp.
    - Rinse with IPA for 2-5 seconds, then dry with N<sub>2</sub>.
  - ZEP520a to be applied for both the Grating and Waveguide Layers.
    - Hot-plate baked for 120 seconds.
    - Develop in n-amyl acetate for 60s at room temp.
    - Rinse with IPA for 2-5 seconds, then dry with N<sub>2</sub>.

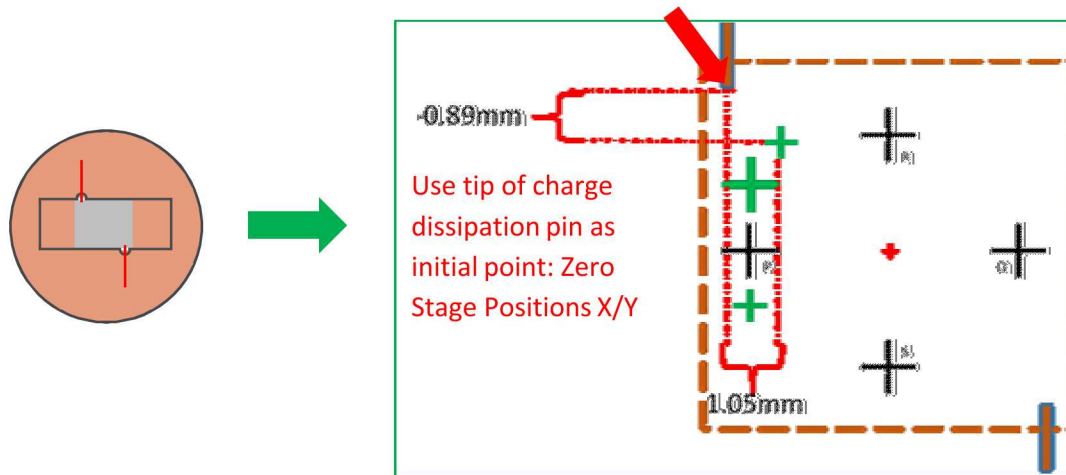
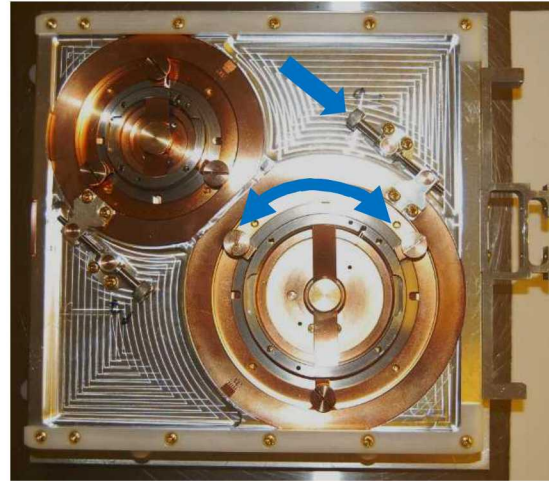
- All of the cassettes were purchased from JEOL.
- Available cassette options are:
  - Full Wafer Holders in 2, 3, 4, and 6 inch diameters.
    - Some are multi-wafer.
    - Pin reference placement. No rotation.
  - Custom Piece Holders (\*pictured)
    - 23mm x 23mm\*
    - 18mm x 18mm
    - 13mm x 21mm\*
    - 8mm x 21mm
    - Holders capable of +/- 2-2.5 degrees of rotation.
- All holders mount samples from the back (top image).
  - Samples are placed into the holder face-down.
  - Allow a minimum of 1mm per edge to be held by the metal frame.
    - Samples should be held in place by two opposing sides, or by all four sides.





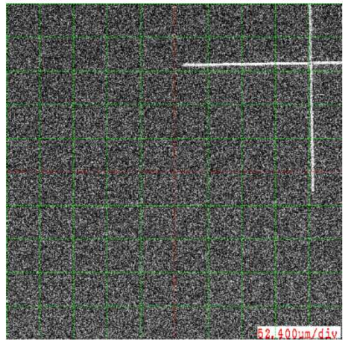
- A custom holder, 13mm X 21mm is selected.
- Samples are placed face-down within the holder, and generally positioned to the center of the holder opening.
  - Note: Placing the sample can be a bit challenging for new users.
- Once the sample is positioned, the holding “puck” is lowered down onto the backside of the substrate.
- Spring clips secure the sample, applying pressure to the center of the puck.



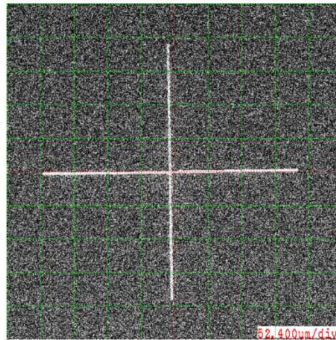


- No alignment needed for the first exposure.
- For exposures that require alignment:
  - Use a low-power microscope, with crosshair reticle, moveable stage, and stage position readout, to determine how much rotation is present on the mounted sample.
    - Note: The cassette will go back and forth between the scope and holding plate.
  - Use the ArcTan function to calculate the rotation.
  - Use the screw located on the backside of the holder to rotate the holder as needed to achieve a final rotation of less than 0.2 degrees. (This feature is only available on the custom holders).
  - Locate a known feature (charge dissipation pin), and zero the position meter to 0,0. Move the stage to a defect or sacrificial mark. Note the X and Y distances.

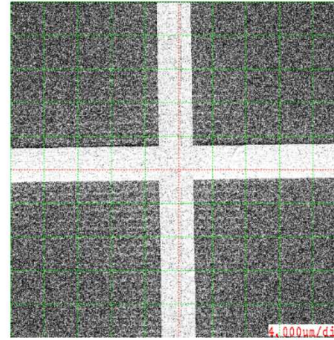




**\*\*** SEM after stage is repositioned to the 2<sup>nd</sup> "mark".



Centering the mark.

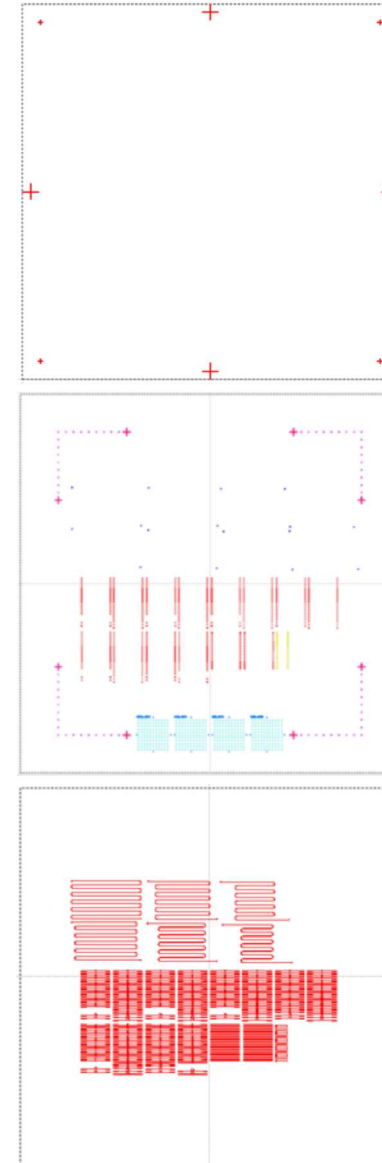


Centering the mark under higher magnification.

	JEOL Coordinates	X= -1125	Y= 5225
( - )	Design Coordinates	X= 0	Y= 5000
<hr/>			
	Offset	X= -1125	Y= 225

- Following basic calibrations of the JEOL, set the system up to utilize the low resolution SEM function.
  - Change the JEOL's coordinate system from "Stage" (absolute) to "Substrate" (Relative). This allows users to easily navigate the substrate, as 0,0 is set to the center of the holder (and theoretically 0,0 of the substrate).
  - Navigate to the position of a known feature or point on the holder (located away from the pattern write regions).
    - Set the SEM to a maximum scan width (524um).
    - Briefly start the SEM, and look for the initial feature. Use stage movement to center the feature on the display.
  - With the SEM OFF, move the stage a distance in X and Y equal to the values determined at the microscope.
  - **\*\*** Briefly start the SEM, and look for the second feature or "mark".
    - Keep the SEM "On" time to a minimum.
    - Use stage movement to center the feature on the display.
    - Reduce the SEM scan width, and re-center the pattern.
    - Note the X and Y coordinates as indicated by the JEOL.
  - Determine the sample's offset from the designed coordinates.
    - Subtract the "Design" coordinate from the JEOL coordinate for both X and Y; this is the "offset" for the sample.
- Edit the calibration settings SETWFR and CHIPAL.
  - Sets the mark detection parameters, and tests mark detection based on entered locations.

- The tool set to Mode 3, 4<sup>th</sup> Lens – 100kV
  - Mode 3 100kV: 500um X 500um write field
- Alignment Marks
  - “Mask” write – no alignment to substrate
  - 130um Aperture, 6nA Beam Current
    - Estimated Beam Diameter: 18.8nm
  - Write Time: 4 minutes
- Gratings + Marks (Original Layer 1)
  - “Direct” write – alignment to 4 Global Marks and 4 Chip Marks.
  - 60um Aperture, 2nA Beam Current
    - Estimated Beam Diameter: 9.6nm
  - Write Time: 10 minutes
- Waveguides
  - “Direct” write – alignment to 4 Global Marks and 4 Chip Marks.
  - 60um Aperture, 1nA Beam Current
    - Estimated Beam Diameter: 7.5nm
  - Write Time: 67 minutes





- Visual-Job (module within BEAMER) was used to generate two of the files needed to write the pattern:
  - SDF (Schedule File)
    - Tells the JEOL how to write the job:
      - Job Sequencing (order of work)
      - Holder Identifier
      - Call-out to Jobdeck file (image info)
      - Option to find Global Marks
      - Option to find Chip Marks
      - Option to use Auto-Height Detection
      - Offset of substrate (Global shift of patterns)
  - JDF (Jobdeck File)
    - Tells the JEOL what to write for the job:
      - Generalized shape and size of holder
      - Global Mark locations and dimensions
      - “PATH” statement is beginning of pattern information.
        - Optional embedded commands to perform calibrations prior to or during write operations.
      - Array statement defines the positions of the pattern(s) using a matrix-style layout.
      - Chip mark locations (from the center of the write cell), and their dimensions.
      - Layer information
        - Sets image, shot pitch, resist base dose values
        - Modulate statements alter the exposure dose by data type.
- The SDF, JDF, and pattern files are scheduled (compiled) into a third file – magazine, which is used by the JEOL as the primary instruction code/set to run the job.



```

;-----
; Coat PMMA 495 A4 Spin RCP#3 3K rpm, 30 sec
; Soft bake 170 C for 120 sec.
; Coat PMMA 950 A4 Spin RCP#3 3K rpm, 30 sec
; Soft bake 170 C for 120 sec.
; Expose time TBD
; Develop time 60 sec in 1:3 MIBK:IPA
; Rinse IPA 3-5 sec.
;-----
JOB/W ,2,2

PATH DIRTST

  ARRAY (0,1,10000)/(0,1,10000)
  ASSIGN P(1) -> ((*,*),S0)

  AEND

PEND

;////////////////////////////////////
LAYER 1
P(1) 'MAEBL_Alignment.v30' (0,0)
SHOT A, 14
RESIST 1000,1000,A
STDCUR 6.0
OBJAPT 7

S0: MODULAT((0, 20))

END

; visual-Job Revision Number 5.6.2. (29036), Oct 16 2018
; Created Mon Nov 12 14:34:20 2018
    
```

JDF

```

MAGAZIN 'GRATING'

#1
%2H
JDF 'Grating',1
EOS 3,'100Kv_Ap60_2nA'
GLMDET 5
CHMDET A,1,999
CHIPAL 4
HSWITCH OFF, ON
OFFSET (1125, -225)

END

; visual-Job Revision Number 5.7.0. (29987), Dec 21 2018
; Created Wed Mar 13 11:24:31 2019
    
```

SDF

```

JOB/W 'GRATING',2

GLMPOS P=(-4500,0),Q=(4500,0),R=(0,4500),S=(0,-4500)
GLMP 4.000,200.000
GLMQRS 4.000,200.000

;-----
PATH LNGB01

1: ARRAY (0,1,10000)/(0,1,10000)
  CHMPOS M1=(-4250,4250),M2=(4250,4250),M3=(4250,-4250),M4=(-4250,-4250)
  CHMARK 4.000,60.000,0,0
  ASSIGN P(1) -> ((*,*),S0)
  AEND

PEND

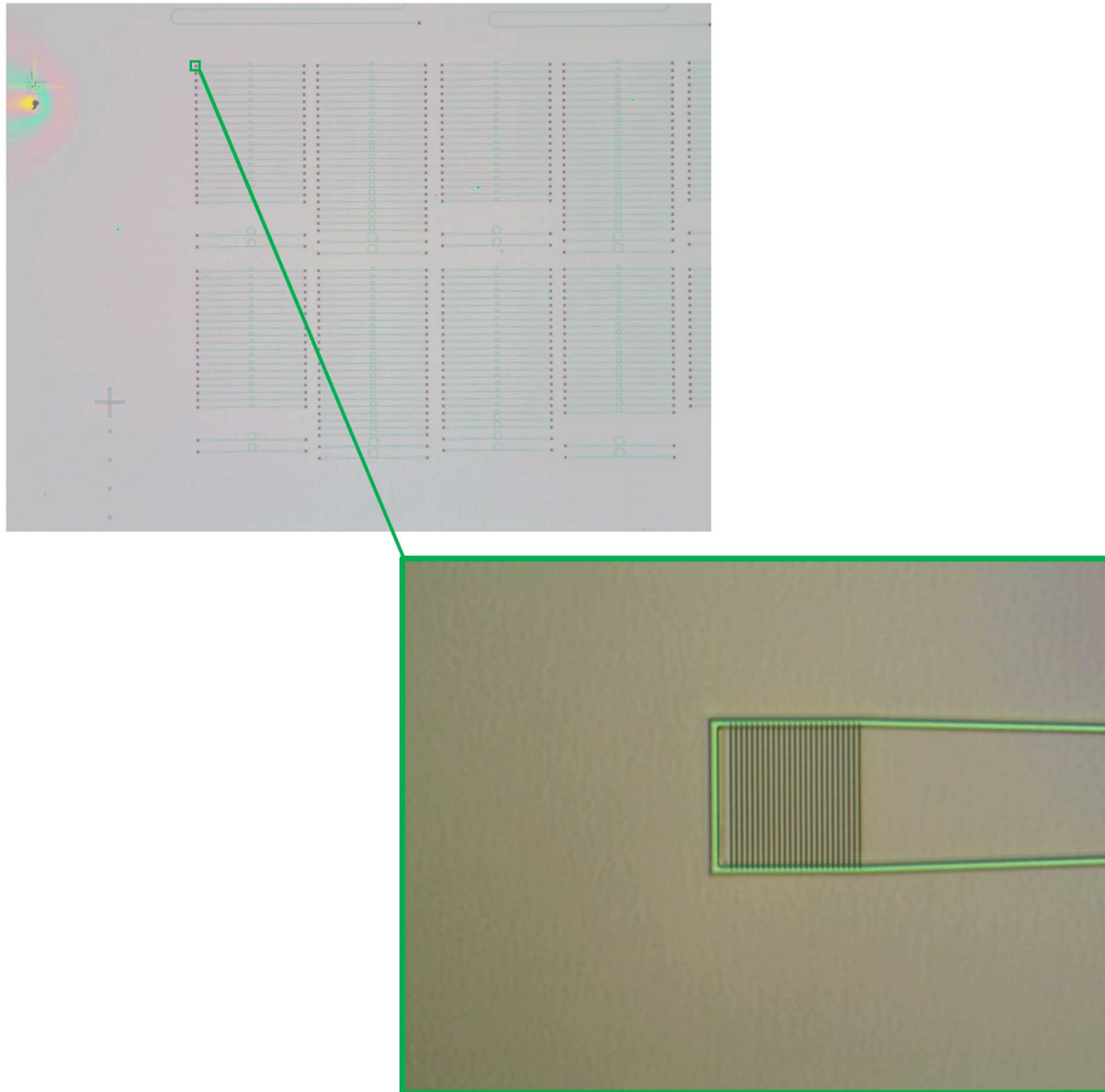
;-----
LAYER 1
P(1) 'MAEBL_Gr_Float_b30.v30' (0,0)
SHOT A, 10
RESIST 200,200,L
STDCUR 2.04
OBJAPT 6

S0: MODULAT((0, 8.3) , (1, 9.4) , (2, 10.5)
- , (3, 11.6) , (4, 12.7) , (5, 13.8)
- , (6, 14.9) , (7, 16.1) , (8, 17.3)
- , (9, 18.4) , (10, 19.6) , (11, 20.8)
- , (12, 22.0) , (13, 23.2) , (14, 24.5)
- , (15, 25.7) , (16, 27.0) , (17, 28.2)
- , (18, 29.5) , (19, 30.8) , (20, 32.1)
- , (21, 33.5) , (22, 34.8) , (23, 36.1)
- , (24, 37.5) , (25, 38.9) , (26, 40.3)
- , (27, 41.7) , (28, 43.1) , (29, 44.5)
- , (30, 46.0) , (31, 47.4) , (32, 48.9)
- , (33, 50.4) , (34, 51.9) , (35, 53.4)
- , (36, 54.9) , (37, 56.5) , (38, 58.1)
- )

END

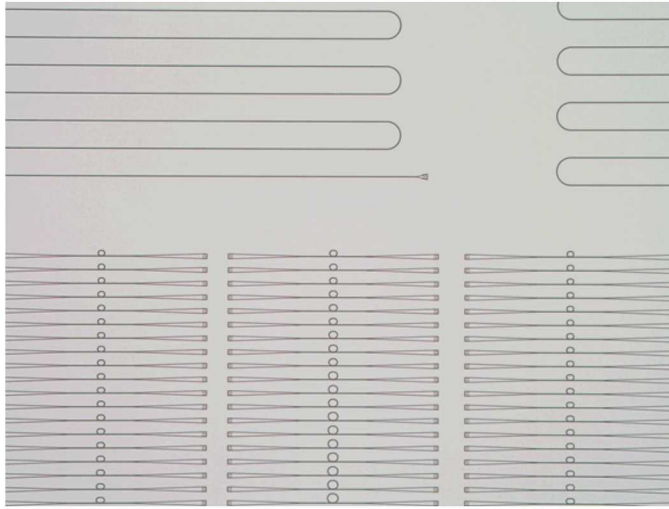
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JDF

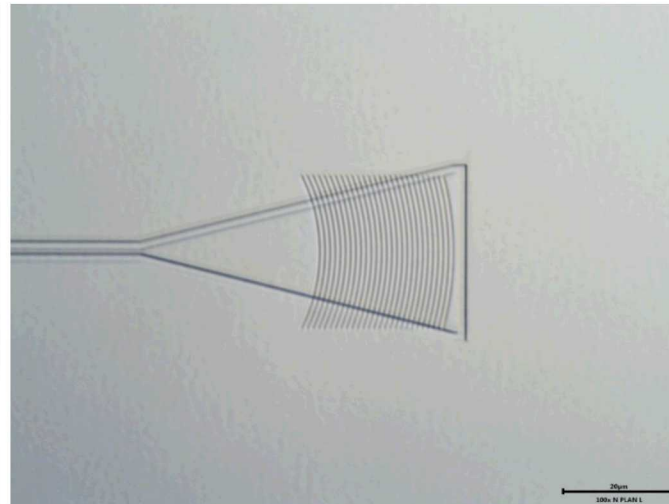
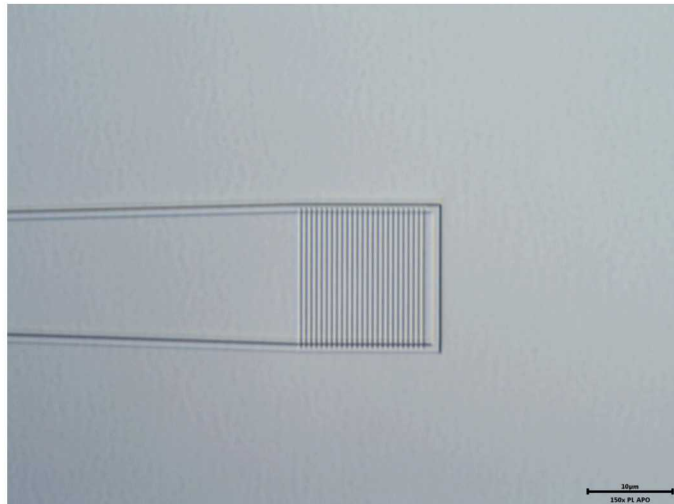


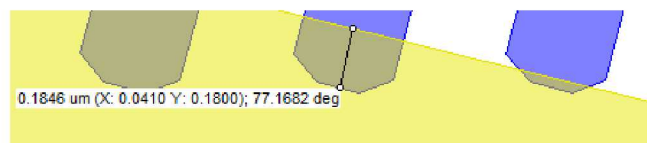
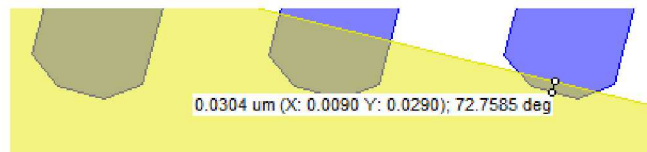
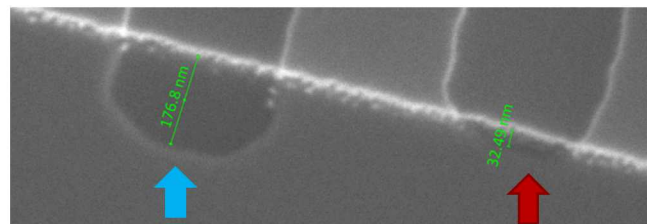
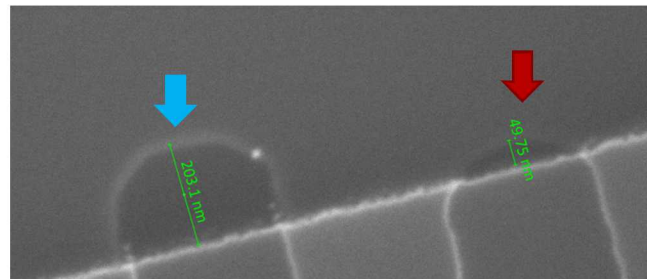
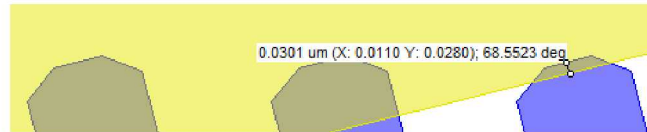
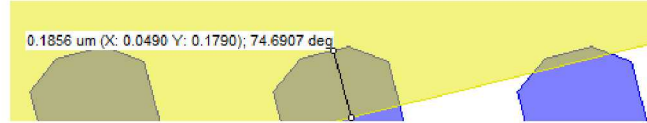
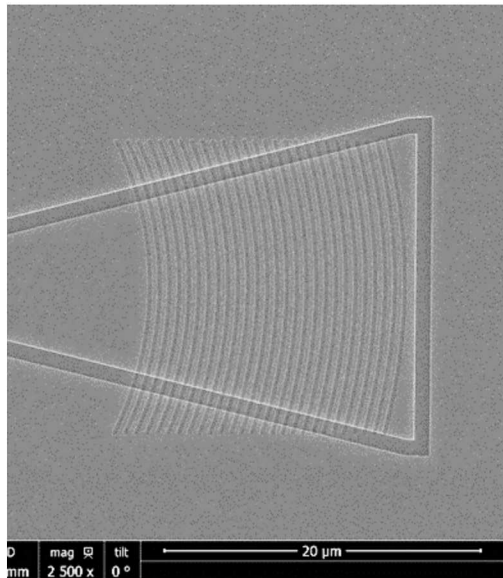
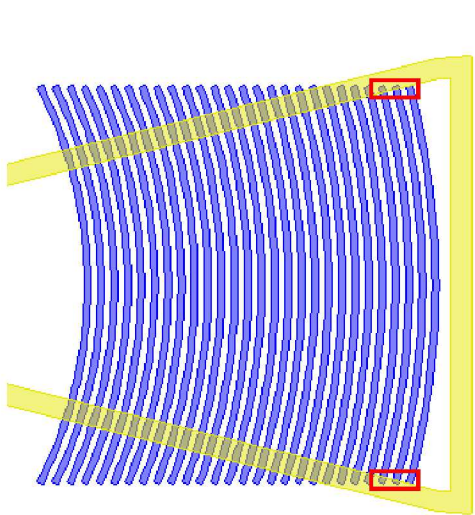
- Alignment of the Gratings Layer to the Alignment Marks Layer was not possible as written.
  - Note: A confirmation/test could have been possible if Vernier marks had been added for each layer.
- Microscopic inspection of the waveguide-to-grating alignment appeared good after expose and develop of the Waveguide Layer.





- The alignment between the gratings and waveguides appear good following etch and resist removal of the waveguides (microscope inspection).





- Inspection by SEM supports the visual results of the microscope.
- The first 2 arcs of a grating coupler were used to compare the differences between the design and final result.
  - 1<sup>st</sup> Arc (far right):
    - Design : ~30nm overlap per side
    - Result : 50nm (top) + 32.5nm (bottom). ~20nm oversized, ~10nm shift to the top.
  - 2<sup>nd</sup> Arc (2<sup>nd</sup> from right):
    - Design : ~185nm overlap per side
    - Result : 203nm (top) + 177nm (bottom). ~5-10nm oversized, ~10nm shift to the top.

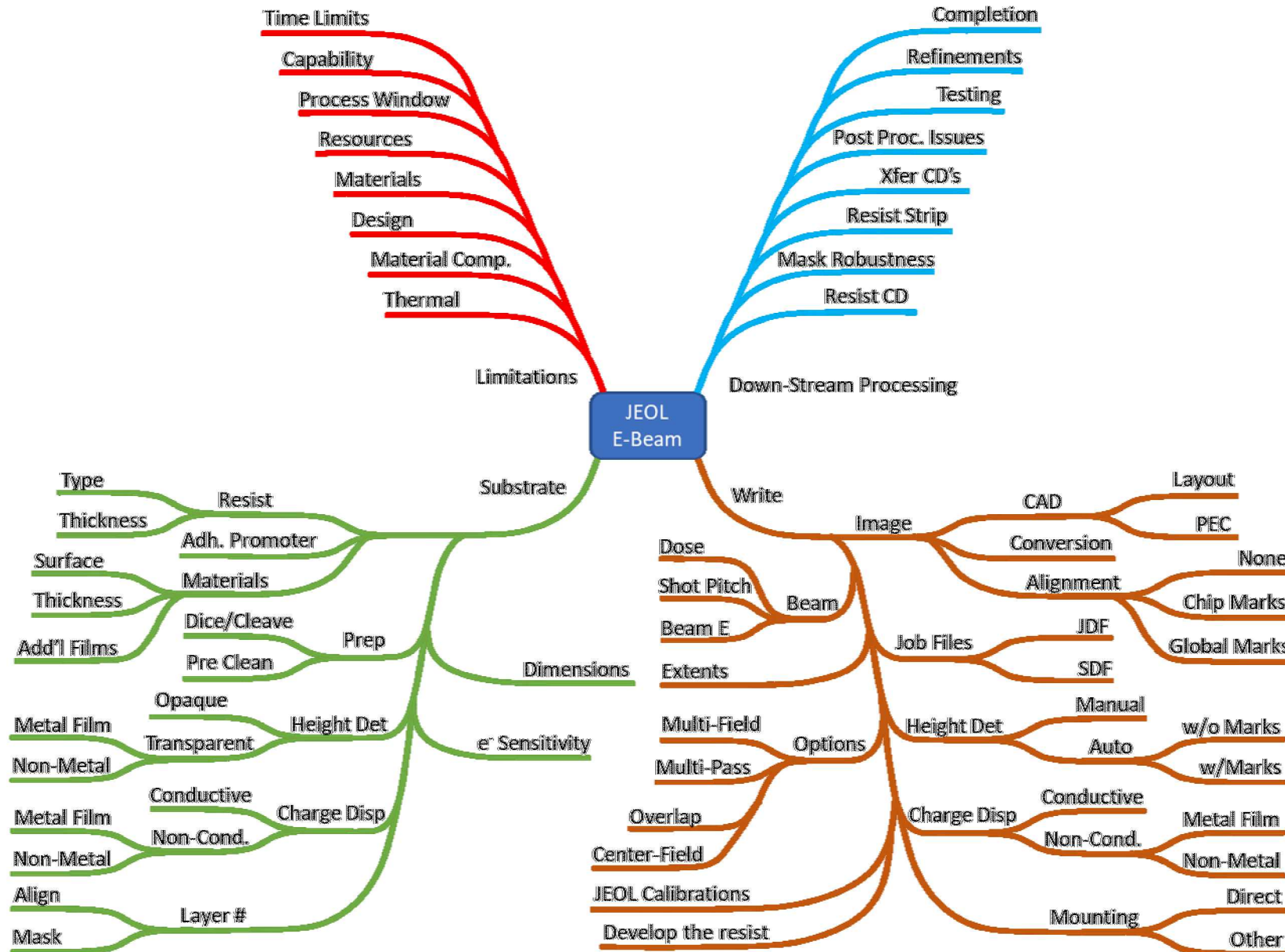




- Based on the SEM images:
  - The placement accuracy is within tools specifications.
  - Areas for potential improvement.
    - Refine the etch process.
    - Reduce the shot pitch for both the grating and waveguide exposures to smooth out edges.
      - Scan clock is potential limit.
    - Change resist from ZEP520a to Anisole-based PMMA, 950 series resist.
      - Higher base dose will permit smaller shot pitch, but write time will suffer.
    - Change develop process.
      - Change time or temperature of the developers to alter contrast.
    - Improve final clean process.

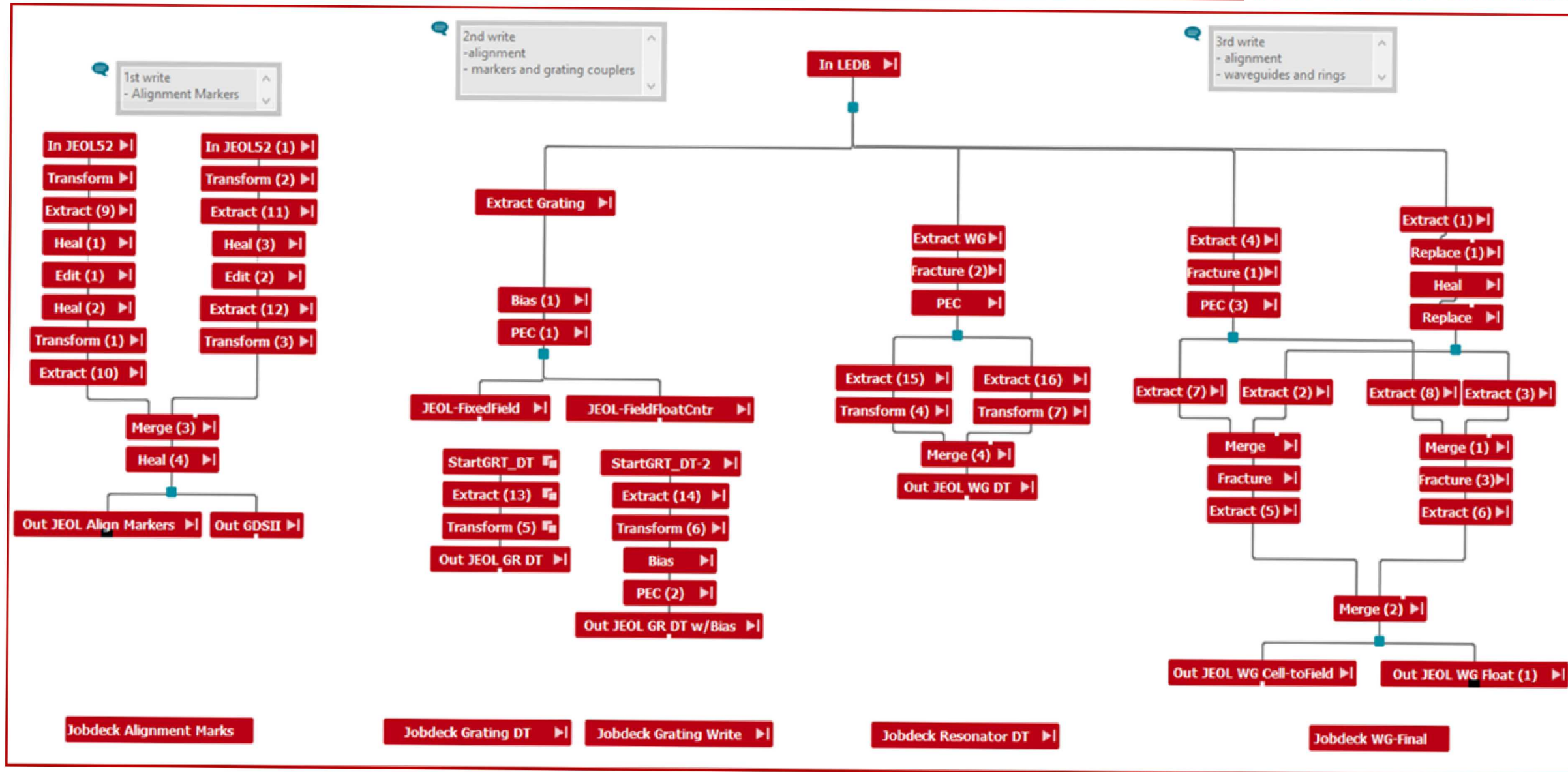
# Back-Up Slides



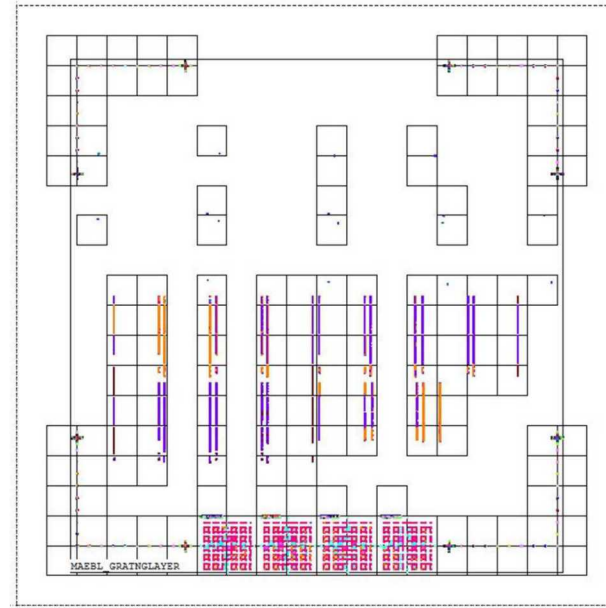


- **Is it feasible?**
  - Be aware of all potential and actual limitations that could impact the design fabrication.
- **The fabrication process is cyclical, not linear.**
  - Success of the final device will be predicated on the capabilities and process windows of downstream and upstream operations.
  - Each step of a process provides a feedback that could potentially impact both downstream and upstream processes.
- **Plan, plan, plan – Research, adapt.**
  - Understand all aspects of the final device: Function, Materials, Critical Dimensions, Order of Fabrication, Process Vulnerabilities.
  - Research and plan out the fabrication process flow.
    - Outline the order of fabrication steps.
    - Identify materials and tools needed, keeping in mind alternatives may be needed.
    - Get device drawing as close to a final state as possible.
      - Changes to pattern density, placement, or dimension have the potential to scrap all previous process work.
      - If the device is fabricated in multiple e-beam exposures, generate a pattern that contains discrete layers for each e-beam exposure.
        - Establish one layer for alignment marks (Global and Chip).
          - If practical, include device features which could be simultaneously fabricated into the layer.
        - Generate a complete pattern that uses a different layer each e-beam exposure/pattern.
        - Use a common point of origin for each layer, ensuring layer to layer alignment.
          - The final, overall pattern establishes the extent ordinates – defining a maximum, common boundary.
      - Ensure the CAD program can output the image into DXF or GDS (GDSII) formats, with GDS (GDSII) preferred.
      - Be sure to draw all e-beam features as closed polygons.
      - Do not draw dots/circles as circles; substitute with polygons to limit the number of vertices/fractures.
      - Be mindful when utilizing arrays, especially arrays of arrays.
    - Determine if Proximity Effect Correction is needed.
  - Evaluate dose and e-beam shot pitch when checking sidewall/edge roughness of either the photoresist or final feature.
    - Be aware of limitations to shot pitch values with regard to resist and the e-beam blanker clock speed.
  - Determine what calibrations may be needed in addition to the basic set of calibrations.
- **Use what was learned to adjust the e-beam process.**
  - Remember, even small changes to the process or design – before or after the e-beam step can have project-stopping effects.
  - Use all test results to affirm or update the e-beam process.



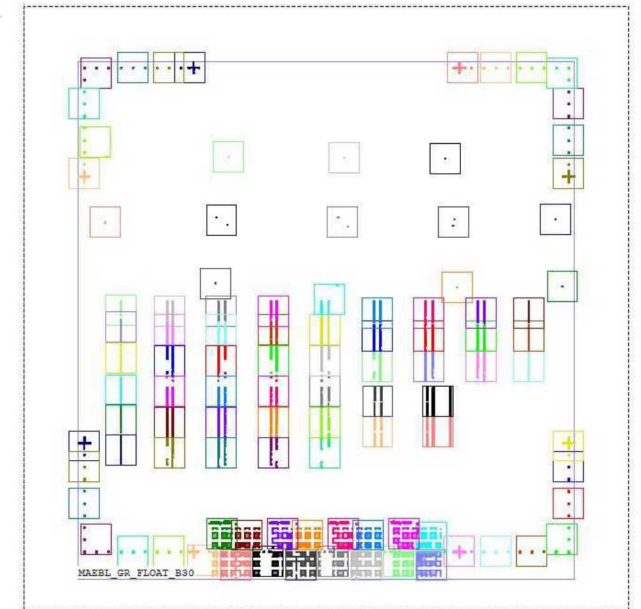


- Look for the field order that best suits the patterns.
  - The top image represents the default write field layout for the JEOL.
    - Features are split between fields – no the best scenario.
  - It would be better to position the fields so no features are written by multiple fields – when possible.



← Grating Layer - Fixed Field Export

Grating Layer - Floating Field Export →





- Additional views of the final features.

