

Project Title: Rapid Patterning and Advanced Device Structures for Low Cost Manufacturable Crystalline Si IBC Cells

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Executive Summary:

The objective was to develop the processing for an interdigitated back contact heterojunction (IBC-HJ) Si solar cell using laser technology for the patterning and contact formation. Laser patterning enables rapid, contactless manufacturing. The IBC-HJ device provides the highest demonstrated efficiency (>26%) due to the a-Si based HJ providing excellent passivation to the front and back surfaces and the IBC providing a high efficiency platform. The interdigitated metal contacts were to be formed by electrodeposition of Cu on laser patterned Ni seed layers. Despite the demonstrated efficiency potential of this device there is no commercial production presumably because of the challenges of patterning and processing the structure in an industrial high throughput environment. Our work sought to address that challenge.

During this project, we investigated many aspects of how the IBC-HJ device operation is influenced by the multi-layer a-Si based passivating and doped layer stacks and their patterning by laser and plasma masking. After an exhaustive focus in the first year on the laser fired emitter (LFE) and contact (LFC) using simpler back / front junction HJ (BHJ / FHJ) cells, we were unable to achieve open circuit voltages greater than 660 mV, compared to the 720 mV needed. We investigated significant variations in the metal doped stack (Al, Al/Ga for LFE and Al/Sb/Ti for LFC), the passivation layers (a-SiN/a-Si n and i) and the laser conditions. An additional issue with our original IBC structure was the presence of an inversion layer at the back surface. This enhanced recombination at the LFC and greatly reduced the Voc. We developed several innovative methods for characterizing and verifying the inversion layer including three terminal test structures allowing independent biasing between the IBC-type electrodes^{1, 2}.

These two limitations in the original design lead to development of a new IBC-HJ process sequence and device structure which we called Plasma Masked Laser Processed (PMLP). It retained the essential high efficiency features and still be manufacturable by design. It replaced the LFC with a standard a-Si n-i HJ contact and eliminates the inversion layer by replacing the previous i-p stack in the gap with an i-n or i-SiN stack. It used laser ablation of a dielectric (a-Si or a-SiN) layer followed by chemical etching to open the n-contact. As in the original design, it required deposition of a patterned stack through a mask in the plasma deposition chamber, typically it was the n-contact pattern. This turned out to be a source of significant problems due to inevitable unwanted deposition under the mask such that SiN or a-Si n-layer was deposited on the p-emitter region. This resulted formation of a blocking contact on the emitter which significantly reduced Voc and FF. Further research is required to understand the region between n and p as it could be a major source of recombination leading to low V_{oc} . Several iterations in PMLP device structure and chemical etching steps resulted in a large improvements, e.g. the efficiency increasing from 3 to 15% and Voc from 450 to 660 mV but they were unable to completely eliminate it. The best IBC-HJ device we fabricated had only 15% efficiency. For perspective, our standard FHJ devices had 20% efficiency.

It is very important to note that all the while we were modifying the basic device process and structure yet still obtaining very low Voc, the implied Voc (iVoc) remained relatively high. For example, the iVoc was > 710 mV while the Voc < 500 mV. This confirms that the laser ablation and etching steps were not degrading the passivation³. In fact one of

the major accomplishments of this project is that we showed that direct laser ablation and chemical etching of various dielectric layers on the back surface can be achieved with negligible (<10 mV) loss in $iVoc$. Originally, we thought this would be one of the biggest challenges. It indicates that laser patterning via direct laser ablation has strong potential for IBC and PERC cell processing. The relatively low efficiencies we obtained were due to the blocking barrier and challenges of plasma masking not due to laser ablation or patterning.

Excellent passivation is needed regardless of the patterning or rear structure. Throughout the project we conducted parallel studies to push the quality and reproducibility of the passivation. This included a detailed study of Si wafer surface cleaning and texturing⁴ and development of a bilayer deposition with hydrogen plasma anneal treatment⁵. These works lead to state-of-the-art $iVoc > 750$ mV for 10 nm i-layer passivation and cells with $Voc=725$ mV and efficiency=20% for 2.5 cm² area⁶. These enhancements in Si passivation engineering are easily incorporated into a manufacturing environment and hence are applicable to the broader implementation and scale up of HJ PV technology.

During 2nd and 3rd years we developed electrodeposition (ED) of Cu on thin laser patterned Ni layers. The ED and laser patterning steps were initially investigated separately using test structures^{7,8}. Different laser conditions different from those for LFC or laser ablation of dielectric layers were developed. Careful optimization was needed to simultaneously minimize the degradation to $iVoc$ and yet ensure complete removal so there was no shorting across the ~ 150 μm gap. The ED of 2-3 μm thick Cu films were carried out using a standard 3-electrode electrochemical cell, with Ni/Si substrates as the working electrode. Developed processing conditions for uniform Cu plating, with excellent adhesion, on laser-scribed Ni contacts for device incorporation. We obtained sufficiently low R_c for ED Cu/Ni/Si of ~ 5 m Ω .cm². We also identified a formation mechanism for the observed parasitic plating of ED Cu in laser scribes. ED was used to fabricate FHJ cells with rear IBC patterned Ni contacts with identical performance as standard evaporated Al metal. This confirmed that ED Cu on patterned Ni could provide similar low contact resistance and uniformity as standard Al metallization.

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1. Background:

The last several record efficiency Si cells have been interdigitated back contact heterojunction devices (IBC-HJ)⁹. The Institute of Energy Conversion (IEC) proposed and demonstrated the first IBC-HJ solar cell device in 2007¹⁰. A wide range of patterning methods have been reported for defining the p and n regions with photolithography as the most common method, although it is considered impractical for low cost manufacturing. The IEC had fabricated IBC-HJ cells with 20% efficiency using three photolithography steps prior to this project¹¹. This solar cell has an implied efficiency, from Suns-Voc measurements before metal patterning, of over 23%. We have developed a unique metal stack of Al-Sb-Ti for a laser fired contact (LFC), where the Sb is an n-type dopant which is critical to form the low resistance ohmic contact. In a previous DOE-supported FPACE program, we found that some patterning processes were harmful to the rear surface passivation while others were more benign but not low cost or manufacturable. We achieved over 17% efficiency for an IBC cell without any photolithography using masking during deposition and a laser fired contact (LFC) process.

Many industry groups are believed to use photolithography although they are purposely vague on patterning: LG (23.4%), Trina (24.3%), Sharp (25.0%), and Panasonic (25.6%) and recently Kaneka (26.7%). Sunpower (25.0%) employs a traditional diffused emitter and base, is silent about their patterning and has recently been using Cu plating. Considerable effort has been made to develop alternative patterning methods. Lasers have been increasingly utilized in fabrication of advanced Si solar cells. BP Solar developed an 18% efficient IBC cell (not HJ) with a LFC and laser defined emitters using

traditional screen printed patterning¹². ANU in Australia reported a 19% IBC cell efficiency (not HJ) using laser patterning and doping¹³. Another promising approach which avoids photolithography is to create individual doped regions by masking during PECVD deposition and then controlled selective growth of nanocrystalline Si for forming shorting ('tunnel') contacts requiring only one alignment step¹⁴. Despite a few groups reporting moderately good IBC cells with mechanical shadow masks during the plasma deposition, avoiding unwanted deposition 'leaking' under the mask is a known problem. To our knowledge, the highest efficiency IBC-HJ device made with laser patterning is from the Belgian team headed by imec who reported a 22.9% device using laser ablation and dry etching however the metal was patterned with lithography¹⁵. Laser processing has been one of the most crucial steps required for the fabrication of a functional IBC-HJ solar cell due to its several unique advantages: flexibility in pattern designing, high spatial resolution, controlled depth of ablation and elimination of complex masking lithography steps. In IBC-HJ solar cell architectures, a-Si:H (i) layers serve as the main passivation layer, which helps to inhibit interfacial defects and consequently enhances minority carrier lifetime (MCL) and implied open-circuit voltage (iV_{oc}). However, laser processing can induce such unwanted defects and heat-induced poly-crystallization, which results in low MCL, fill factor, and iV_{oc} .

Hence fundamental understanding and optimization of the IBC-HJ device structure simultaneously with the laser processing parameters is required. In this project, we intensively studied laser fired contacts, laser fired dopants, laser patterning of the a-Si, and metal layers, and application of plasma shadow masks.

2. Introduction:

Compared to the original SOPO, significant evolution in plans, device structures and processing techniques resulted from early identification of barriers. Based on our efforts with IBC-HJ cells and laser fired contacts (LFC) under a previous DOE/SETO project, we assumed that it would take a year of optimizing the LFC process and multi-layer stack to obtain sufficient $V_{oc} > 700$ mV, that plasma masking would be straightforward and that no major changes to the device structure as envisioned in proposal and original SOPO would be needed. Instead, we assumed that the major challenge was going to be in developing the laser process conditions to ablate the SiN and fully isolate the Ni seed layer without damaging the passivation. We had several contingency strategies to either repair the damage or use indirect laser processing.

In fact both assumptions turned out to be wrong. By the end of the first year we concluded that the LFC approach had to be dropped due to inability to simultaneously achieve high FF and V_{oc} . This was partly due to formation of an inversion layer at the rear surface creating a conductive channel that enables holes to easily flow to the highly defective LFC spots and recombine. Also, the effective diffusion length in these well-passivated n-type wafers was > 1 mm which meant carriers could also diffuse to LFC which were only 0.5 mm apart. Both of these mechanisms resulted in low V_{oc} . Two journal papers were published describing a very innovative application of three-terminal device structures (uniform front p or n contact) with IBC-patterned rear contact (the opposite contact from the front) to characterize the inversion layer and other 2D effects of IBC-HJ. One paper

applied Laser Beam Induced Current (LBIC) and simulation while the second applied electroluminescence (EL).

Because of the initial assumption that direct laser ablation would be difficult, we investigated several laser patterning strategies including indirect ablation (either removing or photo-exposing a photoresist layer) or post-ablation laser annealing we found that direct laser ablation of SiN/a-Si stacks and Ni seed layers was possible with negligible loss (< 10 mV) in implied Voc.

Thus a completely new device structure and approach was needed. In BP2 we developed the Plasma-masked Laser Processed device structure a processing which avoided a LFC and hence was less sensitive to the inversion layer conduction. The basic concept was the ablation of the top 1-2 layers in a multilayer stack (for example the p-i layers in a p/i/SiN/n) followed by an etch if needed as shown in Figure 1. The n-contact was to be made by a standard a-Si n/i layers. Several iterations were investigated (PMLP1-4 and reverse PMLP3) which differed in the order of p and n layer deposition, whether the n-layer was deposited before or after the laser ablation of SiN, thicknesses of the etch stop layers, the specific composition of the multilayer stack and which wet etches were needed to remove the underlying layers. For example, the evolution of the PMLP-2 device is shown clearly in Table 4 and Figure 15 in Section 3.2. Due to the change in technical direction, the DOE required a 6 month no-cost technical extension (NCE) at the end of BP2 to validate the new device concept. This successfully led to further investigations in BP3. However, a major challenge presented itself in all the PMLP iterations. This was the spread of plasma deposited films under the mask ('plasma leakage') spilling over into regions where it was unwanted and leading to a blocking barrier. For example, if we used a mask in the deposition of the 30 nm n-layer, a very thin layer would also be deposited under the masked area on what would become the p-layer. This unwanted plasma leakage had a tapered profile n-layer. Significant efforts over 1.5 years resulted in minimizing its impact and thickness but we were unable to completely eliminate it. Examples of the efforts include replacing the Si shadow mask with magnetic steel masks (made using our own lasers), developing different etching and deposition sequences (this is largely what drove the successive evolution of the PMLP structure), and laser isolation. The impact of the blocking layer, whether n or p, was a very low Voc (sometimes < 0.4 V), low FF ($< 60\%$ due to curvature in the power quadrant in the light) but often normal looking dark IV curves. It is essential to point out that many of these IBC-HJ devices had excellent implied Voc (iVoc) ~ 710 -720 mV before metallization. The pathologically low Voc is too low to be due just to recombination. We proved this by etching off the Al metal after testing cells with Voc < 0.5 V and found that iVoc had recovered to > 700 mV as shown in Table 5 below. All evidence points to the blocking layer formed by plasma leakage under the shadow mask as being responsible for the inability to obtain higher Voc and FF.

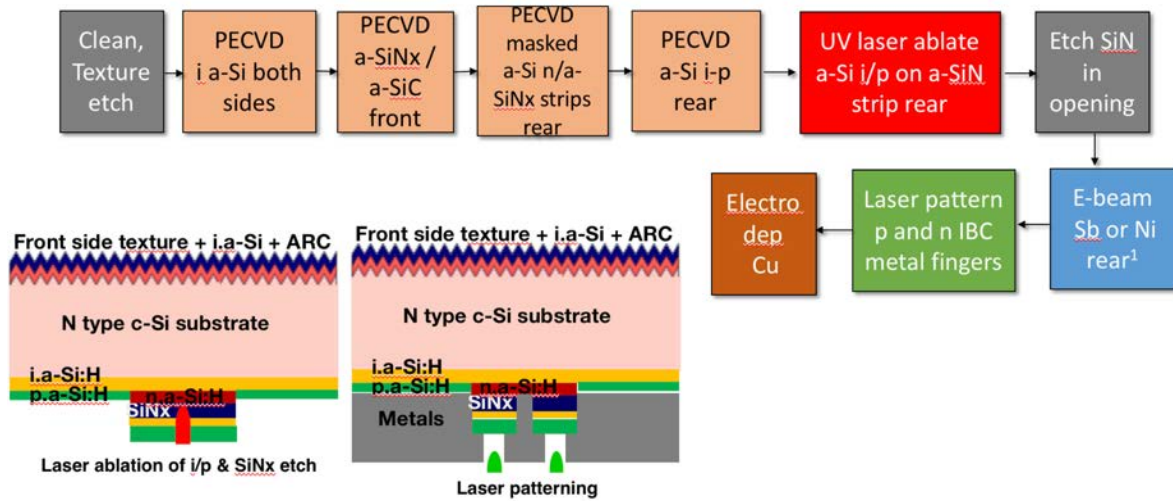


Figure 1. Process flow and diagrams of newly proposed PMLP IBC-HJ device. To replace LFC, UV laser ablation and a-SiN etching are used to open contact to a-Si n-layer. Several variations were developed. Diagram on left shows laser ablation of dielectric stack (such as p/i) followed by SiN etch in HF. Diagram on right shows laser patterning of the Ni metal prior to Cu ED.

A key outcome from this effort has been demonstrating that laser ablation and etching can be applied with negligible loss in passivation to provide low resistance heterojunction metal contacts. Previously, published research papers have shown that using ultra-fast picosecond (ps) and femtosecond (fs) laser processing has induced damages, lower open-circuit voltage (V_{oc}) and fill factor [1], [2]. There has been a minimal investigation of ns laser interaction with the passivation layers and other constituent layers used in different kinds of solar cell architectures [2]–[4]. Hence fundamental understanding and optimization of laser processing parameters are required to ensure efficient ablation of the top sacrificial a-Si:H (p and i) layers to expose dielectric SiN_x layers without affecting the underlying passivation layer. Such optimizations were carried out using ns pulsed lasers with wavelengths of 355 nm and 532 nm to create an extensive understanding of the effects of laser wavelength and ns pulse-width on the passivation and other constituent layers of IBC-HJ structures. Characterization techniques including optical microscopy, μ -photoluminescence (μ -PL), Sinton QSSPCD minority carrier lifetime measurement, scanning electron microscopy (SEM), energy-dispersive X-ray spectroscopy (EDS), ellipsometry, Raman spectroscopy and high resolution (HR) X-ray photoelectron spectroscopy (XPS) along with simulations involving predictive color charts were rigorously applied to develop a fundamental understanding of the laser process development.

Note that at the beginning of this project we had already developed the front surface texture, passivation and etch-resistant antireflection stack under a previous DOE award (the top layers of Figure 1). Therefore this project focused exclusively on the multilayer HJ contacts and structure, metallization and patterning on the rear of the IBC device.

Originally our industrial partner Silevo was going to provide 125 mm square textured wafers with passivation so that we could fabricate them into full size IBC cells. They were

supposed to provide guidance on manufacturability. We were going to provide them wafers with laser patterned Ni to be completed in their Cu-plating. Shortly after the program began, they were acquired by Solar City who then began collaborating with Panasonic on a similar device structure. They withdrew from supporting our project out of conflict of interest. It was agreed with DOE that we would investigate 50 mm square wafers as a fall back. While we were able to scale up our front junction devices to this size, there were formidable challenges to do this for the IBC so with agreement from DOE, we focused on 25 mm square wafers for the remainder of the project.

Below is a table with the milestones and comment regarding how closely they were met.

Table 1. Milestones from the original SOPO (Q1-Q8), the No-Cost Extension (NCE) (Q9-10) and Revised SOPO (Q11-Q14)

SOPO MS # Task #	Milestone Description	% Complete	Comment
<i>MQ1.T1</i>	<i>Obtain $V_{OC} > 650$ mV with HJE (Q1)</i>	100	Obtained $V_{OC} > 690$ mV
<i>MQ2.T1</i>	<i>Obtain $V_{OC} > 650$ mV with LFE or else drop Subtask 1.1.1 (Q2)</i>	100	drop LFE
<i>MQ3.T2</i>	<i>Demonstrate surface recombination velocity (SRV) < 100 cm/s with laser annealing / repassivation after laser ablation of metal on passivation stack (Q3).</i>	100	SRV=10-25 cm/s after lasing without repassivation
<i>MQ4.T1</i>	<i>Obtain $V_{OC} > 700$ mV with HJE and/or LFE IBC cells on 25mm wafer under 1 sun AM1.5. Downselect between HJE and LFE based on maximum V_{OC} and minimum ΔV_{OC} with $R_S < 2 \Omega \cdot \text{cm}^2$ for IBC cells on 25mm wafer.</i>	90	obtain $V_{OC} > 720$ mV on FHJ on 25 mm wafer
<i>MQ5.T2</i>	<i>Obtain isolation $R_{SH} > 1\text{k}\Omega$ (determined on test structures or cells on 25 mm wafers) with laser patterned contacts (Q5)</i>	100	$R_{SH} > 10 \text{ k}\Omega$
<i>MQ6.T3</i>	<i>Demonstrate contact resistance $< 3 \text{ m}\Omega \cdot \text{cm}^2$ and adhesion pull strength $> 0.2 \text{ N/mm}$ (determined on test structures or cells) for laser fired and Cu plated contacts (Q6)</i>	100	obtained $5 \text{ m}\Omega \cdot \text{cm}^2$ and adhesion $> 0.2 \text{ N/mm}$
<i>MQ7.T2</i>	<i>Obtain SRV < 100 cm/s and $R_{SH} > 1\text{k}\Omega$ with laser patterned contacts. Downselect between laser patterning methods.</i>	100	$R_{SH} > 100 \text{ k}\Omega$ and SRV=10 cm/s with laser patterned Ni

MQ8.T4	<i>Fabricate IBC cell with laser processing having 22% efficiency.</i>	60	obtained eff=15.2%
MQ9.T1 (NCE)	<i>Obtain Voc > 700 mV with masked deposition in PMLP device.</i>	90	obtained Voc=652 mV on PMLP2
MQ10.T3 (NCE)	<i>Demonstrate a Voc of >710 mV and alignment tolerance of 20 microns. (it was determined that this was unnecessarily tight tolerance due to laser ablated regions being narrower than the n strips)</i>	70	obtained Voc=652 mV with 50 um tolerance
MQ11.T3.4	<i>Demonstrate $iV_{OC} > 720$ mV on IBC structure with laser processing before metalization</i>	100	obtained iV_{OC} =722 mV before metalization
MQ12.T3.4	<i>Obtain $RS < 2 \Omega.cm^2$ on laser-patterned device structure with plated Cu contact.</i>	100	Obtained $RS = 0.5 \Omega.cm^2$
MQ13.T3.5	<i>Demonstrate Voc > 740 mV on IBC cell with laser patterning</i>	70%	Obtained Voc=633 mV on PMLP3
MQ14.T3.5	<i>Fabricate IBC device having laser patterning with efficiency > 25%</i>	50	Best IBC cell with laser patterning 15.2%

3. Project Results and Discussion:

3.1 Laser fired emitter (LFE) and Contact

3.1a Summary:

The initial approach for the project was to develop laser fired emitters (LFE) and laser fired contacts (LFC). The LFEs and LFCs were designed to eliminate the need for depositing and patterning doped a-Si layers and to reduce the total area of p-n junction and contact, and thereby reduce recombination, like PERC cell architecture. In general, the approach was to deposit a passivating high resistance layer over the Silicon (like i.a-Si:H/SiNx:H), and an appropriate dopant layer like Sb for LFCs or Ga for LFEs. Firing a laser in a spot or line would create a point contact through the high bandgap (E_g) layer (SiNx:H), drive the dopant into the Si wafer, and create an ohmic point/line contact in the case of LFCs, or a point/line junction for LFEs. We had previous experience with LFC but not with LFE.

Both approaches were realized during the project with varying degrees of success. In the case of LFE, moderately high open-circuit-voltage (V_{OC}) was realized (630mV), but a

high fill factor (FF) could not be achieved. A high density of LFE was required for high FF, but too many would eventually reduce V_{OC} due to laser damage of the Si surface passivation. For LFC, the story was very similar. V_{OC} as high as $\sim 705\text{mV}$ was measured, but with low $FF < 70\%$. The best FF achieved with LFC was 72% with a V_{OC} of $< 620\text{mV}$. A comparison of best devices achieved with LFE, LFC, and standard heterojunction is shown below in Table 2 (implied V_{OC} from QSS photoconductive decay measurements.)

Table 2: Summary of best results from LFC and LFE efforts. The first three are FHJ and the last row is an IBC-HJ with LFC. Results for FHJ with LFC shown for highest V_{OC} and highest FF separately to highlight inability to obtain both high V_{OC} and FF simultaneously.

Device	V_{OC} mV	J_{sc} mA/cm^2	FF %	Eff %	iV_{OC} mV
Standard FHJ	725	36.7	75.9	20.2	~ 730
LFE FHJ	570	23.4	55.6	7.5	~ 735
LFC FHJ	662	35.0	64.1	14.8	~ 735
IBC-HJ	617	33.2	56.7	11.6	710

After a substantial effort, it was determined that the LFE and LFC efforts should be dropped, and alternative methods should be pursued, like laser ablation and masked plasma deposition. For LFE, a low-barrier, low-recombination emitter could not be fabricated. At low laser power, junctions with large barriers to conduction were formed, and at higher powers, the laser processing damaged surface passivation. At the laser processing conditions which yielded the highest V_{OC} , the junction still had properties of high resistance/high barrier which limited FF. The tradeoff between V_{OC} and FF was also seen when optimizing LFE coverage – higher coverage resulted in marginally better FF with large reductions in V_{OC} due to laser damage. Laser annealing of the junction and Ga doping were found to be critical to forming the optimal V_{OC} , but not enough to meet project goals.

For LFC, there were similar challenges, where laser damage at the back contact could provide a high recombination pathway, so increasing the laser power, number of pulses, and density of LFC would reduce V_{OC} , but yield a slight increase in FF. We determined that the low FF from LFC was a result of a inversion layer between the $\text{SiNx:H}/\text{c.Si}$ interface that would allow for high recombination. Diode ideality factors (n) were measured > 2 with low laser power conditions (high V_{OC} conditions), which limited FF. FF loss from R_s was found to be consistent across a wide range of process conditions.

3.1b Laser Fired Emitter (LFE)

Laser fired emitter (LFE) studies were carried out to determine laser processing parameters and their impact on V_{OC} , J_{sc} , FF in order to evaluate the overall cell efficiency. Initial studies used metal diode test structures and were followed by rear junction (rear LFE) solar cells.

Effect of laser firing power on test structure metal diode behavior

The devices for laser firing were designed and fabricated by IEC. The laser processing experiments and characterization was done at U Va. The dielectric layers of a-Si or SiN

were deposited on textured or polished surfaces. Metal pads of Al/Ga or Al were then patterned on the dielectric layer in order for laser firing. The Ga is potentially a more effective p-type dopant compared to the more widely used Al. A 532 nm fiber laser with 1 ns pulse width was used to form emitter under different laser powers. The dark I-V curves were measured to evaluate the diode behavior after laser firing.

For structures with SiN dielectric on polished surfaces, Al/Ga metal devices (MC1618_08) showed a much higher forward current than Al-only devices (MC1618_07), indicating a better junction / contact behavior suggesting the Ga was an effective dopant. Thus, devices of Al/Ga metal with SiN dielectrics on polished surfaces were used to further evaluate the device performance and laser firing mechanism is described in the following sections.

Laser firing mechanism through SEM and EDS analysis

The SEM and EDS were carried out for laser firing of devices with Al/Ga metal and SiN dielectric on polished surfaces under different laser powers. Figure 2 shows results for 35% (Figure 2a) and 55% (Figure 2b) power. After laser firing at 35% power, the silicon element is detected in the spot center while the aluminum and gallium elements become undetected. When laser firing power increases to 55%, the detected silicon area covers most of the area of laser fired region as shown in Figure 3b. Also, the melting of silicon after laser firing is confirmed by the morphology changes in SEM. These behaviors suggest that the laser firing can diffuse the metal in the melted silicon to form the emitters; it may ablate some metal under high laser powers.

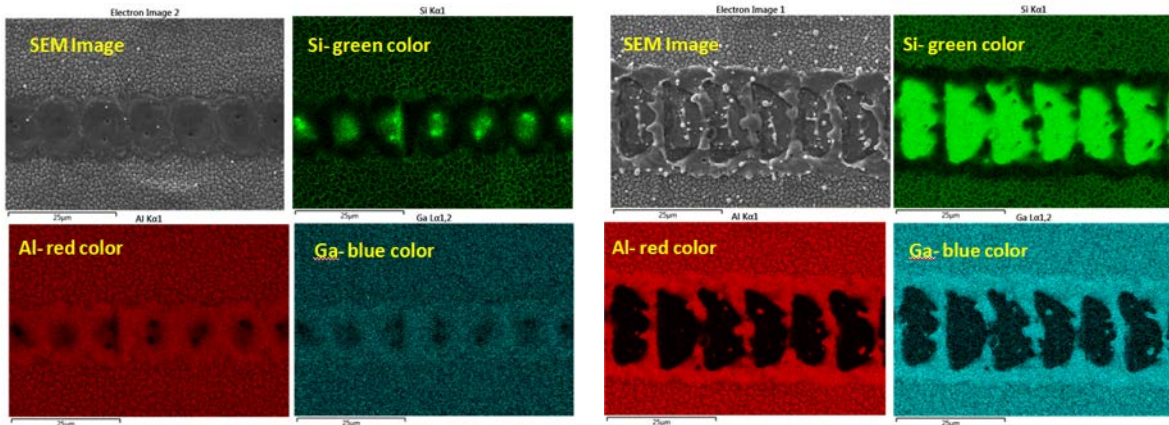


Figure 2: (a, left) SEM and EDS for 35% laser power with Al/Ga for MC1618-08, (b, right) SEM and EDS for 55% laser power with Al/Ga for MC1618-08.

Applying laser firing to rear junction solar cells - device performance

In order to evaluate the device performance under 1 sun illumination, solar cell device structures (Figure 3) were made by IEC for laser studies at UVa with front-side transparent ITO and metal grids for contacts. The Al or Al/Ga metal pads on the back allowed for rear LFE and were 0.56 cm².

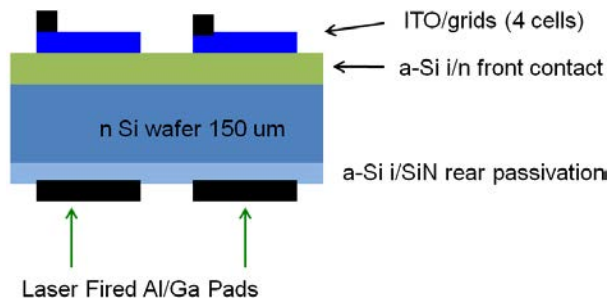


Figure 3: LFE device structure for evaluating device performance

Multiple evenly distributed laser fired lines were formed on the device structure. The number of laser fired lines were optimized to achieve minimum emitter area while maintaining high V_{oc} although this might also result in a lower fill factor. The laser fired line width was $20\text{ }\mu\text{m}$ and the length was 2 mm using a mask to avoid damage from the long dwell time at the laser beam turning points. We continued increasing the number of laser lines until 40 lines which corresponds to an emitter area of 2.8% .

As shown in Figure 4, the short circuit current and open circuit voltage keep increasing until 32 laser fired lines. After 40 laser fired lines, the short circuit current and open circuit voltage start to drop presumably due to increasing laser damage. The maximum open circuit voltage after laser firing was 0.42 V and the maximum short circuit current was $\sim 25\text{ mA/cm}^2$.

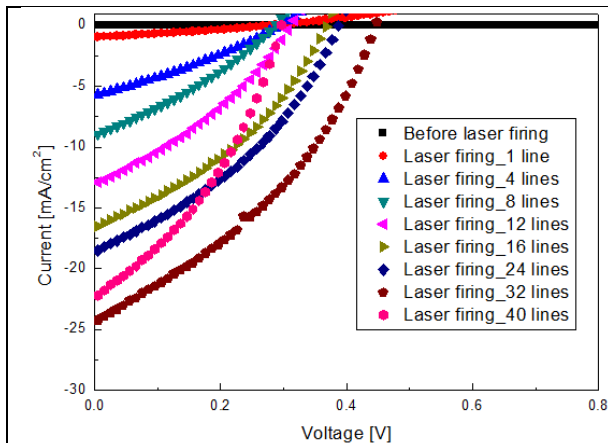


Figure 4: Illuminated I-V curves under different number of laser fired lines for rear LFE cell (Fig. 3)

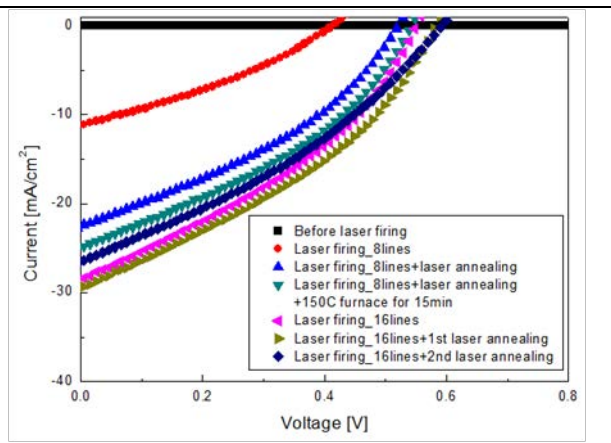


Figure 5: I-V curves for different cell with 8 then 16 LFE lines after laser annealing

Effect of laser annealing for laser fired emitter

Post laser annealing was applied to enhance the performance of laser fired emitters. A 1070 nm fiber laser with 0.1 ms pulse width was used to anneal the devices. The illuminated solar cell device performance after laser annealing is shown in Figure 5, which is based the device structure in Figure 3. The laser annealing after laser firing 8 lines greatly increased the open circuit voltage and short circuit current, demonstrating the effectiveness of laser annealing in enhancing the device performance. After laser

firing another 8 lines followed by laser annealing, the short circuit current and open circuit voltage further increased.

LFE devices with open circuit voltage of 0.63V on semipolished wafer

Based on the optimization of number of laser fired lines and the investigation of laser annealing, we laser fired 20 lines of 6 mm length and then laser annealed 3 times. The results are shown in Figure 6. A 150°C furnace annealing was first given to improve the ITO contact quality. After the laser firing, the open circuit voltage was 0.51 V. After 1 time laser annealing, the open circuit voltage increased to 0.57 V. The 2nd time laser annealing further increased the open circuit voltage to 0.62 V and the 3rd time laser annealing saturated the open circuit voltage at 0.63 V. The J_{sc} was rather low due to the high surface reflection losses. If corrected for the current expected for a well textured front surface ($\sim 38 \text{ mA/cm}^2$), then the V_{oc} would increase to about 0.64V. Given these poor results along with the excellent emitter already available with traditional a-Si p-layers, we downselected away from LFE work consistent with the BP1 Task 1 Milestone.

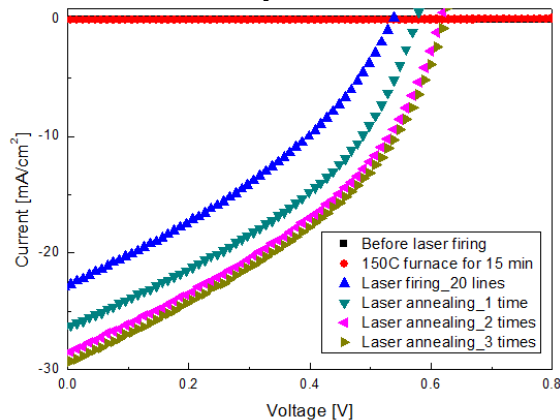


Figure 6: Laser fired emitter and laser annealed devices showing V_{oc} of 630mV

3.1.c Laser Fired Contact

Laser fired contacts (LFC) were essential to the original IBC device structures under consideration in this project. We report here on two LFC studies: one compared two different a-Si based dielectric layer stacks, namely, i/a-SiN_x:H and i/n a-Si. Parallel laser processing studies were carried out at IEC and UVA. The other study compared a 2x2 matrix: two different relevant stacks, a-Si i/p/SiN or i/SiN/i/p with 50 or 200 nm Sb doping layers. The first study used front HJ cells while the second study used an IBC device structure. Results of the LFC work from this program were presented at the 45th IEEE PVSC¹⁶.

Device structures and laser firing conditions

The front HJ (FJ) device structure used for LFC is shown in Figure 7a. The back surface has dielectric stack (10 nm ia-Si/ 50 nm SiN) and metal stack of Ti (5nm) / Sb (50nm) / Al (500nm). Our previous work confirmed that Sb is critical to obtain a low contact resistance. The ohmic back contact needs to be formed by laser firing of the metal through the dielectric stack. To determine the degradation induced by LFC, a similar device structure (Figure 7b) was fabricated, except that the n-type a-Si layer replaced the insulating SiN layer, thus providing a complete operational solar cell without any LFC. The FJ devices

with a-Si n-layers allowed exploring the degradation from laser conditions like the SiN samples.

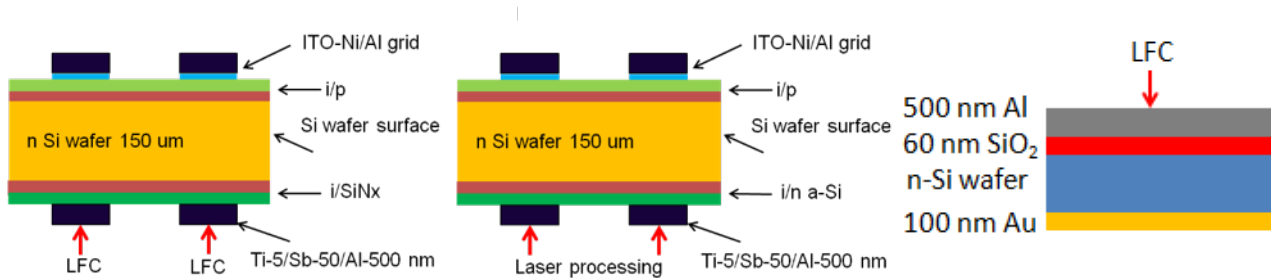


Figure 7: Device structures for LFC of run MC1662. a) front junction with i-SiNx rear stack+Ti/Sb/Al stack. (b) FJ with rear i-n stack+Ti/Sb/Al; (c) Test structure for optimizing LFC process (UVA)

Effect of laser damage

At IEC and UVA, parallel studies were conducted over a wide array of laser firing conditions to evaluate the effect of laser processing on devices with a i-n.a-Si back dielectric stack (Figure 7b). While there were some differences between the two experiments, laser firing at both locations lead to a reduction in V_{OC} with increased laser energy with only a small gain in FF.

At UVA, test structures (Figure 7c) were used to find optimal firing conditions that would fire through a dielectric without damaging lifetime. Those conditions were used to fire standard front HJ devices with the configuration seen in Figure 7b. Figures 8a and 8b shows that with increasing laser processing area (e.g. number of spots), the V_{OC} steadily decreases while the FF initially decreases then slowly recovers. The decrease in V_{OC} is caused by the increase in recombination damage from the LFC. The light JV curves are in Figure 9a. Laser studies at IEC found similar trends in V_{OC} but no change in FF over a narrower range of laser processing conditions (changing both fraction LFC area and energy per contact).

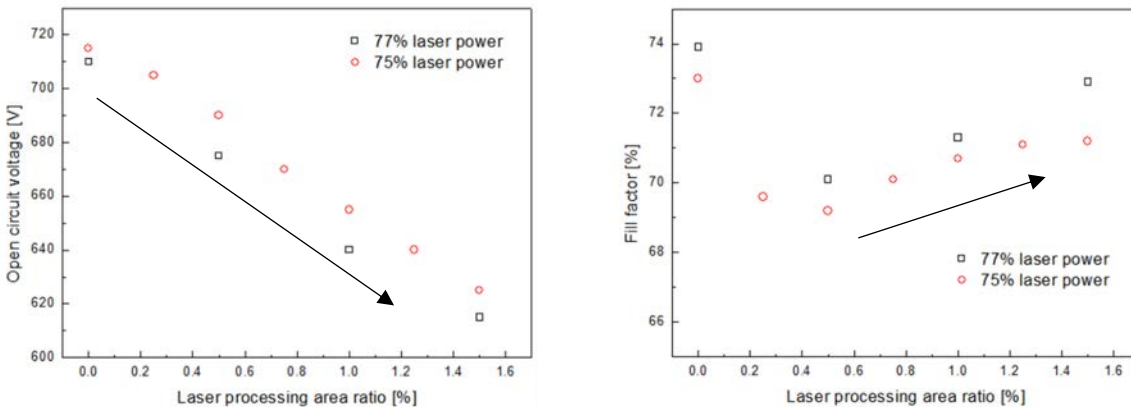


Figure 8: Dependence of V_{OC} and FF on increasing laser firing area ratio under different laser powers for FJ devices in Figure 7(a) open circuit voltage vs laser processed area ratio. (b) fill factor vs laser processed area ratio. Devices: MC1662-01_02 and _03

LFC on FHJ with a-SiNx:H back dielectric stacks

At UVA, the laser power was re-optimized for a-SiN_x:H back dielectrics (Figure 7a), and laser processing area varied. Due to a different dielectric, a higher laser power was needed for optimal contact. At the IEC, the laser power and laser processing area were both varied. In both experiments, an anti-correlation between V_{OC} and FF was observed as seen in JV curves in Figure 9b. As either laser processing area or laser power increased, FF increased, and V_{OC} decreased. The largest V_{OC}'s were ~660mV in experiments at UVA and IEC but with low FF<65%.

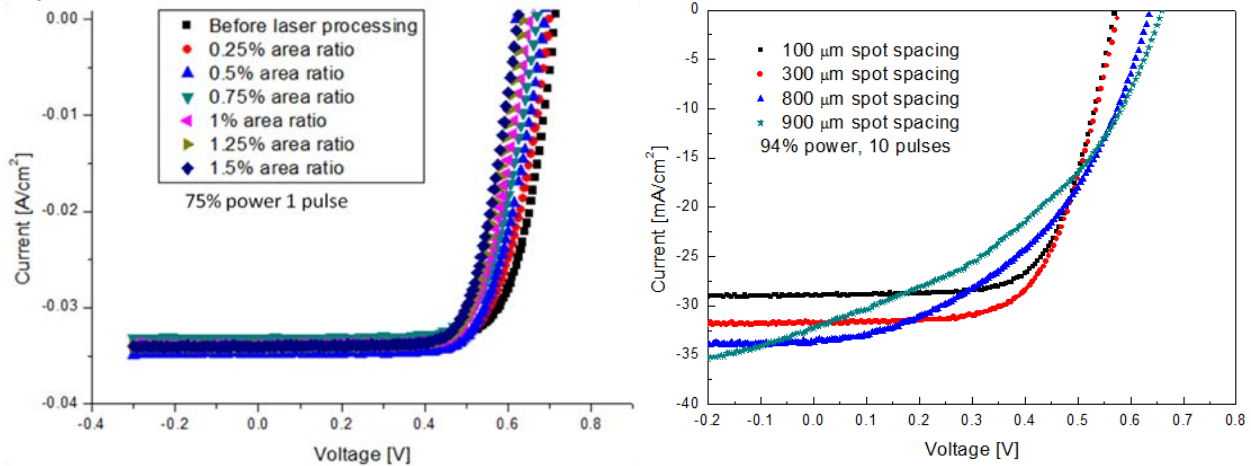


Figure 9 : Illuminated JV curves of FJ devices with (a) *n a-Si* layers after laser processing at 75% power and (b) *SiN_x* layers after LFC under different spot spacing at 94% power. Increasing spot spacing leads to fewer spots, smaller laser processed area fraction.

Diode parameter analysis was applied to understand the decrease in FF at low spacings. After obtaining series resistance (R_s), the FF was corrected for R_s loss. Figure 10b shows that FF losses due to series resistance are low, around 2-4%, while a variation in FF of 40% absolute is seen. Figure 10a shows that at low energy per area (equivalent to small laser processing area) the light ideality factor is $\gg 2$, while the dark ideality factor is nearly independent of laser processing. This indicates that the low FF and high V_{OC} is likely due to a second junction that forms due to an accumulation of minority carriers at the c.Si/a-SiN_x:H interface between laser fired contacts. Under illumination, this accumulation of electrons can form an opposing diode that limits FF and increases V_{OC}. The decrease in V_{OC} is due to increased laser damage with the ideal i/n back dielectric since it already has a high Voc and FF without laser firing. However, the maximum V_{OC} of 660mV is lower than the maximum laser damaged V_{OC} of the i/n devices due to additional losses from the electron accumulation at the back contact in the SiN_x:H devices. Further details can be found in our 45th IEEE PVSC paper referenced above.

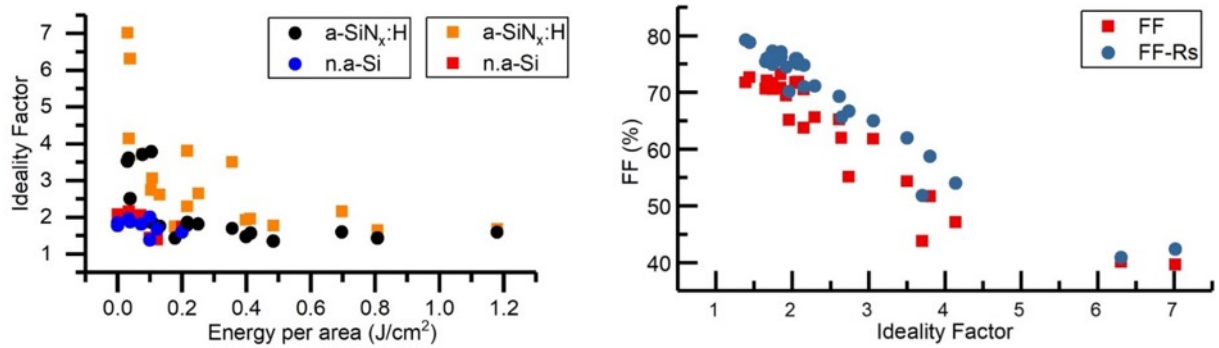


Figure 10: (a) Estimated ideality factor, N , from dark JV (black and blue) and light JV (orange and red) for cell with LFC through a-SiNx:H (orange and black) and n.a-Si:H (red and blue) as a function of E_A (b) measured R_s and corrected FF vs ideality factor

LFC on IBC cells

A wide range of LFC conditions were applied to IBC cells at the IEC. The thickness of the Sb layer over the SiNx:H layer was varied from 50-200 nm, and a i/p/SiNx:H and i/SiNx:H/i/p back dielectric stack were evaluated. Several variables including number of LFC per n-finger strip (CpF =contacts per finger) were studied. Table 3 shows that V_{OC} was low for all i/p/SiNx:H back dielectrics, and the best performance was found with thicker Sb layers. JV curves for some of the IBC cells with LFC are in Figure 11.

Table 3: JV results from 2 IBC devices with 200nm Sb and i/SiNx/i/p stack. Device MC1658-05 results shown for first 60 then 180 LFC contacts/finger (CpF) at 255 mW

Sample	LFC conditions	$V_{OC}(mV)$	$J_{sc}(mA/cm^2)$	FF(%)	$\eta(\%)$
MC1658-05	a) 60/f, 255mW	632	29.6	50.1	9.4
“	b) another 120/f	617	33.2	56.7	11.6
MC1658-06	c) 60/f, 165mW	625	36.05	48.3	10.9

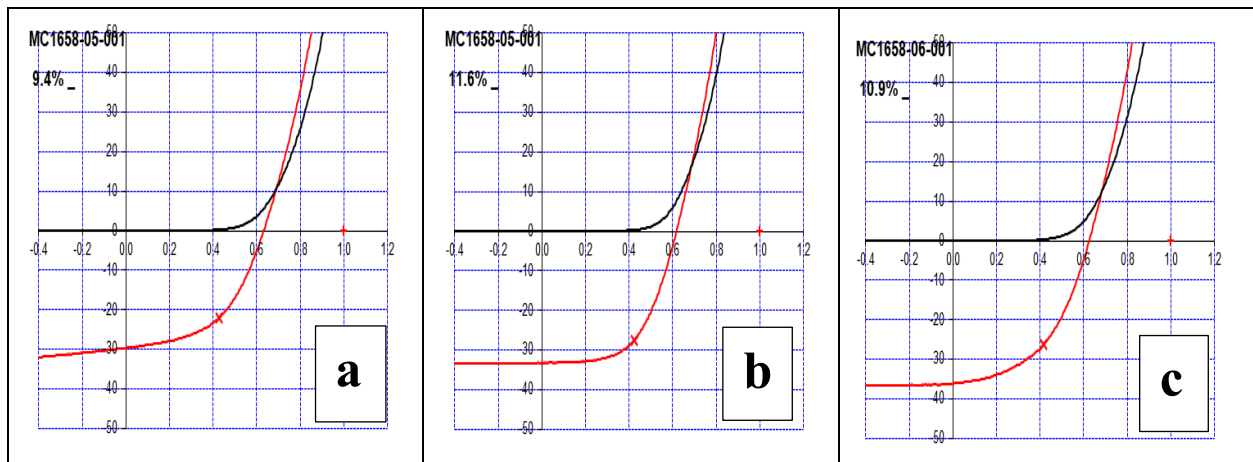


Figure 11: JV curves for IBC cells with LFC from **Error! Reference source not found.** above above with 200nm Sb and i/SiNx/i/p stack: a) MC1658-05 with 60 CpF; b) MC1658-05 with 180 CpF; c) MC1658-06 with 60 CpF

3.2 Development and Evolution New IBC Device: Plasma Mask Laser Patterned (PMLP)

3.2.a Introduction

In order to overcome the limitations of Laser Fired Contact (LFC) structures we investigated a new architecture where we laser pattern dielectric stacks for the IBC structure. In this approach we use a mask to deposit the dielectric stack patterned as a contact of the IBC and then we laser pattern the n region to make contacts hence the name 'Plasma Mask Laser Patterned' (PMLP) IBC solar cells. The first generation structure (PMLP1) is shown in Figure 1 and again Figure 12 and the process flow is shown in Figure 1 in the Introduction. There were 3 further iterations (PMLP2, 3, 4 and Reverse PMLP3) described below. The first generation PMLP structure utilizes masked deposition of a-Si i/n/i/SiN followed by a blanket i/p layer. Then, a UV laser will selectively laser ablate the top a-Si p/i layer so that SiN can be selectively etched chemically allowing for contact to n layer.

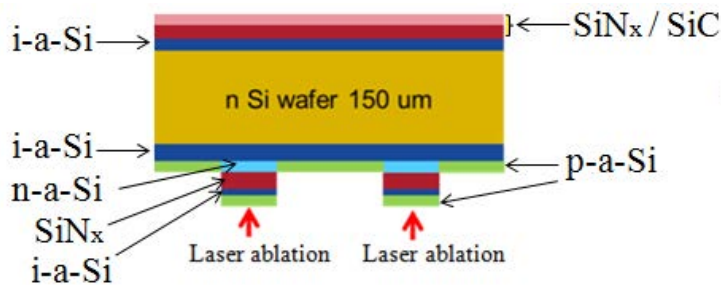


Figure 12. IBC device structure for laser ablation of a-Si for metal contact opening.

The back side is 10 nm i-a-Si / masked deposited 50 nm n-a-Si / 100 nm SiN / 5 nm i-a-Si with a blanket 20 nm p-a-Si layer. The thicker SiN was used to prevent any damage to passivation layer during laser ablation. The 5 nm i-a-Si layer protects the SiN layer during HF etch. The goal is to ablate localized openings in the i-a-Si/p-a-Si layers on top of the SiN layer without damaging passivation layer. With the laser patterned openings, the cell will be completed by selectively etching off SiN and depositing metal contact. The metal should make an ohmic contact with the a-Si n-layer without any laser damage to the passivation layer from laser patterning.

3.2.b PMLP Architecture

The first trial of PMLP cells gave $V_{oc} < 350$ mV, $FF < 40\%$ and efficiency $< 5\%$ though the cells had $iV_{oc} > 710$ mV before metallization. We had never seen such a huge difference ($\Delta V_{oc} > 300$ mV) between iV_{oc} and V_{oc} ($\Delta V_{oc} = iV_{oc} - V_{oc}$). We immediately surmised that the plasma leak (as shown in Figure 13a) while depositing the n/SiN/i through mask resulted in poor p-n junction. This was addressed by using a short HNA etch to remove plasma leakage. For making the stack HNA etch resistant we deposited a stack of n/SiN/SiC instead of n/SiN/i. This etching helped to achieve $V_{oc} > 650$ mV in a rear HJ with similar rear structure as PMLP thereby proving that removing block contact due to plasma

leak at emitter can improve the Voc of the cell. Using HNA etch we improved the Voc to 537mV and efficiency of 8.5% of PMLP IBC cells as shown in Figure 13b.

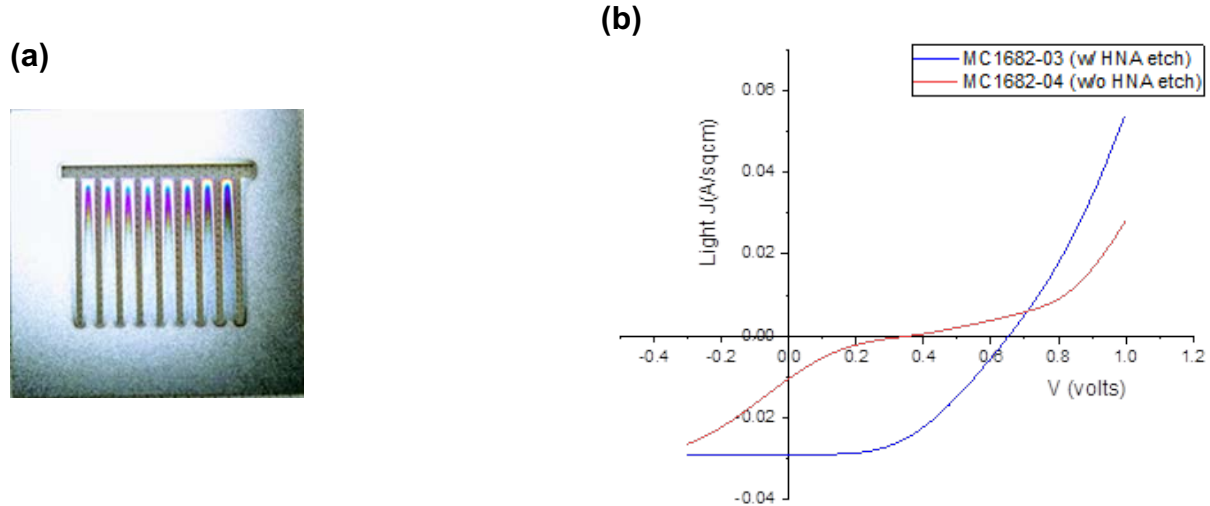


Figure 13. a – Plasma leak of n/SiN dielectric stack deposited using n mask Figure 33. b – J-V curve of Rear HJ cell with and without etching of Plasma leak by HNA

3.2.c PMLP-2 Architecture

A major problem with the initial PMLP structure was that the HNA etch not only etches the unwanted film leakage but also etches SiN and the passivating i layer. To eliminate HNA etch of plasma leaked films a new version called PMLP2 was introduced. The PMLP2 structure is shown in Figure 14 with the important variations in the process. Unlike PMLP, PMLP2 does not involve masked deposition of n layer. It only deposits SiN by mask. Plasma leak from SiN is easily etched in HF with good selectivity unlike HNA etch of n.a-Si:H leak, which also etch the passivating i-layer. Thus in PMLP2 we can better control the etching of plasma leak without affecting the passivation layer.

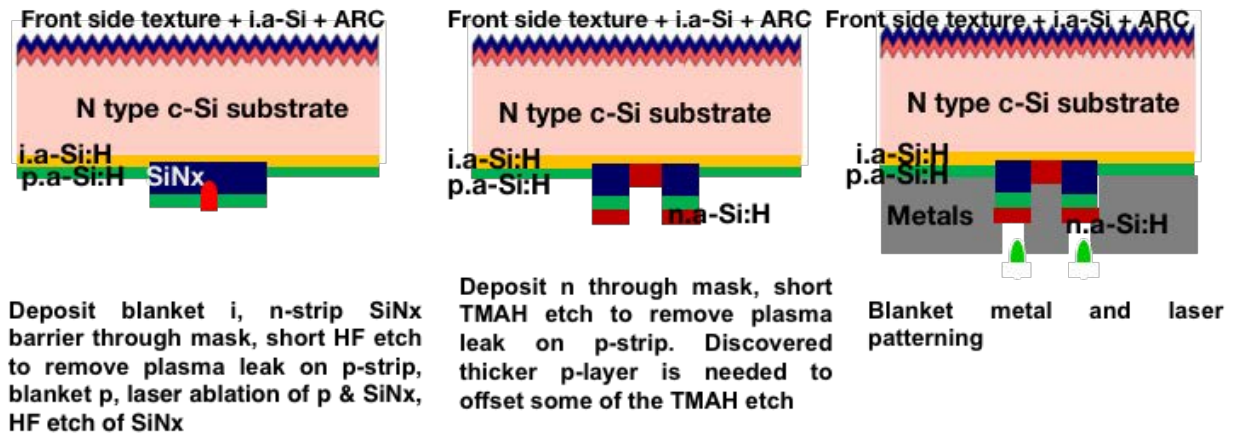


Figure 14. Cross section of improved PMLP2 cell structure and description of key process improvements.

In PMLP2, the SiN is deposited using mask and then laser ablated on the n strip followed by deposition of n layer through n mask. Our first trial of PMLP2 gave a Voc of 565mV with an efficiency of 10.7%. The n leak over the p layer was identified as the major limiting

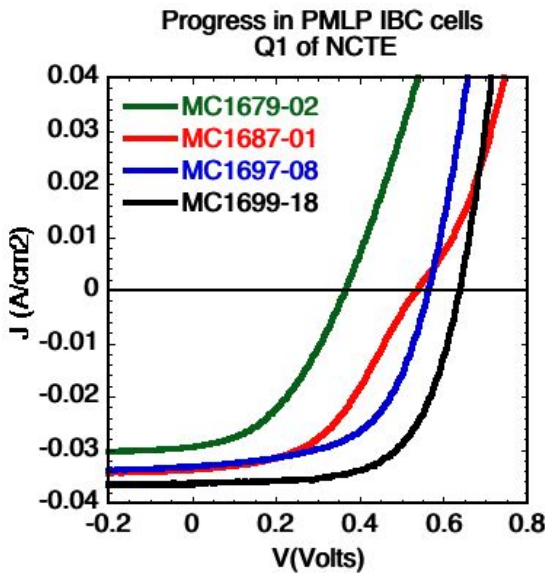
factor. In the 2nd iteration the n leak was removed using TMAH (Tetramethylammonium hydroxide) and SiN leak is etched by HF. However the TMAH etched p layer as well limiting the Voc to 580mV and efficiency to 10.9%.

Additionally, since passivation of the defects at the heterointerface is critical for obtaining high starting iVoc, we put considerable efforts to engineer the interface. A detailed study was done on the effect of different cleaning methodologies for the surface of Si to reduce contamination and make a pristine surface available for the i layer passivation. After developing a protocol for cleaning the Si surface and passivating the Si surface⁴ with the intrinsic i layer which gave initial iVoc of 720-725mV, we developed a novel plasma treatment method that could further improve the interface by using hydrogen to heal the defects. The hydrogen plasma treatment (HPT) was the first demonstration of using DC plasma as a method to engineer the interface to obtain an iVoc of 755mV in Heterojunction technology⁶. The HPT which is a short process followed after the i layer deposition helped to consistently get over >735mV with a minority carrier lifetime of 1-2 ms for 10nm thick i layer annealed at 300 C for 25 minutes.

Table 4 – Variations in PMLP & PMLP2 architectures. The flow shows the evolution and major changes in PMLP2 structure as compared to PMLP

Cell ID	Description	iVoc w/ doped layers (mV)	Voc (mV)	Jsc (mA/cm ²)	FF (%)	Eff (%)	Observations
MC1679-02 (PMLP)	n/SiNx stack through n-mask, blanket p, laser ablation of n-strip, nitride etch and metallize	717	366	29.5	42	4.6	Plasma 'leakage' of n/SiNx films on the p strip before p-layer deposition leading to poor HJ contact.
MC1687-01 (PMLP)	Introduced HF/HNA etch to remove plasma leakage of SiNx/n films	681	537	33.8	47	8.5	HNA etch improved the cells but introduced another challenge as it also etch the passivating i-layer. Low iVoc.
MC1697-08 (PMLP-2)	SiNx through mask, blanket p, laser ablation of n-strip, nitride etch, n-dep. thru mask and metallize	722	565	33.3	57	10.7	Plasma 'leakage' of n-layer films on to the p-layer increased recombination. Reverse order of p and n. Voc improved after HT.
MC1697-07 (PMLP-2)	Introduced TMAH etch to remove plasma leakage of n-layer films	719	580	33.4	56	10.9	TMAH has poor selectivity between n- and p-doped layers. Likely etched the 10 nm p-layer. Voc decreased after HT.
MC1697-04 (PMLP-2)	Increased p-layer thickness to 20 nm	710	636	34.3	60	13	Low iVoc. Better passivation after TMAH etch. Voc improved after HT.
MC1699-18 (PMLP-2)	Increased p-layer thickness to 40 nm	703	652	36.4	64	15.1	Low iVoc. Better passivation after TMAH etch.

We increased the p layer thickness to 20nm which helped retain p after TMAH etching. This improved the Voc to 636mV and efficiency to 13%. We further increased the p layer thickness to 40nm to prevent over-etching which improved Voc to 652mV and efficiency to 15.1%. Table 4 shows the major changes in process with the improvements in cell performance and Figure 15 shows the evolution in JV curves.



Cell ID	Observations/comments
MC1679-02 (PMLP)	Plasma 'leakage' of n/SiNx films on the p strip before p-layer deposition leading to poor HJ contact.
MC1687-01 (PMLP)	HF/HNA removed plasma leakage of SiNx/n films and improved Voc, Jsc, FF but etched the passivating i-layer. Low iVoc (687mV).
MC1697-08 (PMLP-2)	Reverse order of p and n. Using only SiNx (no a-Si or SiC) through mask so only HF etch. Plasma 'leakage' of n-layer films on top the p-layer increased recombination
MC1699-18 (PMLP-2)	Increase p-layer to 40 nm to offset TMAH losses. Low iVoc. Better field effect passivation after TMAH etch. Voc improved after HT.

Figure 15. Evolution from PMLP to PMLP2 structures with the major changes in process

The J-V analysis of the cells in Table 4 shows that the Fill Factor (FF) of the cells are not limited by series resistance (R_s). The cells have $R_s \sim 0.5 \Omega \cdot \text{cm}^2$ which is comparable to 19% efficiency Front Junction (FJ) solar cell. The loss in FF happens due to the high ideality factor ($n > 3$) under illumination for the highest efficiency PMLP2 cells having FF of ~60%.

The dramatic difference between $iVoc$ and Voc (ΔVoc) had not been seen before. Typically ΔVoc was 10-30 mV not 100-300 mV as in Table 1 above. To confirm that it was not due to metalization damage, a few IBC cells had the Al etched off and $iVoc$ was remeasured. Table 5 shows that it recovered to nearly the original value, over 300 mV higher than the Voc . This confirms that the problem is due to injection of current at Voc not due to recombination or poor passivation.

Table 5. $iVoc$ and Voc at various stages in processing. Red data confirms we maintain high $iVoc$ with negligible decrease (2-4 mV) after all laser processing and etching steps. Device Voc is < 350 lower than $iVoc$. Original $iVoc$ is restored to almost same value after removing metal

ID	$iVoc$ before laser processing (mV)	$iVoc$ after laser ablation and HF etching (mV)	Device Voc after metallization (mV)	$iVoc$ after metal etch removal (mV)
MC1679-02	717	715	366	705
MC1679-03	727	723	355	711

3.2.d PMLP-3 Architecture

PMLP2 structures showed problems in repeatability due to misalignments caused due to multiple alignment steps and non-uniform etching of the p layer while etching the n plasma leak. To reduce the number of misalignment steps and to get a better emitter contact we developed the 3rd version of IBC PMLP called PMLP3 in which the n/SiN dielectric stacks are deposited together using an n mask and then the entire passivating i layer is etched to redeposit the blanket i+p layer on a pristine Si surface. The device structure at 3 critical stages for PMLP3 is shown in Figure 16. Completely etching i-layer on p-strip after n-SiN-I stack deposition through mask and then redepositing i+p blanket also reduces the unwanted leak below emitter. This reduces the number of plasma mask steps from 2 to 1 thereby reducing the masking steps as well as possibility of misalignment. Then the stack of n/SiN/i/p is laser ablated to form contact with n region. In this architecture, laser energy gets partially absorbed in a-Si n-layer thereby reducing the damage to passivation layer beneath and we can also increase n-layer thickness without penalty.

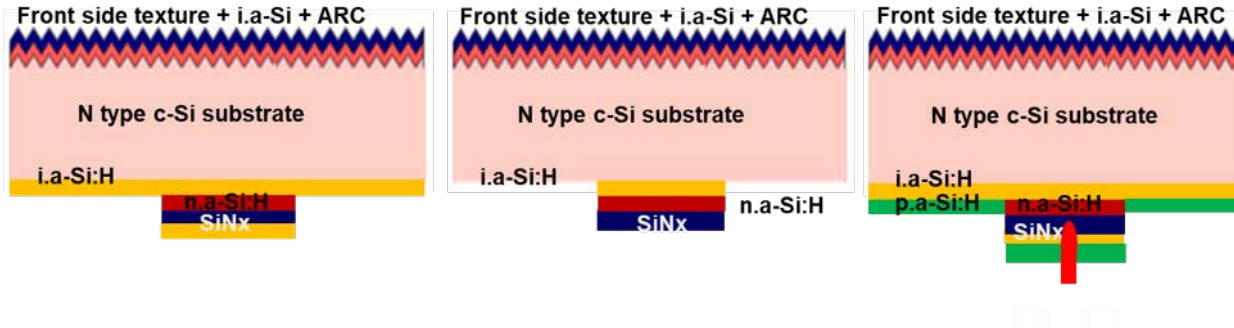


Figure 16. Device structure at various stages for IBC PMLP3 architecture

Adopting the new process steps in PMLP3 we were able to significantly increase the final iV_{oc} of the cells before metallization as compared to PMLP2. The comparison of the loss in iV_{oc} and the ΔiV_{oc} at every step of process in PMLP2 versus PMLP3 is shown in Figure 17. We observe that ΔiV_{oc} for PMLP2 is 52mV after the entire process whereas for PMLP3 it is only 20mV. Thus before metallization in PMLP2 the highest iV_{oc} was 680mV which has been pushed to 716mV in PMLP3 structure by reducing loss at every step. Having n doped layer to absorb laser also reduces laser damage from ΔiV_{oc} of 25mV to 7mV. Thus in PMLP3, we were able to get >700mV iV_{oc} before metallization for the first time in IBC configuration solar cells.

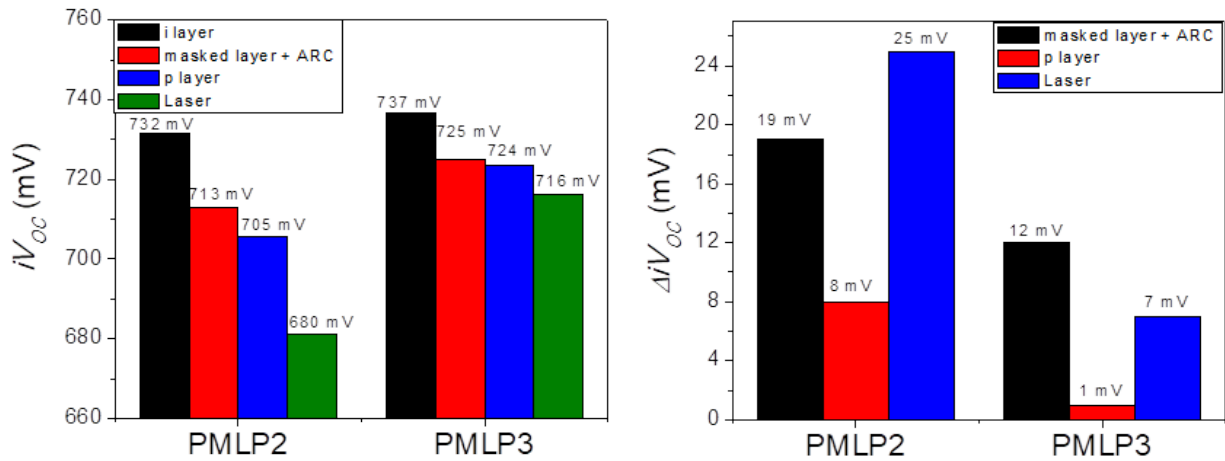


Figure 17. Comparison of loss in iV_{oc} and ΔiV_{oc} after every step for PMLP2 and PMLP3 architecture

The J-V curve of PMLP3 cells are shown in Figure 18. The cells showed S curve with low V_{oc} of ~ 500 mV and FF of 27% which improved after mild annealing. After annealing at 150°C the V_{oc} improved to 637 mV and FF to 53%. Further annealing had no significant effect on the cell performance and can be observed in the table in Figure 18. The poor performance of the cells was equated to the plasma leak which caused overlap of n and p region resulting in shunting of the cell.

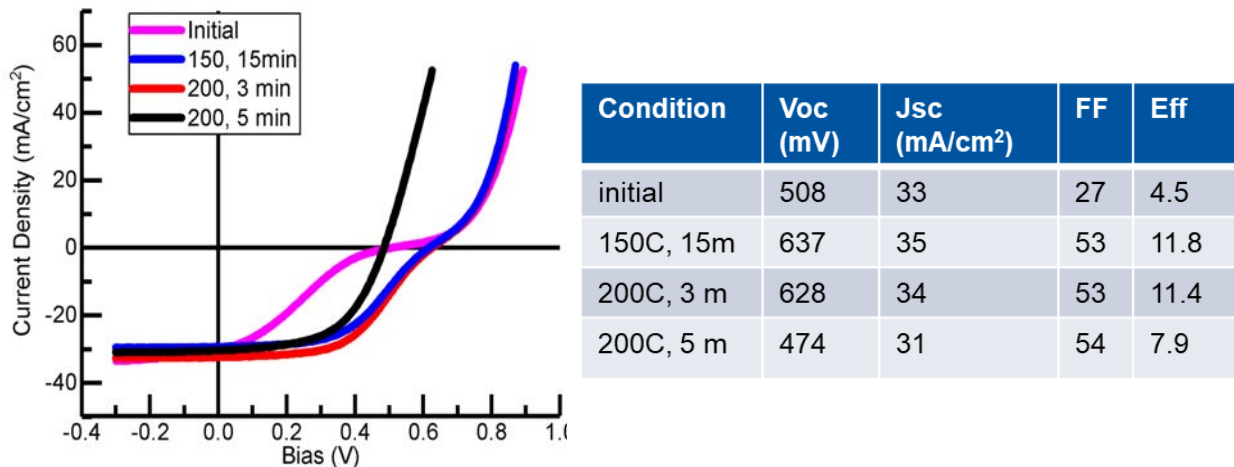


Figure 18. J-V curve of PMLP3 along with the cell parameters

Plasma leak, which was a major deterrent for making higher efficiency devices, was minimized using optimized etching methods. Firstly we removed i capping layer which simplified the etch process to 2 steps (HF for SiN leak then TMAH for n layer leak removal).

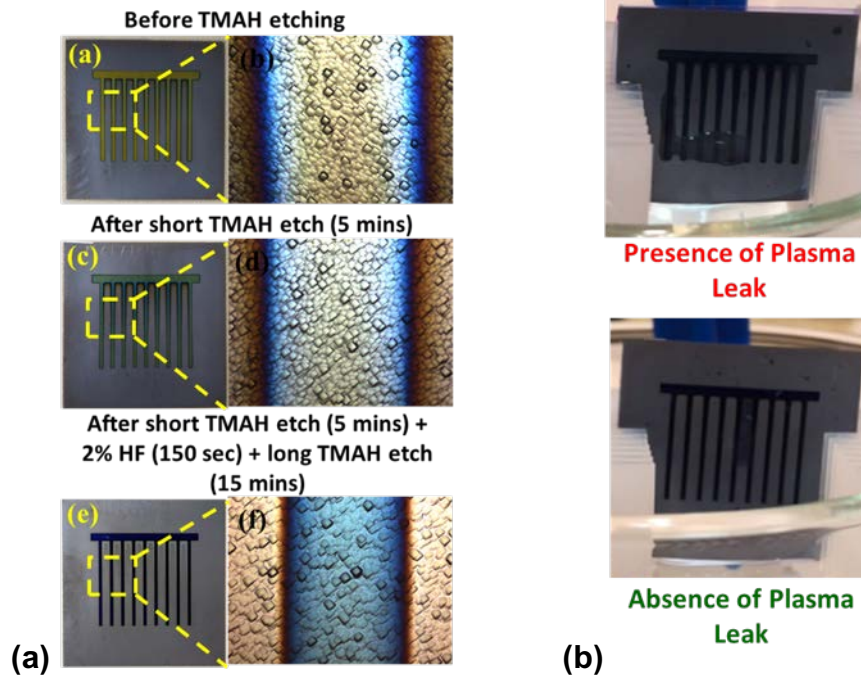


Figure 19: a. Optimized TMAH and HF etch to minimize plasma leak
b. Detection of plasma leak using DI water

As observed previously HNA etching is difficult to control due to its high etch rate and is not scalable option therefore we have used TMAH and HF for plasma leak removal. As shown in Figure 19a, we optimized TMAH + HF etch process to get sharp edges for the n region. We also found a new method to detect complete removal of plasma leak called Hydrophilic test where affinity of SiN to water around the edges of n strip was used as a metric to check if the plasma leak has been completely removed and this can be seen in Figure 19b.

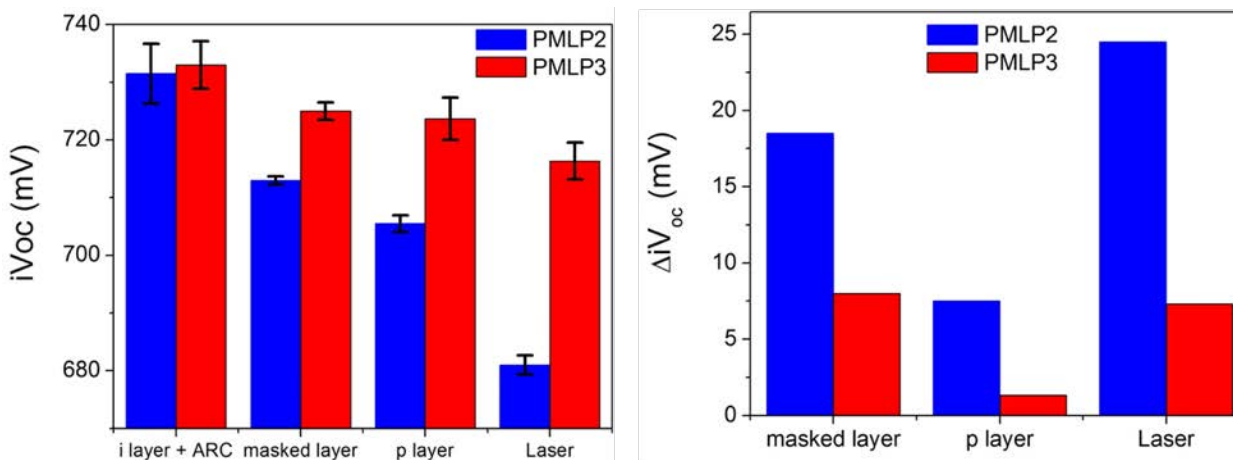


Figure 20. Comparison of PMLP3 vs PMLP2 after process optimizations (Error bar is used to show the standard deviation across a large batch of cells)

Optimizing the i layer and doped layer conditions we were able to see consistent improvement in PMLP3 cells versus PMLP2. We were consistently able to fabricate PMLP3 cell structures having higher iV_{oc} and less V_{oc} degradation after every process step versus PMLP2 as can be observed in Figure 20 and 21. Since there is no PECVD process after laser ablation there is no possibility of misalignment or overlap which was a problem in PMLP2. The n/SiN through mask in PMLP3 has less iV_{oc} degradation as compared to only SiN in PMLP2 (Step 2 – masked layer in Figure 20 and 21).

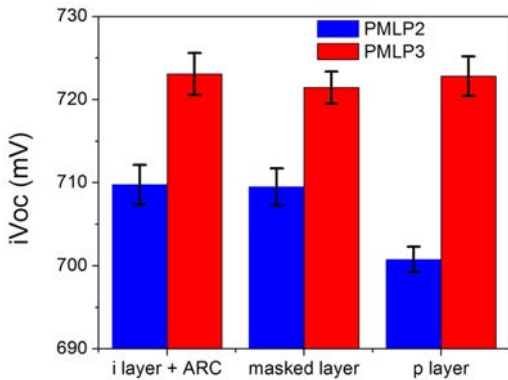
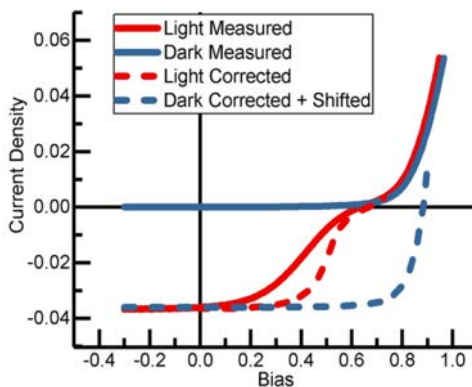


Figure 21. Second iteration of PMLP3 versus PMLP2 (Error bar is used to show the standard deviation across a large batch of cells ~8-12).

After p layer, iV_{oc} of PMLP3 is better than PMLP2; additionally etching and redepositing i layer before the p layer helps to form a pristine passivation interface. We observe less degradation in PMLP3 after laser process since n layer absorbs some laser power & prevents degradation of underlying i layer. Due to this n layer before laser ablation the laser damage has been significantly decreases from ~25mV to less than 7mV in PMLP3. For the first time, PMLP3 enabled us to achieve $iV_{oc} > 720\text{mV}$ on IBC cells after all processing steps as shown in Fig. 21; i.e. plasma masking, laser ablation, multiple etching steps, depositing i+p emitter, and shipping to UVA and back to IEC. We have also optimized the etching process to have minimized exposure time of the cells to chemicals thereby decreasing iV_{oc} degradation. Though the results in Figure 21 are different from Figure 20 (i.e. in different batch of cells) yet they have very similar iV_{oc} trends which demonstrate consistency and reproducibility in PMLP2 and PMLP3 structures.



	V_{oc}	FF	FF_c	R_s	n	$J_0(\text{mA/cm}^2)$
Light	633	36.5	53.5	5.2	2.8	1.2E-2
Dark	923	73.5	76.8	1.2	2.3	2.8E-6

Figure 22. Light and Dark J-V characteristics of PMLP3 cells

While the PMLP3 cells have very promising value of $iVoc = 710-720mV$ before metallization, their Voc drops to $<650mV$ and $FF < 60\%$ after metallization due to the S shaped curve in light J-V. However the dark J-V shows normal behavior with no blocking curve and low R_s as seen in Figure 22 where we also show the pseudo dark J-V curve by shifting the dark curve by J_{sc} and correcting for R_s . The Pseudo dark I-V shows good FF & Voc , low R_s and normal I-V which suggests good n-contact (i.e. the contact formed using laser ablation + etching is an good contact). The low FF is likely due to hole collection/injection barrier at p-strip. The 'Dark Voc' is 300 mV higher than light Voc, (table in Figure 22) which is consistent with blocking hole injection (no holes in dark for recombination). Normal FJ cells have 'dark Voc' which is only 20-30 mV higher than the light Voc. The Laser beam induced current (LBIC) scanning in Figure 23 shows uniform current collection across device with some small damage due to laser ablation. The Forward bias LBIC shows uniform reduction in photo-current and the LBIC voltage sweep is consistent with JV. Thus the low Voc and FF is attributed to p-contact (plasma leak over emitter) and not n-contact (laser ablated contact). The randomness of low Voc (550-630 mV) suggests sample-to-sample variability like etching damage or plasma leakage thickness over the emitter.

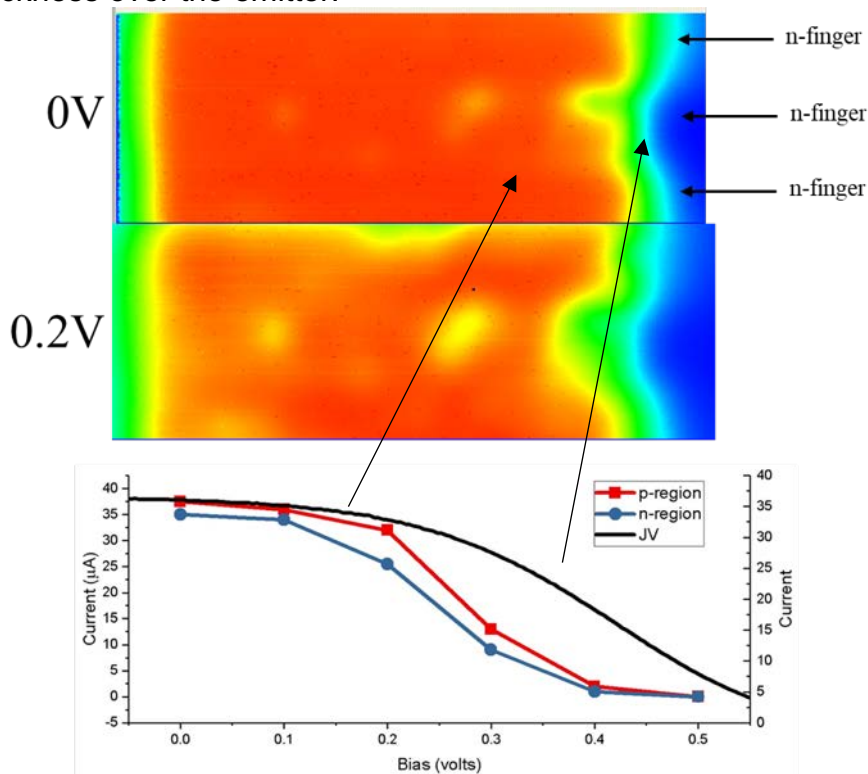


Figure 23. Laser beam induced current (LBIC) scanning of PMLP3 cells

In order to further push the Voc of the cell we fabricated PMLP3 cells with varying thickness of i layer, using different etchants like KOH/TMAH and varying annealing temperature. The results of $iVoc$ degradation at every step of the process is shown in Figure 24. In step 2 and 3 (S2/S3) i.e. ARC and deposition of n/SiN through mask the increase in $iVoc$ is due to annealing of i layer. The decrease in $iVoc$ due to etching of rear i layer in step 4 (S4) is due to complete lack of passivation layer on p-strips of the cell. The increase in $iVoc$ in step 5 (S5) is due to repassivation of rear surface.

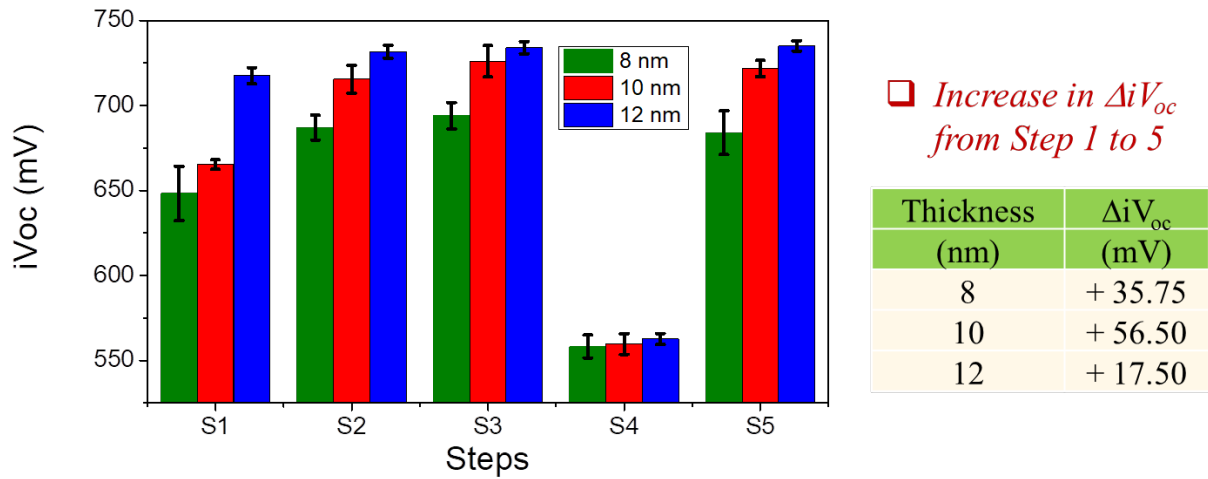


Figure 24. Varying thickness of *i* layer in PMLP3 series

Thus with these optimizations we were able to achieve an average iV_{oc} ~730 mV after all of the PECVD and laser process steps prior to metalization. Inspite of the high iV_{oc} before metallization, the V_{oc} of the final devices dropped drastically to ~450mV as shown in Figure 25. The uniform Photoluminescence (PL) of the cell shows no localized low emission which equates to superior passivation whereas electroluminescence (EL) shows non-uniform carrier collection. Increasing the bias current (200 mA to 1A) cannot overcome the barrier to injection in EL. Together with the light and dark JV analysis from Figure 22, the EL & PL results confirm that plasma leak through the mask doesn't affect cell passivation but affects its electrical characteristics shown by non-uniform hole collection and injection. Therefore exceedingly low V_{oc} is not due to poor passivation instead devices have carrier collection/injection problem.

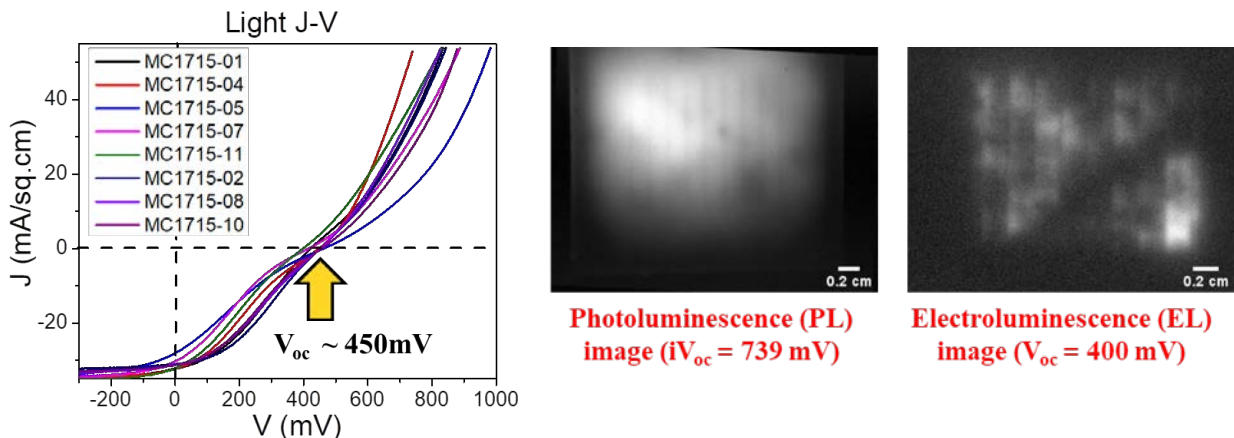


Figure 25. J-V curve of PMLP3 (left) with Photoluminescence (PL) and Electroluminescence (EL) image of the cell from this batch

Understanding the current collection problem in 2-dimensional (2D) contacts like IBC (PMLP3) structure is difficult. Therefore it was studied in 1D structure Heterojunction cells with Back Junction (BJ). BJ cells have p/n junction at the rear side and are illuminated from the front as shown in Figure 26. Test structures having intentional n/SiN through n

mask like PMLP3 cells at the rear side as shown in Figure 26 were fabricated to determine source of Voc loss. We compared standard BJ cell with test structures having n/SiN with and without (w/o) Plasma Leak Etch (PLE).

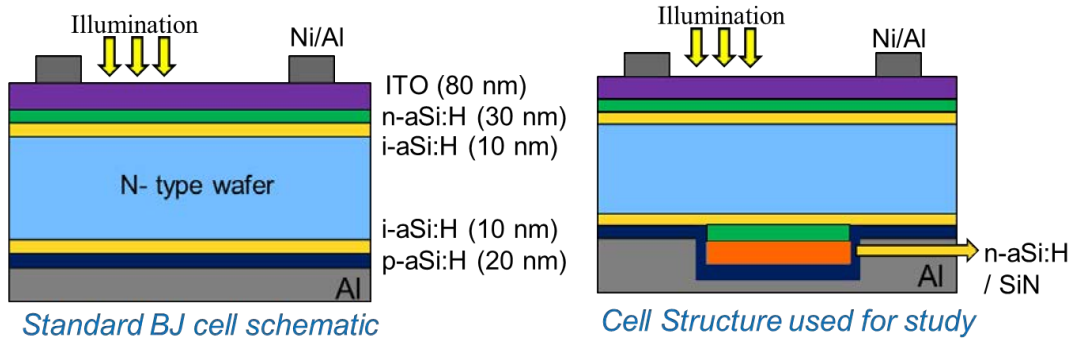


Figure 26. Back Junction (BJ) cell structure used to study of Voc loss in IBC cells

We also investigated SiN leak on cell performance (not shown) however n leak is more detrimental hence only those results are presented. The J-V results in Figure 27 shows that reference BJ cell have good Voc ~670mV as expected. BJ cell without (w/o) PLE of n leak shows ~400 mV drop in Voc compared to Reference cell indicating even few nm of n layer leak is very detrimental. BJ cell with PLE of n leak shows ~100 mV drop compared to the reference cell. This could be attributed to the non-uniform etch or contamination introduced during etch process.

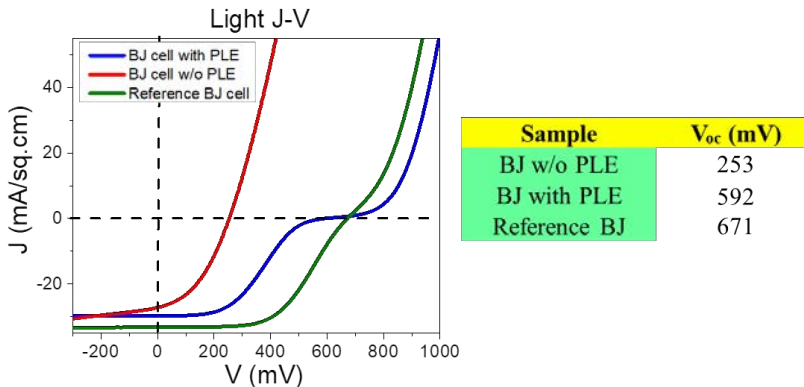


Figure 27. J-V curve of BJ cells with and without plasma leak etch (PLE)

In Figure 28, EL of BJ cell w/o PLE of n leak shows very low intensity even at high bias (1A). The n plasma leak region is dark accounting for region of low carrier injection. The PL of BJ cell w/o PLE of n leak in Figure 28 also shows the n pattern. The i/n passivation is superior to i/p passivation therefore n strip is bright. The n strip in the PL resembles the plasma leak distribution. Thus from the J-V of the BJ cells backed up with the EL & PL it is evident that the n leak is detrimental for the PMLP3 cells accounting for its low Voc. This experiment was critical to prove that plasma leak and its etching process is the limiting factor for cell performance.

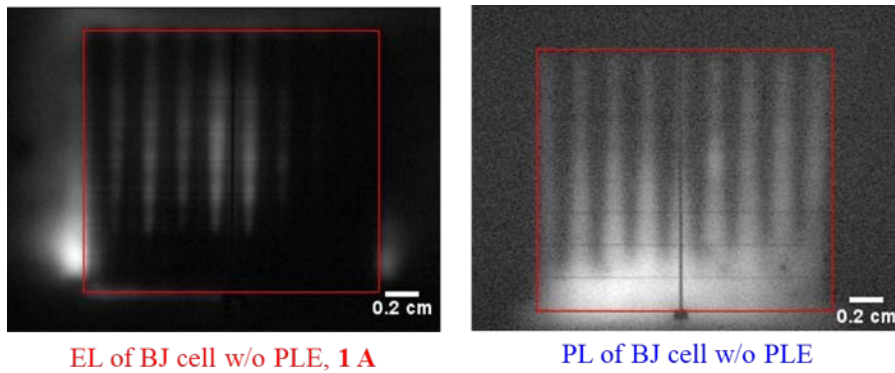


Figure 28. EL and PL of BJ cells without PLE

In order to mitigate the root cause of plasma leak which comes from the gap between the silicon mask and the cell in PECVD we fabricated in-house Stainless Steel (SS) masks with magnetic holder designed & fabricated using laser at IEC to reduce plasma leak. Figure 19 shows n/SiN deposited using Si mask and SS mask with magnetic holder developed at IEC. We can visibly see well defined pattern and considerable decrease in the plasma leak.

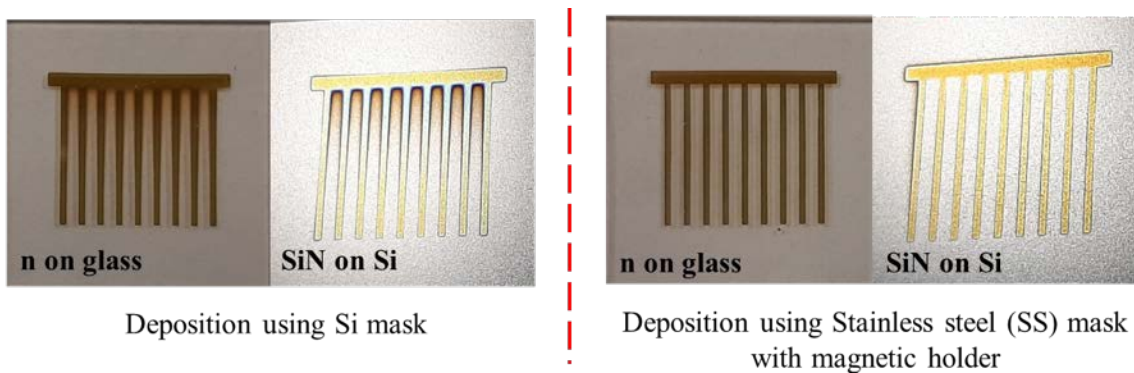


Figure 29. n and SiN deposited using Si mask and SS mask with magnetic holder

We then fabricated PMLP3 cells with magnetic SS mask developed in-house to overcome plasma leak problem. We also tried using HNA as an alternative to KPH/TMAH to ensure complete removal of plasma leak and fabricated cells with and without HNA etch to study the effect of n leak. Figure 30 shows that irrespective of the plasma leak etch an average $iVoc > 710$ mV was achieved for all cells using the SS mask with magnetic holder after all the PECVD Process. The laser optimization further decreased the $iVoc$ loss due to laser damage. $\Delta iVoc$ is lesser for UV laser (~ 1 mV) as compared to Green laser (~ 5 mV).

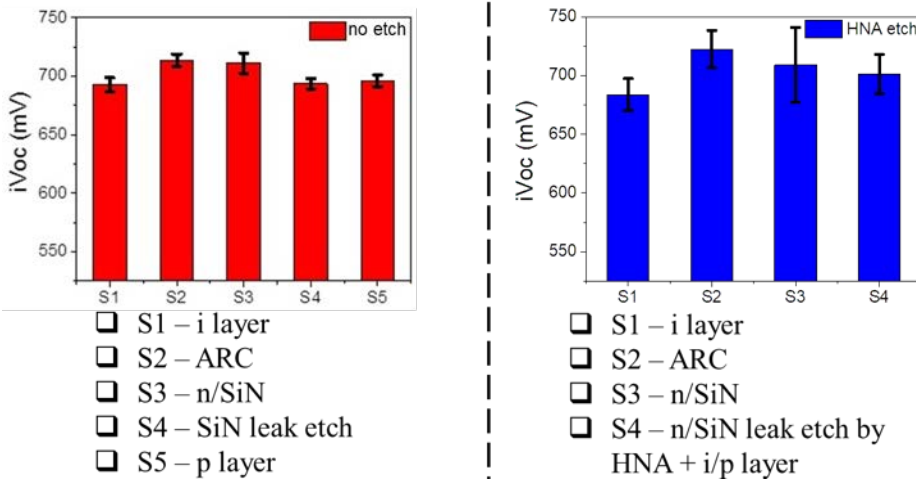


Figure 30. Comparison of iVoc degradation of PMLP3 cells with and without plasma leak etch using HNA

The dark and light J-V characteristics of the PMLP3 cells are shown in Figure 31. The dark curve of cells with no etch show lower threshold voltage whereas HNA etched cells have higher turn on voltage. Thus n leak considerably reduces the voltage of the device. Whereas in the light curve, both with and without HNA etch show similar poor behavior with $V_{oc} \sim 450\text{mV}$ suggesting common problem.

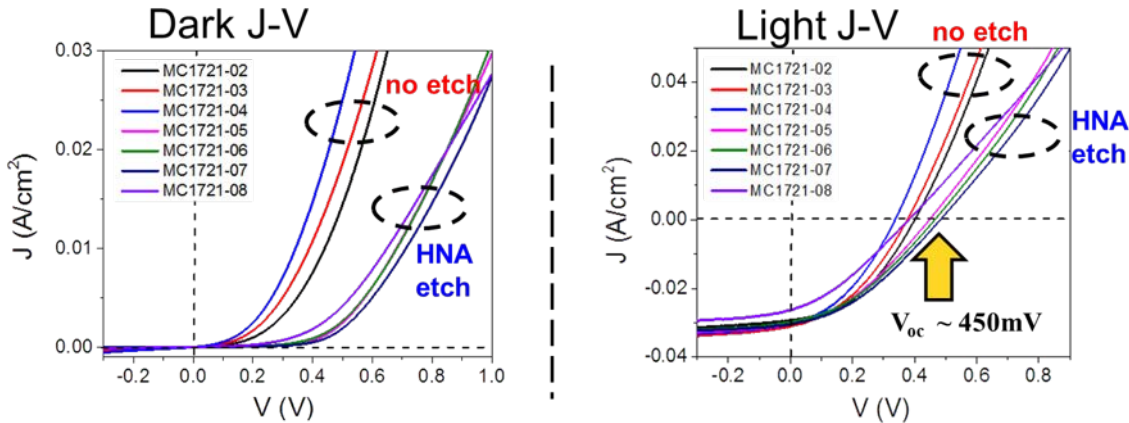


Figure 31. Dark and light J-V of PMLP3 cells with and with plasma leak etch fabricated using SS mask with magnetic holder

The comparison of iVoc of the cells before metallization and V_{oc} after metallization in Figure 32 shows that irrespective of the etch there is a considerable drop in the V_{oc} ($\sim 300\text{mV}$). Theoretically it is not possible to get such low V_{oc} by high recombination alone and $V_{oc} < 550\text{mV}$ (iVoc of Bare Si) can only be caused by an opposing diode.

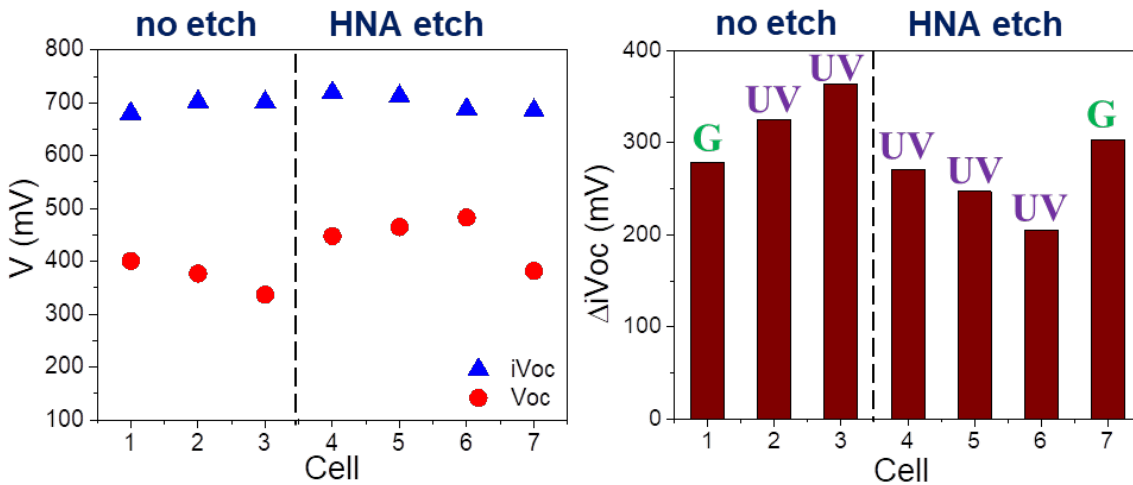


Figure 32. Comparison of $iVoc$ vs Voc of cells with and with plasma leak etch (left) $\Delta iVoc$ of same cells (right)

Therefore the possible causes of low Voc / poor electrical performance of the devices can only be accounted for by one of the following cases:

1. *Opposing Schottky barrier (n/Al Interface)*: This could be due to no n layer to form contact with Al, nano or poly crystallization of n/i layer, SiN residue after etching or n effusion making layers etch resistant
2. *Residual n contamination of emitter junction (p/n Interface)*: This could be due to n plasma leak, unable to etch leak completely causing poor emitter p/i/N(wafer) junction etc.

In order to find the possible cause of this problem we designed experiments to investigate these 2 possible barriers to higher efficiency and find pathways to proceed to the next structures from the results of these experiments.

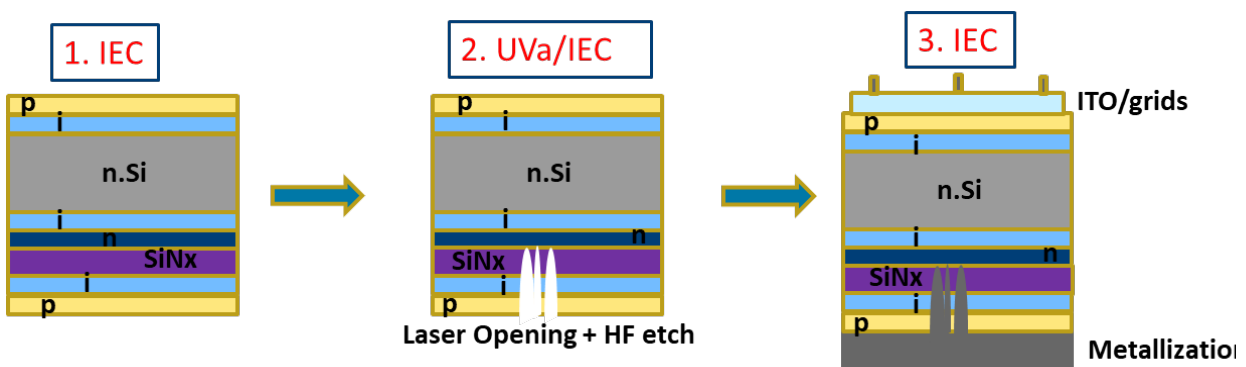


Figure 33. Test structures using FJ cells having rear side similar to the PMLP3 architecture cells used to diagnose schottky barrier problem

Front Junction (FJ) cell were used to identify the first possible cause of low Voc which is an opposing Schottky barrier. The rear side of the FJ cells was modified to mimic the rear structure of PMLP3. This structure will help to eliminate the effect of rear emitter since the emitter is in front in this case.

To investigate the Schottky barrier problem we compare FJ cells with PMLP3 rear architecture with laser ablated contacts versus Standard FJ cell. If $\Delta iV_{oc} > 100$ mV then it's likely the problem is an opposing Schottky contact. If $\Delta iV_{oc} < 100$ mV then the problem is not in n-contact, it would suggest that we need a cleaner p/i HJ by reducing the n-leakage. The results of these FJ cells for different laser power and i layer conditions are given in Figure 34 showing all cells with similar rear structure as PMLP3 had $V_{oc} > 650$ mV after metallization regardless of UV or Green laser ablation or power (best was 680 mV). Since ΔiV_{oc} is less than 100mV and V_{oc} of all the cells are greater than 550mV we can infer that the opposing diode isn't the schottky contact. The light and dark J-V of the FJ cells are shown in Figure 25. The light and the dark J-V curves of the FJ cells have same behavior confirming that there is no blocking diode due to the laser ablated contacts (in contrast to PMLP3 IBC cells). This experiment confirms IBC emitter structure is the main problem and the source of opposing diode.

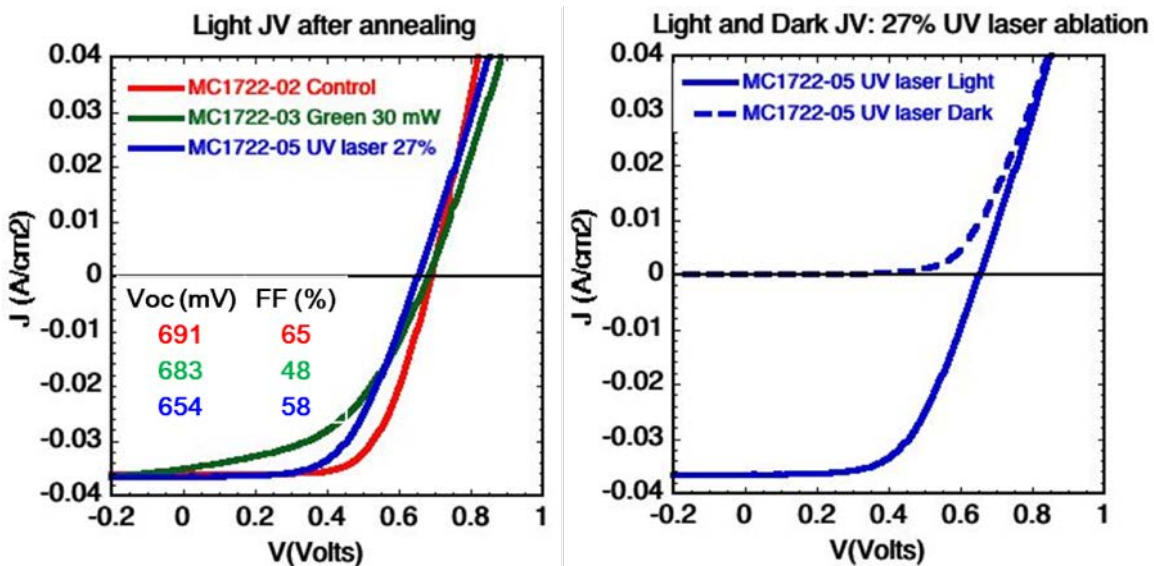


Figure 35. a) Light J-V of FJ cells having modified IBC rear architecture similar to PMLP3 cells ablated with different lasers; b) Light and dark curve of best cell

3.2.e Reverse PMLP-3/ PMLP-4 Architecture

Since the problem lies in the emitter contact the best approach is to flip the order of deposition i.e. i/p will be deposited first followed by laser opening of n-strip. Reversing the order (depositing i/p initially instead of i/n) helps in forming pristine emitter at the beginning prior to any n-leakage to address the problem of contamination of emitter junction. Thus N(wafer)/i/p interface is not subjected to contaminants introduced during etching or n plasma leak thereby helping to overcome blocking behavior in the cell. This new architecture is called Reverse PMLP3 or PMLP4.

In PMLP3 we deposit the n at a temperature of 250°C followed by p at a temperature of 200°C however in reverse PMLP3 or PMLP4 we deposit p initially at 200°C. This introduces new requirements for PECVD layer processing due to differences in deposition temperature i.e. we had to first develop a low temperature n layer compatible with p. After

developing an optimized n layer at lower temperature we develop SiN at lower temperature to be used as an etch barrier for protecting the i/p layer beneath. This SiN layer is called Etch Sacrificial Layer (ESL). In order to open contacts for depositing n layer we follow 2 approaches – one is direct laser ablation where the dielectric layer is ablated to open the n strip, second the layer, usually a photoresist is used to selectively open the n strip using the laser exposure. This layer is called Laser Sacrificial Layer (LSL). The 2 approaches for making PMLP4 cells as described above is shown in Figure 36.

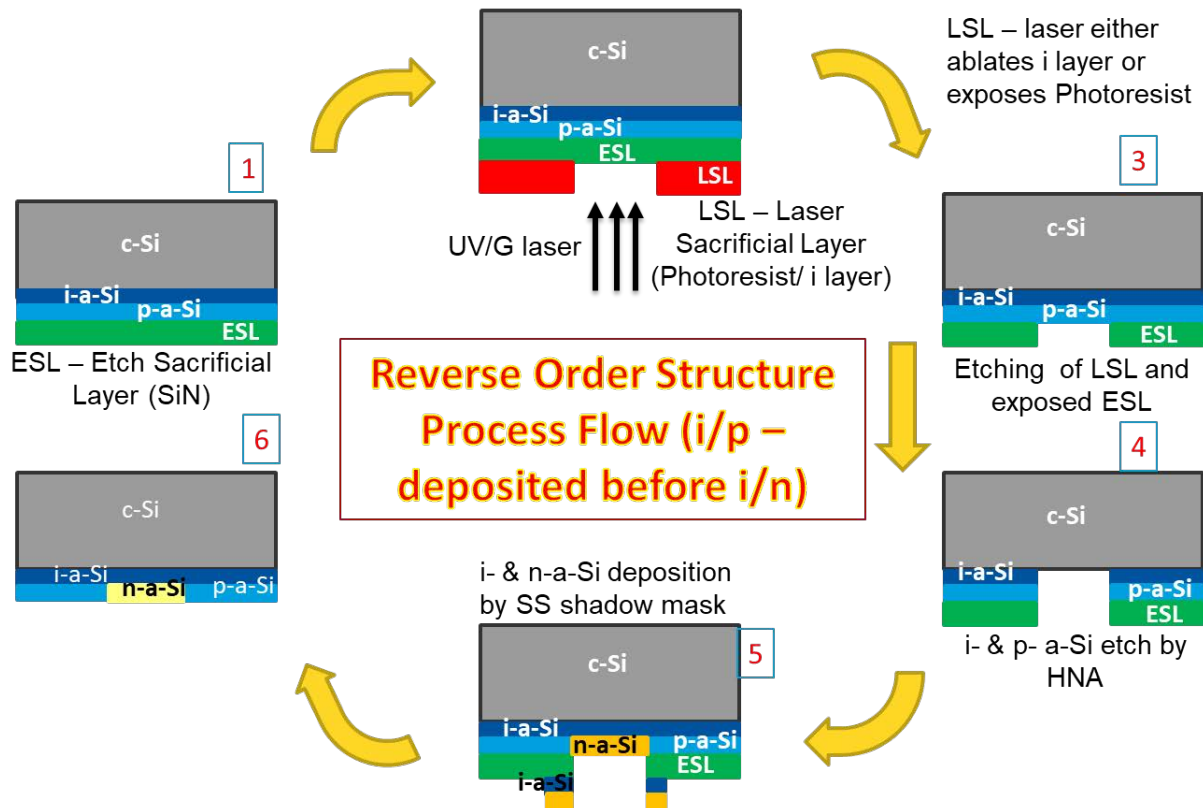


Figure 36. Process flow of reverse PMLP3 or PMLP4 architecture

Though depositing p-i layer first gives a pristine p-i emitter it has multiple challenges. Firstly, there is no masked deposition before Laser ablation making it difficult to align the laser and ablate the n fingers. Since the n layer is deposited after p layer it has a potential n-layer plasma leak on top of p which still needs to be etched. Despite these complexities, PMLP4 has lower thermal budget since the cell has all layers at deposited at 200°C to make it compatible with p layer.

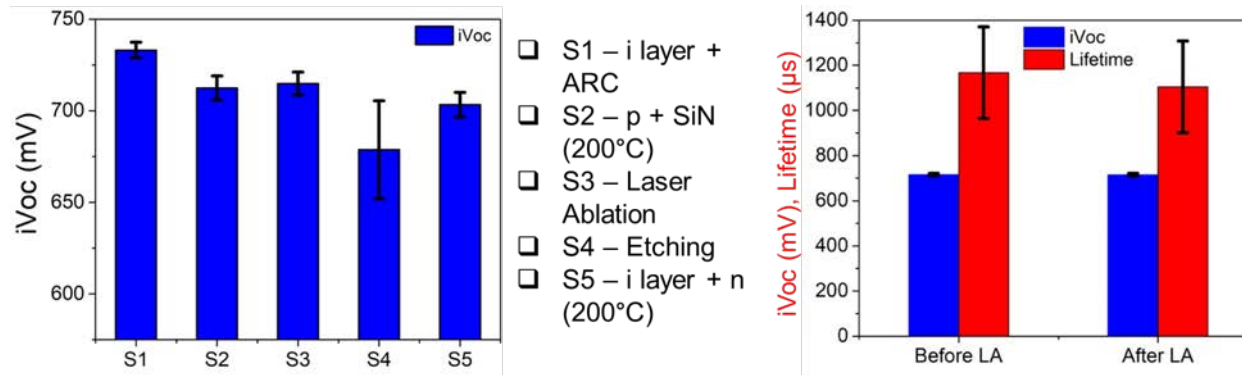


Figure 37. $iVoc$ degradation after every step for PMLP4 (left) lifetime and $iVoc$ degradation before and after laser ablation [LA] (right)

The degradation of $iVoc$ at every step of processing for reverse PMLP3 architecture is shown in Figure 37. The reverse PMLP3 or PMLP4 cells demonstrated $iVoc > 730mV$ with i layer passivation and showed a highest $iVoc$ of 740 mV with Hydrogen Plasma Treatment (HPT). We had to develop a low temperature (200°C) SiN and n layer for reverse architecture and obtained $iVoc=710-723$ mV from batch of reverse PMLP3 IBC after all deposition, etching, laser patterning and plasma mask steps. We increased yield and improved repeatability by using the same shadow mask to guide laser patterning as used in metallization thereby minimizing misalignment problem despite of the absence of patterned n fingers.

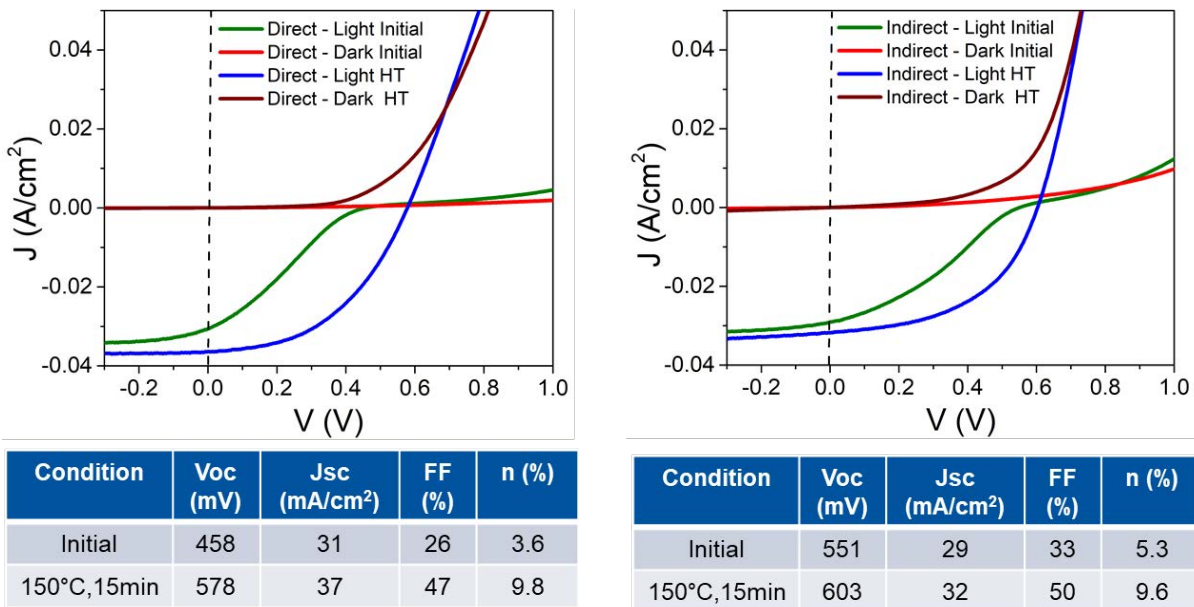


Figure 38. a – Light and Dark curve of Direct LA PMLP4 cells Figure 38. b – Light and Dark curve of Indirect Laser Exposed PMLP4 cells

The JV curve of direct laser ablated (LA) and indirect laser exposed (LE) PMLP4 cells are shown in Figure 38 a and b. The cleaner p-i emitter in PMLP4 (for both direct LA and indirect LE) improves Voc to ~600mV from 450 mV obtained in PMLP3 cells. JV shows drastic improvement after Heat Treatment (HT) which means HT helps to overcome

strong blocking barrier making the contact ohmic. The reason for dramatic impact of mild HT is unclear however it is evident that HT ‘turns on’ the diode conduction in the dark and overcomes S curve in the light. The cells are not shunted and Fill Factor is not limited by series resistance ($R_s < 1 \Omega\text{-cm}^2$). The J_{sc} value of 37mA/cm^2 for direct LA PMLP4 cell is highest obtained in our IBC cells in this project and improved V_{oc} by $>130\text{mV}$ as compared to PMLP3 cells.

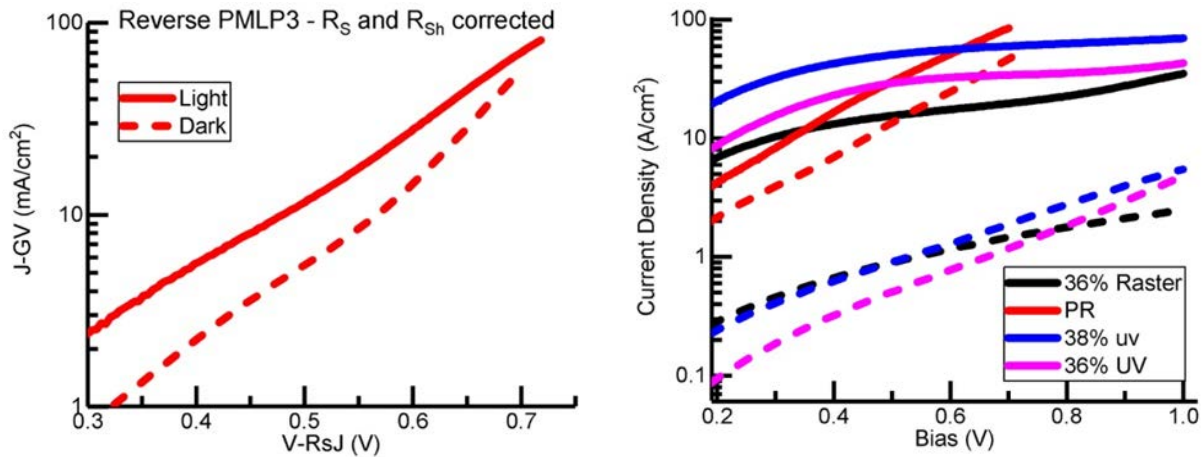


Figure 39 – series and shunt resistance corrected J-V curve of PMLP4 cells (left) Dark JV curve of PMLP4 cells in log scale (right). Note: PR means photoresist which is same as ‘LE’ laser exposed terminology above.

Table 6 – Series and shunt resistance corrected JV characteristics of PMLP4 cells

	V_{oc} (mV)	J_{sc} (mA/cm ²)	FF (%)	Eff (%)	R_s ($\Omega\text{-cm}^2$)	R_{sh} (mS/cm ²)	n	J_0 ($\mu\text{A/cm}^2$)	FF'' (%)
Light	603	31.7	50.0	9.6	0.43	4.7	4.6	92	54.8
Dark					0.87	2.7	3.1	3	63.0

The series and shunt corrected JV for PMLP4 cells are shown in Figure 39 and the values of the parameters are given in Table 2. From the analysis we can conclude that Fill factor of the cells are not limited by R_s and the R_s values are similar to FHJ solar cells ($R_s < 1\Omega\text{-cm}^2$). The V_{oc} of the cell corrected for shunt is 613mV and there is slight increase in resistance at high injection which could suggest a slight barrier at higher injection. The Dark JV curves in Figure 29 have nearly exponential (nonlinear) behavior in log scale and does not show blocking behavior (except direct LA raster scanned with 36% UV laser). From table 2 we can infer that high ideality factor ($n \sim 3$ to 4) and high J_0 (of the order of μA) limits FF & V_{oc} .

We thus observe that pristine p-i emitter in reverse PMLP3/ PMLP4 has helped improve blocking behavior (from 450 mV to 600mV) however it doesn't completely eliminate the problem. A critical experiment to validate that the problem was not occurring during the

e-beam metalization or between the Al/doped layers was to etch the Al away and remeasure iV_{oc} . We found the cells still have $iV_{oc} > 700\text{mV}$ after etching off metal implying passivation is retained during metalization. Therefore reducing the blocking contact either from plasma leak or architecture of the cell are the possible methods to realize cells with $V_{oc} > 700\text{mV}$.

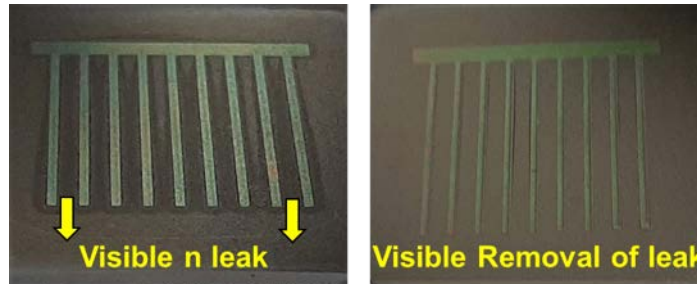


Figure 40. n leak in PMLP4 cells inspite of using SS mask with magnetic holder

The major concern in PMLP4 cells still remains the plasma leak introduced during the PECVD process. Though using SS mask considerably reduced the leak as compared to Si mask, some plasma leakage remained unavoidable even after using SS magnetic mask. The n leak introduced due to the slightest gap between the mask and sample still remains a major source of blocking contact. In Figure 40 we can see after i/n deposition the gaps between the magnetic masks still results in plasma leak visible at an inclined angle (left image). After prolonged etching in HF, the remniscent SiN below the leak helps to lift off some of the leak due to the undercut created (right image). However complete removal of the leak was not achieved due to the spatial non-homogeneous nature of wet chemical etching. We tried to remove the n leak using multiple etch processes and visual feedback however trace amount of n residue on p finger can still cause blocking emitter Al-n-p-i-(n-Si wafer) contact leading to loss in V_{oc} of the cell.

3.3 Laser Processing Development: Patterning of Dielectric and Ni layers

3.3.a Introduction:

Laser processing has been one of the most crucial steps required for the fabrication of a functional IBC-HJ solar cell portion of this project due to its several unique advantages: flexibility in pattern designing, high spatial resolution, controlled depth of ablation and elimination of complex masking lithography steps. In IBC-HJ solar cell architectures, a-Si:H (i) layers serve as the main passivation layer, which helps to inhibit interfacial defects and consequently enhances minority carrier lifetime (MCL) and implied open-circuit voltage (iV_{oc}). Generally, laser processing can induce such unwanted defects and heat-induced poly-crystallization, which results in low MCL, fill factor, and iV_{oc} .

Previously, published research papers have shown that using ultra-fast picosecond (ps) and femtosecond (fs) laser processing has induced damages, lower open-circuit voltage (V_{oc}) and fill factor¹⁷. There has been a minimal investigation of ns laser interaction with the passivation layers and other constituent layers used in different kinds of solar cell architectures¹⁸. Hence fundamental understanding and optimization of laser processing parameters are required to ensure efficient ablation of the top sacrificial a-Si:H (p and i) layers to expose dielectric SiN_x layers without affecting the underlying passivation layer. Such optimizations were carried out using ns pulsed lasers with wavelengths of 355 nm and 532 nm to create an extensive understanding of the effects of laser wavelength and ns pulse-width on the passivation and other constituent layers of IBC-HJ structures. Also, the fabrication of IBC solar cells was carried out using a-Si:H sacrificial layer, shown in figure 41, and sacrificial photoresist layer exposure by laser light and development of the photoresist, followed by selective chemical etching to eliminate any laser-induced damages.

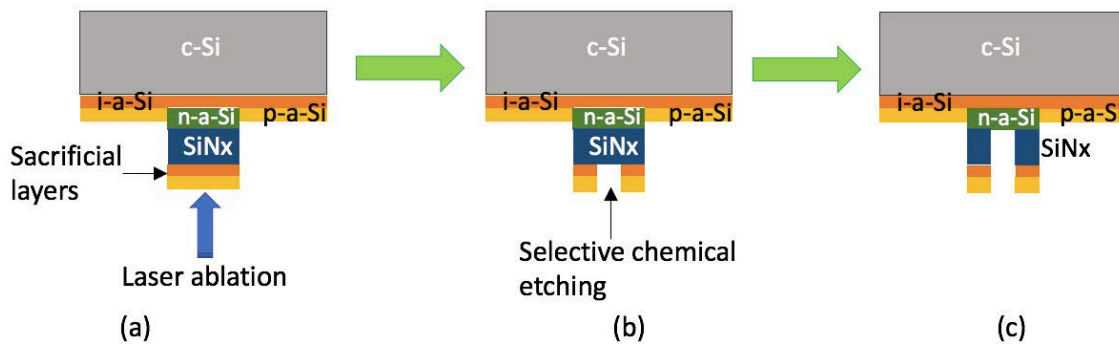


Fig. 41. (a) to (c) Schematics of direct laser ablation on PMLP3 devices followed by selective chemical etching

A rigorous set of characterization techniques like optical microscopy, μ -photoluminescence (μ -PL), Sinton QSSPCD minority carrier lifetime measurement, scanning electron microscopy (SEM), energy-dispersive X-ray spectroscopy (EDS), ellipsometry, Raman spectroscopy and high resolution (HR) X-ray photoelectron spectroscopy (XPS) along with simulations involving predictive color charts were carried out for a fundamental understanding of the laser process development.

3.3.b Patterning by direct laser ablation of sacrificial a-Si:H-based layers

Ablation by 532 nm wavelength laser

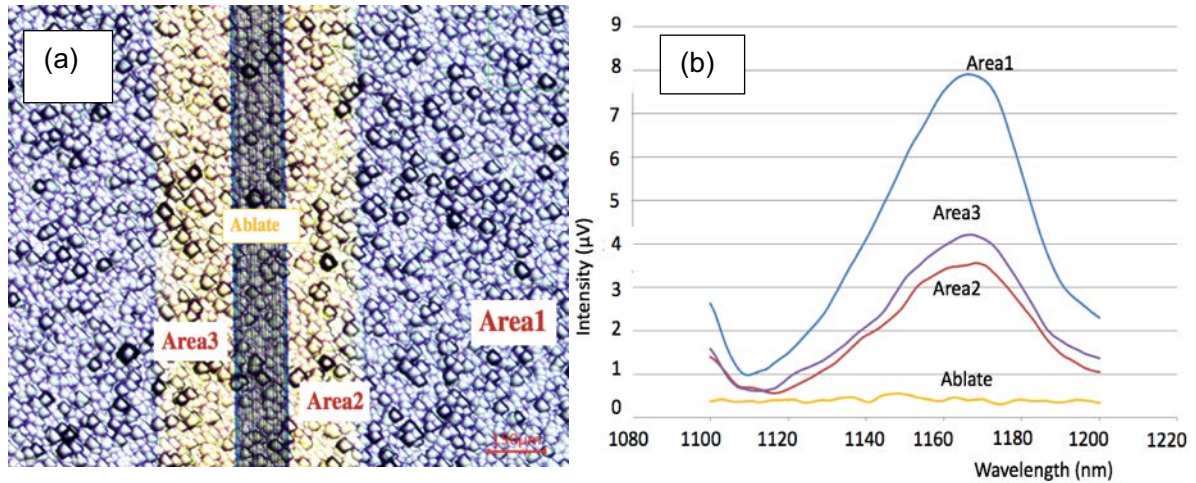


Fig. 42 (a) Optical image of green laser processing of MC 1715-08 sample and (b) the μ -PL data showing the loss of passivation at the ablation region.

The laser used was IPG Photonics YLP-G-10 ytterbium fiber laser with 532 nm wavelength. The laser had the maximum average power of 10 W, 1.3 ns pulse width, $\sim 4.48 \mu\text{J}$ pulse energy, and Gaussian beam profile of $\sim 20 \mu\text{m}$ focused spot size at the FWHM. For laser patterning IBC solar cell devices, the green laser parameters were 30 kHz repetition rate, $\sim 80\%$ overlap, and laser power at 0.61 J/cm^2 fluence at focus and a total ablation line width of $\sim 150 \mu\text{m}$. On measuring the lifetime, it was found that there was a significant drop in iV_{oc} ($< \sim 20 \text{ mV}$) and MCL ($\sim 900 \mu\text{s}$), which are tabulated in Table 7. The μ -PL characterization, as shown in fig. 42 (a) and (b), revealed that the passivation was impacted at the ablated region.

Such performance degradations were investigated by various analytical techniques, and

Table 7. MCL and iV_{oc} before and after direct green laser ablations on MC 1715 and MC 1721 series

Sample	MCL (μs) before laser	iV_{oc} (mV) before laser	MCL (μs) after laser	iV_{oc} (mV) after laser
MC 1715-08	1272	711	700	692
MC 1721-10	1607	715	727	695

the laser parameters underwent optimizations for PMLP3 devices fabrication. The parameters were found to be 30 kHz repetition rate, $\sim 0\%$ overlap, laser fluences from 0.427 J/cm^2 to 1.27 J/cm^2 , the focused spot size of $20 \mu\text{m}$ at the FWHM, and $\sim 150 \mu\text{m}$ width laser ablation lines. Next, details on the effect of laser processing on optical properties, morphology, elemental composition, and structural changes are described.

The passivation quality can be characterized by photoconductance carrier lifetime measurement and μ -PL technique. The μ -PL is a reliable tool to measure the degree of passivation at a spatial resolution in microns. In the case of both-side-textured passivated Si substrates, the radiative recombination emits PL at around 1150 to 1170 nm wavelength. The μ -PL data for different laser conditions are shown in fig. 43. There is a drop in the PL signal as laser fluence increases from the unablated to 1.27 J/cm² laser condition.

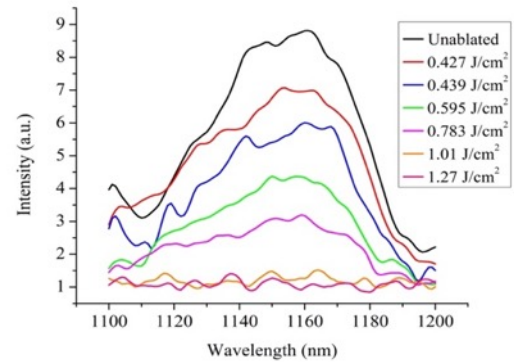


Fig. 43. μ -PL data for different laser

In fig. 44 (a) to (f), the optical images show the laser ablation spots for all the laser energy densities. Prior to the taking of optical images, standard white balancing and color default were performed. The thickness change in the SiN_x layer observed in an interference pattern seems to become prominent as the laser power is increased.

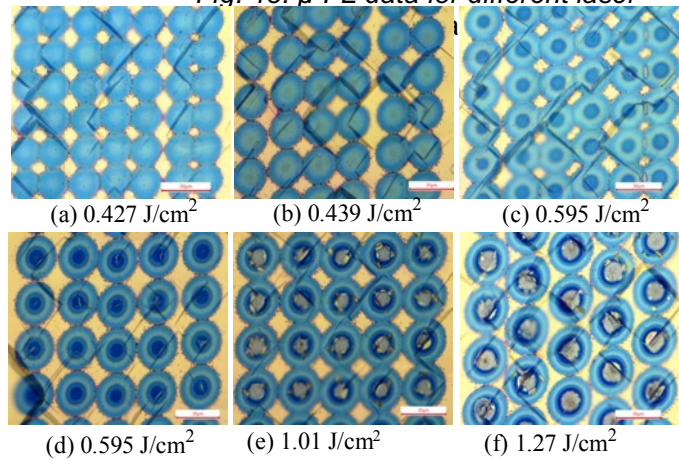


Fig. 44 (a) to (f). Optical images of different laser processed regions at different fluences

The color identification chart, which can serve as a reliable stand-alone tool for

determining changes in layer-thickness and optical constants under

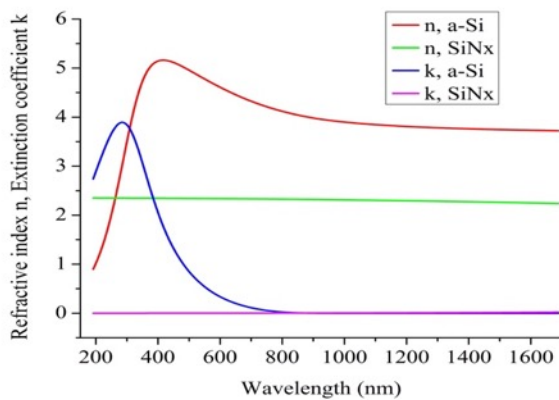


Fig. 45. Optical constants n , k vs wavelength (nm) curve for different layers in IBC-HJ

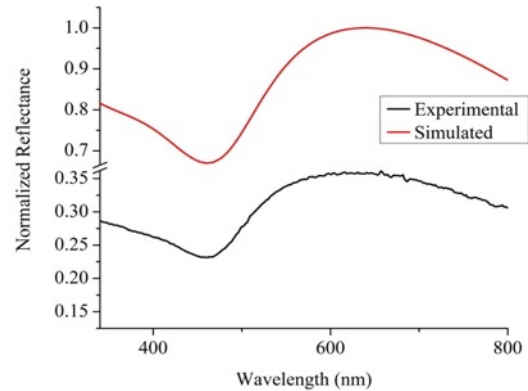


Fig. 46. Normalized Reflectance vs Wavelength (nm) curve of IBC-HJ device.

laser processing, was developed for IBC-HJ cell investigations. The optical constants, refractive index n and extinction coefficient k , were measured using an optical ellipsometer with 5 nm roughness consideration at 70° incidence angle. The results are shown in fig. 45. The measured n and k values were fed into Essential Macleod software

for simulations of normalized reflectance and color chart. From the simulation, the total thickness of top blanket a-Si:H layers was calculated to be ~26 nm, which is close to the aim thickness of 30 nm as-deposited by PECVD. The optical reflectance was measured by an optical spectrophotometer. Although both the normalized experimental and

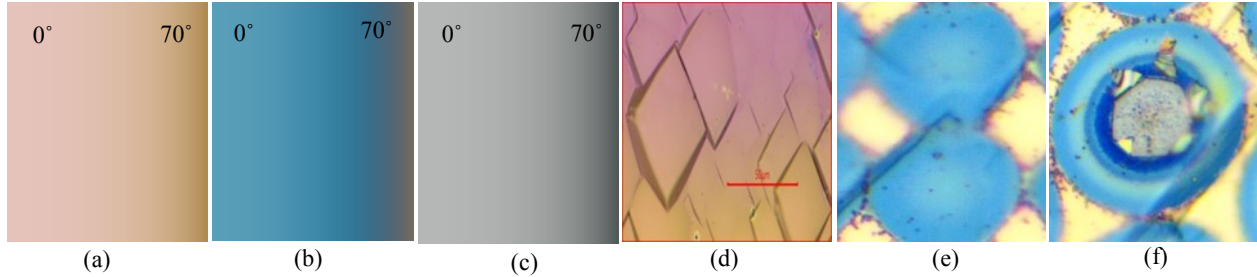


Fig. 47 (a) to (c) Simulated colors and (d) to (f) respective optical images of IBC-HJ device

simulation curves closely match each other, as shown in fig. 6, the difference in the magnitude of normalized reflectance is due to the semi-polished textured surface, while the simulations were made on the assumption of a smooth surface.

The simulation also provided a color chart for a range of incidence angle from 0° to 70° for each layer. In fig. 47 (a) to (c), we show the simulation colors due to different layers in the IBC-HJ device after each of their successive removal and fig. 47 (d) to (f) show the actual optical images. The different predicted colors could be compared with the actual optical colors, thus allowing to determine the changes in the laser processed layer thicknesses. Hence, the color identification chart can be a reliable tool for determining the thickness of a particular layer.

In fig 48, the SEM images show the formation of rings on the SiN_x layer as a function of laser fluence. At energy density greater than 50%, the top SiN_x layers rupture and peel off at the laser spot center. Since SiN_x is transparent to 532 nm laser, the laser fluence

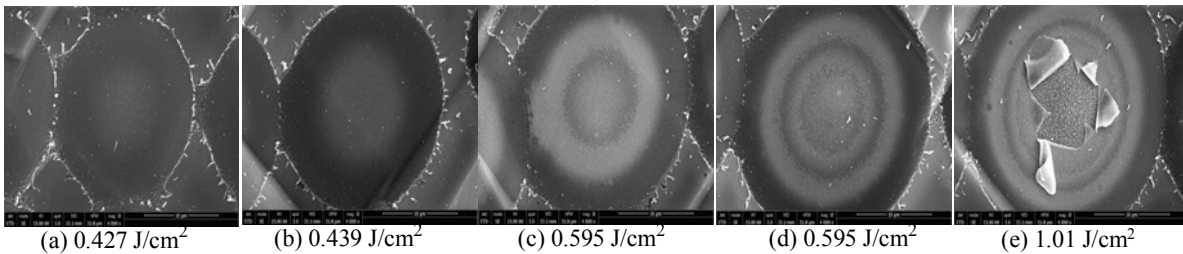


Fig. 48 (a) to (f) SEM images of ablated spots at different laser fluence

coincides with the melting threshold of Si¹⁹. At the center of the laser beam, the underneath a-Si:H (n and i) layers are in the molten liquid state for long enough time for H₂ gas pressure to build up and escape along with possible a-Si vapor²⁰. Due to the laser heat, the surrounding a-Si layer melts all around the laser spot.

Fig. 48 (a) shows the laser removal of a-Si:H thin film at a laser fluence of 0.427 J/cm². As the laser fluence is increased further, some fringe formation can be observed on the surface, as seen in Fig. 48 (c). At higher laser fluence, the top sacrificial a-Si:H layer is

ablated away, and some of the laser light is absorbed by the n-layer underneath the SiN_x . The SiN_x layer is essentially transparent to 355 nm wavelength of the laser, so most of the light absorption occurs in the n-layer. The laser light absorption causes heating, melting, and vaporization of the n-layer along with the release of H_2 . The vapor absorbs part of laser energy, and high temperatures are generated. The high temperature causes ionization of the vapor and forms a plasma. The rapid laser heating in a localized region and formation of plasma generates a shock wave as it expands. Due to the presence of an over-layer of SiN_x , the generated pressures are much higher than without over-layer. The generated shock wave gives rise to the observed fringes as the material solidifies after laser heating. As the laser fluence is increased further, the generated plasma pressure becomes higher, and rupture of the SiN_x layer occurs as observed in figures 8 (e). This interpretation was further validated by EDS and XPS characterization.

The line-mapping EDS spectra acquisition was made at 3 kV beam energy so as to only measure the nitrogen element N ($\text{K}\alpha_1$) (denoted by green color spectrum) along the scan length D, which corresponds to the existence of SiN_x layer. From Fig. 49 (a) and (b), we

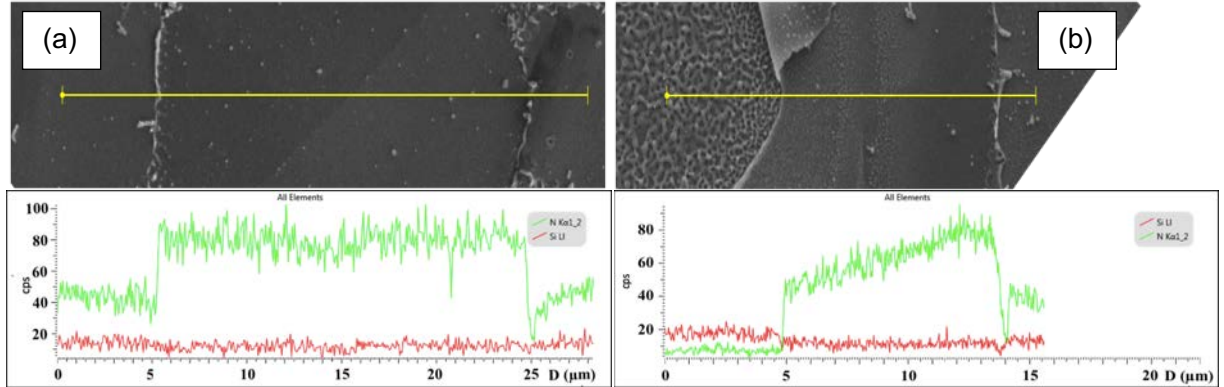


Fig. 49 Line-map EDS spectra for N $\text{K}\alpha_1$ at (a) 0.427 J/cm^2 and (b) 1.01 J/cm^2 fluences.

can see that as laser fluence increases from 0.427 J/cm^2 to 1.01 J/cm^2 , a dip in N-peak at the center of the laser spot was observed, which indicates the decrease in the SiN_x layer thickness. In Fig. 49 (b), at laser fluences of 1.01 J/cm^2 , the line mapping was done for the half of the laser spot area. Note that the gradual decline in the N peak, ultimately plummeting down at the center. This shows that the exposed SiN_x thickness tapers towards the spot center. This concludes that at fluences greater than 0.427 J/cm^2 , a gradient in SiN_x thickness is formed, ultimately leading to rupture.

All Raman scattering data had been taken as an average of 15 scans with each of 25 seconds of acquisition time at a particular location on each laser-ablated spot. Using n and k values from Fig.45, the calculated absorption depth for 405 nm blue wavelength Raman excitation laser in a-Si:H layer ($n = 5.155$; $k = 1.954$) is $\sim 16.49 \text{ nm}$ and

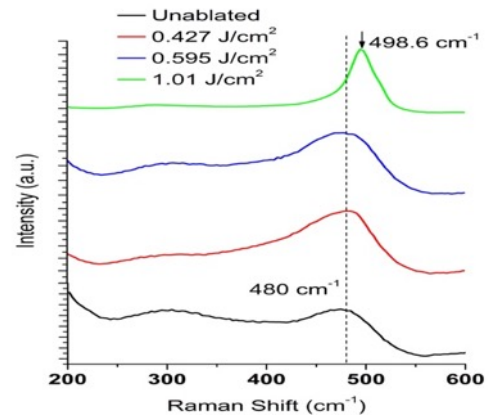


Fig. 50 Raman spectra of underneath a-Si:H passivation layer undergoing amorphous to polycrystalline phase under various laser fluences.

for SiN_x layer ($n = 2.344$; $k = 0.0003$), it is $\sim 54.9 \mu\text{m}$. Hence, $\sim 16\%$ of incident blue light intensity gets transmitted through 30 nm of the top sacrificial a-Si layer and reaches the SiN_x layer. In Fig. 50, we show the Raman scattering data of underneath a-Si:H layer undergoing phase changes from amorphous to polycrystalline form at different laser fluences. Here we can see that there is a Raman shift of Si peak from crystalline Si peak at 520.6 cm^{-1} to a broad peak from 470 cm^{-1} to 495 cm^{-1} centered at $\sim 480 \text{ cm}^{-1}$, which signifies the presence of a-Si:H layer. There is a slight shift of a-Si:H peak with an increase in laser fluence. At 1.01 J/cm^2 , there is an observable sharp peak at 498.6 cm^{-1} approaching towards crystalline Si peak. A decreasing trend of a broad $\sim 800 \text{ cm}^{-1}$ peak was also observed with an increase in laser fluences, which is assigned to the presence of SiN_x ²¹.

The HR-XPS measurements were done with $50 \mu\text{m}$ spot size, so the data gives an average over two laser spots of $20 \mu\text{m}$ beam diameter with a $\pm 0.2 \text{ eV}$ error. The XPS spectra have C (1s) peak calibrated to 284.8 eV, according to ASTM/ NIST. There is a decreasing trend in Si(2p): N(1s) ratio, indicating an increasing exposure of the SiN_x layer, with an increase in laser fluence. The anomaly in Si(2p): N(1s) ratio at a laser fluence of

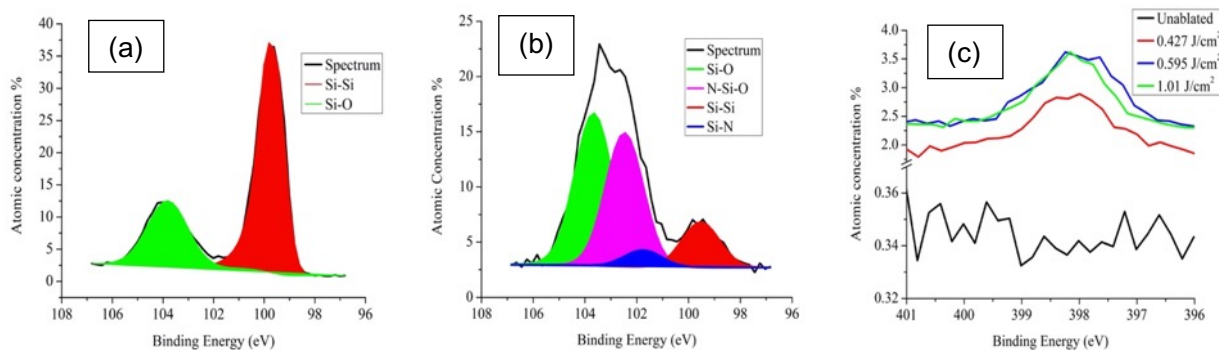


Fig. 51. XPS Si(2p) spectra of (a) unablated, (b) 0.595 J/cm^2 fluences, and N(1s) spectra of (c) at each of the laser fluences.

greater than 1.01 J/cm^2 can be explained by the fact that greater amount of SiN_x is exposed, which account for sudden increase in Si (2p) count, which has been discussed earlier. In Fig. 51 (a), as the laser fluence increases, the peak of Si (2p) decreased at 99.4 eV, and an increase in Si-O peak was observed at 103.5 eV, indicating SiO_2 formation, as reported by J.W. He et al. [15]). The increasing Si-N peak at 101.84 eV, as well as possible N-Si-O complex peak at 102.64 eV under 0.595 J/cm^2 fluence, are found to coincide with the literature²² as shown in the figure 51(b). The increasing N (1s) peak at 397.9 cm^{-1} due to the N-Si bond shows the presence of the SiN_x layer, as shown in Fig. 51(c)²³. The overall XPS study and Raman reveals that the a-Si:H layer can be laser ablated to expose the underneath SiN_x layer using ns laser processing without affecting the passivation.

Ablation by 355 nm wavelength laser

The laser Coherent Matrix-355-8-50 DPSS UV laser with a 355 nm wavelength was used. The laser provided a maximum average power of 8 W at a 50 kHz repetition rate, 25 ns pulse width, and Gaussian beam profile of $\sim 25 \mu\text{m}$ focused spot size at the FWHM. For the laser processing of IBC-HJ solar cells, each of the nine ablation line patterns had a

length of 13.5 mm and a total width of $\sim 150 \mu\text{m}$ and was made within $\sim 500 \mu\text{m}$ defined areas of the device samples. Since there was no built-in guide beam system for this laser, the misalignment was a major issue as it could lead to unwanted damage to the devices. So, the problem was solved by pre-alignment of either of the two external low power laser systems (CW blue 440 nm and red 632 nm lasers; both 50 mW before the actual UV laser ablation was done on samples. The blue laser was mostly used except for alignment on a photoresist (PR) coated samples.

Before optimization, the UV laser processing caused significant loss in iV_{oc} ($\sim 25 \text{ mV}$) and MCL ($< 800 \mu\text{s}$) where the parameters were 50 kHz repetition rate, 80% overlap pulse-to-pulse, power range from 26% to 29% at focus with the spot size of $\sim 25 \mu\text{m}$. After optimization, the laser parameters were 30 kHz repetition rate, $\sim 0 \%$ overlap pulse-to-pulse, power ranged from 27% to 28.5% for PMLP3 MC 1715 series. After laser processing, insignificant

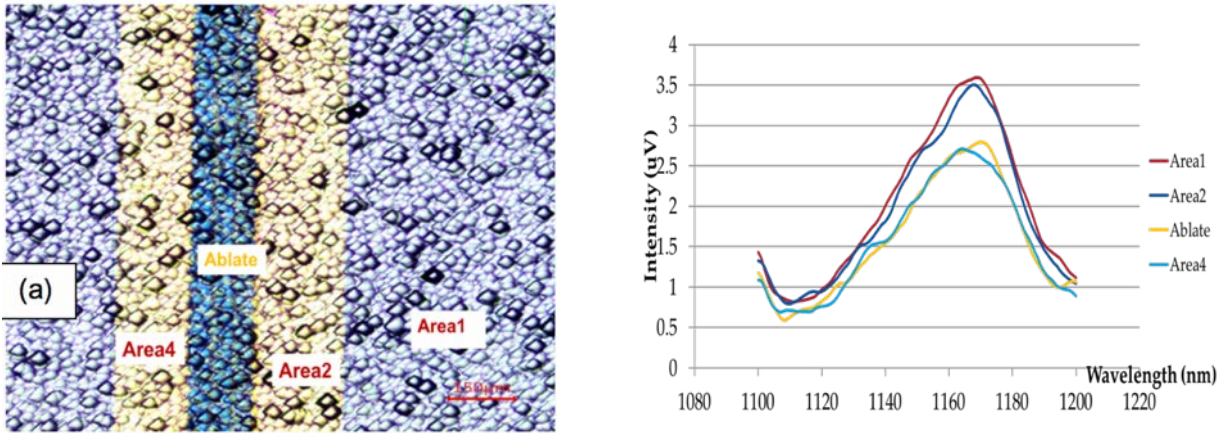


Fig. 52 (a). Optical image of a $150 \mu\text{m}$ wide ablation line on MC 1715-11 and (b) $\mu\text{-PL}$ data showing negligible damage of underneath passivation layer across the ablation line on MC 1715-11

Table 8: MCL and iV_{oc} before and after optimization for direct UV laser ablation on MC17515 series

Sample	MCL (μs) before laser	iV_{oc} (mV) before laser	MCL (μs) after laser	iV_{oc} (mV) after laser
MC 1715-04	807	682	786	682
MC 1715-11	2190	720	1755	719

loss in iV_{oc} ($< 3 \text{ mV}$) and MCL were observed, which are tabulated in Table 8. Preservation of the passivation at the ablated region had been shown in the $\mu\text{-PL}$ curve, shown in fig. 52b..

Similar optimizations were done with broader power ranges from 30% to 38% range, at focused $\sim 70\ \mu\text{m}$ spot size, keeping all the laser parameters the same for inverse PMLP3 devices (MC 1721, 1729 and 1730 series). Similar negligible losses in iV_{oc} and MCL were observed. Hence, direct UV laser ablation of sacrificial a-Si:H layers was accomplished for IBC-HJ cell fabrications without a significant effect on carrier lifetime.

3.3.c Patterning by direct ablations and exposure of photoresist

The novelty of using a photoresist (PR) coating on PMLP2, PMLP3, and reverse PMLP3 sample devices was that only the top sacrificial PR layer coat would either be exposed or directly ablated by the UV laser light without any direct laser-induced heat damaging the device. After proper development of the laser-exposed areas, selective chemical etching was done, followed by stripping off the remaining PR layer. This concept needs no complex masking and ensures flexible spatial-resolved patterning. The positive PRs used in this project were AZ1505 and AZ5214. At first, AZ1505 was used, but later on, AZ5214 replaced it to ensure a thicker coating to protect the samples.

The UV laser parameters used were 50 kHz repetition rate, 80% overlap pulse-to-pulse, and $\sim 150\ \mu\text{m}$ line widths at the focus. The processing window was relatively small, with an optimum range of powers was from 26% to 28%. There were a-Si conglomerations, forming poly-Si globules. So, the direct ablation of the PR approach was not followed.

Keeping all other laser parameters, the same, the power range was found to be from 20% to 25% for $\sim 1.4\ \mu\text{m}$ thick PR exposure. After a (1:100 v/v) HNA etch for 10s and 2% HF for 5s, the cross-sectional SEM images, shown in fig. 14, showed the success of this approach. A negligible drop in iV_{oc} ($< 6\ \text{mV}$) and in MCL, shown in Table 9, was observed after laser exposure. Hence, optimized UV laser exposure to the PR layer had induced negligible damage to the IBC solar cell devices.

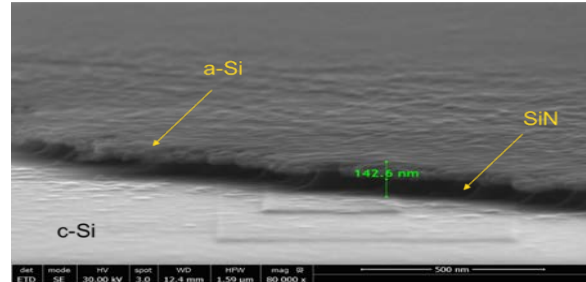


Fig. 54. SEM image of MC 1710-04 structure after UV laser exposure of PR at 24% followed by 10 sec of (1:100 v/v) HNA solution etch and 5 minutes of 2% HF etch.

Table 9. MCL and iV_{oc} before and after laser exposure of PR layer

Sample	Structure	MCL (μs) before laser	iV_{oc} (mV) before laser	MCL (μs) after laser	iV_{oc} (mV) after laser
MC 1710-04	PMLP2	679	699	573	693
MC 1730-11	Inverse PMLP3	1280	721	1227	720

3.3.d Laser patterning of nickel films for copper electrodeposition:

For patterning Ni films for Cu electrodeposition, the UV laser parameters were 50 kHz repetition rate, ~ 30% overlap pulse-to-pulse with a spot size of ~25 μm at the focus. A (3 X 3) matrix of powers (37.5%, 38%, 38.5%) and HNO_3 -based Transene Nickel Etchant TFB etch time (30s, 45s, 60s) was followed to process un-passivated samples from the MC 1681 series samples. Deep laser ablation trenches were formed along the center of the ~ 50 μm width scribed line. The laser parameters were optimized to a larger spot size of ~80 μm and passivated samples from MC 1681 series were processed at powers of 37.5% and 38%, followed by HNO_3 -based Transene Nickel Etchant TFB with etch times of the 30s and 45s. The issue of deep ablation trenches was avoided. Sample series MC 1718 were also laser processed with the same optimized parameters with powers 37% and 37.5%, and followed by HNO_3 -based Transene Nickel Etchant TFB with etch times of 45s and 60s. The detailed characterizations of all these samples were accomplished at the University of Delaware.

Post analysis of fabricated devices:

A major issue of alignment of laser-ablated patterns and post-laser Al metal deposition performed at the University of Delaware was observed with an error of $\pm 70 \mu\text{m}$ due to tolerance of steel mask dimensions during PECVD. A possible short between p-metal and n- metal strip through the overlapped laser ablation seemed feasible. In fig. 15, we can see this possible connecting short, resulting in lower shunt resistance in a reverse PMLP3 MC 1729 series sample. This issue was resolved by using the steel mask and 1" X 1" sample holder, used for the PECVD process, and doing laser ablation of both ~150 μm width and total raster scan in MC 1730 series. This strategy eliminated the possible misalignment during metal deposition.

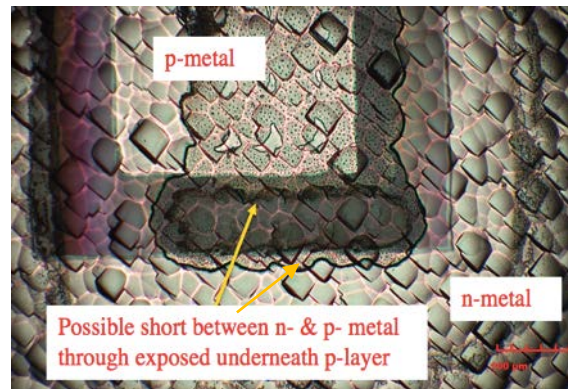


Fig. 55. Optical image of possible short between p- and n- metal strips through exposed underneath p-layer in MC 1729

3.3.e Conclusion

The green 532 nm wavelength nanosecond pulsed laser patterning required for the fabrication of IBC-HJ solar cells without damaging its passivation was successfully demonstrated. The laser fluence for the patterning needed to be less than 0.427 J/cm^2 , where the sacrificial layer of a-Si:H gets ablated and exposing the SiN_x layer so that it can be selectively chemically etched for IBC-HJ device fabrication. With the increase in laser fluence, the removal of the SiN_x layer was observed due to the laser light absorption by underlying layers and the development of vapor pressure. The underlying a-Si:H (n and i) layers, acting as passivation and dopant layers, crystallize to the poly-crystalline phase as laser fluence is increased beyond 0.595 J/cm^2 . At laser fluences greater than 1.01 J/cm^2 , direct laser crystallization was observed and resulted in the rupturing of the SiN_x layer at the center of the laser spot. The presence of the SiN_x layer after the laser ablation of the a-Si:H layer was confirmed by line-mapping EDS and Raman measurements. The Raman data also showed the gradual crystallization of a-Si:H layer underneath the SiN_x layer with an increase in laser fluence. The XPS measurements showed the growth of

SiO₂, SiN_x, a complex N-Si-O at the surface (at 0.595 J/cm²), and a decrease in the Si/N ratio after laser processing. The optical constants of the layers were measured using ellipsometry, which helped to generate the color charts, which can be reliably used to identify the changes in layer properties under different laser processing parameters. Such a method can also be used for multi-layer identification in different thin-film devices.

One of the major issues with UV laser processing was the alignment of UV laser ablations onto the IBC-HJ devices. This issue was resolved by using external laser systems, which acted as a guide beam. In this project, there had been several methodologies adopted to laser process IBC-HJ solar cell devices. Direct UV laser ablations of PR-coated samples caused crystallization and damage in the devices. Direct UV exposure of PR coated samples were successfully done, preserving the lifetime and iVoc (< 5 mV drop) after laser processing. The optimization of the UV laser parameters was accomplished for direct UV laser ablations of sacrificial a-Si:H layers, and a negligible drop in iVoc (< 3 mV), and MCL was measured after laser processing. Imperfect alignment of UV laser patterns and the Al metal contact strips along with the vertical directions, resulting in a short between the n- and p- metal strips, was resolved by using the PECVD steel mask and a 1" X 1" sample holder while drawing both ~150 μm width ablation lines and raster scans. Due to the successful optimization, both ablation schemes resulted in a minor drop in iVoc (< 5 mV) and MCL. Thus, nanosecond pulsed laser was successfully demonstrated for the patterning of IBC-HJ devices without significant change in carrier lifetime and iV_{oc}.

3.4 Development of Electroplated Cu Films for Back Contact Application

3.4.a Experimental Procedures

The deposition and characterization of electrodeposited (ED) Cu films was conducted over the entire contract period but most intensively in BP2 and BP3. Some of the work was presented at the 46th IEEE PVSC²⁴. Baths were optimized for electrodeposition of Cu (ED Cu) on structures of 65 nm evaporated Ni seed layers on 1"x1" 150 μm thick textured-Si wafers (Ni/Si). Some of the Ni layers were uniform for various characterization studies, and others were laser patterned as required to create IBC contacts. Electrochemical experiments were carried out using a standard 3-electrode cell, with Ni/Si substrates as the working electrode, Pt gauze as the secondary electrode, and a saturated calomel reference electrode (SCE). All voltages are given with respect to SCE. Cyclic voltammetry (CV) and electrodeposition measurements, carried out with a PAR PARSTAT 2273 potentiostat, were used to optimize bath and deposition conditions. CV assisted determination of plating potential, as well as bath concentrations and pH.

Best quality deposits were plated from Ar-purged aqueous baths containing 0.1 M CuSO₄ and 1 M H₂SO₄ (pH~0) at deposition potentials between -0.25 - -0.3 V without stirring of the solution. These conditions reproducibly gave smooth films with uniform morphology at a growth rate of ~0.1 μm/min. Some films were processed with short (30s – 5 min) pre-deposition steps to improve adhesion and attenuate pinhole formation, where ED Cu was plated at standard conditions for a short time before briefly stopping and restarting deposition.

Adhesion pull tests were carried out after ED Cu plating with various pre-deposition step times onto Ni/Si substrates. A sample with 1 min pre-deposition step showed excellent adhesion, where the wafer broke during the test at a force of ~5 N, before any Cu peeled from the substrate. A sample with a 5 min pre-deposition, however, showed Cu peeling from the Ni at just ~1 N, indicating that longer pre-deposition steps are deleterious for ED Cu adhesion. With further optimization of bath conditions, it was found that ED Cu films exhibited suitable adhesion without pre-deposition steps.

For ED Cu/Ni contact resistance (R_C) measurements, a modified transmission line method (TLM) pattern was developed (Fig. 56). The structure consists of a masked evaporated Ni layer deposited on textured-Si, with several fingers of increasing separation distance. These fingers are initially connected by a large tab to allow contacting for Cu electrodeposition. Following plating, the tab is cleaved from the sample, leaving the now ED Cu-plated fingers electrically isolated. Resistance (R) is measured between the plated fingers, producing a linear plot of R with finger separation distance, from which contact resistance is determined.

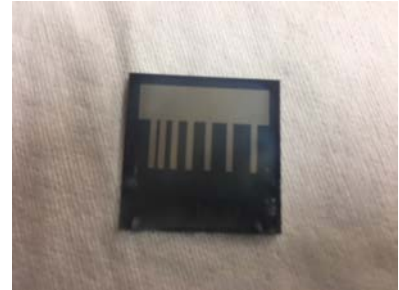


Fig. 56. Modified Ni/Si TLM pattern for R_C measurements of ED Cu contacts.

A ~2.5 μm ED Cu film was plated on a Ni/Si TLM pattern with a 1 min pre-deposition step. Contact resistances for ED Cu/Ni/Si, along with bare Ni/Si for comparison, are presented in Table 10. For ED Cu/Ni/Si, $R_C = 11.7 \text{ m}\Omega\cdot\text{cm}^2$ was determined, which improved to ~5 $\text{m}\Omega\cdot\text{cm}^2$ with a 15 min anneal at 150°C in air. This shows a significant improvement over the bare Ni films, $R_C \sim 80$ and ~65 $\text{m}\Omega\cdot\text{cm}^2$ with and without anneal, respectively. The measured R_C for the ED Cu/Ni/Si sample is very near the milestone MQ6.T3 target of <3 $\text{m}\Omega\cdot\text{cm}^2$. It is likely the Cu films may have slightly oxidized during storage and measurement, and improved values will be expected with encapsulation and/or storage of the TLM samples in a dry desiccator.

Table 10. R_C measurements for ED Cu/Ni/Si samples, determined from the TLM approach.

Sample	ρ ($\text{m}\Omega\cdot\text{cm}^2$)
Ni/Si (control)	78.1
Ni/Si + ann.	64.5
ED Cu (~2.5 μm)/Ni/Si	11.7
ED Cu/Ni/Si + ann.	5.4

3.4.b Electroplated Cu on Laser Patterned Ni for Interdigitated Back Contacts

An IBC design was developed for laser scribing of contact patterns suitable for Cu plating. The contact design was developed to maintain electrical isolation of n- and p-strips, while including tabs to allow contacting for simultaneous plating on both sets of fingers. Fig. 57a shows the final contact design, which proved the most practical to handle in the laboratory, showing tabs separated to allow contact to each set of fingers using two clips, which were shorted during plating. Laser processing was carried out at the lowest power that allowed electrical isolation of the contact strips, generally using single pass of a defocused laser, giving scribes ~100 μm wide. The substrates used for these studies

were 65 nm Ni layers evaporated on a-SiN_x/Si substrates. a-SiN_x is an insulator and will not plate Cu. Some samples also received a stack (10 nm intrinsic a-Si/a-SiN_x) passivation layer on each side of the wafer to monitor lifetime during processing. Following patterning, these samples showed no change in lifetime, indicating that wafer passivation is maintained during laser scribing.

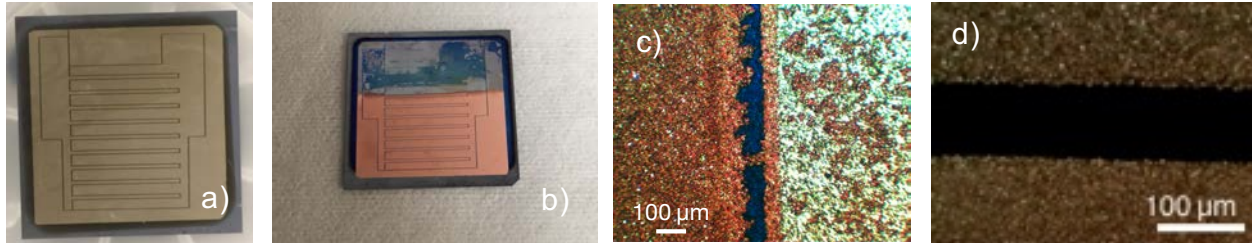


Fig. 57. a) Laser-scribed IBC pattern for Cu plating, b) ED Cu film on a laser scribed sample, c) OM image of Cu bridges formed across a laser cut during plating, and d) OM image of ED Cu on a masked patterned Ni/Si.

Cu plating was carried out on laser-scribed samples at optimized conditions. Fig. 57b shows a photo of a representative laser-scribed sample following Cu plating. The deposited ED Cu film is uniform with good adhesion, but unexpected Cu plating outside of the contact area is observed. Cu bridges were found to have grown from the edges of the laser scribes during plating, seen in the optical microscope (OM) image in Fig. 57c, shorting both the fingers and to the area outside of the contacts. Comparison experiments using Ni contact strips deposited through a shadow mask found no Cu growths into the gaps, exhibiting sharp well-defined contact edges (Fig 57d).

These observations suggest a conductive residue, likely Ni, remains in the scribes after patterning, that allows Cu to plate across the gaps. The presence of residual Ni in the scribes could not be confirmed, however, gentle etch treatments were carried out to remove any possible residues. Following Cu plating on a substrate that had been etched in FeCl₃, OM shows the cuts are now very clean with no evidence of significant Cu growth from the edges of the scribes (see OM image in Fig. 59a). Electrical isolation of the contact strips was confirmed with shunt resistance measurements.

A further reason for the formation of Cu growths into the scribes may be the result of microscopic roughness along the edges of the Ni laser cuts (Fig. 58a), which will exacerbate the formation of Cu growths into the scribes during plating (Fig. 58b). This is attenuated with etching, likely due to the chemical treatment smoothing the edges

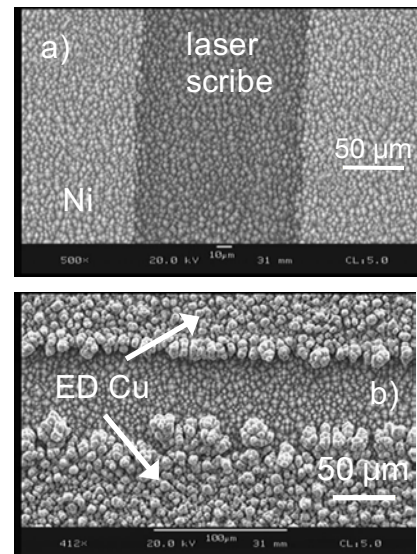


Fig 58. SEM of laser scribe in a Ni film a) before and b) after Cu plating.

of the cuts and lessening the frequency these unwanted features.

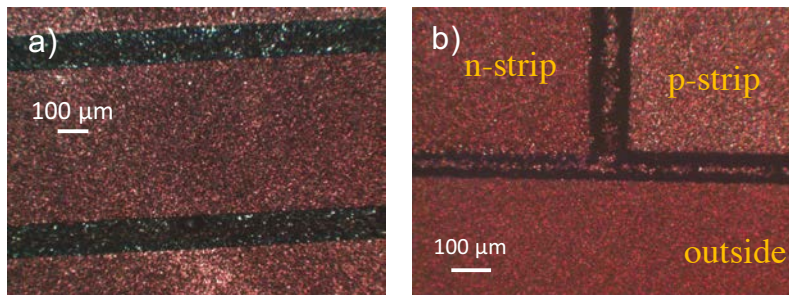


Fig. 59. Optical microscope images of laser-scribes on observed on this sample, a thick ED Cu/Ni/Si_x/Si substrates following treatment in a) ED Cu strip is now present along FeCl₃- and b) HNO₃-based Ni etches.

the center of all the laser cuts. On closer inspection of the OM image of the FeCl₃-etched sample (Fig. 59a), a thin, uniform Cu strip is observed directly along the center of the cuts. Despite the presence of this parasitic Cu plating, these samples showed very high shunt resistances, indicating the contacts are electrically isolated. Fig. 60 shows an SEM image, along with Si and Cu EDS maps of the same area, of a portion of a Cu stripe formed in the scribe of a patterned ED Cu/Ni/Si_x/Si sample that had received HNO₃ etching. The stripe can be seen to consist of discrete Cu islands within the scribe, some of which have coalesced during growth, and that are not in contact with the ED Cu or Ni films at the scribe edges.

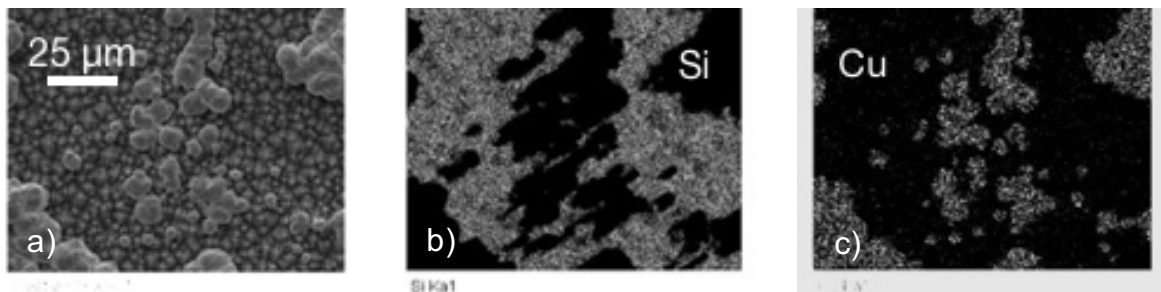


Fig 60. (a) SEM and (b) Si and (c) Cu EDS maps of a portion of the Cu stripe feature formed in a scribe of a laser patterned ED Cu/Ni/Si_x/Si sample that had received a 30 s HNO₃ etch prior to plating. Brighter regions in the EDS images indicate presence of the selected element.

To optimize laser conditions for patterning, the effect of a double pass of a focused laser was tested to monitor control of scribe width and removal of residual species. These samples showed a ~130 μm scribe in the Ni film, but now with a ~20-30 μm wide laser-damaged trench along the center of the cuts, likely due to overlap of the laser passes, and that had not been observed with single laser pass scribing. However, following HNO₃ etching and Cu plating, none of the double laser pass samples exhibited the Cu-stripe feature, despite the large area of exposed Si, indicating a difference in the properties of the scribed regions depending on the laser conditions.

The effects of laser conditions on processing were further emphasized through studies varying laser powers. At lower power (<37.5%), Cu shorts were found to easily form during plating, even with etching, due to insufficient ablation of Ni. However, the Cu stripe feature was not observed at these laser conditions. Plating to substrates patterned at higher laser powers (>37.5%), resulted in more well-defined scribe edges with fewer Cu growths formed into the scribe lines, however, the parasitic Cu stripe is consistently observed. This apparent trade-off does highlight the sensitivity of sample stacks and Cu plating to processing conditions, and difficulty in identifying an optimized processing regime for this sample system that avoids parasitic Cu plating.

These observations of processing effects on the nature of parasitic ED Cu did, however, assist the development of a mechanism for the formation of the Cu stripe feature (Fig 61). With a single laser pass, damage from laser ablation and etching to the SiN_x layer opens pinholes to the more conductive c-Si wafer. These small points of higher conductivity in the resistive layer can form very high localized current densities, sufficient to nucleate Cu and allow subsequent rapid growth of island-like features [25, 26]. Once a seed is formed, further growth of Cu becomes energetically easier and, with time, these islands can grow to several microns in size (Fig. 60). Raman spectroscopy indicated the presence of insulating a-Si in the scribes, likely from degradation of SiN_x , though this phase is likely of insufficient thickness to prevent plating at the high current densities. The different morphology of the Cu stripe with FeCl_3 -etched samples (Fig. 3a), may suggest a slower growth rate due to a different degree of etch damage to SiN_x with this treatment. In contrast, for the double-pass laser patterned pieces, no plated Cu stripe is formed during plating. The wide damage trench exposes a significantly larger area of the Si wafer, which results in much lower current densities during plating, and insufficient to deposit Cu metal, than what is expected through a pinhole feature. The degradation of a larger area of SiN_x would also form a thicker insulating a-Si layer to further attenuate Cu nucleation. These observations of laser damage affecting both the integrity of underlying layers and growth of subsequent films, highlights the need for careful optimization and control of laser conditions for processing of PV devices.

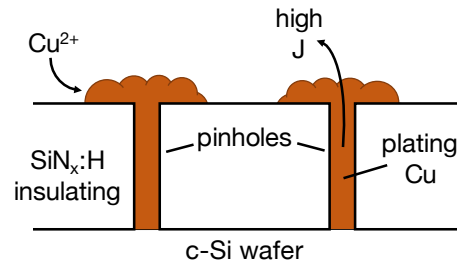


Fig. 61 Schematic of the proposed mechanism for the formation of the Cu stripe feature.

3.4c Electroplated Cu Back Contacts for Front Junction Devices

To confirm the feasibility of ED Cu back contacts for Si-based devices, previously processed front junction (FJ) cells with good performance were selected for re-contacting. Al back contacts were removed by etching, and new ED Cu/Ni back contacts were processed. Two evaporated 65 nm Ni patterns were deposited; a blanket layer covering the entire rear of the device, and through a p-pattern contact shadow mask. ~2 μm ED Cu were plated to the seed Ni layers at best conditions, using -0.25 V deposition potential. Dry resist was used to protect the front of the device. Table 11 shows the JV data before

and after re-contacting. The device performance shows very little change with ED Cu/Ni contacting, with small J_{sc} improvements, ~ 1 mA, maintaining efficiencies near 18%. Both devices show an improvement in series resistance (R_s), suggesting an improved R_c , with ED Cu contacting compared to the standard Al back contacts. These results do indicate Cu plating is a feasible, and industrially-significant, approach for processing of high quality contacts for Si-based solar cells.

Table 11. JV parameters for FJ cells before and after re-contacting with ED Cu/Ni back contacts.

Sample	Contact	Pattern	V_{oc} / mV	J_{sc} / mA/cm ²	FF %	Eff %	R_s / Ω cm ²
MC1662-08	Al	-	714	35.1	71.3	17.9	1.16
	Cu	blanket	709	36.1	69.5	17.8	1.01
MC1662-06	Al	-	709	35.3	70.8	17.7	1.51
	Cu	p-patt.	709	36.1	69.5	17.8	0.87

Regarding MQ6.T3 “Demonstrate contact resistance $< 3 \text{ m}\Omega\cdot\text{cm}^2$ and adhesion pull strength $> 0.2 \text{ N/mm}$ (determined on test structures or cells) for laser fired and Cu plated contacts (Q6)” we came very close to meeting the contact resistance goal by measuring values of $\sim 5 \text{ m}\Omega\cdot\text{cm}^2$ using TLM and we exceeded the adhesion goal.

3.4.d Conclusions

Under this task we have: 1) Developed processing conditions for uniform Cu plating, with excellent adhesion, on laser-scribed Ni contacts for device incorporation; 2) Confirmed low R_c for ED Cu/Ni/Si of $\sim 5 \text{ m}\Omega\cdot\text{cm}^2$; 3) Developed a formation mechanism for the observed parasitic plating of ED Cu in laser scribes; and 4) Demonstrated the feasibility of ED Cu contacts for devices, with no observed loss in performance compared to standard Al metal back contacts.

4.0 Key Innovations and Conclusions:

We undertook a very challenging task with a very ambitious goal for such a small team. Although we failed to meet the final milestone of a IBC-HJ device fabricated with laser processing having 25% efficiency, we identified many of the obstacles and worked creatively to mitigate them. We did meet 10 of the 14 milestones, but the ones we missed are the most significant. Some solutions required minor changes while others required major revision of the device process and structure. But they were all driven by characterization and analysis of materials and devices. We never lost sight of the goal of developing a low cost manufacturable IBC-HJ. This limited the tools we could employ.

A number of innovations resulted from this work:

1. The importance of Ga as a dopant in forming laser fired emitter junction.

2. The viability of lower cost nanosecond lasers in processing Si solar cells by either direct patterning or indirect ablation plus etching. In particular, they can pattern an entire IBC structure with minimal loss in passivation (iVoc). We were able to ablate and etch openings ~ 2 cm long for the HJ n-contact on 9 fingers long with less than 5 mV loss in iVoc.
3. Characterization of 2D current flow and specifically the inversion layer was demonstrated using 3 terminal test devices where one side had IBC-type electrodes allowing independent biasing of the contact layers.
4. A process and procedure to produce laser patterning Ni layers and then grow Cu by ED was demonstrated having low contact resistance, excellent shunt isolation, and good adhesion.
5. A new concept was established for depositing the a-Si i-layer which is essential for good passivation. This involves a bilayer stack each ~ 4 nm thick followed by a hydrogen plasma treatment and has given state-of-the-art iVoc > 740 mV for 8 nm i-layers.

Key conclusions are:

1. Despite significant variation in the LFC metal and dielectric stack, and in laser conditions, the LFC concept appears to be unacceptable for HJ devices. This is partly due to the inversion layer which increases the flow of current for recombination at the defective LFC spot.
2. Plasma masking is very challenging. Avoiding unwanted 'plasma leakage' under the shadow mask is nonuniform in thickness but can extend tens or hundreds of microns from the edge despite the intended film being < 10 nm. Etching was partially successful but was limited by the fact that the layer we wanted to remove and the layer underneath were nearly the same. More selectivity in etching would be helpful.

5.0 Budget and Schedule:

The official start date was 8/01/16 and original end date was 7/30/19. Due to various contractual delays and modification of the SOPO we did not actually start working on the project until 01/01/17 which was five months after the official start date. We requested a six month No-Cost Extension (NCE) in 2018 so the revised end date became 1/31/2020. All funds have been expended and cost share requirements were met. The total Federal share was \$1,124,491 and the cost share provided by UD and UVa was \$125,084.

6.0 Path Forward:

Currently, there are no commercial IBC-HJ products. Panasonic was rumored to be devoting part of their 'gigafactory' in Buffalo NY operated with Tesla but that is now very unlikely. Us Sunpower is not interested in the HJ approach. US bifacial HJ module manufacturer Sunprime has not expressed an interest in the IBC approach. Thus we

have been unable to find an industry partner. Despite this, there are groups around the world still pursuing IBC-HJ designs by various innovative processing approaches.

Many of the concepts developed here regarding laser patterning, ablation plus etching, and passivation are likely to be of interest to advancing the PERC cell. Further research is recommended to understand the region between n and p as the source of high recombination leading to low V_{oc} .

We found the shadow masking of PECVD layer to be challenging, however, masking a PVD layer could be easier and simpler. This could lead to development of alternate device structures with PVD deposited carrier selective contact layers.

7.0 Publications Resulting from This Work:

Journal Publications:

1. "Analysis of silicon wafer surface preparation for heterojunction solar cells using X-ray photoelectron spectroscopy and effective minority carrier lifetime" Ugochukwu Nsofor, Lei Zhang, Anishkumar Soman, Christopher Goodwin, H. Liu, Kevin Dobson, Ujjwal Das and Steven Hegedus, *Solar Energy Mat. Solar Cell*, 2018, <https://doi.org/10.1016/j.solmat.2018.03.006>
2. "Study of Passivation in the Gap Region between Contacts of Interdigitated Back Contact Silicon Heterojunction Solar Cells: Simulation and Voltage-modulated Laser-beam-induced-current" Lei Zhang, Nuha Ahmed, Christopher Thompson, Ujjwal Das, and Steve Hegedus, *IEEE J Photovoltaics* 2018, Vol 8, pp. 404-412 <https://DOI: 10.1109/JPHOTOV.2017.2783852>
3. "Electroluminescence Analysis for Spatial Characterization of Parasitic Optical Losses in Silicon Solar Cells", by Nuha Ahmed, Lei Zhang, Gowri Sriramagiri, Ujjwal Das, and Steven Hegedus, *Journal of Applied Physics* (March 2018) <https://doi.org/10.1063/1.5007048>
4. "Correlation between in Situ Diagnostics of the Hydrogen Plasma and the Interface Passivation Quality of Hydrogen Plasma Post- Treated a-Si:H in Silicon Heterojunction Solar Cells" Anishkumar Soman, Ugochukwu Nsofor, Ujjwal Das, Tingyi Gu, and Steven Hegedus, *ACS Appl. Mater. Interfaces* 2019, 11, 16181–16190 DOI: 10.1021/acsami.9b01686
5. " N. Ahmed, L. Zhang, U. Das and S. Hegedus, "Electroluminescence Characterization of Recombination in Back Junction Silicon Heterojunction Test Structures: Role of the Inversion Layer," in IEEE Journal of Photovoltaics, vol. 10, no. 2, pp. 634-643, March 2020.
6. "Nano-second Pulsed Laser Patterning of Interdigitated Back Contact Heterojunction (IBC-HJ) Silicon Solar Cells", A. Sinha, A. Soman, U. Das, S. Hegedus and M. C. Gupta (under preparation)

Conference Presentations/Proceedings:

1. "Processing Approaches and Challenges of Interdigitated Back Contact Si Solar Cells" U Das and S Hegedus. *44th IEEE PVSC*, Washington DC June 2017.
2. "Electroluminescence Analysis For Separation of Series Resistance From Recombination Effects in Silicon Solar Cells with Interdigitated Back Contact Design" Nuha Ahmed, Lei Zhang, Ujjwal Das, and Steven Hegedus. *44th IEEE PVSC*, Washington DC June 2017.
3. "Hydrogen Plasma Post-Deposition Treatment for Passivation of a-Si/c-Si Interface for Heterojunction Solar Cell by Correlating Optical Emission Spectroscopy and Minority Carrier Lifetime" A Soman, U Nsofor, L Zhang, U Das, T Gu, S Hegedus. *44th IEEE PVSC*, Washington DC June 2017.
4. "Gap passivation structure for scalable n-type interdigitated all back contacts silicon hetero-junction solar cell processes" Lei Zhang, Ujjwal Das, Steven Hegedus. *44th IEEE PVSC*, Washington DC June 2017.
5. "Improving the Interface Passivation of Si HJ Solar Cells by Interrupted Deposition of Thin a-Si:H Film" Ugo Nsofor, Anishkumar Soman, Ujjwal Das, Steve Hegedus, *Proc. 45th IEEE PVSC Waikoloa HI, June 2018*.
6. "Effect of dielectric layers on laser-fired-contact performance in a-Si/c-Si heterojunction Solar Cells" Ujjwal Das, Christopher Thompson, Ugo Nsofor, Zeming Sun, Mool C. Gupta, and Steven Hegedus, *Proc. 45th IEEE PVSC Waikoloa HI, June 2018*.
7. "Direct Laser Isolation For Interdigitated Back Contact Heterojunction Solar Cells" Zeming Sun, Ugo Nsofor, Nuha Ahmed, Ujjwal K. Das, Steven Hegedus, and Mool C. Gupta, *Proc. 45th IEEE PVSC Waikoloa HI, June 2018*.
8. "Direct Laser Patterned Electroplated Copper Contacts for Interdigitated Back Contact Silicon Solar Cells" Kevin D. Dobson, Zeming Sun, Ugochukwu Nsofor, Ujjwal Das, Arpan Sinha, Mool Gupta, and Steven S. Hegedus, *Proc. 46th IEEE PVSC Chicago June 2019*
9. "a-Si:H/c-Si interface hydrogenation for implied Voc = 755 mV in Silicon heterojunction solar cells" Anishkumar Soman, Ugochukwu Nsofor, Ujjwal Das, Tingyi Gu, Steve Hegedus, *Proc. 46th IEEE PVSC Chicago June 2019*
10. "Interdigitated Back Contact (IBC) Heterojunction (HJ) Si Solar Cell Fabrication by Laser Patterning" Arpan Sinha, Anishkumar Soman, Ujjwal Das, Steven Hegedus and Mool Gupta, submitted IEEE PVSC Calgary, June 2020

8.0 Students Contributing to This Work:

Name	BS/MS/PhD/ Postdoc	From: (Semester- Year)	To: (Semester- Year)	Current Affiliation	Position,
Ugochukwu Nsofor	PhD, UD	Fall 2016	Fall 2018	Engineer, Intel	

Nuha Ahmed	PhD, UD	Fall 2016	Summer 2019	Instructor, Delaware Tech Comm. College
Lei Zhang	PhD, UD	Fall 2016	Spring 2018	Engineer, Global Foundry
Zeming Sun	PhD, UVa	Fall 2016	Fall 2018	Post-doc, Cornell
Arpan Sinha	PhD, UVa	Fall 2018	Spring 2020	Graduate Researcher, Electrical Engr. (UVa)
Anish Soman	PhD, UD	Fall 2018	Spring 2020	Graduate Researcher, Electrical Engr. (UD)
Pat Conroy, Jason Alexander	BS, UD	Summer 2017	Spring 2020	Undergrad researcher, lab assistant

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9.0 References: List literature references cited in the report, using the format provided in RPPR Attachment 3.

¹ Lei Zhang, Nuha Ahmed, Christopher Thompson, Ujjwal Das, and Steve Hegedus, "Study of Passivation in the Gap Region between Contacts of Interdigitated Back Contact Silicon Heterojunction Solar Cells: Simulation and Voltage-modulated Laser-beam-induced-current" *IEEE J Photovoltaics* 2018, Vol 8, pp. 404-412 [https://DOI: 10.1109/JPHOTOV.2017.2783852](https://doi.org/10.1109/JPHOTOV.2017.2783852)

² N. Ahmed, L. Zhang, U. Das and S. Hegedus, "Electroluminescence Characterization of Recombination in Back Junction Silicon Heterojunction Test Structures: Role of the Inversion Layer," in *IEEE Journal of Photovoltaics*, vol. 10, no. 2, pp. 634-643, March 2020.

³ A. Sinha, A. Soman, U. Das, S. Hegedus and M. C. Gupta "Nano-second Pulsed Laser Patterning of Interdigitated Back Contact Heterojunction (IBC-HJ) Silicon Solar Cells (under preparation)

⁴ Ugochukwu Nsofor, Lei Zhang, Anishkumar Soman, Christopher Goodwin, H. Liu, Kevin Dobson, Ujjwal Das and Steven Hegedus, "Analysis of silicon wafer surface preparation for heterojunction solar cells using X-ray photoelectron spectroscopy and effective minority carrier lifetime" *Solar Energy Mat. Solar Cell*, 2018, <https://doi.org/10.1016/j.solmat.2018.03.006>

⁵ Anishkumar Soman, Ugochukwu Nsofor, Ujjwal Das, Tingyi Gu, and Steven Hegedus, "Correlation between in Situ Diagnostics of the Hydrogen Plasma and the Interface Passivation Quality of Hydrogen Plasma Post- Treated a-Si:H in Silicon Heterojunction Solar Cells" *ACS Appl. Mater. Interfaces* 2019, 11, 16181–16190 DOI: 10.1021/acsami.9b01686

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⁷ Zeming Sun, Ugo Nsofor, Nuha Ahmed, Ujjwal K. Das, Steven Hegedus, and Mool C. Gupta, "Direct Laser Isolation For Interdigitated Back Contact Heterojunction Solar Cells" *Proc. 45th IEEE PVSC Waikoloa HI*, June 2018.

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