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Development of a FELIX Based Readout System for ITk Strip Hybrid Module Demonstrator for ATLAS Phase-II Upgrade

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Abstract: The Large Hadron Collider (LHC) will undergo a major upgrade around 2024 with a roughly tenfold increase in luminosity. It results in corresponding increases in particle rates and radiation doses that the current ATLAS Inner Tracking Detector cannot cope with. Therefore the ATLAS experiment will build a new all-silicon tracking system called the ITk (Inner Tracker) that includes an inside pixel detector close to the beam line and a strip detector in outside layer. Meanwhile the ATLAS experiment will adopt the Front-End Link eXchange (FELIX) system as the interface between the data acquisition and front-end electronics for all sub-detectors in the Phase II Upgrade. In this contribution, we present a prototype of FELIX based readout system for the strip hybrid module. Its hardware, firmware and software GUI application will be discussed, as well as integration test results.

Keywords: ATLAS experiment; ATLAS ITk; Strip detector; Data acquisition

Contents

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1 Introduction

The Large Hadron Collider (LHC) will undergo Phase II Upgrade around 2024 to reach a peak instantaneousluminosityupto$7.5\times10^{34}cm^{-2}s^{-1}$ [1]. Thiswillprovideunprecedentedopportunities for Standard Model precision measurement and increase the potential for new physics discovery. During the same long shutdown, the ATLAS detector will have major upgrades to address huge radiation damage and cope with a higher average pile-up of 200 inelastic proton-proton interactions per bunch crossing [2]. A new all-silicon Inner Tracker (ITk) will replace the current inner detector, which consists of a pixel detector at small radius close to the beam line and a large area strip detector surrounding it. Its schematic layout is shown in the Figure 1. The new strip detector consists of four barrel layers and six end-cap rings on both forward regions, covering $165m^2$ silicon sensors which is 2.5 times that of the current silicon strip system [3]. In total, it will have roughly 60 million strip channels. This added complexity requires a re-design of the ATLAS data acquisition (DAQ) system.

[2] ITk Strip Detector Upgrade

The new ATLAS Strip Detector is designed based on staves and petals concept. Its four barrel layers consist of 392 staves on both sides (196 staves on each side of z = 0 in Figure 1). Each barrel stave is populated with 28 modules. In the end-cap system, each disk consists of 32 identical petals which has 9 modules on each side with six different sensor geometries to cover the wedge shaped petal surface. The layout overview of stave and petal is shown in the Figure 2. The staves and petals are mounted on global support structures with integrated cooling system. The EoS (End of Structure) board that is placed at the end of the structure is the interface between the staves/petals and the off-detector electronics [4]. The main components of EoS are radiation hard lpGBT (low power

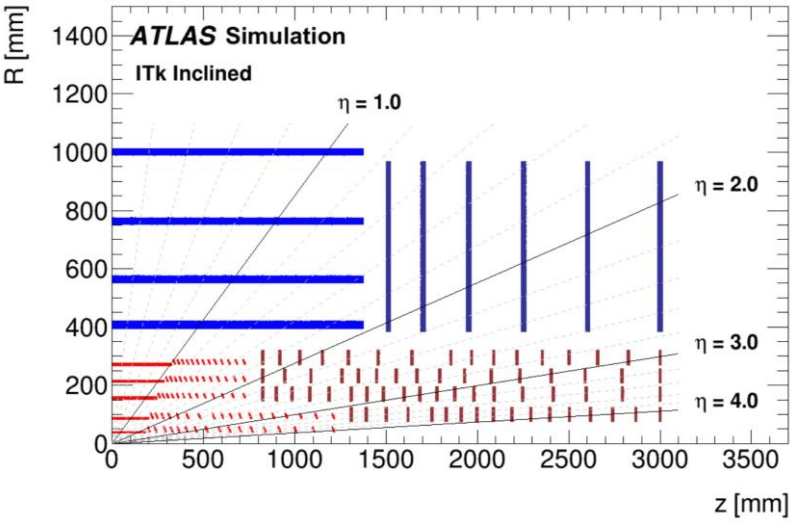


Figure 1: Schematic layout of the ITk for the ATLAS Phase II Upgrade[3]. Here only the upper right quadrant is shown, with the interaction point at zero and the beam line aligned along the horizontal axis. The Pixel Detector elements are in red, while the Strip Detector parts are shown in blue.

GigaBit Transceivers) ASICs and an optical transceiver modules VTRx plus (Versatile Transceiver) [5][6]. The EoS board distributes TTC information (Trigger, Timing and Control) to the front-end ASIC chips, and also sends detector event data to the DAQ system of FELIX (Front-End LInk eXchange) in the back-end via high speed optical links [3] [7].

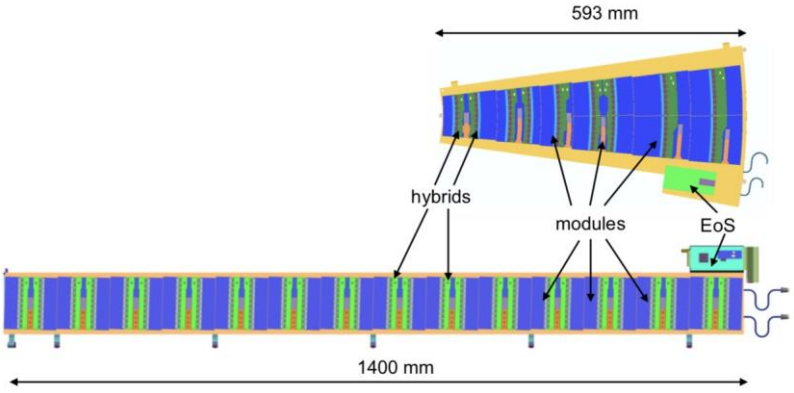


Figure 2: Overview of end-cap petal (upper) and barrel stave (lower) components in ITk Strip Detector[3].

3 Hardware

The basic unit of both strip stave and pedal is strip hybrid module which consists of strip sensors and one PCB board hosting several front-end ASIC (Application Specific Integrated Circuit) chips.

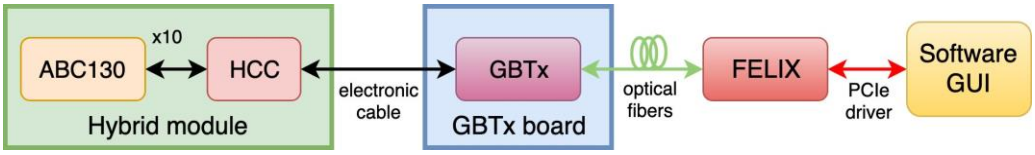
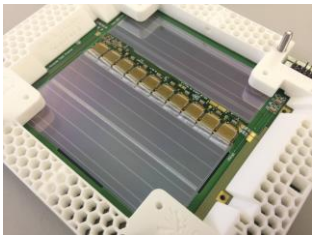
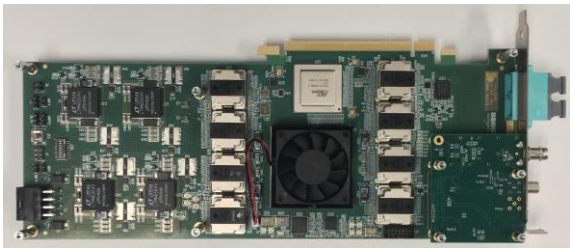


Figure 3: Block diagram of the Prototype DAQ system

Its current prototype hosts ten readout ASIC chips (named as ABC130) and one Hybrid Controller Chip (named as HCC) [8]. Its full chain of the prototype readout system mainly includes a strip hybrid module, a GBTx (GigaBit Transceivers) board and the FELIX system, as shown in the Figure 3. Each ABC130 chip processes analog signals from 256 silicon strips, and employs the binary readout architecture. The analog part includes charge integration, pulse shaping and amplitude discrimination. The ABC130 implements multiple-trigger data flow: first level trigger for data buffering and a second level asynchronous trigger for data readout. It also has an internal injection circuit connected to each input for calibration purpose. As for the HCC chip, it provides a high impedance drop point for the control and clock lines shared by all ABC130 chips along the strip stave. And it also gathers serialized detector data from ABC130 chips, and drives a point-to-point connection to the GBTx board. The GBTx board has a radiation hard GBTx ASIC functions as an interface between front-end electronics and optical links [9]. In the ATLAS Phase II Upgrade, a new version of lpGBT ASIC will be used which was not released when this prototype DAQ system was developed.



(a) Strip hybrid module



(b) FELIX hardware for ATLAS Phase I Upgrade

Figure 4: Hardware components in the integration

FELIX is the core of the new Trigger/DAQ architecture in the ATLAS upgrade [10]. It provides bi-directional optical data transmission including downstream slow control path and upstream detector data path. The FELIX hardware is shown in the Figure 4b [11]. It is equipped with one 16-lane PCIe Gen3 interface and eight onboard MiniPODs [12]. Each MiniPOD has 12 links connected to FPGA (Field Programmable Gate Array) transceivers, providing 48 bi-directional optical links in total [13].

4 Firmware

In the current phase, the FELIX firmware is being developed mainly for the ATLAS Phase I Upgrade, which had a successful Pre-production Readiness Review in August 2019. Its main functional blocks includes GBT Wrapper, Central Router, and PCIe DMA engine. The GBT

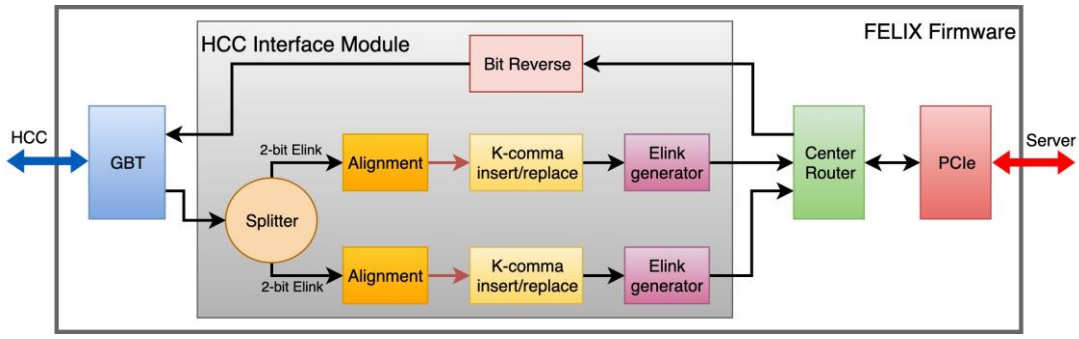


Figure 5: Block diagram of HCC interface firmware

wrapper supports radiation hard GBT (GigaBit Transceiver) protocol with a line rate of 4.8 Gb/s with FEC (Forward Error Correction) encoding [14] [15]. The Central Router processes and routes data streams between GBT wrapper and PCIe DMA engine. The FELIX firmware supports two interface protocols: direct mode and 8b10b mode. In the direct mode, zeros are presented in the idle state. And in the 8b10b mode, literally the data streams are 8b10b encoded. Since HCC ASIC on the strip hybrid module has an unique communication protocol for both data path and command path, an specific interface module should be developed inside the FELIX firmware for encoding and decoding the HCC protocol, as shown in the Figure 5. The HCC ASIC has two input signals besides the reference clock: L0_CMD and R3_L1. The L0_CMD line is composed of two 40 Mbps time-multiplexed independent data streams: The level-0 trigger signal (active high) and the command input (active low). The R3_L1 line is composed of the regional readout request signal and the level-1 trigger. In this way, when HCC chip is in idle state, a 40 MHz clock train is seen on both of the L0_CMD line and R3_L1 line. In order to be compatible with the HCC input protocol, one bit of the 2-bit Elink data is inverted for command path in the FELIX firmware as shown in the Figure 6 [16]. As for the HCC output data, it has two 8b10b encoded data streams interleaved bit by bit. The FELIX firmware should swap the middle two bits in the 4-bit Elink data, which is also shown in the Figure 6. In this case, the 4-bit Elink data will be separated into two 2-bit Elinks, each one is a valid 8b10b encoded data stream. Then the 2-bit Elink data stream should be aligned, and their control commas should be replaced as well. With this specific encoder/decoder firmware module, the FELIX hardware can communicate properly with the strip hybrid module.

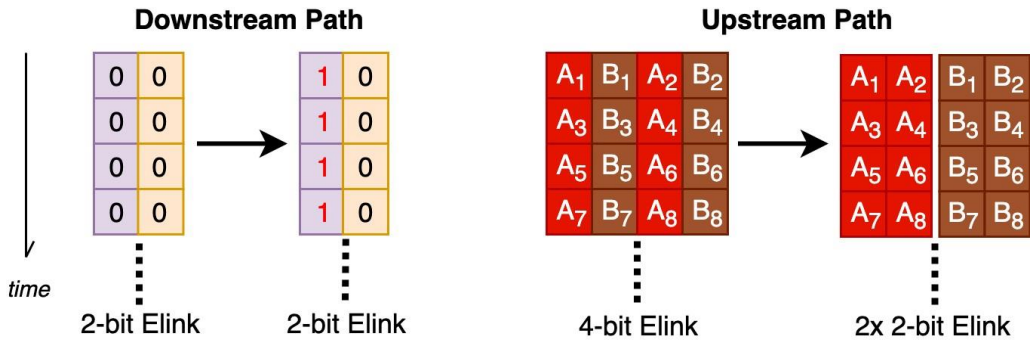


Figure 6: Bit Processing for HCC protocol in FELIX Firmware

5 Software

In the Prototype DAQ system, we also developed a Python GUI application based on PyQt library[17]. It can issue trigger and control commands, and carry out injection and calibration tests. The software will call FELIX low-level tools to send and receive data through the PCIe interface. As shown in the Figure 7, its first page is for HCC and ABC130 basic operations like initial configuration and register read/write communication. The second page is mainly for different types of injection tests, including strobe delay scan, three point-gain test, and channel calibration test. The software will store and analyze received ABC130 and HCC data in the local server. And the test status will be reported in the log window of the GUI application.

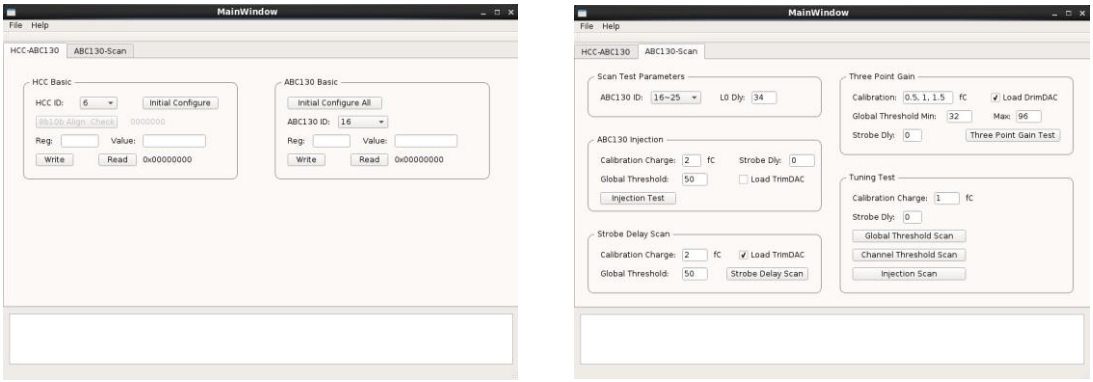


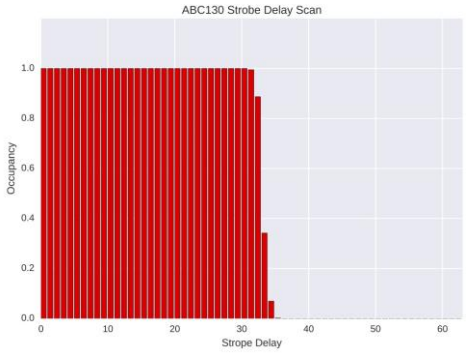
Figure 7: GUI software for system integration test

6 Integration Results

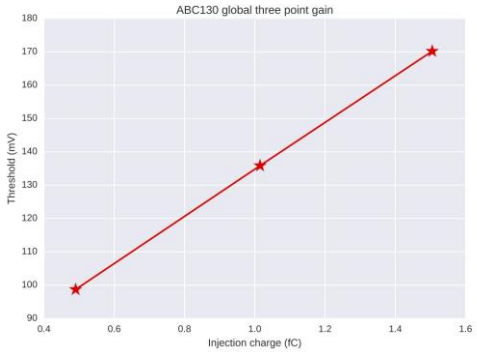
We have performed several types of integration tests besides the fundamental register read/write tests. The ABC130 ASIC implements injection circuits for the calibration purpose. The charge range of injection signal is 0-9 fC with step size of 0.035 fC. A tunable delay of the injection signal with respect to the clock phase can be configured via a specific 6-bit register (named as strobe_delay) to guarantee a good timing relationship between the injection signal and the level-0 trigger. This strobe delay range covers at least two clock periods (25 ns). With different strobe

delay value, the occupy test results is shown in the Figure 8a. Another useful test is three-point gain test which injects three different input signals for all 256 channels. The distributions of gain and offset in 256 channels can be acquired.

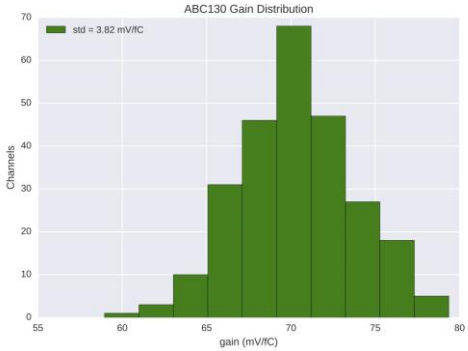
Since each analog channel of ABC130 has an independent amplification stage followed by a discriminator with an adjustable threshold. The calibration test should be carried out to eliminate the threshold variance between different channels. The test procedure includes global threshold scan and channel threshold scan with binary search. The global threshold scan is to adjust the 8-bit global threshold to have average channel occupancy of 50%. And the channel threshold scan is to adjust the local 5-bit channel threshold to have all channels occupancy of 50%. The tuning results of threshold distribution is showed in Figure 9. The effective threshold deviation after tuning is improved from 0.163 fC to 0.038 fC. These test results show the capability of the FELIX based readout system for silicon sensor test and calibration.



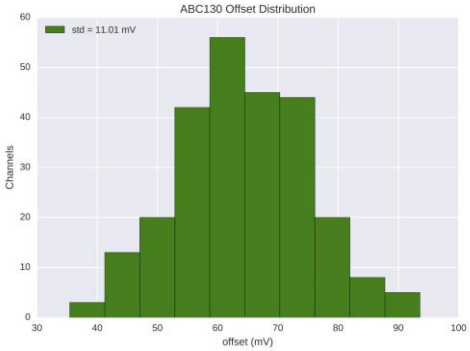
(a) Strobe delay scan



(b) Three-point gain



(c) Gain distribution



(d) Offset distribution

Figure 8: Test results of strobe delay scan and three-point gain test

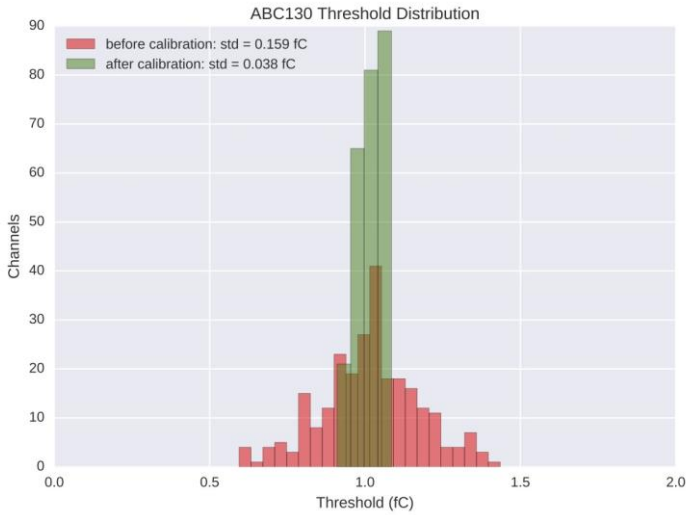


Figure 9: Threshold Distribution before and after calibration

7 Conclusion

A prototype of readout system has been developed for Strip Track demonstrator in ATLAS Phase II Upgrade. A specific interface firmware has been designed and implemented inside FELIX, as well as a user-friendly GUI application. The readout system can communicate properly with the HCC and ABC130 front-end electronics on the strip hybrid module. Several commissioning tests have been carried out successfully, like strobe delay scan, three-point gain test and calibration test. These test results prove the feasibility of the integration between ITk Strip Detector and FELIX DAQ system in ATLAS Phase II Upgrade.

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