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DFF Layout Variations in CMOS SOI – Analysis of Hardening by Design Options

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***Abstract*— Four D Flip-Flop (DFF) layouts were created from the same schematic in Sandia National Laboratories' CMOS7 Silicon-on-Insulator (SOI) process. Single Event Upset (SEU) modeling and testing showed improved response with the use of a shallow (not fully bottomed) N-type Metal-Oxide-Semiconductor Field Effect Transistors (NMOSFETs), extending the size of the drain implant, and increasing the critical charge of the transmission gates in the circuit design and layout. This research also shows the importance of correctly modeling nodal capacitance, which is a major factor of upset critical charge. Accurate SEU models enables the understanding of the SEU vulnerabilities and how to make the design more robust.**

***Index Terms*— Single-Event Upset, Transmission Gates, Sequential Circuits, Radiation Hardening by Design**

I. Introduction

A goal of radiation hardening by design (RHBD) for single event upset (SEU) is to deliver the lowest soft error rate (SER) with the least impact on speed, size, and power. In fact, one may want to meet the SER requirement with some margin, while providing the best overall circuit performance. Some RHBD design techniques come with hefty speed, size, and/or power penalties, but some techniques impose only small (or no) penalties [1]. This paper examines several layout options that are available in Sandia National Laboratories' CMOS7 process and their respective impacts on SER. The layout variations are based upon what a layout engineer can do within the constraints of the process, while maintaining a compact layout.

The soft error rate for a sequential circuit depends on many factors. However, comparing two different layouts of the same basic circuit design can be done by examining the cross-section versus linear energy transfer (LET) curves. The layout with the higher single event upset (SEU) LET threshold and lower SEU cross-section per flip flop will produce a lower soft error rate.

This paper presents a SEU analysis of four different layouts of the same D flip-flop (DFF) circuit. All layouts use the exact same transistor level schematic. We present the distinguishing characteristics of the layouts, Technology Computer Aided Design (TCAD) simulations, heavy ion test data, and a discussion of the results based on Monte Carlo Radiative Energy Deposition (MRED) simulations [2][3].

II. CMOS7 DFF Design and Layout Variations

A. CMOS7 Process and Transistor Layouts

Sandia National Laboratories' CMOS7 microelectronics fabrication process is 0.35μm Silicon-on-Insulator (SOI) technology. The Si thickness is 250 nm and the buried oxide thickness in 200 nm. There are five aluminum metal layers for circuit routing.

There are a couple different transistor layouts available, differing usage of the body tie. The primary N-type Metal-Oxide-Semiconductor Field Effect Transistor (NMOSFET) is called a Body Under Source FET (BUSFET) [4]. The primary P-type MOSFET (PMOSFET) is called a Body Tied to Source FET (BTSFET). A top view of both transistors is shown in Fig. 1. The body and source implants abut, the top is silicided, and they share a common contact. The body source contact is typically connected to power or ground rails in the layout. The only different between the BUSFET and the BTSFET is the depth on the source implant. The N+ source in the BUSFET is not fully bottomed to the buried oxide or is a shallow implant. The P+ source implant in the BTSFET is fully bottomed or is a deep implant. Circuit design or layout personnel have the option of shallow and deep N+ implants, but P+ implants are always deep. One final note about Fig. 1 is that the source/drain implants do not extend out to the sidewall oxide in this

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experiment, so a body region surrounds all the source/drain implants.

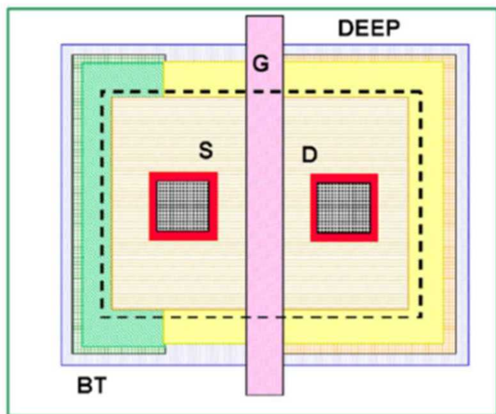

Fig. 1. Top view of the BUSFET and BTSFET showing the abutted body tie (BT) and source (S). For the N-type BUSFET the source implant is not fully bottomed (shallow) and for the P-type BTSFET the source implant is fully bottomed (deep).

The second layout variation for NMOSFETs and PMOSFETs is shown in Fig. 2. This is the isolation FET (IFET). In this layout, the source and body are isolated from each other, so they can be at different potentials. The isolation gate is biased the same as the body, keeping the Si under the isolation gate in depletion. The IFETs are used for transmission gates in designs, which are used in latches and memory in circuit design. The source and drain can switch in the IFET. The layout of the IFET is bigger than the BUSFET/BTSFET and the body resistance from the gate to the body tie is higher. The N+ source and drain implants can be shallow or deep, while the P+ source and drain implants are always deep.

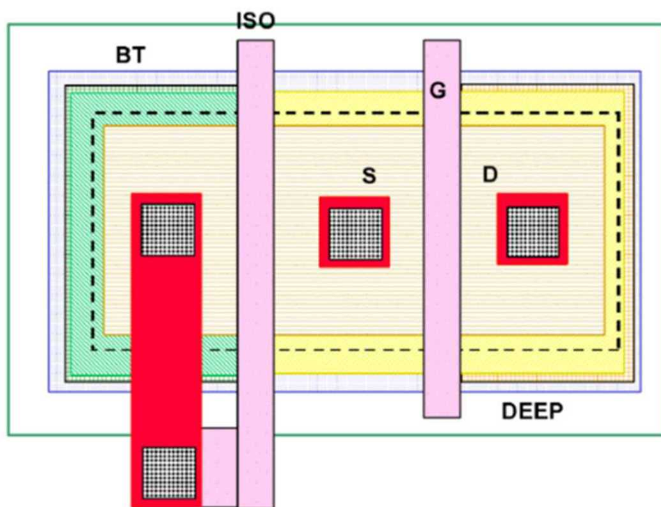

Fig. 2. Top view of the IFET showing the isolated BT. For the N-type IFET the source implant is shallow and for the P-type IFET the source implant is deep.

B. D Flip-Flop (DFF) Circuit Design

The DFF circuit design used in this research is shown in Fig. 3. This is a master-slave design using transmission gates and has an asynchronous reset input. The clock distribution to the transmission gates is not shown in the figure to maintain simplicity, but it is noted that no single event transients latched errors has been recorded in this technology, so the transistors in the clock path are not relevant for SEU analysis. All of the PMOSFETS in the design have gate width (W) of 3.2 μm and gate length (L) of 0.45 μm. The NMOSFETs in the design are all W of 1.6 μm and L of 0.35 μm except for the NMOSFETs in the NAND gates. The NAND gate NMOSFETs have the W doubled to 3.2 μm.

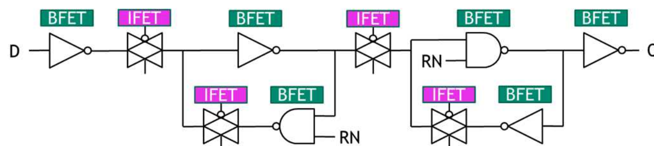

Fig. 3. Schematic of the DFF circuit used in this research. BFET refers to BUSFET or BTSFET transistor implementation and IFET refers to the isolated FET implementation. PMOSFET transistor W/L is 3.2 μm/0.45 μm. NMOSFET W/L is 1.6 μm/0.35 μm, except in the NAND gate where W is 3.2 μm.

The transistor types under is each part of the circuit is identified in Fig. 3. BFET indicates the used of the BUSFET or BTSFET. In the NAND gate, a PMOSFET drain was shared between two BTSFETs in the same Si island and the two series NMOSFETs shared the same Si island.

The DFFs were tiled into two identical 1 kbit shift register chains. The clock and reset lines were distributed in a tree like fashion to all DFFs. SEU testing was conducted clocking an alternating data input at 1 MHz, which maximally exercises all the transistors in the DFF for upset. SEU static simulation must multiply the resulting cross-section or SER by 0.25, 0.5 to account for upsets in either the master or slave stage and 0.5 for the stage state being a high or a low.

C. DFF Layout Variations

For this paper, the focus is on four layout variations of the DFF circuit design. There are two variations of layout topology and two variations of N+ implant depth. The two layout topologies are shown in Fig. 4. The top layout is referred to as standard and uses the minimum design rules for each transistor, which would create the smallest layout area. It is noted that each logic circuit shown in Fig. 3 is independent in this layout, i.e. their Si islands are distinct. The transmission gates could easily be combined with inverter gates to make a more compact layout, but this experiment kept them separate. The bottom layout is like the top except that the drain area is increased three times by extending it away from the gate. This provides a bigger layout area for the DFF but also a bigger target for radiative particles.

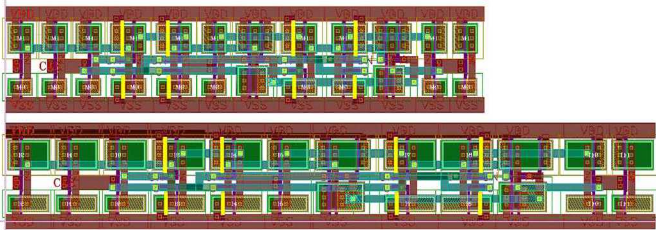

Fig. 4. Top view of the two layout topologies used in this research. The top layout uses the minimum design rules to compact the layout and is called standard. The bottom layout expanded the drain area by a factor of three and is called extended drain.

The next layout variation applied was changing the N+ implant depth. The standard layout makes all the NMOSFET drains deep or fully bottomed. The shallow layouts keep all of the NMOSFET drains shallow, no N+ implant reaches the buried oxide. The two layout topologies and two N+ implant depth variations were used to create four DFFs. Table I shows the variations and names each DFF layout.

TABLE I
DFF LAYOUT VARIATION EXPERIMENTS

Experiment	Layout Topology	NMOSFET Variation
Baseline	Standard	Standard
Shallow	Standard	Shallow
Extended Drain	Extended Drain	Standard
Extended Shallow	Extended Drain	Shallow

III. TCAD SIMULATION RESULTS

The TCAD campaign performed on the NMOSFET is summarized in Fig. 5, which shows the device layout with the simulated ion event locations. The ion events were all normally incident with approximate LETs of 12.5, 25, and 50 MeV-cm^2/mg at each location. The 3D TCAD was performed using Silvaco Atlas in mixed-mode with the TCAD transistor configured OFF connected to an ON transistor in an inverter circuit configuration [5]. Fig. 6 shows a set of drain current responses along the x-axis for the BUSFET (Fig. 5). This shows the highest charge collection is at the drain-gate boundary and decreases as the events go into the drain and into the gate, as expected. Ion events in the deep drain and in the body around the deep drain (not under the gate) do not result in significant charge collection. The BTSFET had similar simulation results.

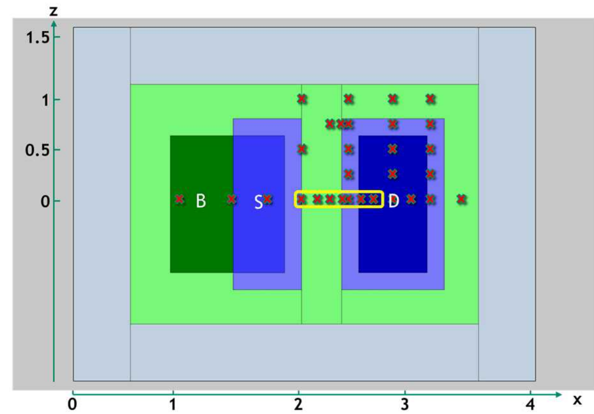

Fig. 5. Top view of NMOSFET layout. P regions are shown in green and N regions are shown in blue. Red Xs show normally incident ion event locations used in TCAD simulations.

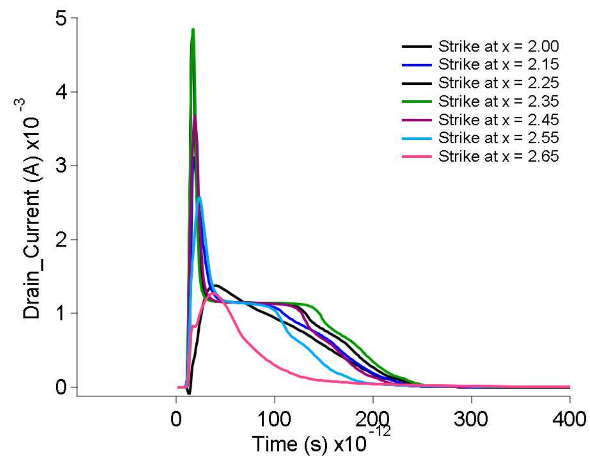

Fig. 6. Drain current results from BUSFET TCAD SEU strikes (LET ~50 MeV-cm^2/mg), along x-axis, z=0, where x=2.35µm is gate-drain boundary. Highlighted by yellow box on Fig. 5.

TCAD simulations were also performed on the other transistor types used in this research. Simulations with the shallow BUSFET transistor did result in significant change. Charge collection is still the highest at the gate-drain boundary and decreases as the events go into the drain and into the gate. However, relevant charge collection extends all the way through the drain implant. As a result, simulated MRED charge collection volumes will be larger for the shallow BUSFET.

TCAD simulations with the extended drain BUSFET/BTSFET transistors resulted in no apparent change in the drain current in the gate-drain region. The charge collected in the deep drain and body around the drain were lower. Since those were already not included in the sensitive volumes, the extended drain sensitive volumes will match the ones with no extended drain.

The last set of TCAD simulations was performed on the IFET devices. The results generally matched the BUSFET/BTSFET results, except that the charge collection was larger due to increased bipolar gain. A combined plot of the drain current for NMOSFET TCAD simulations is shown in Fig. 7. The figure shows the drain currents from ion strikes at the gate-drain

boundary for the baseline, extended drain, shallow, and IFET NMOSFETs and in the center of the drain for the baseline, extended drain, and shallow NMOSFETs.

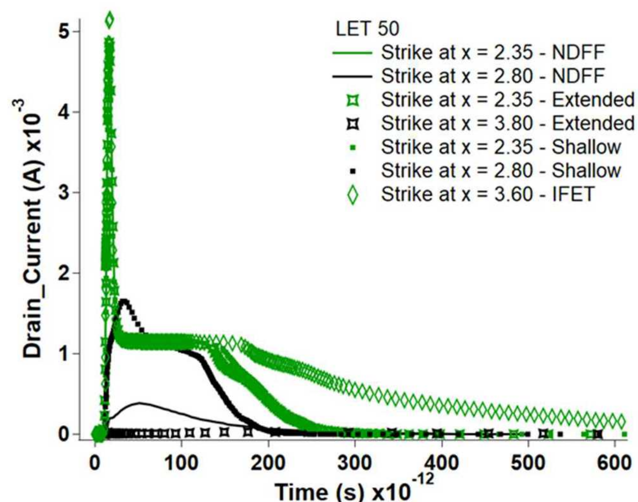

Fig. 7. Drain current results from baseline, extended drain, shallow, and isolation NMOSFET TCAD SEU strikes (LET ~50 MeV-cm^2/mg), along x-axis, z=0. x=2.35µm is the gate-drain boundary for the baseline, extended, and shallow TCAD simulations and x=3.60µm is the gate-drain boundary for the IFET. The other strikes shown are in the center of the drain implant.

A plot of the integrated charge collection for the same simulations is given in Fig. 8. This also shows the deposited charge of 125 fC. The charge collection in the drain is low for all cases but the shallow NMOSFET. The ion strikes at the gate-drain boundary are all similar in charge collection except for the IFET, which has a much large bipolar gain due to the increased body resistance in that layout.

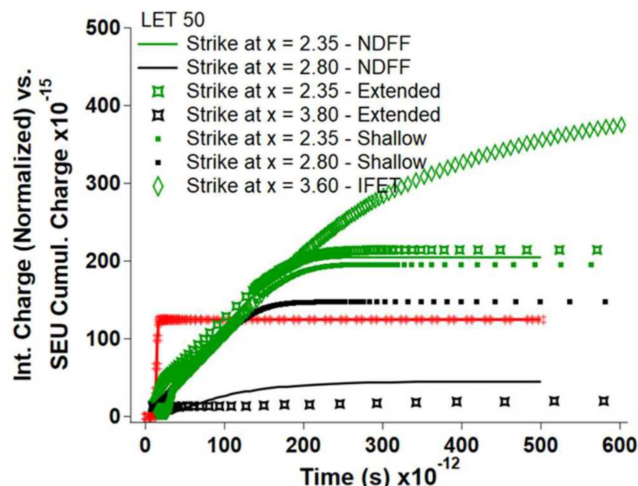

Fig. 8. Integrated charge collection of the drain current curves shown in Fig. 7. The red line shows the deposited charge which is 125 fC.

IV. Heavy Ion Experiment Results

Each DFF layout variant was tiled into two 1-kbit shift registers. Two test chips were created from these shift registers. The first test chip had the baseline, extended drain, and extended shallow shift registers. The second test chip had the baseline and the shallow shift registers. Both test chips had the baseline design to compare the data sets to ensure that the experiments received comparable beams.

An alternating stream of 1s and 0s was input to the shift register, changing every clock cycle. The shift register was clocked at 1 MHz during the exposure. The test was performed dynamically so that we could accumulate large numbers of upsets in the testing. No clock dependency of SEUs has been observed in this semiconductor process, so the results are reflective of a static test. The SEU responses of these layouts are similar in cross-section, so the collection of many SEUs allows us to distinguish between them.

Five different ions (Cu, Kr, Ag, Pr, and Ta) and four incident angles (0°, 30°, 38°, and 45°) were used. The characteristics of the normally incident particles is provided in Table II. Tested beam fluences were either 1x10^9 ions/cm^2 or whatever produced 1000 SEUs in each shift register.

TABLE II
Incident Particle Characteristic in SEU Experiment

Ion	LET at Si, MeV-cm^2/mg	Energy at Si, MeV
Cu	20.9	689
Kr	29.5	896
Ag	44.4	1083
Pr	60.8	1351
Ta	79.7	1702

A log-linear plot of individual DFF cross-section versus LET is shown in Fig. 9. The onset LET increases in the order of (1) baseline, (2) shallow, (3) extended drain, to the (4) extended shallow. This is reasonable, as making the drain bigger or using a shallow implant increases the drain capacitance, increasing the upset critical charge. The cross-section for every data point also varies in the same order as the onset LET, which was not expected. The shallow drain region should add to the cross-section, while the deep drains do not, resulting in the shallow drain layouts having a higher cross-section at the higher LETs. When plotted on a linear-linear scale, the cross-sections of these layouts continue to diverge with a stable slope at high LETs, as shown in Fig. 10.

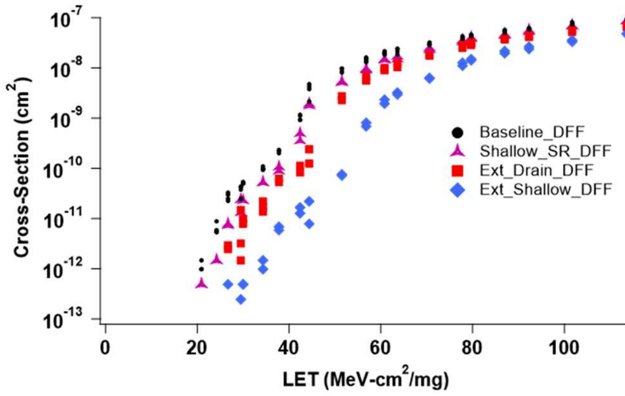

Fig. 9. Log-linear plot of Texas A&M University cyclotron data for the four DFF layouts; baseline, shallow, extended drain, and extended shallow.

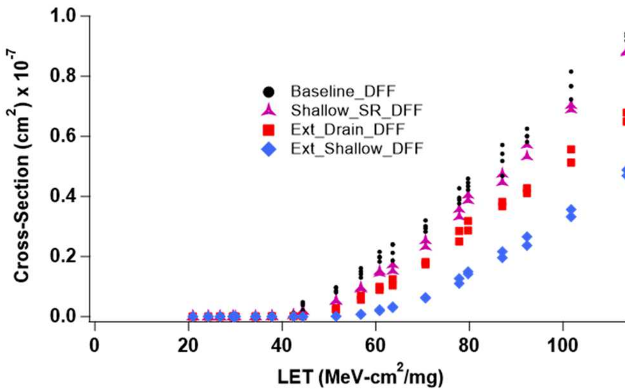

Fig. 10. Linear-linear plot of Texas A&M University cyclotron data for the four DFF layouts; baseline, shallow, extended drain, and extended shallow.

V. MRED Modeling

The goal of using modeling and simulation in the MRED tool for this research is to understand why shallow DFFs do not have a higher cross-section with the upper LET test results. TCAD modeling showed a potentially larger cross-section in all the NMOSFETs due to the charge collection in the drain implant. As a result, the MRED modeling only focusses on the direct ionization charge collection results in the test data. The LET where direct ionization SEUs dominate the results is seen in Fig. 9, where the SEU curves look like log-normal or Weibull distributions. This is approximately LET > 40 MeV-cm^2/mg for the baseline, shallow, and extended drain DFFs and approximately LET > 50 MeV-cm^2/mg for the extended shallow DFF. Upsets output of the MRED scripts below those levels are the result of direct ionization plus a rare indirect ionization event, which is reported by the tool. To calibrate to the SEU data where rare events occur, the MRED model would need to implement the back end of line (BEOL) materials accurately.

Since the calibration was in the direct ionization region, the MRED target material was defined as a 40 µm x 40 µm x 25 µm Si block. The sensitive volumes were set in the middle of the block. The sensitive volumes were developed from the TCAD simulations and three different sets of volumes were defined: deep NMOSFET, shallow NMOSFET, and deep PMOSFET. Note that the extended shallow NMOSFET was larger than the shallow NMOSFET, but the approach used to define them was the same. The IFET were the same set of sensitive volumes as above, but the charge collection efficiencies were increased to match the TCAD data. A couple examples of the top view of the MRED sensitive volumes is shown in Fig. 11. This illustrates the relative cross-section difference between the two transistors.

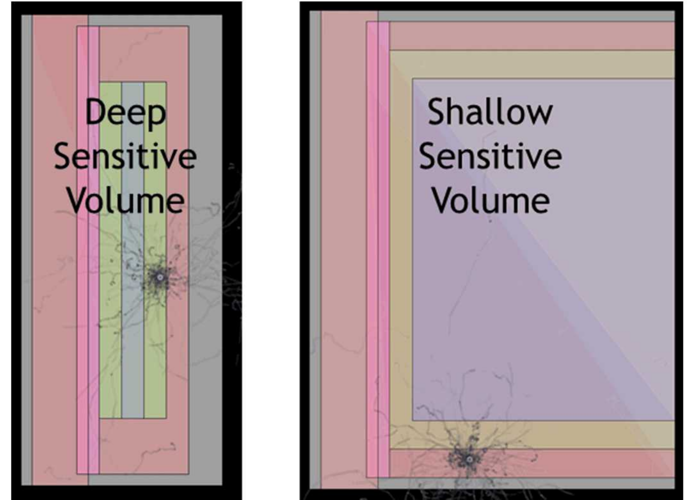

Fig. 11. Top view of MRED sensitive volumes for the deep PMOSFET and NMOSFET and the shallow NMOSFET.

The key challenge to the MRED calibration was getting the critical charge for upsets at each circuit node in the DFF variations accurate. Fig. 12 shows 2D cut planes from the TCAD simulations for the deep and shallow NMOSFETs. The drain-body junction capacitance is the main difference between these two layouts and will be the impact to critical charge. The deep NMOSFET has a perimeter-based capacitor and should be calculated as such. The shallow NMOSFET has both a perimeter-based capacitor and an area-based capacitor and should be calculated as the sum of both terms. The only data point to use for the capacitance comes from the process design guide and gives 1.6 fF/µm^2 for the shallow NMOSFET capacitance. From this starting point, the remaining terms were estimated:

- Deep PMOSFET junction capacitance – 0.32 fF/µm
- Deep NMOSFET junction capacitance – 0.24 fF/µm
- Shallow NMOSFET junction capacitance – 0.06 fF/µm plus 0.8 fF/µm^2.

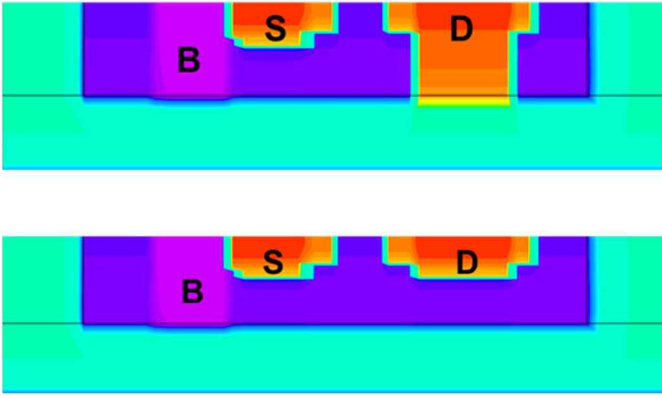

Fig. 12. Top view of MRED sensitive volumes for the deep PMOSFET and NMOSFET and the shallow NMOSFET.

MRED simulations were executed for all four DFFs with the ions, energies, and angles from the SEU testing. The rare event bias in the sampling was set to 200 times. The critical charge for each transistor in the DFF circuit was determined in advance using the dual double-exponential current source technique [7]. Each DFF had a difference set of nodal capacitances added from the estimates above. The nodal capacitances continually increased from the baseline to the shallow to the extended drain and finally to the extended shallow, which is consistent with the SEU date (Fig. 9 and Fig. 10). The simulation results for cross-section versus effective LET is given in Fig. 13. This is a good match of the SEU data generally showing the same overall response. However, at the upper LETs, the model does show the shallow drains to have a higher cross-section, which does not agree with the data.

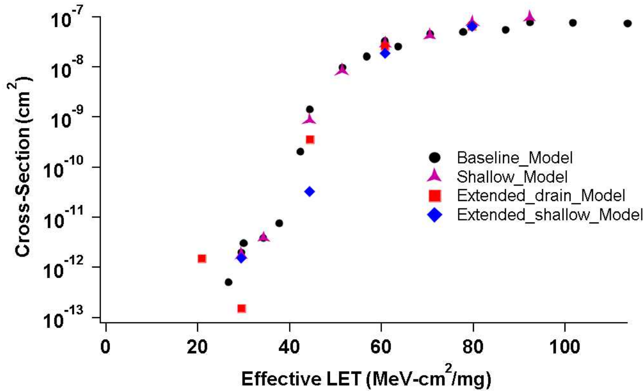

Fig. 13. MRED SEU simulation results.

VI. Hardened By Design Implications

The original assumption from the use of the shallow drains in the circuit design and layout was that it would add nodal capacitance to increase the critical charge (onset LET), but that it would also have a higher cross-section. SEU test data and MRED simulations showed that not to be the case. Instead, the increase in the shallow sensitive volume cross-section is offset by the increase in node capacitance and the reduced bipolar gain in the shallow drain. Another way to look at this is to examine the cross-section versus effective LET for NMOSFET and PMOSFET hits. These are given in Fig. 14 and Fig. 15. The model shows the PMOSFET hits do follow the trend of the SEU data, but the NMOSFET hits show a higher cross-section at the upper LETs.

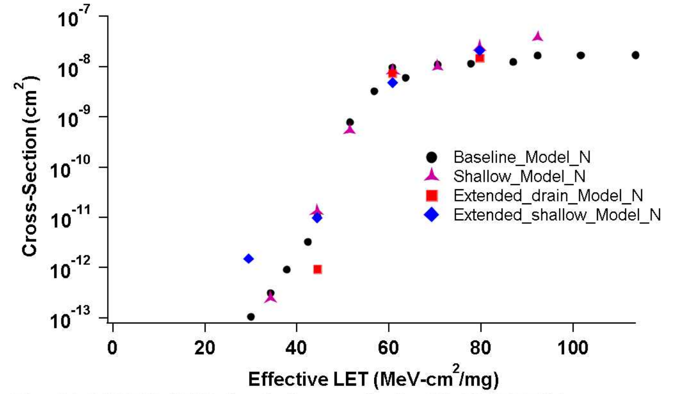

Fig. 14. MRED SEU simulation results for NMOSFET hits.

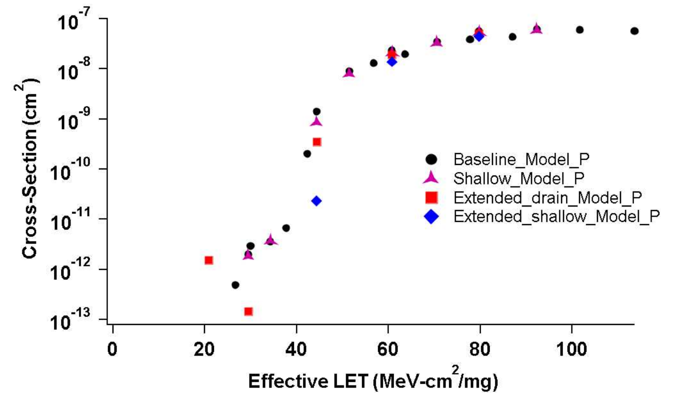

Fig. 15. MRED SEU simulation results for PMOSFET hits.

A second hardened by design (HBD) finding is that increasing the size of the drain may not negatively affect SEU performance. In the experiments in this research, this had a positive effect on SEU performance, but this may not be the general case. If a design needed a little more SEU hardness, extending the size of the drain is an option to add more capacitance. In some layouts, the size penalty of this may be minimal if there is space already available. This is often the case as it is difficult to maximally use layout area.

The IFET outputs in Fig. 3 were the primary contributor to the SEU hardness in these DFFs. One reason for this is the increased bipolar gain of these transistors and there is no way to make the body tie closer or less resistive in this technology. But, the second reason is that these nodes also had the lower critical charge. So, there was a need to increase the SEU hardness of a DFF, the solution might just be increasing the hardness of ion strikes to those nodes.

The last HBD implication to be considered in the size and speed penalties of the layout techniques. Implementing a shallow versus deep NMOSFET drain cost no size penalty. Extending the drain by three times, as shown in Fig. 4, caused a 36% increase in area. However, this could be lowered if applied more optimally, i.e. at the softest circuit nodes. For speed penalties, clock-to-Q simulations were performed with typical transistor parameters. Clock-to-Q times were 398 ps for baseline, 407 ps for shallow, 408 ps for extended drain, and 435

ps for extended shallow. These are not large timing penalties but increasing the node capacitance does slow down the circuit.

VII. Conclusions

Comprehensive testing and modeling of circuit design and layout variations may result in developing new single event effect HBD strategies. In the case of CMOS7, the upset rate of DFFs can be reduced by:

- Using shallow NMOSFET drains
- Extending the size of the drain implant
- Increasing the critical charge of the transmission gates (IFETs).

All these changes come with little or no HBD penalties.

Accurately modeling the capacitance and sensitive volume size and efficiencies is important to the understanding of the single event hardness. While the resulting MRED simulation in this study did not exactly match the SEU data, the simulations gave great insight into the DFF layout variations. It is also important that TCAD and SPICE have the same accurate capacitance values.

The last conclusion of this research is one that was noted in its performance. A lot of time and effort was spent trying to calibrate the model to the lower LET region where the indirect ionization effects dominated. Only when it was recognized that these were the result of rare events and that the BEOL materials needed to be included, did the focus turn to calibrate the direct ionization region. The MRED tool outputs provides information on the types of events that cause the SEUs and this is valuable to focus on the model.

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