Development and Validation of a SiC based 50-kW Grid-Connected PV Inverter

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***Abstract*— The future power grid will involve increasing number of power converters while growing the complexity of the power systems. The future of the power converters is driven by the developments in the wide bandgap semiconductor devices. In this paper, a 50 kW string PV inverter designed and developed using all SiC semiconductor devices is presented. The inverter design includes additively manufactured power block, symmetrical Y-core inductors for ac side filter, and advanced inverter controls for grid support functionality. This inverter utilizes the conventional three-phase voltage source inverter topology and optimizes the design for SiC based devices. The paper includes details on power module design, heatsink optimization, symmetrical Y-core filter inductor design, inverter thermal design, and further experimental validation of the inverter performance. In addition to the quantification of inverter efficiency and quality of the output, the paper also presents the validation of advance grid-support functions required by the IEEE 1547 standards for interconnection of distributed energy resources.**

Keywords—advanced grid-support functions, inverter validation, PV inverter, SiC inverter

I. INTRODUCTION

Successful integration of hundreds of gigawatts of solar photovoltaics (PV) into the electric power system requires transformative power conversion system designs that optimize various trade-offs in conflicting objectives such as performance, reliability, functionality and cost. The future of the power converters (including PV) will be driven by the advancements in the wide bandgap semiconductor devices [1]. These devices can provide very high switching speeds, lower switching losses, and can reduce the size of the associated filter [2]. Although, in the current market these devices are more expensive than Silicon devices with similar ratings, recent studies have shown that the economic parameter (cost/power) for wideband gap devices will approach that of Si devices in the next decade as the cost reductions are accelerating [3]. The use of SiC provides advantages of high switching speeds, high power density, high temperature operation, and lower system losses. Even though SiC device based PV inverters are being designed and many technical challenges associated with them are being solved, a commercial scale single-stage, two-level PV inverter operating at high dc-bus voltage with all grid-support functionalities has still not been developed [4]. Furthermore, most of the SiC based PV inverters demonstrated are developed using commercial power modules [4] – [6] . These power modules are not optimized to achieve the efficiency and power density target metrics defined by the US Department of Energy's Sunshot program [7]. The high switching speeds realized by the SiC devices enable the reduction in size of the ac-filter. Most SiC based inverters developed use the traditional E-I core or U-I core based inductors which result in asymmetrical flux distribution for the three phases [8], [9]. Furthermore, a PV inverter with advanced controller which enables the grid-support functions as required by the IEEE 1547 standards for interconnection of distributed energy resources (DERs), has not been developed and presented.

In this paper, a three-phase 50kW, 480V SiC based single-stage two-level PV inverter is presented and validated. This paper elaborates on different parts of the inverter that have been optimized to exploit the advantages offered by SiC devices and then presents the results showing optimal performance of the developed inverter. The development and evaluation of different parts of the inverter is presented in Section II. This includes development of the power modules and heatsink, the symmetrical Y-core filter inductors, the controller and the control algorithms, and the inverter thermal design. The validation of the developed inverter is presented in Section III through experimental results, quantifying the efficiency, output quality, and controller performance. The conclusions and main developments are summarized in Section IV.

II. DEVELEOPED INVERTER

In this section, the different parts of the developed PV inverter are discussed. The developed three phase 50kW PV inverter utilizes SiC MOSFETS and diodes as the semiconductor devices in the power block, has new

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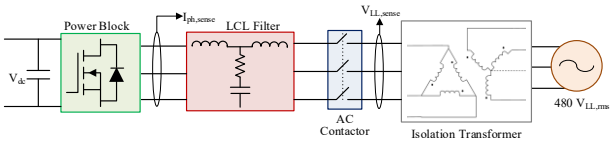


Fig. 1. Electrical schematic of the developed three-phase 50kW, 480V inverter prototype setup.

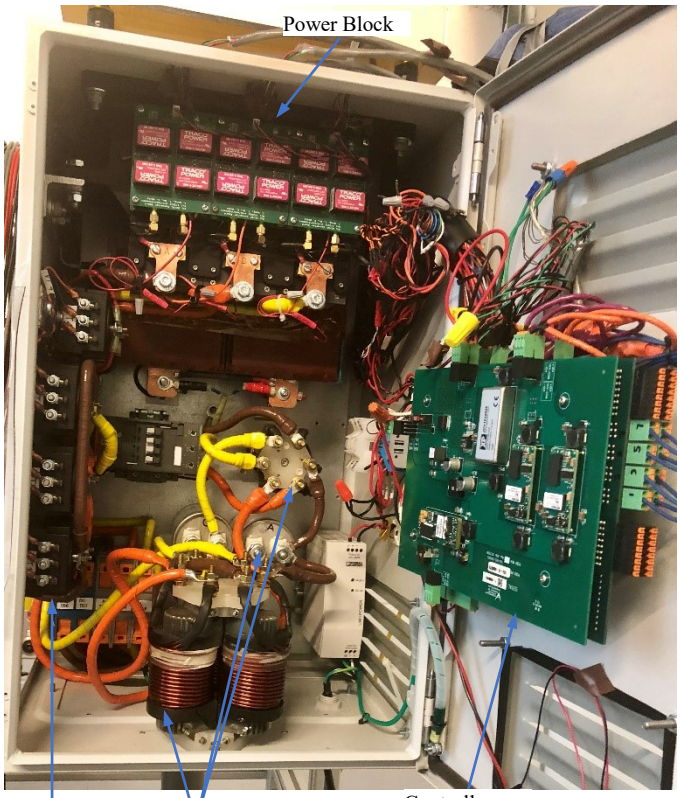


Fig. 2. Inside view of the developed three-phase, 50 kW, 480 $V_{LL,rms}$ SiC based inverter prototype.

symmetrical Y-core inductors in the ac filter, and has a controller with advanced inverter functions for grid support functionality. The electrical schematic of the setup and the inside view of the developed inverter prototype is shown in Fig. 1 and Fig. 2, respectively. In the next subsection, the development and evaluation of the power modules is presented.

A. 1.7 kV 50 kW PV Inverter Power Block

Half-bridge power semiconductor modules are fabricated for the PV inverter using 1700 V bare die samples of SiC MOSFETs and SiC Schottky diodes. The current ratings of single SiC MOSFET and SiC Schottky diode bare die are around 34 A and 50 A, respectively. Multiple devices are paralleled to achieve the required current rating. The main objective of the module design is to increase the overall heat dissipation area by splitting the phase leg module into two submodules, i.e. a high-side switch module and a low-side switch module which are attached to two separate heatsinks. Each submodule consists of a DBC substrate attached to the

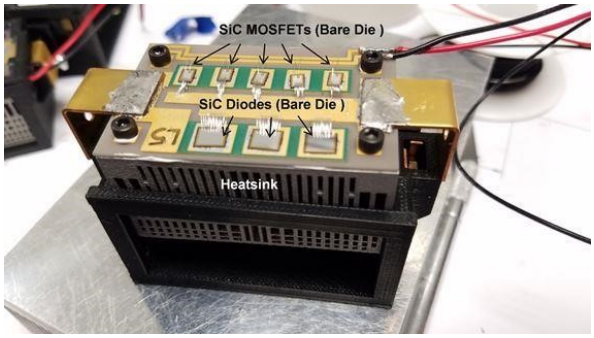


Fig. 3. Power module assembly.

flow channel via thermal interface material. The aluminum flow channel is electrically insulated from the positive and negative DC bus by the aluminum nitride substrate. The high voltage DC bus interconnects the power module from the left side of air flow channel while the gate driver and control interfaces on the right side. A decoupling circuit board, adjacent to the DC buses, is designed to minimize the power loop parasitic inductances and improve switching performance.

In addition, the heatsinks were optimized using Genetic Algorithms, a machine learning algorithm that imitates the natural evolution process proposed in the Darwinian evolutionary theory. While using Genetic Algorithms coded in MATLAB, to generate design chromosomes of heatsink, FEA simulations are used to evaluate the fitness value of each. Following the optimization method, a heatsink model has been generated, and the detailed design and analysis of the heatsink has been previously presented in [10], [11].

The fabricated power module is shown in Fig. 3, where only the low-side switch of the phase leg module is shown. The high-side switch has the same structure, which is reversely stacked on top of low-side switch. The single-phase assembly with the fan is shown in Fig. 4. The volume of this single-phase power block is ~20 in^3 and the total combined volume of the power stage for the three-phase inverter is ~60 in^3. The development of the full power block and its evaluation is presented next.

The power block of the three-phase inverter mainly includes three air-cooled half-bridge power modules, fans, DC-link capacitors, DC bus bars, and gate drivers. The actual hardware prototype of the three-phase inverter is shown in

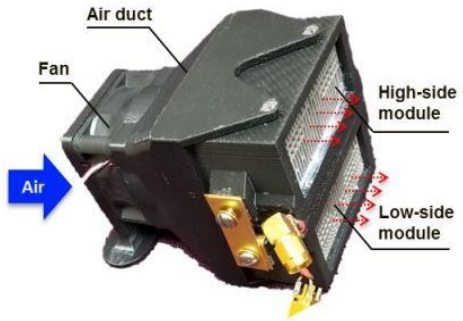


Fig. 4. Single phase block assembly of the power stage.

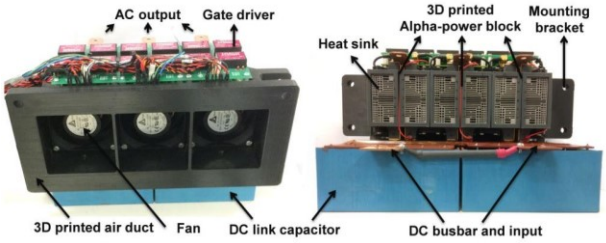


Fig. 5. Hardware prototype of power block based 50 kW three phase inverter: front view (left) and back view (right).

Fig. 5, with an overall volume of ~671 in^3. The power density for a 50-kW operation is 75 W/in^3.

The developed inverter power block was evaluated as individual part before full system validation. Fig. 6 illustrates three-phase AC current when the three-phase inverter operates at 1 kV DC bus voltage and ~ 48 kW output power. The inverter AC output current is close to pure sinusoidal wave, with some switching ripples and minor distortion at zero-crossing point. The switching ripple can be better suppressed with higher filtering inductance and/or higher order harmonic filters in the future grid tied operation. Based on the power analyzer measurement results, the inverter output AC current (I_{rms2}) is around 60 A RMS with a total harmonic distortion of ~2.5%. The inverter line-to-line fundamental RMS voltage is around 460 V (U_{rms4}). However, the overall inverter line-to-line RMS voltage (U_{rms2}) is much higher than the fundamental value because of the high switching ripple and its side-band harmonics. The inverter input and output active power are 48.15 kW and 47. 28 kW respectively, resulting in an efficiency of ~98.2%.

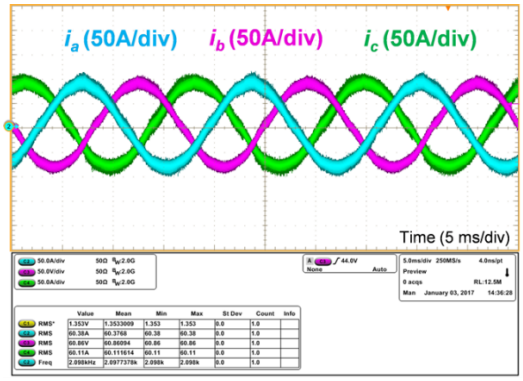
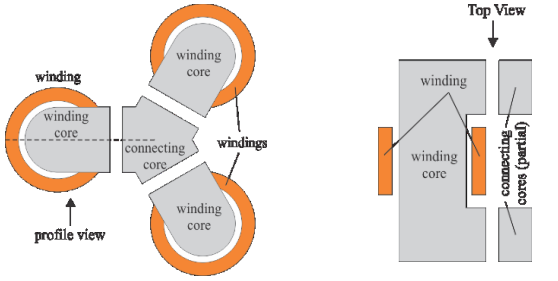


Fig. 6. Three-phase AC current of the three-phase inverter operating at 1 kV DC bus voltage and ~48 kW output power.

The design, development and evaluation of the inverter-side and grid-side inductors of the LCL filter in the inverter is presented in the next sub-section.

B. AC Filter

As can be seen in Fig. 1, an LCL filter is placed between the inverter and utility. Using [12] – [14], desired values of inverter-side inductance, capacitance, and line-side inductance were determined to be 188 µH, 14 µF, and 35 µH, respectively.



(a) Top view (b) Profile view

Fig. 7. Symmetrical Y-core inductor.

A 3-phase symmetrical Y-core inductor topology was used [15]. This arrangement is not subject to the inherent magnetic imbalance of 3-phase E-core inductors. Further, this coupled topology is smaller than using independent phase inductors. The Y-core inductor is compared to other topologies in [16]. Fig. 7 illustrates the magnetic arrangement of the Y-core inductor, with Fig. 7a (left) showing a top view, and Fig. 7b (right) showing a profile view of one of three identical legs in a cross section (see dashed line of Fig. 7a). The windings are wound around winding cores; the flux is combined centrally through top and bottom connecting cores. Air gaps are placed between the winding and connecting cores. In this effort, a high silicon content laminated magnetic steel core is used. A photograph of the two Y-core inductors is given in Fig 8. The first step in the inductor design was to execute a time-domain simulation based on the highest input voltage and full-load conditions. This simulation is used to establish the current spectrum seen in the three phases.

The inductor design was performed using a poly-physics multi-objective optimization in which encapsulating volume and loss are minimized subject to constraints. Constraints include bending radius, packing factor, aspect ratio, mass, current density, inductance, inductance symmetry, peak winding temperature, peak bobbin temperature, and loss. The particular design was chosen from the resulting Pareto-optimal front. A paper fully describing the inductor design process will be forthcoming.

The *q*- and *d*-axis inductances were tested using the procedure described in [16]. Figs. 9 and 10 depict the absolute inductance (flux linkage divided by current) versus current for the two inductors. Therein, the 'target' inductance describes the desired value, and 'DM' denotes prediction by the Design Model [16]. The legends 'DM*0.9' and 'DM*1.1' indicate a deviation of ± 10% from the design model. There is an excellent correspondence between the DM and measured

Fig. 8. Line side (right) and inverter side (left) inductors.

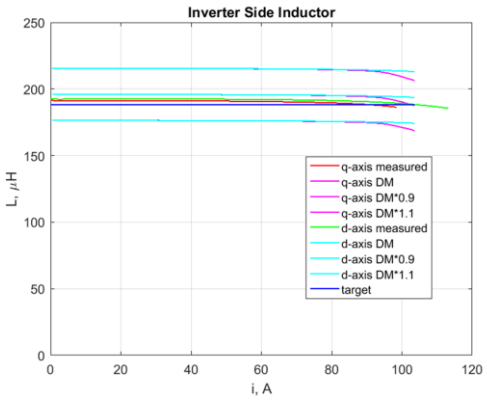


Fig. 9. Inverter-side inductance.

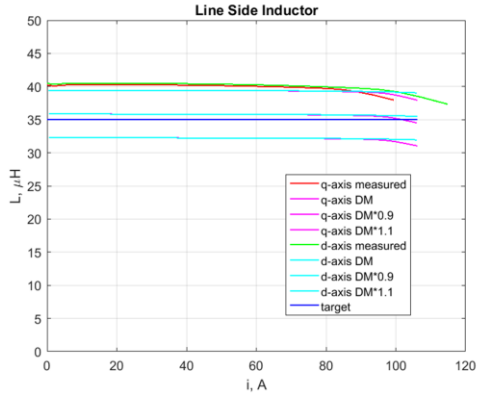


Fig. 10. Line-side inductance.

inductance for the inverter-side inductor; in the case of the line-side inductor the measured inductance is greater than predicted. A possible explanation is that in the physically smaller line-side inductor variances in air gap and leakage paths have a relatively larger impact than in the larger inductor.

C. Controller and Control Algorithm

National Instrument's single-board RIO (SBRIO) with General Purpose Inverter Controller (GPIC) mezzanine card were selected as the primary controller for the inverter prototype. The SBRIO is composed of a Xilinx Zynq-7000, 667 MHz dual-core ARM Cortex-A9 processor, an Artix-7 FPGA, and a mezzanine card connector that is used to connect with GPIC. Furthermore, interface boards were developed to tap the FPGA output directly, in order to implement high switching frequencies enabled by the SiC devices. Based on the transient-domain inverter model and the current control, advanced inverter control functions including Volt-VAR (VVAR), Volt-Watt (VWATT), and Frequency-Watt (FWATT) are developed and implemented. The developed control algorithms were validated using a developed controller hardware-in-the-loop testbed which can be used to trouble-shoot and validate control algorithms without the risk of damaging the hardware [17]. The complete controller assembly is shown in Fig. 11. The developed control algorithms are evaluated, and the validation results are presented in Section III.

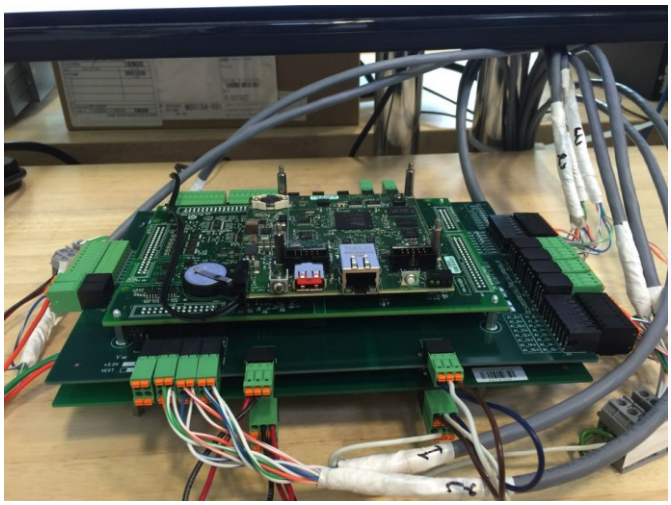


Fig. 11. Complete assembly of the inverter controller including the developed interface boards.

D. Inverter Assembly and thermal design

Components in the inverter system feature different thermal specifications and the entire system is also defined with environmental and mechanical specifications. Therefore, the system thermal design is key to the packaging and thermal management of the inverter system. The goal is to satisfy the component thermal limitations while pushing the volumetric power density. The layout of major components inside the inverter is shown in Fig.12. Here the only cooling method for thermal management is air cooling and the incoming air temperature is chosen to be 40 ºC.

During the design of the power block, three fans were utilized to remove the excessive heat from the inverter. The fans were attached to the power modules through a specially-designed air duct to maximize the air volume passing through the power modules. With a large air outlet on top side of the enclosure, the fans pull the hot air through the heat sinks which is expelled into the ambient environment. The reason why the power block is installed close to the air exit is because among all the components, the power block generates the largest amount of heat, and being close to the end of air

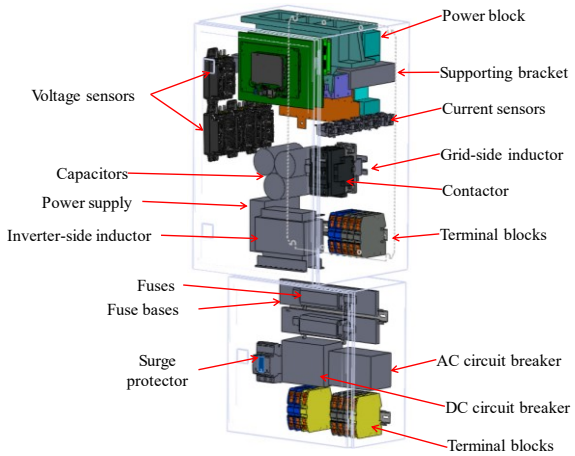


Fig. 12. Layout of components in the inverter system.

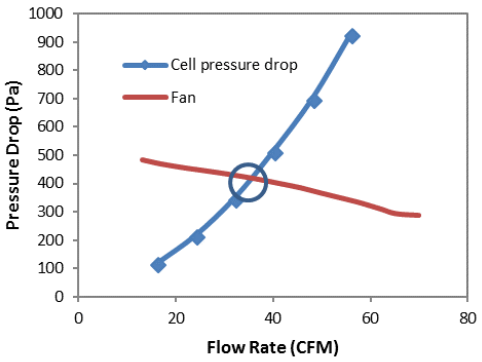


Fig. 13. Comparison of heat sink pressure drop and fan performance curve. It is for one power module.

cooling path avoids the heating of other components and mitigates the need for additional cooling.

The cooling air enters the enclosure through several vents on the enclosure. Determination of effective cooling air inlets and passages to dissipate thermal energy from these components is another important issue associated with the thermal design. Determination of the size and position of air vents helps to fulfill the temperature restrictions and thermal targets for components. A preliminary simulation shows that, in order to limit the power block's temperature rise below 40 °C, more than 100 in^2 of venting area is required for the ambient air to enter the enclosure. Another factor associated with the cooling performance is the volumetric flow rate of the fan. To determine the flow rate, heat sink pressure drop, and fan performance must be known. In this analysis, the measured pressure drop versus flow rate for the fan was graphed with the heat exchanger pressure drop to retrieve the flow rate, as shown in Fig. 14. The working volumetric flow rate is determined to be 36 cubic feet per minute (CFM) for a single and fan (1/3/ of power block).

Based on the inverter component layout, thermal specifications, and the air flow rate, thermal analyses were conducted to obtain the system-level temperature distribution inside the inverter. There were two types of thermal analyses

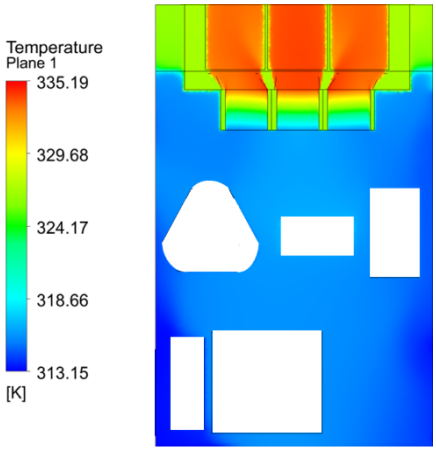


Fig. 14. Interior temperature distribution of the inverter.

applied to the system. The first one is a qualitative estimation based on the conservation of energy and constant mass flow rate. This method assumes that all the generated thermal energy is dissipated into the cooling air and there is no heat loss via other media. Meanwhile, the mass flow rate through each power module is equal and constant. It provides us an approximated temperature profile inside the inverter. Another more comprehensive method of thermal analysis is computational fluid dynamics (CFD) simulation. One advantage with the CFD simulation is that it presents the details of the air flow, temperature field and the pressure drop. Even though the two thermal analysis methods seem obviously distinct, they provided very close results under appropriate assumptions and can validate each other mutually.

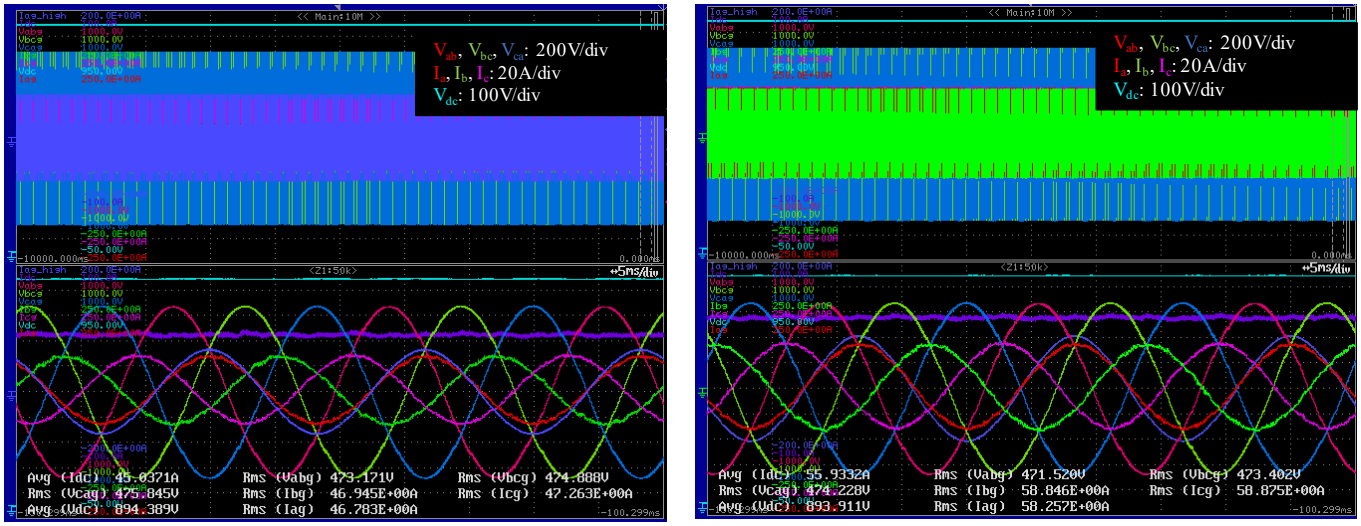
The first method used the flow rate of 36 CFM to estimate the increase of air temperature after passing through the power block and it was calculated to be 15°C. The second method simulated the entire inverter system and the updated temperature distribution within the inverter cabinet is presented in Fig. 14. In this graph, the relative impact of the inductor heat and power block heat can be seen based on the air temperature. Because of the high volumetric flow of air, the inductors cause a relatively small increase in the air temperature before the air enters the power block. It is seen that the power block still generates the largest heat and highest temperature rise. Dedicated fans are required to effectively conduct the hot air away from the power block. The temperature rise of the cooling air after passing through the power block is 17 °C. The higher temperature results from the slightly reduced airflow caused by the higher system pressure drop. Here, the simulation is system-level and simplifications are made when developing the power block and inductor models.

The validation of the inverter and control algorithms along with quantification of the inverter output quality and efficiency is presented in the next section.

III. Prototype Inverter Validation

In this section, the developed inverter is validated, and the inverter performance is presented. First the inverter operation in voltage control mode and current mode is presented. The quality of the inverter output waveforms is also quantified along with efficiency. Furthermore, the inverter operation during various grid events is presented to demonstrate the grid-support functions. The electrical schematic of the experimental setup for all the grid connected tests is shown in Fig. 1. The output from the inverter is connected to the grid through a Δ-Y transformer. This transformer is used to limit the common-mode (CM) current, since a CM choke was not included in the experimental setup. The grid was formed using Ametek's RS90 grid simulator. The inverter switching frequency for these tests is 20 kHz while the dc-bus voltage is maintained at about 900 V.

The inverter output waveforms when operating in open-loop, voltage-control mode connected to a resistive load is shown in Fig. 15. The THD of the load currents for 40 kW and 50 kW power being supplied by the inverter is measured to be about 2.35% and 2.14%, respectively. Similarly, inverter



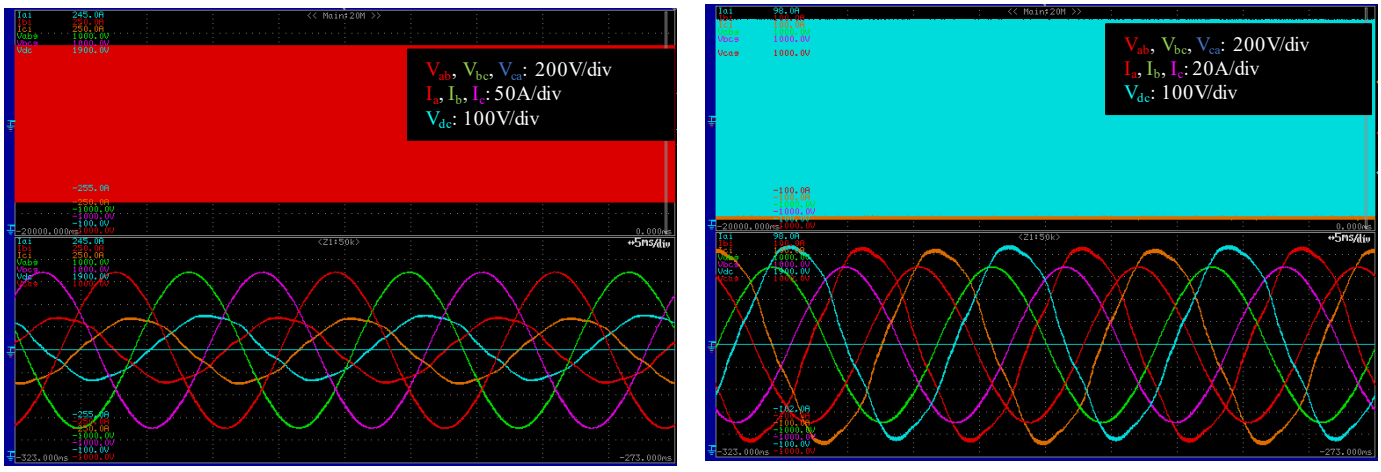
(a) Output Power = 40 kW (b) Output Power = 50 kW

Fig. 15. Measured three-phase waveforms of line-to-line voltages and line currents for different output power and output line-to-line voltage of 480 V for open-loop voltage-control mode of operation. AC-voltage scale: 200 V/div, DC-voltage scale: 100V/div, I scale: 20 A/div.

output waveforms when operating in closed-loop, current-control mode connected to a grid-simulator is shown in Fig. 16. The THD of the current injected into the grid is measured to be 3.62% and 3.94%. The inverter efficiency as measured at different loads with dc-bus voltage is shown in Fig. 17. The peak efficiency of the inverter is computed to be 98.2 ± 0.053% while the California Energy Commission (CEC) efficiency is computed to be about 97.72 ± 0.05%. It should be noted that the efficiency calculation includes losses in the controller and the thermal management system (fans). The measured efficiency is higher than conventional Si based PV inverters.

The next set of tests were done to verify the developed advanced inverter controls and to validate inverter performance during different grid events. The VVAR controls allows the inverter to help maintain the grid voltage by injecting or absorbing reactive power during any voltage event. Fig 18 shows the VVAR curve used for the verification. The grid-simulator used for the tests was coded to provide voltage steps at different time intervals as shown in Fig. 19. The inverter was capable of changing the reactive power injected into the grid through these voltage changes. It should be noted that the voltage results in Fig. 19 is the peak voltage measured at the point of common coupling (PCC).

The next verification is for VWATT grid-support function verification. The VWATT curve used for the verification is presented in Fig. 20. During this test the grid simulator was programmed to provide voltage steps as shown in Fig. 21. The reference active power is calculated based on the programmed VWATT curve (see Figs. 20 and 21). It can be observed from Fig. 21 that the active power injected into the grid followed the reference computed from the VWATT curve.



(a) Output Power = 41.5 kW (b) Output Power = 50 kW

Fig. 16. Measured three-phase waveforms of line-to-line voltages and line currents for different output power in current control mode of operation at 897 V dc bus.(a) ac-voltage scale: 200 V/div, dc-voltage scale: 100V/div, I scale: 50 A/div; (b) ac-voltage scale: 200 V/div, dc-voltage scale: 100V/div, I scale: 20 A/div.

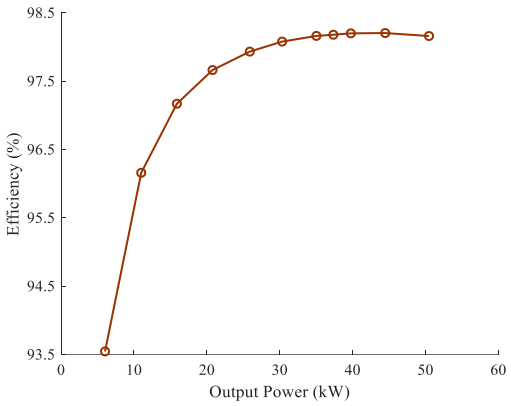


Fig. 17. Measured inverter efficiency at different loads.

In addition to regulation functions, voltage and frequency ride-through are also implemented in the controller. Fig. 22 provides the experimental result from a sample voltage ride through testing. In this verification, the over voltage 1 (OVR1) setting was tested. This OVR1 setting gets activated when the grid voltage is over 110% but less than 120% of the nominal voltage. For that operating region, the inverter is required to ride-through until 0.92 seconds. If the voltage does not return

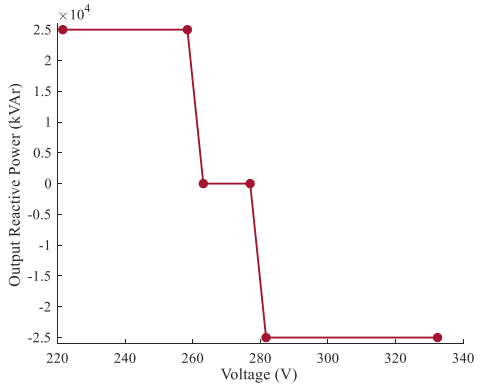


Fig. 18. Volt-VAr curve used in experimental verification.

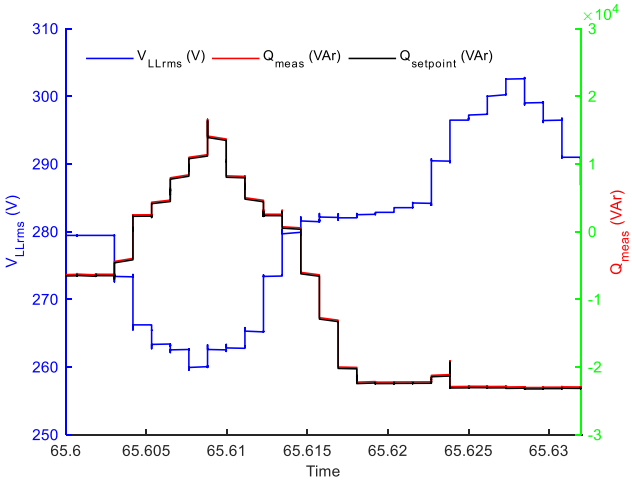


Fig. 19. Test results showing voltage steps, reference and measured reactive power injected into the grid.

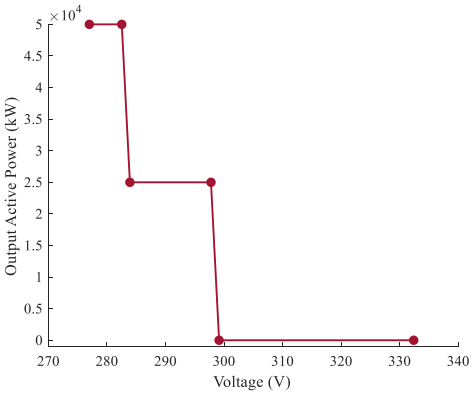


Fig. 20. Volt-Watt curve used in experimental verification.

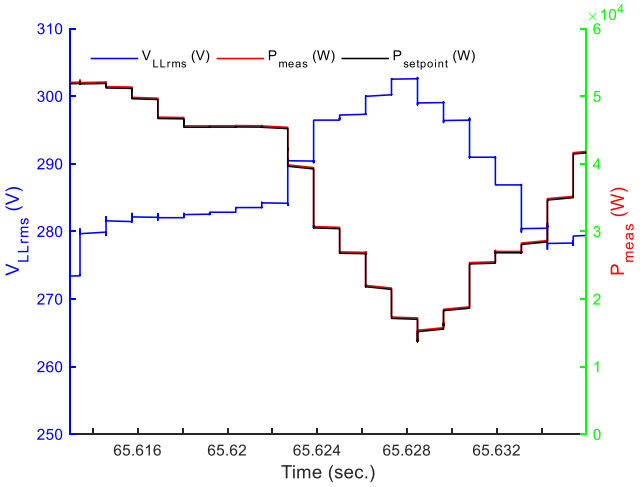


Fig. 21. Test results showing voltage steps, reference and measured active power injected into the grid.

to the normal range by that time, the inverter should trip. In the test results it can be observed that the voltage exceeded 1.1 PU (431 $V_{ph,peak}$) at about 0.45 seconds. At 0.75 seconds, the voltage reduced to normal range, and thus did not trigger the trip signal. At 1.3 seconds, the voltage increased to 1.1 PU and stayed at this voltage level. The trip signal was triggered after

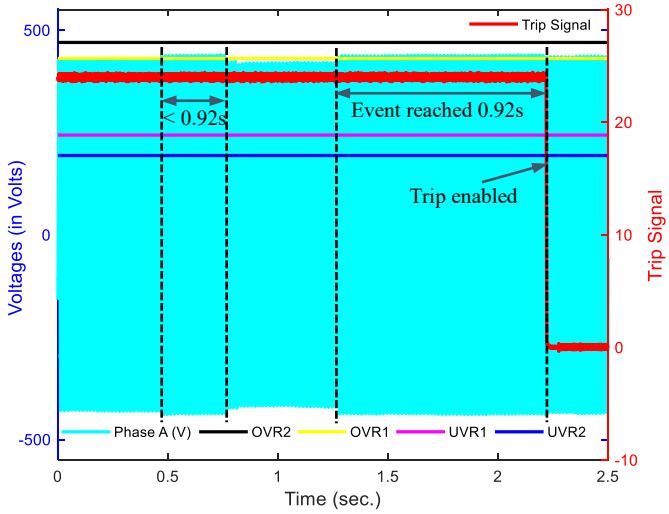


Fig. 22. Experimental results for VRT showing two overvoltage events.

0.92 seconds as expected and required. It should be noted that, the trip signal shown in Fig. 22 is the actual 24 V signal being sent to the three-phase AC contactor by the controller. The second OVR1 event occurs at about 1.3 seconds and when the ride-though limit is reached at about 2.22 seconds, the controller sends 0 V to the contactor coil to trip it.

IV. Conclusion

In this paper a three-phase, two-level, 480V, 50kW PV inverter designed with SiC power devices has been presented and validated. The different parts of the inverter have been presented to demonstrate the optimization in each to get full advantage of the high-voltage, high switching speed SiC devices. The inverter functionality has been tested and its performance has been quantified in terms of output waveform THDs and inverter efficiency at different loads and in both voltage and current control modes of operation. The acceptable inverter performance has also been demonstrated while inverter is performing grid-support functions. The development of such inverter and its validation will encourage PV inverter manufacturers to adopt wide bandgap devices in their products and resulting in higher efficiency and low-cost inverters. This will further facilitate the proliferation of PV into the electric power systems.

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