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DESIGN, ANALYSIS AND COMPARISON OF INSULATED METAL SUBSTRATES FOR HIGH POWER WIDE-BANDGAP POWER MODULES

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ABSTRACT

In this technical paper, design, analysis and comparison of insulated metal substrates for high power wide-bandgap semiconductor-based power modules is discussed. The paper starts with technical description and discussion of state-of-the-art direct bonded copper substrates with different ceramic insulators such as AlN, Al_2O_3 and Si_3N_4. This is followed by introduction of insulated metal substrates, material properties and options on each layer, and design approach for high power applications. The properties of dielectric thickness, and impact on power handling capability of the substrate are discussed. Insulated metal substrate design approach for SiC MOSFET based power modules is presented. Finite element analysis-based characterization and comparison of different designs including steady-state and transient thermal response is presented. The results show that IMS is a promising alternative to DBC in high power modules with improved transient thermal performance. IMS provides flexible building structure with multi-layer stacking options and variable thicknesses at different layers.

NOMENCLATURE

AlN Aluminum Nitride
DBC Direct bonded copper
FEA Finite element analysis
GaN Gallium nitride
HEMT High electron mobility transistor
htc Heat transfer coefficient
IMS Insulated metal substrate
MOSFET Metal-oxide-semiconductor field-effect transistor
Si Silicon
Si_3N_4 Silicon nitride
SiC Silicon Carbide
WBG Wide-bandgap

INTRODUCTION

Power semiconductor modules used in power converters are responsible for processing and transferring the electrical power between the source and the load with the desired performance. The efficiency of such systems has become quite high due to recent advancements in silicon based power semiconductor devices, usually above 95% for systems rated more than 1 kW output power. With the advancements in wide-bandgap (WBG) based power semiconductor devices such as SiC MOSFET and GaN HEMT, efficiency figures above 98% have been reported in literature [1, 2]. However, even with very high efficiency figures, a significant amount of power is dissipated in a small area due

to increased power demand from the electrical load, increased power density of power modules and reduced chip size with the introduction of wide-bandgap devices [3]. Therefore, the performance of the materials used for packaging, integration of power modules, and design of thermal management systems have become the focus points of the next generation power electronic systems, especially in application domains such as electric vehicles and more electric aircraft [4]. Technical guideline in the U.S. Drive EETT Roadmap in [5] estimates 3.3 times increase in power handling capability (30 kW to 100 kW) for the electric traction drive system, and 1.4 times increase in operating temperature (180°C to 250°C) for the power semiconductor module used in the power electronic converter. Furthermore, the power density of the power electronics is expected to increase 4.6 times (18 kW/L to 100 kW/L).

The power module for high power systems is designed to accommodate semiconductor dies, provide electrical connection/isolation to/from other components, and extraction and transfer of generated heat in the dies, and finally protection from environmental conditions (e.g. dust, humidity). The illustration of a conventional power module cross section is presented in Figure 1, where various components of the structure are highlighted. The structure is composed of different materials such as aluminum for bond wire, copper for electrical terminals, aluminum nitride for ceramic based direct bonded copper substrate etc. This multi-layer, multi-material based structure has limited heat extraction capability. Furthermore, certain layers in the structure shown in Figure 1 are subject to high mechanical stress due to different coefficients of thermal expansion (CTE) between layers during power and environmental cycling of the module, thus leading to limited lifetime and early failures caused by thermal stress [6]. Direct bonded copper substrate in the power module provides the two-layer substrate structure where the top layer is utilized for die attachment, interconnect and electrical terminal placement. The bottom layer is insulated from the top layer with a ceramic layer in between and is attached to the base plate, which is designed as a heat spreader. The ceramic has to provide excellent thermal and electrical performance in terms of thermal conductivity and breakdown voltage to transfer the generated heat in the dies to the heat sink, and to isolate the live terminals on top of the DBC from the rest of the system. Various insulator materials have been studied in literature for direct bonded substrates. Fundamental properties of the three most common ceramic materials used in industry are presented in Table 1.

In DBC, aluminum oxide is the commonly used isolator in substrate design where mechanical strength and relatively high coefficient of thermal expansion are desired, and power density is not a concern. The manufacturing of Al_2O_3 is relatively cheaper than AlN due to existence of oxide layer on the ceramic to form the bonding between the metal and ceramic. Although the standard thickness for Al_2O_3 is presented as 381 μm in Table 1, 500 and 630 μm values are also encountered for high voltage

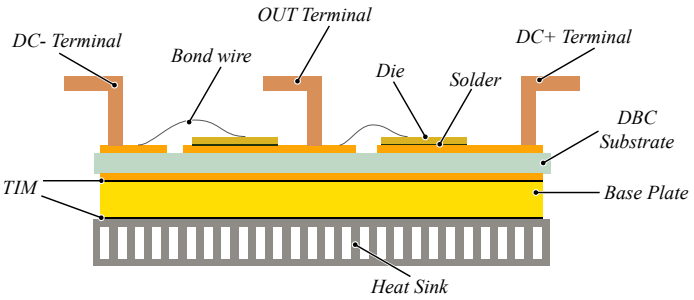

FIGURE 1. Illustration of a conventional power module cross section [6].

designs. Aluminum nitride is the high performance dielectric option among all the ceramics presented in Table 1 due to high thermal conductivity and breakdown voltage. AlN is two to three times more expensive than Al_2O_3, and is also known as a brittle material. The standard thickness of AlN is stated as 630 μm and 1 mm thickness is used in very high voltage applications. Due to mechanical strength and brittle structure of AlN, 630 μm thick insulator is commonly used in applications where 2-3 kV isolation is required. On the other hand, Si_3N_4 is mechanically stronger in comparison to AlN, and therefore it is possible to machine Si_3N_4 thinner than standard thickness 630 μm. This brings the opportunity to match the thermal performance of AlN based DBC at low voltage applications, using Si_3N_4 without compromising the electric isolation performance. Finally, the HT-07006 is the dielectric polymer/ceramic blend from Henkel that has excellent dielectric strength and can be processed in very thin layers. These two properties make it an attractive solution for high power applications despite the lower thermal performance with respect ceramic materials. Furthermore, polymer materials have a wide elastic deformation range and the thermal expansion performance is not of interest in substrate applications [7].

In this paper, design, analysis and comparison of insulated metal substrates for high power wide-bandgap semiconductor-based power modules is discussed. In the next section, the structure and the design of the IMS, and structural comparison with AlN based DBC will be provided. This will be followed by the discussion of the steady-state and transient finite-element based thermal simulations conducted in COMSOL Multiphysics. In the final section, the junction temperature analysis of the SiC MOSFETs based on different substrates under different load conditions will be presented.

TABLE 1. Standard layer thickness of insulators and fundamental properties [7]

Material	Standard Thickness [μm]	Heat Transfer Coefficient [W/(cm^{2}K)]	Breakdown Voltage [kV]
Al_2O_3	381	6.3	5.7
AlN	635	28.3	12.7
Si_3N_4	635	11	8.9
HT-07006	152	1.41	11

INSULATED METAL SUBSTRATE DESIGN FOR HIGH POWER MODULES

Steady-State and Transient Thermal Analysis

The substrate design evaluated in this study is based on a half-bridge SiC MOSFET power module, where three SiC MOSFET dies are paralleled per switch and placed on a electrically isolated substrate from the coolant. The electrical schematic of the half bridge module is presented in Figure 2. Kelvin connection for the SiC MOSFETs is used for gate and source terminal to optimize the switching performance independent of load current. The SiC MOSFET dies used in this work are rated at 900V, 30mΩ (CPM3-0900-0030A) at room temperature and manufactured by CREE. Traditionally, such a design will be realized on a direct bonded copper substrate, presented in Figure 1, that provides electrical isolation using the AlN dielectric layer between two copper planes. The dies are soldered on different copper islands and then connected via bond wires to form the three terminal half-bridge structure.

In this work, insulated metal substrate is utilized to replace the DBC. The DBC is formed by 640 μm AlN ceramic insulator sandwiched with 300 μm copper on both sides. The insulated metal substrate provides flexibility to the designer in terms of number of stacked layers and thickness in each layer to optimize thermal and electrical isolation performance. Therefore, the flexibility of the design can be utilized to overcome some of the challenges of IMS such as low thermal conductivity of dielectric layer, as stated in Table 1. The cross-section and isometric views of the insulated metal structure, which is targeted to replace the DBC in Figure 1, are presented in Figures 3 and 4 respectively.The SiC MOSFET dies are soldered on two electrical isolated copper cores, that are designed for lateral heat spreading across the substrate to improve transient thermal performance and steady state thermal resistance. These two copper cores are isolated from the bottom copper layer using the HT-07006 dielectric film, and from each other with non-conductive epoxy based filler. The thickness of the copper core is 1.6 mm, dielectric film thickness is 152 μm and the bottom layer copper thickness is 70 μm. The expanded view of the IMS is presented in Figure 5 where the structure of each layer can be seen clearly. Once the copper core, dielectric layer 1 and bottom layer are bonded, additional layers can be added to the structure. In this case, the dielectric layer 2 and the top layer are added to the design to accommodate isolated electrical terminals for gate-source connections of the SiC MOSFETs and DC- terminal for the half-bridge design.

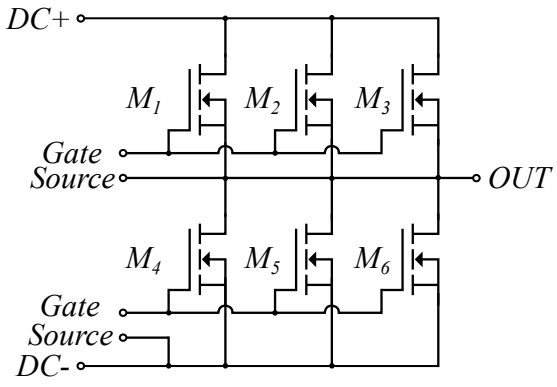

FIGURE 2. Electrical layout of the half bridge module.

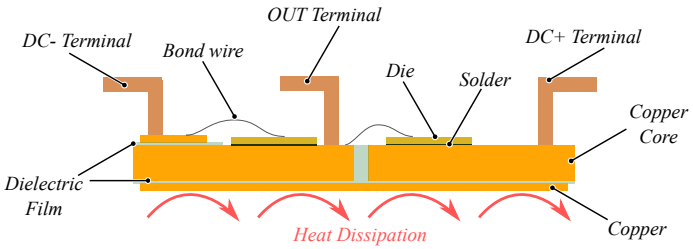

FIGURE 3. Cross section of the insulated metal substrate structure.

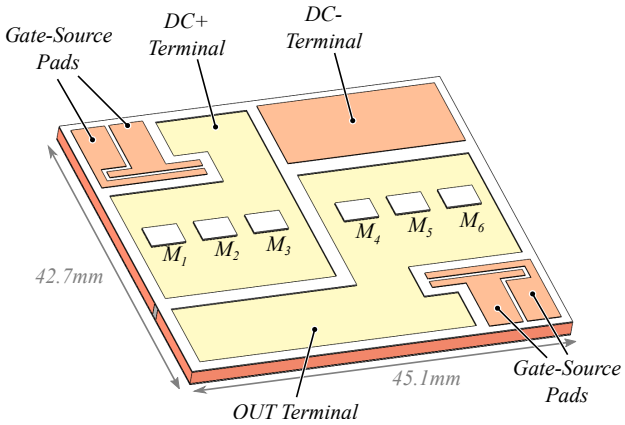

FIGURE 4. Isometric view of the insulated metal substrate.

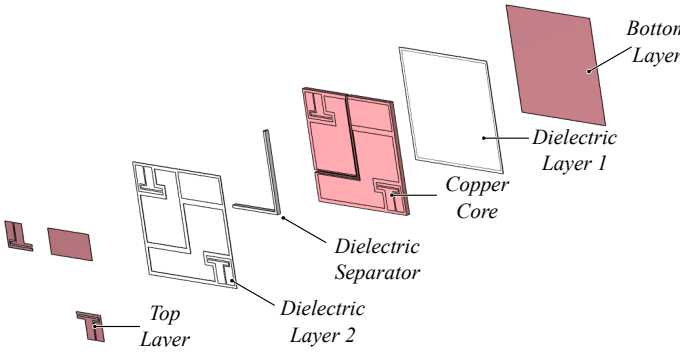

FIGURE 5. Expanded view of the insulated metal substrate.

ANALYSIS AND COMPARISON OF DBC AND IMS

The analysis of the DBC and IMS are conducted in COMSOL Multiphysics finite element simulation tool based on representative electrical and thermal operating conditions of a wide-bandgap power module. The base temperature of the substrates is set to 65°C, which is the typical coolant temperature in automotive systems [8]. The heat transfer coefficient between the coolant and the base of the substrate is defined as 5000 W/(m^2K) to represent the cooling performance of a typical liquid cooled cold plate, and the interface thermal resistance between the substrate and the cold plate [9]. Each of the SiC MOSFET dies shown in Figure 4 is considered as an individual heat source with 45 W constant heat source on the top surface of the die for steady-state thermal analysis. Once the system reached steady-state, the heat sources are set to 0 W, and the cooling profile of the system analyzed in a time dependent simulation for transient thermal response analysis.

For the meshing of the substrates, free triangular mesh is applied at the surface of the system with 0.2 mm maximum feature size on the die surface and 0.5 mm maximum feature size on the surface of the substrate. The surface mesh is then distributed to 5 layers in the die, 5 layers in the die attach, 20 layers in the copper core, 5 layers in the dielectric layer and 5 layers in the bottom layer in order to capture head spreading and temperature distribution across the substrate under test with high accuracy and resolution. Similar settings applied to the DBC model for consistency.

The steady-state thermal analysis results for DBC and IMS are presented in Figure 6 with surface temperature distribution for DBC and IMS in Figures 6a and 6c, and isothermal temperature distribution inside the substrates in Figures 6b and 6d respectively. The DBC provides symmetrical temperature distribution among top and bottom switches in the half-bridge with 144°C maximum junction temperature on the surface of the die M_2. Furthermore, the temperature distribution presented in Figure 6b shows that heat spreading across the DBC is limited and this results in hot spot areas around the heat sources. Such temperature distribution across the DBC is one of the reasons for having base plates in conventional power modules. As the DBC has limited heat spreading capability, base plate provides a larger surface area for the heat transfer from the dies to the heat sink. On the other hand, with IMS, the maximum junction temperature across the half bridge module reaches to 152°C on the surface of the die M_2. The surface temperature distribution in Figure 6c shows that there is an asymmetry in temperature distribution between the top and bottom switches in the half bridge. The dies M_4-M_6 have lower temperature in comparison to the dies M_1-M_3 under same loading condition. The reason for this asymmetry can explained with the design of the copper core in the insulated metal substrate. As shown in Figure 5, the copper core is divided into two pieces and separated with a dielectric separator in order to provide isolated copper islands for top and half switches in the half-bridge configuration. The thermal conductivity of the dielectric separator is less than 0.6 W/(m.K) and therefore the separator also acts as a thermal insulator between two sections of the copper core. Furthermore, it can be seen from Figure 5 that the right side of the copper core is slightly larger than the left side to accommodate the wire bonding of M_1-M_3 dies and output terminal of the half-bridge. The increase in the copper core volume leads to improved heat spreading for M_4-M_6 dies and the thermal separation with the dielectric separator limits the heat transfer between the isolated islands within the copper core. The difference in the temperature distribution in the copper core can be observed in Figure 6d.

The transient thermal impedance of each SiC MOSFET die on IMS and DBC substrates is obtained by recording the cooling performance of each die in a time dependent simulation. The time dependent simulation is run for 100 seconds and the initial condition for the transient analysis is defined as the results of the presented steady-state analysis. As the junction temperature of each die can be recorded, the base temperature is fixed to 65°C and the initial heat loss across each die is fixed to 45 W, the transient thermal impedance can be calculated at every time step. The transient thermal impedance values of six dies placed on DBC, IMS and comparison with DBC and IMS solution for the most stressed dies are presented in Figures 7, 8 and 9 respectively. In Figure 7, it can be seen that the symmetrical thermal performance presented in Figure 6a is achieved by the well matched steady state thermal impedance for individual dies on the DBC. The steady-state thermal impedance difference among six dies is less than 0.1 °K/W. On the other side, transient thermal impedance for the dies on IMS is presented in Figure 8. The impact of asymmetrical copper core design discussed in previous section can be clearly seen in the steady-state thermal impedance values. Although the thermal impedance difference between paralleled dies can be considered negligible, there is approximately 0.2 °K/W between the paralleled die groups. Finally, the transient thermal impedance comparison of the most stressed dies M_2 and M_5 is presented in Figure 9. The comparison results for

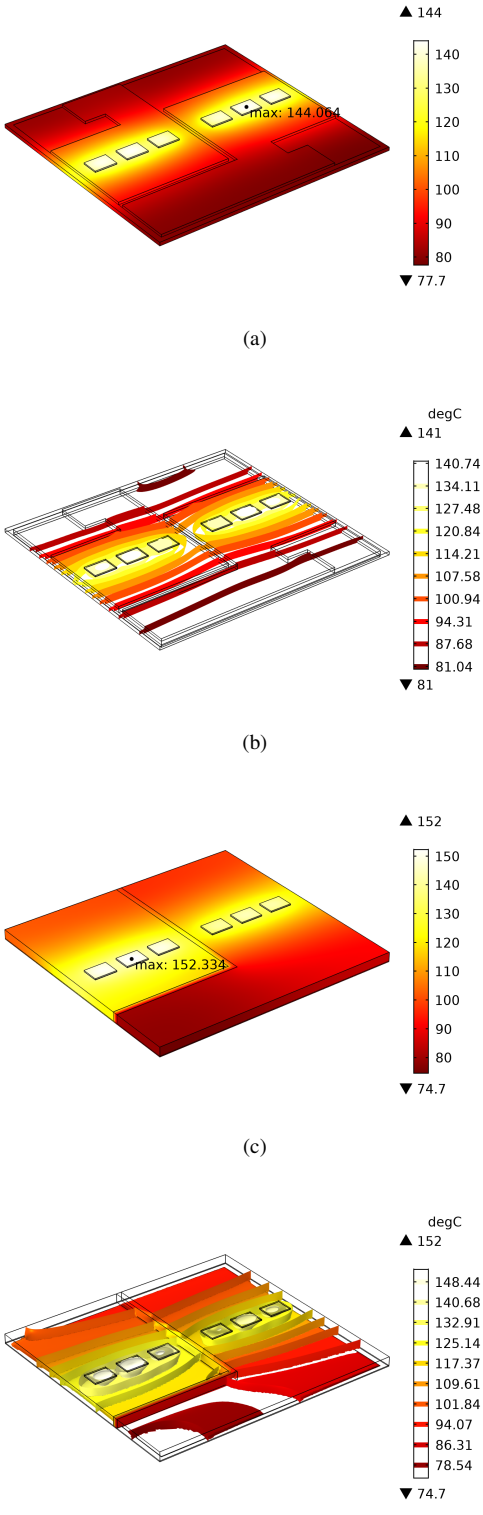

FIGURE 6. Steady-state thermal analysis results for DBC and IMS: (a) surface temperature distribution on DBC, (b) isothermal temperature distribution in DBC, (c) surface temperature distribution on IMS, (d) isothermal temperature distribution in IMS.

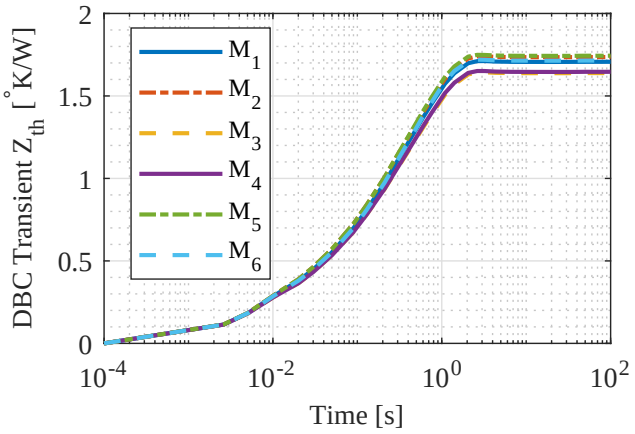

FIGURE 7. Transient thermal impedance of each die on DBC.

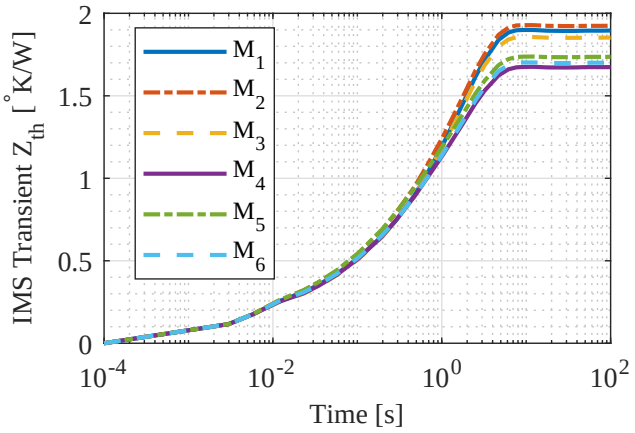

FIGURE 8. Transient thermal impedance of each die on IMS.

M_2 shows that although the small core area provided for M_1-M_3 in IMS results in higher steady-state thermal impedance, the transient thermal impedance between 10 ms and 1 s is significantly improved when it is compared with DBC based solution. The results for the die M_5 show that if the copper core area is sufficiently large enough, then the steady-state thermal impedance of a SiC MOSFET die on a AlN based DBC can be matched with an IMS solution with improved transient thermal impedance below 1 s.

Thermal Analysis in an Inverter Scenario

The transient thermal impedance curve for each die can be used in a power electronics simulation tool for evaluation of mean junction temperature T_j and junction temperature variation ΔT_j under typical power electronic inverter operating scenarios.

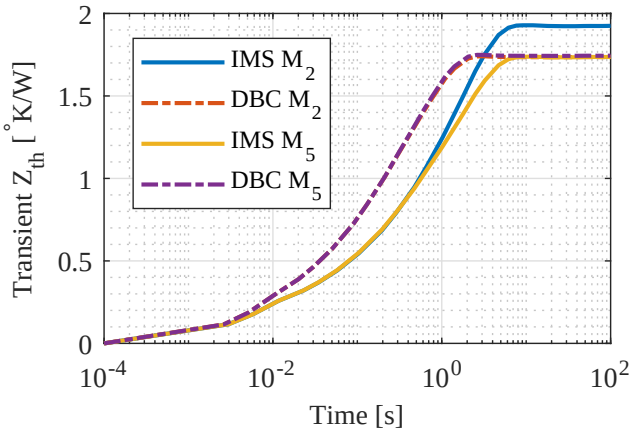

FIGURE 9. Comparison of transient thermal impedance of M_2 and M_5 on DBC and IMS.

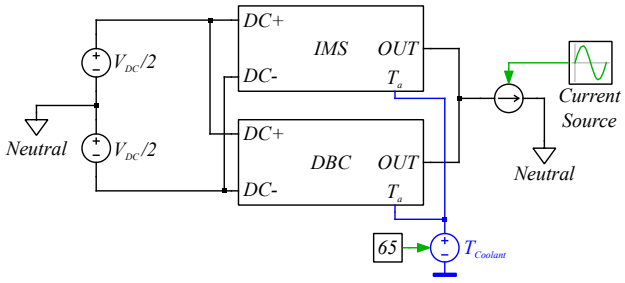

FIGURE 10. Schematic of the model for the thermal analysis of the substrates in an inverter scenario.

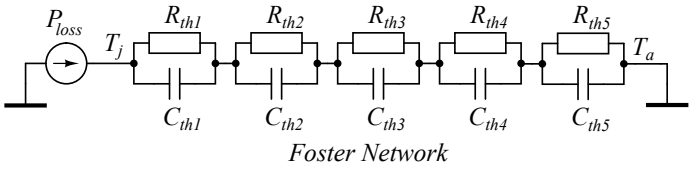

FIGURE 11. Thermal model of a SiC MOSFET die in the model.

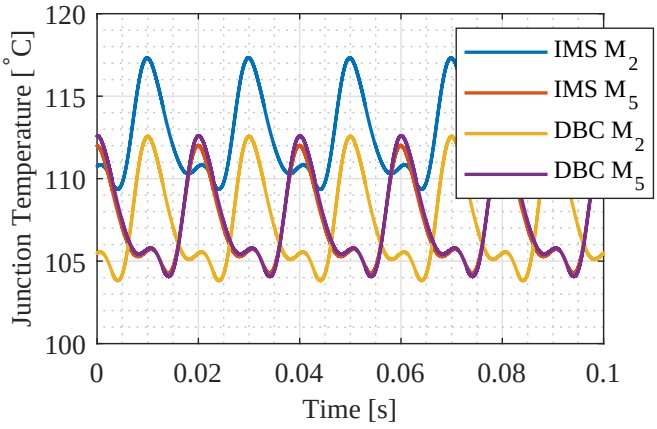

FIGURE 12. Junction temperature of the most stressed dies at 50 Hz load frequency.

The simulation tool consists of electrical and thermal domains which are coupled with current, voltage and temperature dependent semiconductor loss models obtained from device manufacturer. In the electrical model, device current and voltage waveforms are simulated for estimation of switching and conduction losses at a given junction temperature defined by the thermal domain. Using the device loss model, the instantaneous power loss is fed in to the thermal model for calculation of junction temperature for the next instant. The schematic of the developed model for the thermal analysis of the substrates in an inverter scenario is presented in Figure 10. A half-bridge inverter topology is selected with 30 kHz switching frequency, 600 V DC link voltage and modulation index of 0.9. The output current is set to 100 A_{rms} per substrate (200 A_{rms} total) with power factor of 0.85 and fundamental period of 50 Hz. In each substrate block, there are six SiC MOSFET loss models P_{loss} coupled to the Foster network based thermal model of an individual die presented in Figure 2. The Foster network for each die is developed based on curve fitting to the individual transient thermal impedance curves presented in Figures 7 and 8. The Foster network based thermal model for a SiC MOSFET die is presented in Figure 11 and the network parameters for dies on DBC and IMS are presented in Tables 2 and 3 respectively in the appendix.

The junction temperature trajectory of the SiC MOSFET dies on DBC and IMS based on the defined operating scenario are presented in Figure 12. It can be seen that the junction temperature variation frequency is equal to the load frequency. In variable frequency drives used in traction systems, high current operation is required to produce high torque at very low motor speeds [10]. Therefore, large junction temperature variations may occur across the SiC MOSFET dies in low speed, high torque operating region. In order to evaluate this effect, the fundamental frequency of the load is swept from 25 Hz to 400 Hz. The mean junction temperature and junction temperature variation using different substrates with respect to load frequency is presented in Figures 13 and 14. It can be seen that although the mean junction temperature does not change significantly with load frequency, the junction temperature variation is strongly impacted by it. At frequencies below 100 Hz, IMS provides lower junction temperature variation and this will eventually lead to more reliable operation and longer life time. It is reported in literature that high number of cycles can be achieved in a power module if the junction temperature is reduced, even if the mean junction temperature is increased of the same amount [11].

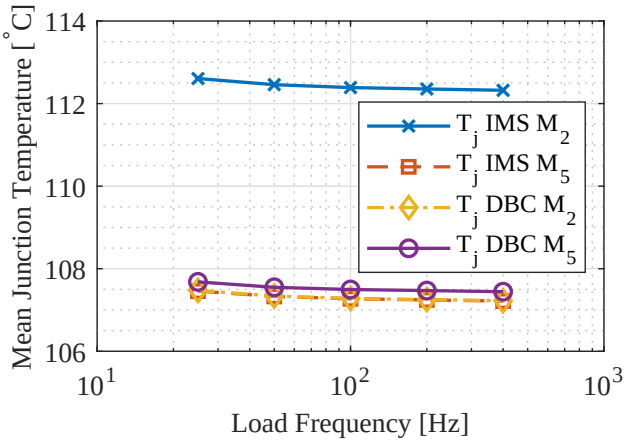

FIGURE 13. Mean junction temperature of the most stressed dies with different load frequencies.

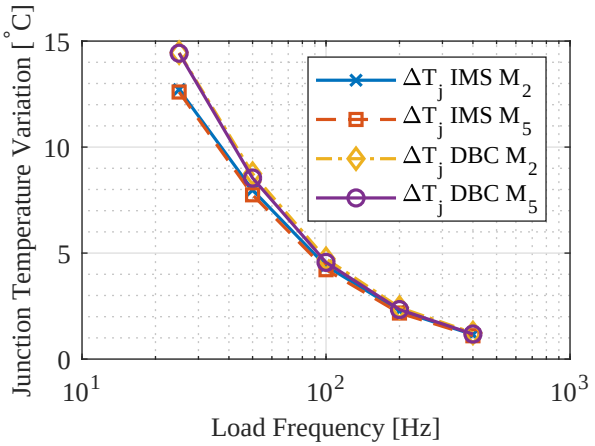

FIGURE 14. Junction temperature variation across the most stressed dies with different load frequencies.

CONCLUSION AND FUTURE WORK

In this work, design and analysis of insulated metal substrate, and comparison with direct bonded copper for high power wide bandgap based power modules is presented. Design structure and fundamental properties of insulated metal substrate are discussed and compared with conventional direct bonded copper substrate using different insulators. Finite element analysis based simulation and comparison of IMS and DBC with AlN insulator for a SiC MOSFET based half-bridge inverter is presented. The steady state and transient thermal analysis shows that IMS provides improved heat spreading underneath the SiC MOSFET dies that leads to improved transient thermal performance. The transient thermal model for each SiC MOSFET die is generated based on FEA results and used in a inverter scenario for evaluation of mean junction temperature and junction temperature variation under different operating conditions. The results indicate that IMS can be an alternative to DBC for high power modules, and IMS can also reduce junction temperature across the semiconductor die at low load frequencies due to increased thermal capacitance across the substrate. As part of future work, designed IMS and DBC samples will be built and characterized experimentally at high voltage, high power conditions for validation of the proposed approach.

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Appendix: Foster Network Parameters

The Foster network thermal parameters for SiC MOSFET dies on DBC and IMS are presented in Tables 2 and 3 respectively.

TABLE 2. FOSTER NETWORK THERMAL PARAMETERS FOR DIES ON DBC

Impedance		Z_{th}				
i		1	2	3	4	5
M_1	R_{thi} [°K/W]	1.037	0.0001043	0.2847	0.3868	0.0008247
	τ_i [s]	0.5348	0.1801	0.006643	0.08564	0.7555
M_2	R_{thi} [°K/W]	0.4384	0.5196	0.2769	0.4957	0.007333
	τ_i [s]	0.08641	0.5562	0.006492	0.5289	0.02078
M_3	R_{thi} [°K/W]	0.003954	0.3663	1.01	0.0003221	0.2601
	τ_i [s]	0.1235	0.07553	0.5345	0.6592	0.00595
M_4	R_{thi} [°K/W]	0.2427	0.9493	0.3726	0.08221	0.001436
	τ_i [s]	0.005379	0.5256	0.06857	0.5236	0.541
M_5	R_{thi} [°K/W]	0.3019	0.0001493	1.018	0.1443	0.2818
	τ_i [s]	0.007285	0.5903	0.5376	0.114	0.08627
M_6	R_{thi} [°K/W]	0.1034	0.1858	0.07542	0.2737	1.078
	τ_i [s]	0.003498	0.009938	0.0836	0.07754	0.5159

TABLE 3. FOSTER NETWORK THERMAL PARAMETERS FOR DIES ON IMS

Impedance		Z_{th}				
i		1	2	3	4	5
M_1	R_{thi} [°K/W]	0.0007517	1.331	0.003436	0.3001	0.263
	τ_i [s]	1.33	1.593	0.4072	0.1347	0.00628
M_2	R_{thi} [°K/W]	0.2473	0.2526	0.1334	1.294	0.0001455
	τ_i [s]	0.005828	0.09667	0.2392	1.596	1.712
M_3	R_{thi} [°K/W]	0.2631	0.05461	1.197	0.3398	0.001128
	τ_i [s]	0.006367	1.632	1.61	0.1688	1.752
M_4	R_{thi} [°K/W]	0.0009016	0.9154	0.4157	0.08099	0.2625
	τ_i [s]	1.37	1.652	0.1845	1.677	0.006316
M_5	R_{thi} [°K/W]	0.4281	1.657e-6	0.2654	0.02313	1.021
	τ_i [s]	0.1561	1.981	0.006433	0.5854	1.63
M_6	R_{thi} [°K/W]	0.3684	0.02919	8.675e-5	1.028	0.2766
	τ_i [s]	0.1801	0.3495	2.085	1.664	0.006885