Flexible Intelligent Real-time dc-ac grid Emulator (FIRE): Power Electronic Hardware-in-the-Loop (PE-HIL) Amplifier

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***Abstract*—Grid modernization efforts are leading to increased penetration of power electronics in the existing alternating current (ac) bulk power systems (BPS). Some examples of power electronics based applications that are being developed in BPS include high-voltage direct current (HVdc) systems, renewable generation systems, energy storage systems, and others. One of the requirements to succeed in the goals of grid modernization (like increased efficiency and reliability) is to setup a platform that can evaluate basic building blocks of such systems. For example, the basic building block of a modular multilevel converter (MMC)-based HVdc system is a submodule (SM). The evaluation platform will provide means to innovate new SM circuit architectures, new semiconductor devices in the SM, new gate-drivers, new controllers, and others. The flexible intelligent real-time dc-ac grid emulator (FIRE) platform incorporates the evaluation capability to evaluate the basic building blocks. The FIRE platform incorporates this evaluation capability through the power electronic hardware-in-the-loop (PE-HIL) concept. The PE-HIL for MMC-HVdc system can evaluate SMs in the MMC. In this paper, the design of amplifier required to perform PE-HIL simulation is presented. Experimental results of the amplifier and the simulation results of the PE-HIL concept utilizing the amplifier are presented.**

I. Introduction

Increasing presence of power electronics is anticipated in the next few decades. The increased presence is expected through developments in (i) solid-state power substations [1], (ii) newer architectures of high-voltage direct current (HVdc) converters to reduce costs and improve efficiency of operation with advanced features (like fault-tolerance, virtual inertia, etc.) [2], [3], and (iii) advanced integration methods of renewables and/or energy storage and/or electric vehicles directly to high-voltage alternating current (ac) grid through multi-port power electronics. These technologies typically consist of several basic building blocks of power electronics like the submodule (SM) in a modular multilevel converter (MMC). The SM includes several components like the power electronics circuit, semiconductor devices, gate-drivers, cooling mechanisms, protection system, capacitors, and others. With innovations to improve the efficiency, reliability, and costs happening in each component of the SM, the requirement for an evaluation platform assumes significance.

In this paper, a power electronic hardware-in-the-loop (PE-HIL) concept is proposed. This concept can be used to evaluate the basic building blocks like the SM in MMC-HVdc systems under realistic dc-ac system operating conditions. The PE-HIL capability is a part of the flexible intelligent real-time dc-ac grid emulator (FIRE) platform. The FIRE platform will include other components that would be explained in future manuscripts to emulate large-scale ac-dc networks. In this paper, the PE-HIL amplifier is presented with experimental results to show its performance.

II. MMCs

The circuit diagram of a three-phase MMC is shown in Fig. 1. The basics of operation of the MMC is explained in detail in [2] and is not repeated here.

A. MMC Model

The dynamics of the arm currents in the MMC of Fig. 1 are given by (1), where $v_{\mathrm{sm,y,i},j}$ is the output voltage of SM-i in arm-y, phase-j. It can be observed from (1d) that there are only five independent arm currents.

The dynamics of the SM capacitor voltages in the MMC of Fig. 1 are given by

$$C_{SM}\frac{\mathrm{d}v_{\mathrm{cy,i},j}}{\mathrm{d}t} = -\frac{v_{\mathrm{cy,i},j}}{R_p} + S_{\mathrm{yi1},j}i_{\mathrm{y},j} + (1 - S_{\mathrm{yi1},j}) \times (1 - S_{\mathrm{yi2},j})\, i_{\mathrm{y},j}\mathrm{sgn}\,(i_{\mathrm{y},j})\,, \quad \forall \mathrm{y} \in (\mathrm{p},\mathrm{n}), \forall j \in (a,b,c). \tag{2}$$

Equations (1) and (2) are the set of semi-explicit DAEs that represent the overall dynamics of the MMC.

Under normal operating conditions when one of the devices in the SM is always turned ON, (1c) and (2) become

$$v_{\mathrm{y},j} = \sum_{\mathrm{i}=1}^{N} S_{\mathrm{yi1},j}v_{\mathrm{cy,i},j}, \forall \mathrm{y} \in (\mathrm{p},\mathrm{n}), \forall j \in (a,b,c), \tag{3a}$$

$$C_{SM}\frac{\mathrm{d}v_{\mathrm{cy,i},j}}{\mathrm{d}t} = -\frac{v_{\mathrm{cy,i},j}}{R_p} + S_{\mathrm{yi1},j}i_{\mathrm{y},j}, \quad \forall \mathrm{y} \in (\mathrm{p},\mathrm{n}), \forall j \in (a,b,c). \tag{3b}$$

When the SMs are in blocked state, (1c) and (2) become

$$v_{\mathrm{y},j} = \sum_{\mathrm{i}=1}^{N} v_{\mathrm{cy,i},j}.\mathrm{sgn}\,(i_{\mathrm{y},j}), \forall \mathrm{y} \in (\mathrm{p},\mathrm{n}), \forall j \in (a,b,c), \tag{5a}$$

$$C_{SM}\frac{\mathrm{d}v_{\mathrm{cy,i},j}}{\mathrm{d}t} = -\frac{v_{\mathrm{cy,i},j}}{R_p} + i_{\mathrm{y},j}.\mathrm{sgn}\,(i_{\mathrm{y},j})\,, \quad \forall \mathrm{y} \in (\mathrm{p},\mathrm{n}), \forall j \in (a,b,c). \tag{5b}$$

The sgn(.) function in (5a) introduces stiffness in the arm current dynamics. There is no numerical stiffness observed in the SM capacitor voltage dynamics. To simulate MMCs, numerical stiffness based separation has been considered to speed-up the simulation of MMCs [4]. The overview of the separation method in [4] is shown in Fig. 1. The same separation method is utilized to perform PE-HIL simulation, with the SM in the MMC being the device under test. In this paper, the PE-HIL amplifier is designed and evaluated under different operating conditions.

III. Power Electronic Hardware-in-the-Loop (PE-HIL) Concept

The PE-HIL concept for an MMC-HVdc system has been developed such that one of the SMs of the system can be evaluated under realistic operation conditions. That is, the SM needs to be connected to a current source as shown by the separation technique summarized in Fig. 1. The current source generates the operating arm current. The components of the PE-HIL concept include: (i) an arm current source emulator that connects to the SM hardware under evaluation, (ii) HIL simulator, and (iii) a data processing and control unit between the HIL simulator and the arm current source emulator. The overview of PE-HIL concept is shown in Fig. 2. The arm current source emulator is the PE-HIL amplifier, which is the main focus of this paper. The HIL simulator and data processing and control unit are explained briefly with information on the design, with the PE-HIL concept simulated in the next section.

A. Arm Current Source Emulator

The arm current source emulator is based on power electronic circuit shown in Fig. 3. It consists

$$(L_o + L_s)\frac{\mathrm{d}i_{\mathrm{p},j}}{\mathrm{d}t} - L_s\frac{\mathrm{d}i_{\mathrm{n},j}}{\mathrm{d}t} = -\left(R_o + R_s\right)i_{\mathrm{p},j} + R_s i_{\mathrm{n},j} + \frac{V_{\mathrm{dc}}}{2} - v_j - v_{\mathrm{cm}} - v_{\mathrm{p},j}, \forall j \in (a,b,c), \tag{1a}$$

$$(L_o + L_s)\frac{\mathrm{d}i_{\mathrm{n},j}}{\mathrm{d}t} - L_s\frac{\mathrm{d}i_{\mathrm{p},j}}{\mathrm{d}t} = -\left(R_o + R_s\right)i_{\mathrm{n},j} + R_s i_{\mathrm{p},j} + \frac{V_{\mathrm{dc}}}{2} + v_j + v_{\mathrm{cm}} - v_{\mathrm{n},j}, \forall j \in (a,b,c), \tag{1b}$$

$$v_{\mathrm{y},j} = \sum_{\mathrm{i}=1}^{N} v_{\mathrm{sm,y,i},j} = \sum_{i=1}^{N}\left[S_{\mathrm{yi1},j}v_{\mathrm{cy,i},j} + \left\{\left(1 - S_{\mathrm{yi1},j}\right)\left(1 - S_{\mathrm{yi2},j}\right)v_{\mathrm{cy,i},j}\right\}\mathrm{sgn}\left(i_{\mathrm{y},j}\right)\right], \forall \mathrm{y} \in (\mathrm{p},\mathrm{n}), \forall j \in (a,b,c), \tag{1c}$$

$$\mathrm{sgn}\left(x\right) = \begin{cases} 0 & \text{if} \quad x < 0 \\ 1 & \text{if} \quad x > 0, \end{cases} \qquad v_{\mathrm{cm}} = \frac{1}{6}\sum_{j=a,b,c}\left(v_{\mathrm{n},j} - v_{\mathrm{p},j}\right), \qquad \sum_{j=a,b,c} i_{\mathrm{p},j} = \sum_{j=a,b,c} i_{\mathrm{n},j} \tag{1d}$$

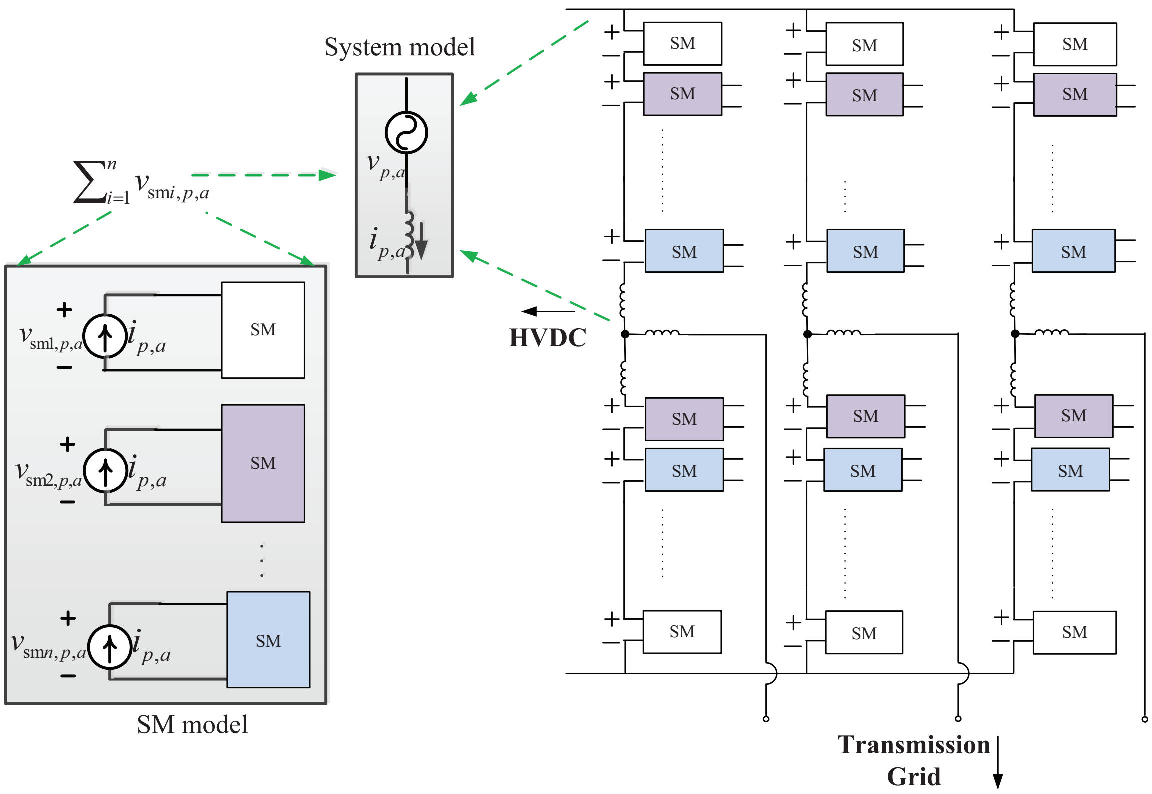

Fig. 1: Circuit diagram of MMC and numerical stiffness based stable separation of states of MMC for faster simulation.

of Silicon Carbide (SiC) MOSFET H-bridge, filter (L_1-R-C), anti-SM, and a stress inductor (L_2). The SiC H-bridge is controlled by the data processing and control unit such that the current through the inductor (L_1) connected to the H-bridge follows the arm current reference. The inductor (L_1) current and the R-C voltage (that are a part of the filter marked in Fig. 3) are measured and fed back to the data processing and control unit for the above-mentioned control purposes. The filter stage is sized to remove the harmonics present in the current and maintain high control bandwidth. The H-bridge is

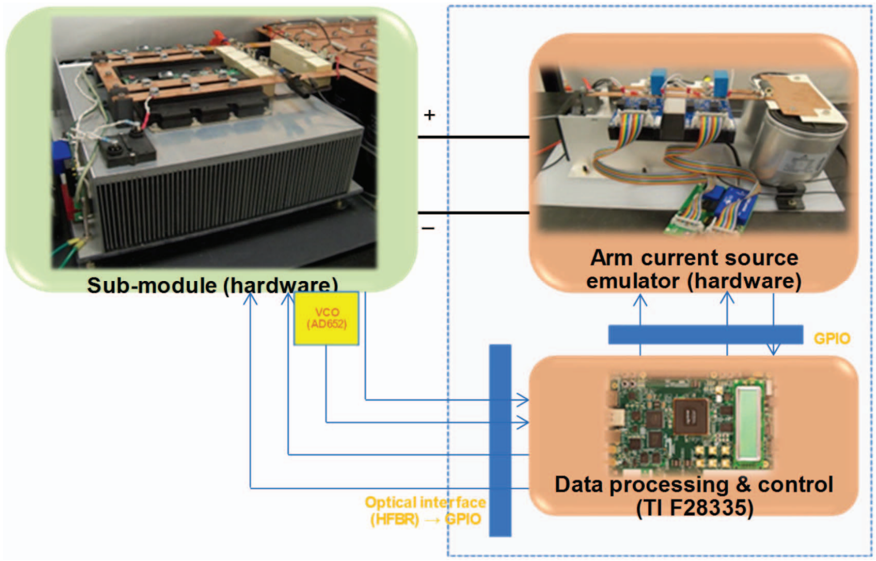

Fig. 2: PE-HIL concept to evaluate an SM in MMC.

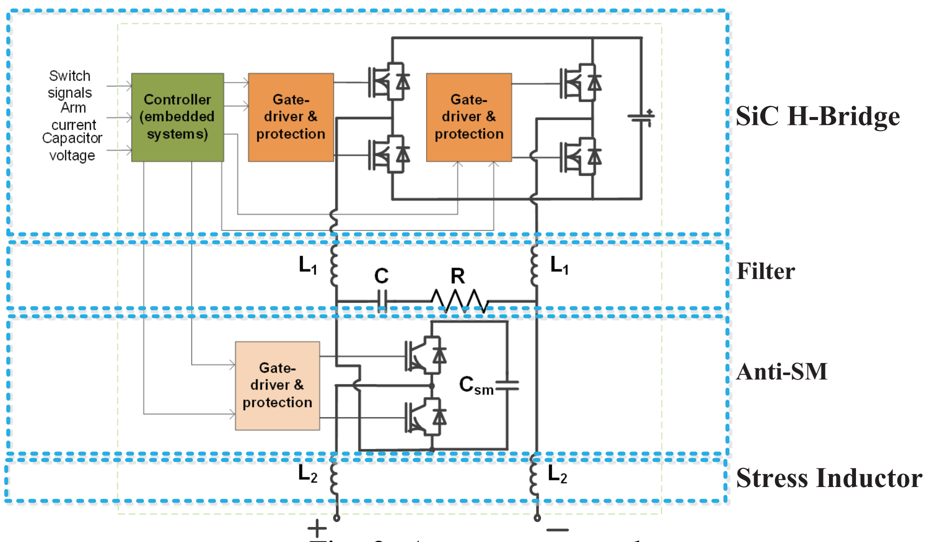

Fig. 3: Arm current emulator.

based on SiC devices, rather than Si devices, to enable high-frequency switching that can reduce the filter size and improve the bandwidth. The anti-SM is controlled to cancel the voltage at the output of the SM to reduce the voltage stress on SiC H-bridge and size of the filter-stage. The SM hardware, which connected to the arm current source emulator, produces a square-wave output voltage with maximum voltage of the order of several kVs. The magnitude of the voltage applied by the dc voltage source connected to the SiC H-bridge depends upon the SM hardware output voltage, desired arm current reference, and size of the filter. It is 2 times higher than the dc-link voltage of the SM capacitor in the absence of the anti-SM. The higher magnitude of the voltage applied requires SiC devices with higher voltage blocking capability, thereby, increasing the cost significantly. Moreover, in the absence of the anti-SM, a larger filter inductor (L_1) is required to remove harmonics present current, which makes it difficult to achieve the desired high control bandwidth. The stress inductor (L_2) reduces the voltage stress on filter and SiC H-bridge that may be observed from latencies in anti-SM and SM switching. It also helps filter the high-frequency components produced by the high-frequency voltage

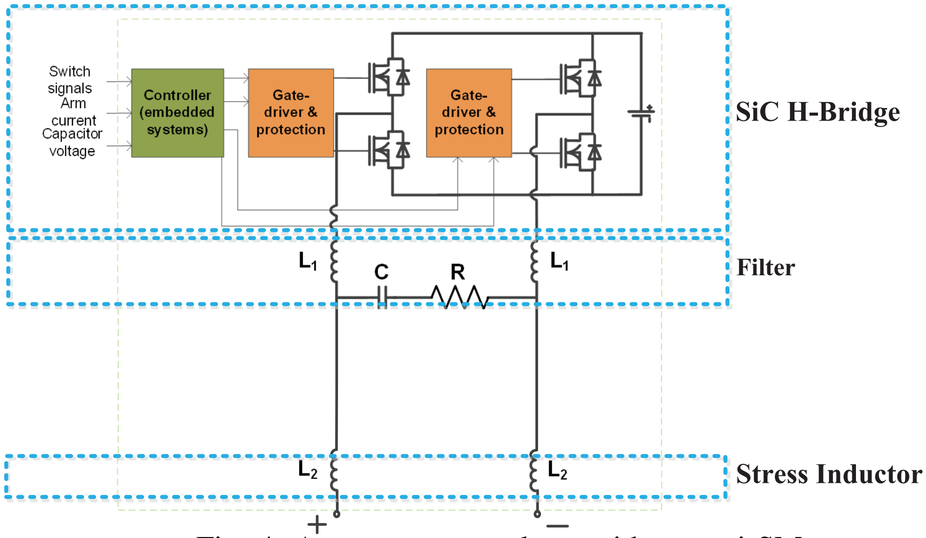

Fig. 4: Arm current emulator without anti-SM.

of the SiC H-bridge.

Without Anti-SM: The design of the arm current source emulator without the anti-SM is shown in Fig. 4. In this case, the voltage required to be produced at the ac-side of the SiC H-bridge is given by

$$v_{\mathrm{HB}} = 2\left(L_1 + L_2\right)\frac{di_{\mathrm{arm}}}{dt} + v_{\mathrm{sm}}, \tag{6}$$

where i_{arm} is the arm current reference and v_{sm} is the SM hardware output voltage. The arm current reference consists of ac and dc components. The frequency of the ac component in the arm current reference is the frequency of the connected ac grid. The peak value of the SiC H-bridge ac-side voltage is given by

$$v_{\mathrm{HB,max}} = 2\omega\left(L_1 + L_2\right)I_{\mathrm{o}} + V_{\mathrm{cap}}, \tag{7}$$

where ω is the grid frequency, $I_{mathrmo}$ is the peak value of the ac component in the arm current reference, and V_{cap} is the capacitor voltage of the connected SM. The value of $v_{\mathrm{HB,max}}$ is 3200 V with $L_1 = 0.5$ mH, $L_2 = 1$ mH, $V_{\mathrm{cap}} = 1600$ V, and $I_{\mathrm{o}} = 1414$. These values were obtained for the MMC-HVdc system described in [5]. That is, the dc-side capacitor voltage of the SiC H-bridge required is 3200 V.

Furthermore, for the currents produced to exactly mimic the arm current reference with low harmonics, a larger filter will be required. This is specially true when the arm current references have low magnitude compared to the rated current.

With the anti-SM, the peak value of the SiC H-bridge ac-side voltage is given by

$$v_{\mathrm{HB,max}} = 2\omega\left(L_1 + L_2\right)I_{\mathrm{o}}. \tag{8}$$

For the parameters mentioned above, the value of $v_{\mathrm{HB,max}}$ is 1600 V. That is, the dc-side capacitor voltage of the SiC H-bridge is 1600 V.

B. HIL Simulator

The HIL simulator simulates the MMC-HVdc system in real-time and generates the arm current and modulation index references at every instant. The real-time simulation of the MMC-HVdc system in the HIL simulator is explained in detail in [6]. The arm current and modulation index references produced by the HIL simulator is sent to the data processing and control unit. The arm current reference is sent in packets containing harmonic component magnitudes in $qd0$ reference frame that includes i_q, i_d, $i_{\mathrm{circ},q}$, $i_{\mathrm{circ},d}$, and $i_{\mathrm{circ},0}$. Similarly, the modulation index reference is also sent in packets containing harmonic component magnitudes in $qd0$ reference frame. The measured frequency from the HIL simulator is also sent to the data processing and control unit. The data processing and control unit controls the current produced by the arm current source emulator at the reference value by varying the switching commands to the arm current source emulator. The data processing and control unit also emulates the local SM controller described in [7]. It produces the SM switching signals based on the arm modulation index reference sent by the HIL simulator. The modulation index is incremented by a small value generated by the local SM capacitor voltage controller. It feeds back the average value of the SM capacitor voltage from the SM hardware to the HIL simulator.

C. Data Processing and Control Unit

The data processing and control unit is based on TI F28335 with a 1G Ethernet adapter (W5500 Ethernet chip or Xpress DR+) that connects it to the HIL simulator. It uses general-purpose input-outputs (GPIOs) to interact with the SM through optical connections and with the arm current source emulator through wires. The optical connection to the SM from the controller is similar to the implementation in a real-world MMC-HVdc substation.

IV. PE-HIL Concept Simulation Results

In this section, a real-world MMC system is considered to simulate the designed PE-HIL concept. A 401-level study MMC system is considered based on the France-Spain MMC-HVDC interconnection described in [5]. Only one MMC is considered. The dc-link is assumed to be a dc-source and the ac-side is assumed to be a 3-phase ac-source. The parameters of the arm current emulator utilized in the simulation of the PE-HIL concept are provided in Table I. The corresponding requirements in the arm current emulator without the anti-SM are also provided in Table I for comparison purposes. The higher inductor shown in Table I for the case without an anti-SM arises due to high harmonics observed in the currents produced when the ac-side current is less than half the rated current in the MMC. The PE-HIL concept simulation parameters are provided in Table II, where the delay between the HIL simulator and data processing and control unit emulates the data transmission delay through Ethernet.

The PE-HIL concept is simulated under two case-studies: (i) steady-state operation and (ii) step-change in the q-axis current reference. The concept is simulated for an arm current emulator with an anti-SM. The corresponding results are presented in

TABLE I: Arm Current Emulator Parameters

Parameter	Value with anti-SM	Value without anti-SM
H-Bridge dc voltage	1600 V	3200 V
L_1	0.5 mH	0.5 mH
L_2	1.0 mH	2.0 mH
C	5 μF	5 μF
R	5 Ω	5 Ω
Switching frequency	10 kHz	10 kHz
Sampling frequency	10 kHz	10 kHz

TABLE II: PE-HIL Simulation Parameters

Parameter	Value
Delay between HIL simulator and data processing and control unit	2 ms
Delay between measured data and data processing and control unit	100 μs

Figs. 5-6. The figures show the PE-HIL amplifier producing the arm currents as determined by the real-time simulation algorithms in the HIL simulator. They also show the SM capacitor voltage of the connected SM to indicate the performance of the connected SM in the PE-HIL concept.

The PE-HIL concept without an anti-SM in the arm current simulator is simulated under two case-studies: (i) steady-state operation and (ii) step-change in the q-axis current reference. The corresponding results are presented in Figs. 7-8. Under steady-state conditions in Fig. 7, the SM capacitor voltages are seen to diverge. Under the step change shown in Fig. 8, it may be observed that the currents have high harmonics in spite of doubling the inductance of L_2. These simulation results indicate the necessity of utilizing an anti-SM, especially when a high-voltage SM is evaluated in the PE-HIL concept.

V. Experimental Results

The PE-HIL amplifier or the arm current source emulator is developed to evaluate SMs from the real-world MMC system described in Section IV. The capacitor voltage in the SM is rated at 1600 V and the SM is capable of withstanding 2000 A current. The amplifier has been developed to produce up to 100 A current and withstand 1600 V produced by the SMs. The corresponding parameters of the arm current emulator for the tests evaluated are provided in Table III.

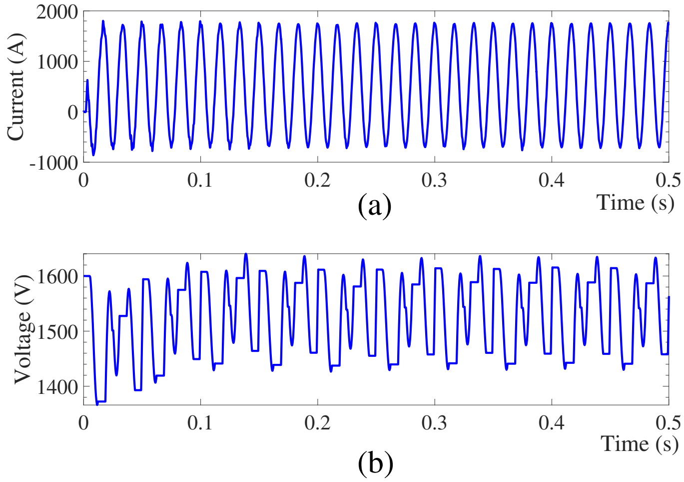

Fig. 5: PE-HIL simulation results with an anti-SM utilized in the arm current emulator and with $i_{q,\mathrm{ref}} = 2828$ A: (a) arm current and (b) SM capacitor voltage.

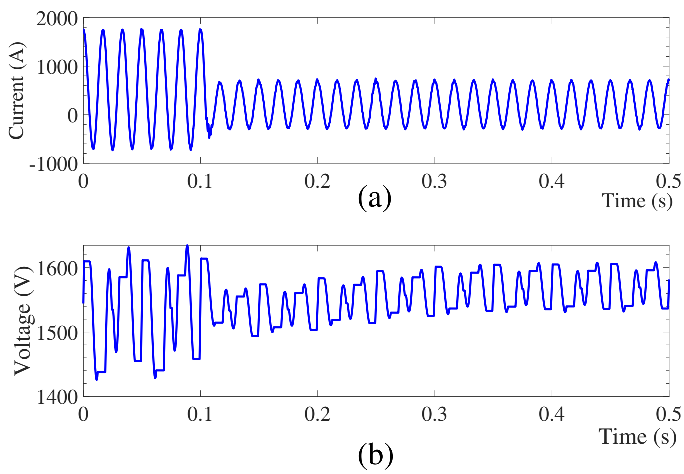

Fig. 6: PE-HIL simulation results with an anti-SM utilized in the arm current emulator and under step-change in $i_{q,\mathrm{ref}}$ from 2828 A to 1000 A: (a) arm current and (b) SM capacitor voltage.

TABLE III: Arm Current Emulator Parameters

Parameter	Value with anti-SM
H-Bridge dc voltage	$150 - 200$ V
L_1	1.0 mH
L_2	4.5 mH
C	5 μF
R	5 Ω
Switching frequency	10 kHz
DSP Sampling frequency	10 kHz

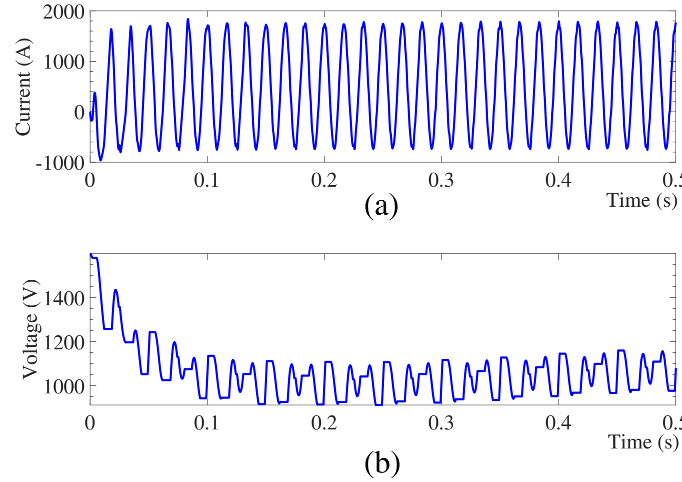

Fig. 7: PE-HIL simulation results with an anti-SM utilized in the arm current emulator and with $i_{q,\mathrm{ref}} = 2828$ A: (a) arm current and (b) SM capacitor voltage.

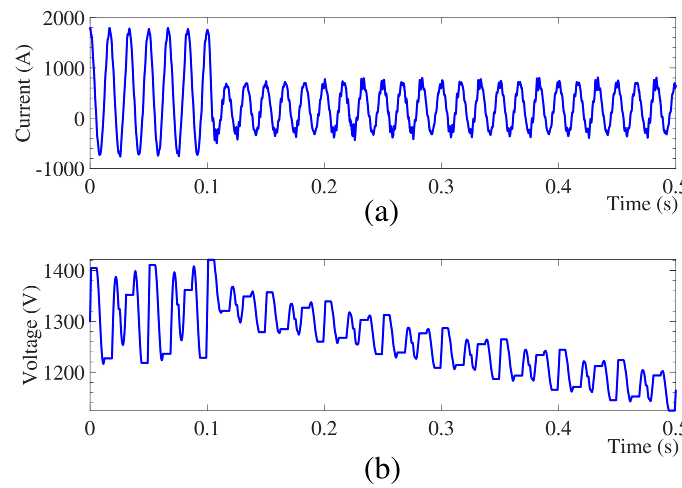

Fig. 8: PE-HIL simulation results with an anti-SM utilized in the arm current emulator and under step-change in $i_{q,\mathrm{ref}}$ from 2828 A to 1000 A: (a) arm current and (b) SM capacitor voltage.

The arm current produced by the PE-HIL amplifier is shown in Fig. 9(a). The reference arm current contains 6.125 A ac and 2.5 A dc, and the H-Bridge dc voltage utilized is 150 V. The arm current produced by the PE-HIL amplifier with H-Bridge dc voltage of 200 V and reference arm current containing 12.25 A ac and 5 A dc is shown in Fig. 9(b). The currents follow the reference closely.

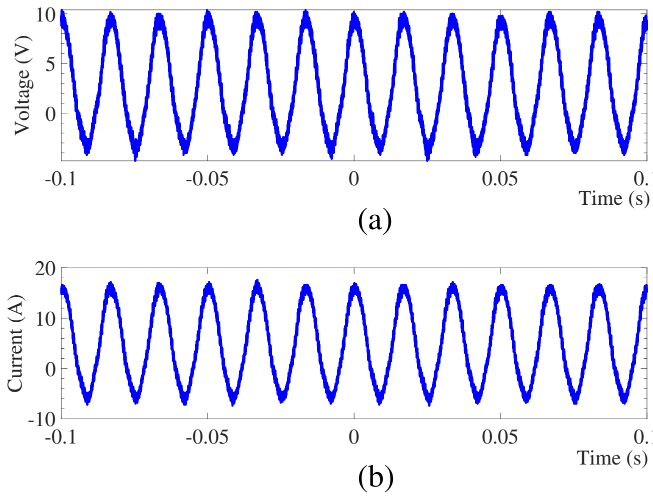

Fig. 9: Currents produced by PE-HIL amplifier in experiments: (a) H-Bridge dc voltage of 150 V, and (b) H-Bridge dc voltage of 200 V.

In each of the cases, the SM capacitor voltage is maintained at 50 V and the SM is switched at approximately 60 Hz.

VI. Conclusions

The PE-HIL concept to evaluate SMs in MMC-HVdc system is presented in this paper. The design of the concept consists of arm current source emulator, HIL simulator, and data processing and control unit. The designed PE-HIL concept is simulated to showcase its successful operation. The arm current source amplifier is designed, developed, and evaluated. Experimental results showcasing the successful operation of the amplifier is presented. In the future, the simulated PE-HIL concept will be experimentally evaluated.

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