SAND2019-1994C

Design Iteration of Medium Voltage, kW-Scale Hybrid Switched Capacitor Converters

Jason Neely, Jarod Delhotal, Josh Stewart, Robert Brocato, Jack Flicker
Sandia National Laboratories, Albuquerque, NM 87185 USA

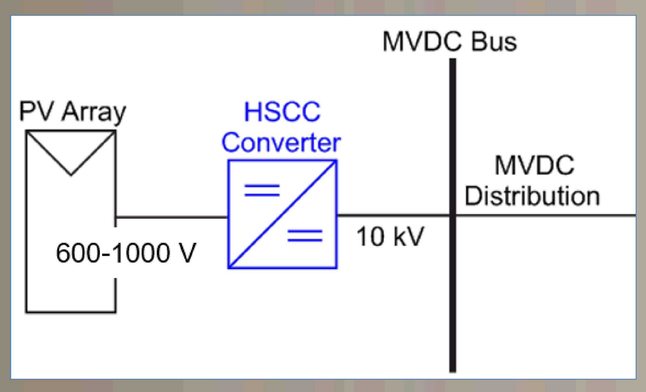
Acknowledgement - This project is funded by ARPA-E under award 1428-1674. The team thanks Dr. Eric Carlson, Dr. Isik Kizilyalli, ARPA-E, and the Department of Energy for their support.

Motivation:

A challenge for fulfilling state and utility renewable portfolio standards is the high levelized cost of solar PV energy ($109.8/MWh) compared to other sources (e.g. a conventional coal plant at $60.4/MWh). The higher cost is due primarily to the high installed cost of commercial and utility scale solar PV systems (relative to capacity factor). Medium voltage DC (MVDC) distribution architectures may realize cost reductions.

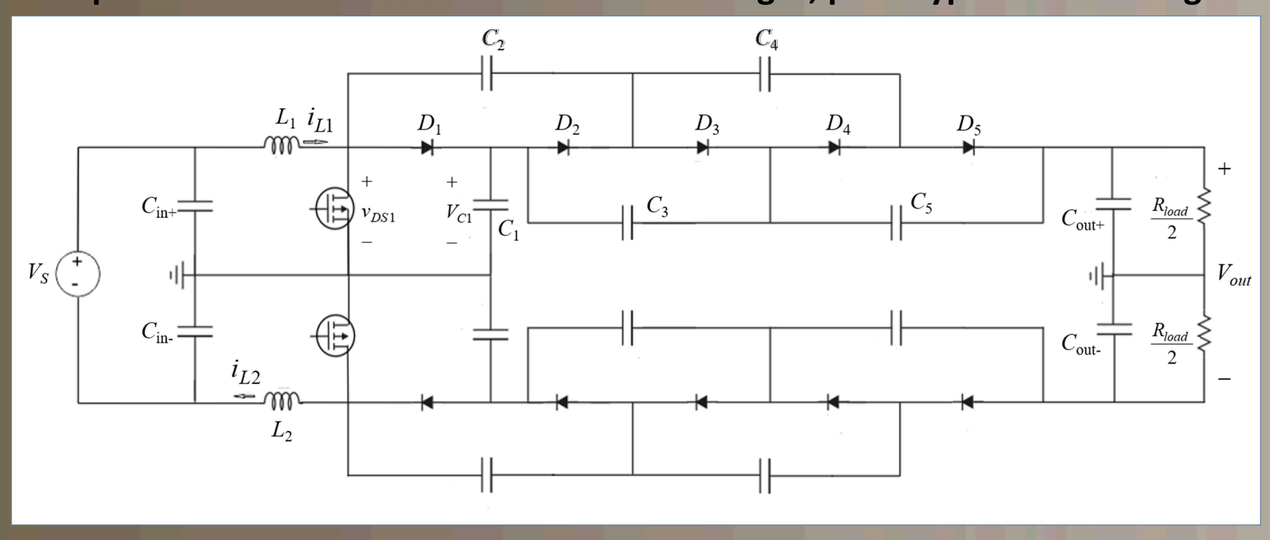
In this work, we developed a novel circuit topology for boosting PV power from the panel array to a medium voltage DC (MVDC) voltage for distribution. Targets are:

- **10 kV output voltage**
- **Gain of up to 20X**
- **> 95% Efficiency**

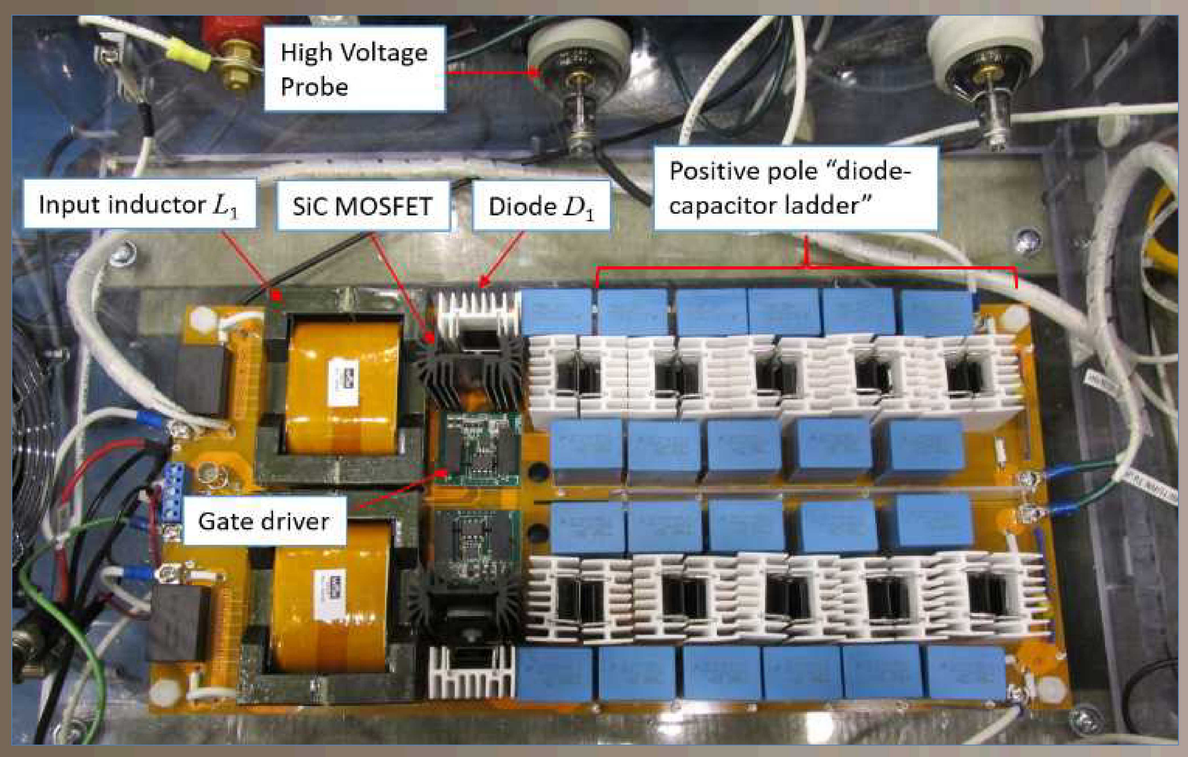


- The HSCC combines a traditional boost converter topology and a "diode-capacitor ladder" with N stages, to act as a voltage multiplier.
- A bipolar HSCC effectively contains two HSCC converters with a positive pole and a negative pole, each with one controlled switch

Bipolar HSCC schematic shown with N=2 stages, prototypes had 4-5 stages

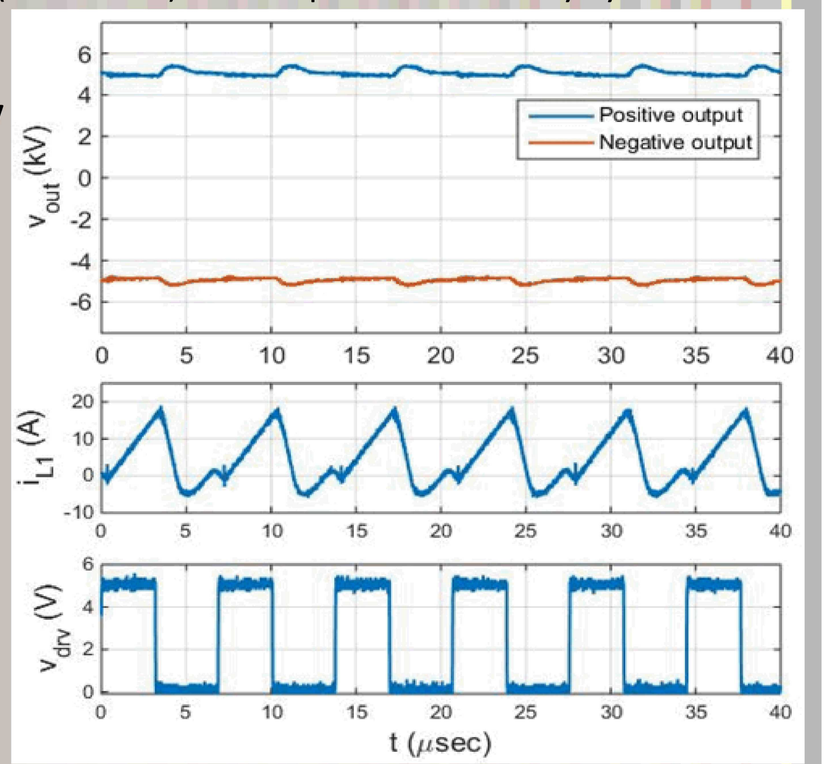


Three prototypes were built and evaluated. Shown here is Prototype 2 with N = 5 stages; the positive and negative poles of the converter occupy the top and bottom halves of the circuit.



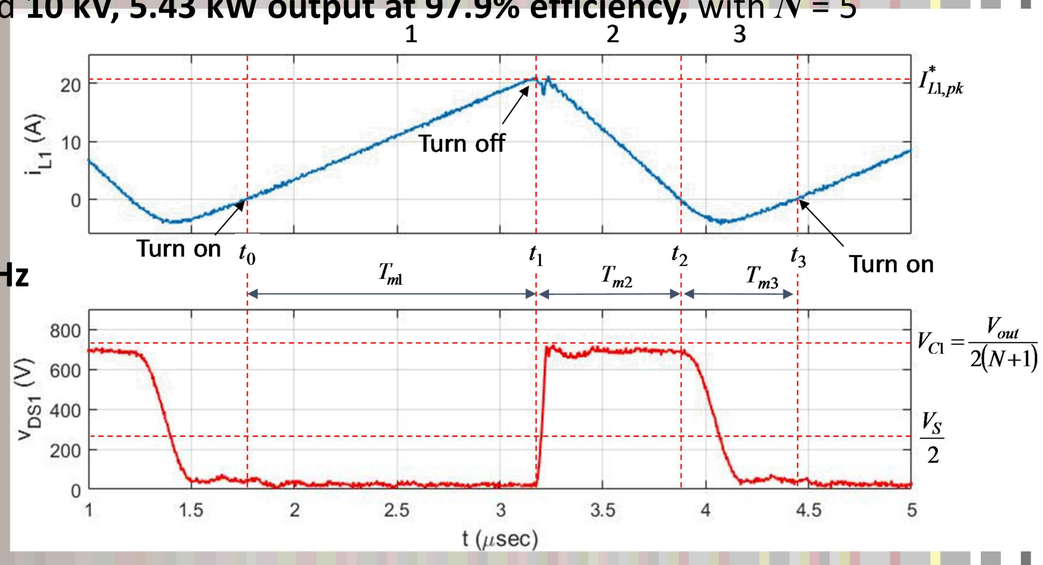
Prototype 1 achieved **10.1 kV, 2.57 kW output with 95.3% efficiency** with a pilot design (with N = 4) and simple constant duty cycle control.

Switching frequency fixed: 140 kHz



Prototype 2 included revisions to circuit parameters and new switching scheme. Circuit parameters were optimized in simulation using validated models. For the control, the MOSFET switches *on* as the inductor current rises through the i_L=0 crossing (reducing loss) and then switches *off* when a reference peak current is reached. Prototype 2 achieved **10 kV, 5.43 kW output at 97.9% efficiency,** with N = 5

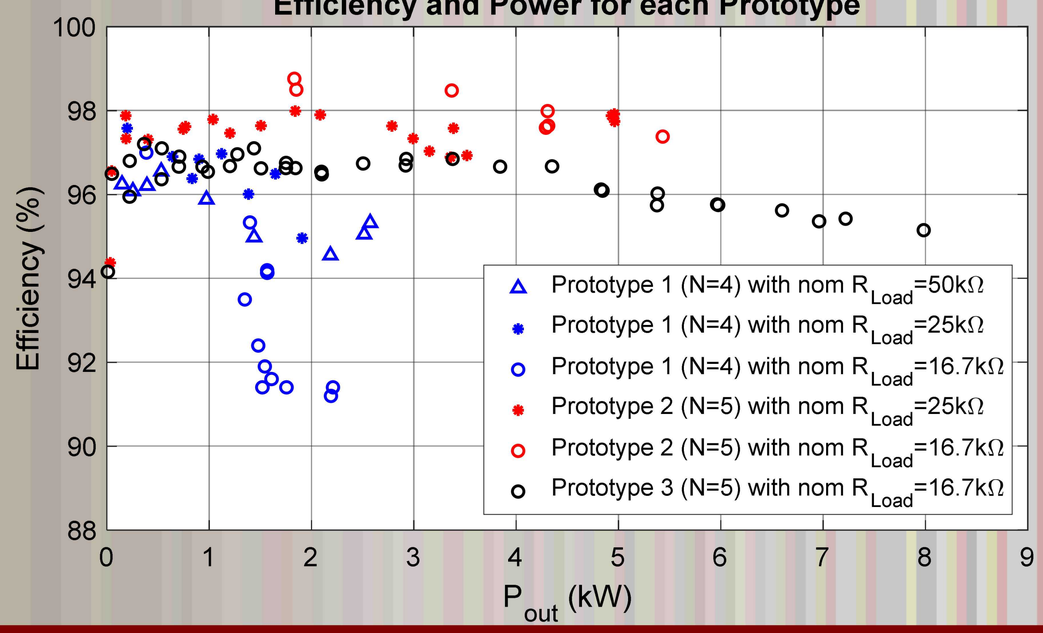
Switching frequency variable: 250-375 kHz



Prototype 3 included a larger heat sink for the MOSFETs. This increased the power handling but added parasitic inductance, reducing efficiency. Prototype 3 (N = 5) achieved **10.7 kV, 7.98 kW, 95.2 % efficiency**.

Prototype	V_{out} (kV)	P_{out} (kW)	Gain at Peak Power	Efficiency (%)
1	10.1	2.57	16.8	95.3
2	10.0	5.43	19.3	97.9
3	10.7	7.98	18.5	95.2

Efficiency and Power for each Prototype



Sandia National Laboratories is a multi-mission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC., a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525. This poster is approved as document 749944.