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Diode-Integrated SiC DMOSFETs

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Built-in P-N body diodes are susceptible to high-voltage drops as well as a possible degradation due to electron-hole recombination induced expansaion of basal plane dislocations in to stack faults [1] regarding Silicon Carbide (SiC) metal-oxide-semiconductor, field-effect transistors (MOSFETs). Due to these conditions, the use of an externally connected anti-parallel SiC Schottky barrier diode (SBD) to suppress the conduction of the intristic P-N diode was implemented. The use of an external SiC SBD incurs both additional chip/assembly costs and presents significant parasitic circuit inductance associated with package or board level interconnection of the the MOSFET with the external SBD. This work features a SiC Double-implanted-MOSFET (DMOSFET) device structure with a junction-barrier-Schottky (JBS) rectifier integrated into the MOSFET unit cell. These high-voltage SiC devices could be used in a variety of power conversion circuits in the next-generation of energy storage, automotive, solar and wind energy systems.

The total chip size of the diode-integrated SiC DMOSFETs is 2.61 mm x 2.61 mm. The device fabrication was conducted on 10 µm thick N- epilayers, designed for supporting a 1200 V breakdown voltage rating. The devices were fabricated on GeneSiC's established 150 mm SiC MOSFET process line.

After device fabrication and on-wafer device characterization, selected chips were diced and packaged into custom packages for more detailed high-current and high-temperature characterization, which is reported in this paper. Figure 1 shows the output characteristics of the diode-integrated MOSFETs in the first and third quadrant of operation up to a drain current of 80 A, as the gate voltages were swept from 0 V to 20 V. In the first quadrant, typical MOSFET characteristics are observed. The device exhibits a $R_{DS,ON}$ of 100 mΩ at V_{GS} = 20 V. In the third quadrant, electrical characteristics resembling a JBS diode are observed instead of the P-N diode characteristics typically observed in a DMOSFET structure. The diode turns on with a knee voltage of ~1V. The bending or flattening of the diode characteristics at higher drain current magnitudes is due to self-heating. The synchronous rectification mode of the DMOSFET is also observed in the third quadrant, with the application of positive gate voltages. Figure 2 shows the temperature stability of the gate threshold voltage, which drops by 50% as the temperature is increased from room-temperature to 150°C. The third quadrant operation measured at 25°C and at 150°C are compared in Figure 3. A clear positive temperature coefficient of diode forward voltage is observed, which is not seen in the parasitic P-N diode of the DMOSFET. This is very important for paralleling multiple die without risk of thermal runaway. The impact of the negative gate bias on the integrated JBS diode performance is shown in Figure 4. At lower source-drain currents, a gate bias invariant characteristics is observed, while the impact of the negative gate bias is more visible at higher source-drain currents, as the parasitic P-N diode of the MOSFET gets activated. The temperature variation of the diode forward voltage is shown in Figure 5. The sub-threshold I-V characteristics measured on the integrated JBS diode is shown in Figure 6. An ideality factor of 1.07 is extracted from these measurements, which is indicative of homogenous Schottky interface. A barrier height of 1.08 eV is also extracted which is typical for the Schottky metal used for fabrication and the associated processing performed for realizing these devices. More detailed data on these devices is presented in the full paper.

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[1] S. H. Ryu *et al.*, "Effect of Recombination-Induced Stacking Faults on Majority Carrier Conduction and Reverse Leakage Current on 10 kV SiC DMOSFETs" Mater. Sci. Forum, vol. 740-742, pp. 1127-1130, 2009.

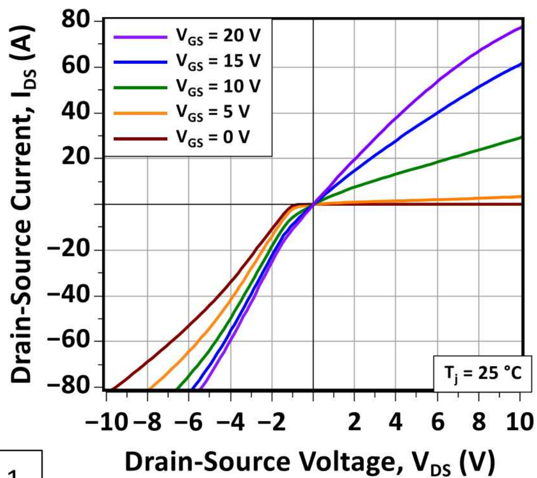


Fig. 1

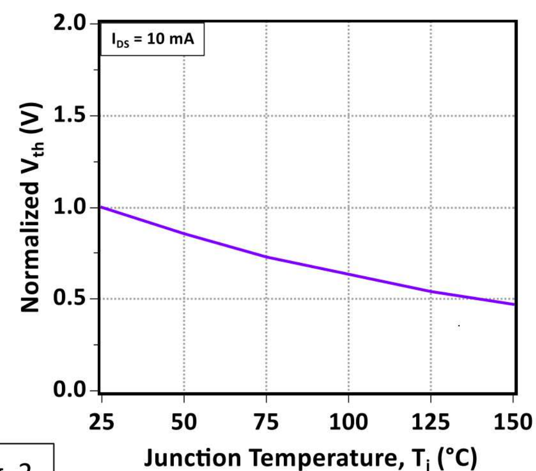


Fig. 2

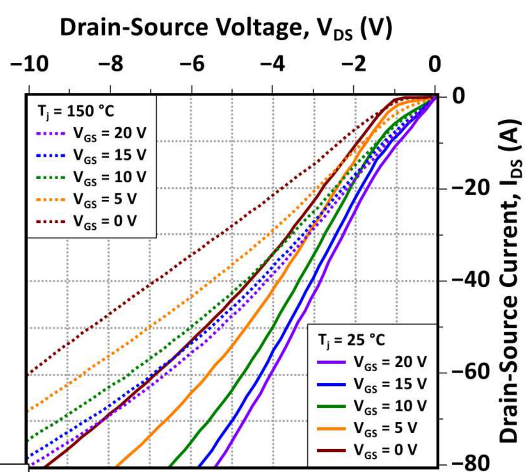


Fig. 3

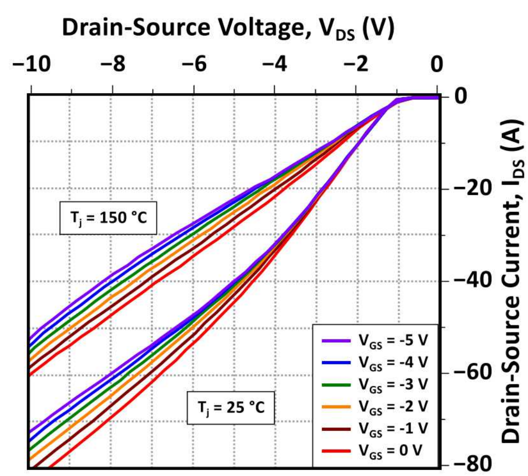
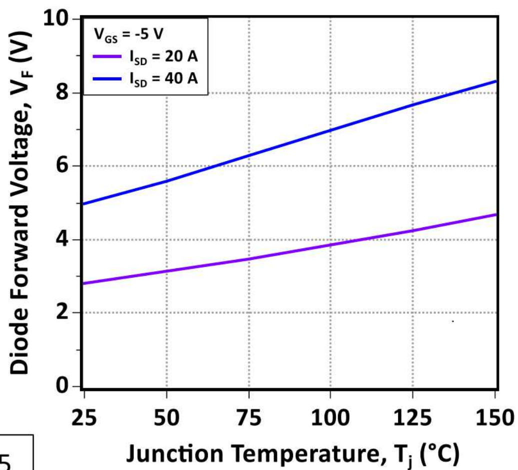
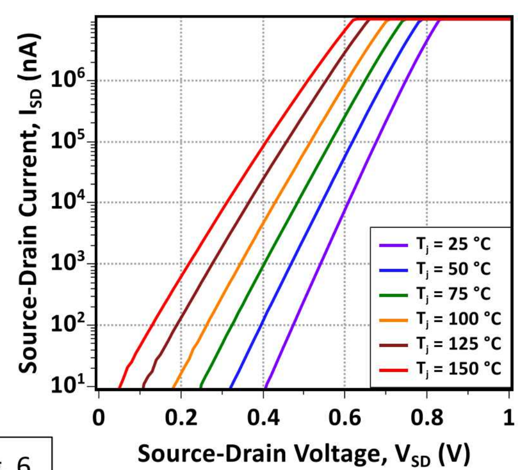


Fig. 4



V_GS = -5 V
I_SD = 20 A
I_SD = 40 A
Diode Forward Voltage, V_F (V)
Junction Temperature, T_j (°C)

Fig. 5



Source-Drain Current, I_SD (nA)
Source-Drain Voltage, V_SD (V)
T_j = 25 °C
T_j = 50 °C
T_j = 75 °C
T_j = 100 °C
T_j = 125 °C
T_j = 150 °C

Fig. 6