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Using Graphene to Enable Trusted Microelectronics

An LDRD Project Final Report

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Prepared by
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Using Graphene to Enable Trusted Microelectronics

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Abstract

This report summaries the work of a 2-year LDRD project aimed at using graphene in integrated circuits in ways that would both obfuscate their function and enhance their level of trust. We have studied (both experimentally and theoretically) process steps, optical properties, design/layout of circuits, and many kinds of analytical techniques. Our conclusion is that graphene shows promise in this application, but additional work must be done to improve compatibility with existing CMOS manufacturing facilities – particularly in the area of contamination.

LDRD: Using Graphene to Enable Trusted Microelectronics

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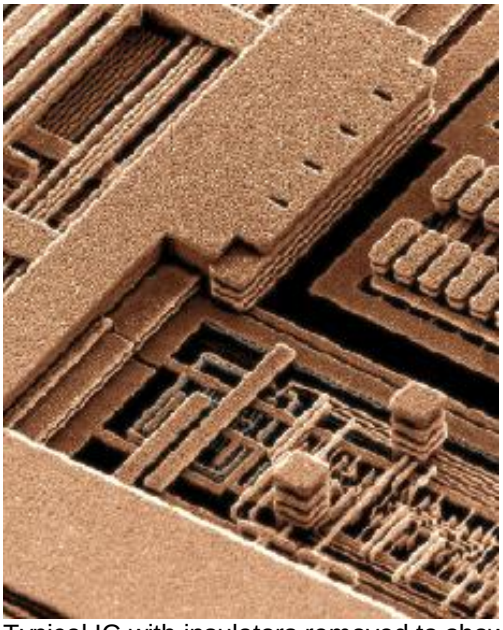
Introduction

Containing up to billions of transistors and literally miles of wiring in an area of about 2-3 square cm, modern microelectronic integrated circuits are amazingly complex. Despite that, they can be reverse engineered by some fairly straightforward techniques. This poses a great risk to systems architects who would prefer that the intent and functionality of their circuitry remain unknown to those who might attempt to subvert, corrupt, or copy the technology.

Microelectronic components are pervasive in both civilian and military/government arenas. While the reverse engineering of the circuits in a child's game might have economic consequences, the loss of trust in components used in the nation's military, intelligence, communications, or utility infrastructure could have disastrous consequences to national security. Because of the ubiquity of microelectronics, the work performed in this LDRD touches *all* government agencies, and our effort to provide *trust* in microelectronic components fits with Sandia's core mission to help ensure the nation's security.

A key element in the reverse engineering process is the mapping of electrical interconnections among the individual devices and circuit modules. In fact, it is the interconnections in the first few layers of wiring that provide the biggest clues to the circuits' intended functions (modern ICs have up to 15 layers of metal wiring stacked on top of each other and separated by thin layers of insulators). The reverse engineering and mapping of these bottom layers is usually done through a combination of optical, x-ray, and SEM techniques. However, if some of the wiring were to be replaced by graphene, which is conductive enough to provide adequate connectivity but is only one atom thick and therefore virtually undetectable, it would be extremely difficult for an



Typical IC with insulators removed to show wiring.

adversary to discern the function of the circuit. Furthermore, the use of undetectable graphene wiring might make it possible to incorporate additional circuitry in the IC, opening up new possibilities for the anti-tamper and counterintelligence communities.

In this context, the use of graphene in ICs is clearly a tool for obfuscation, and could be used as part of a larger program to enhance the level of trust in IC manufacturing. Obfuscation techniques, or trusted-foundry topics in general, are usually not funded by the IC community. Instead, they're typically the purview of anti-tamper or counterintelligence organizations. None of those organizations had approached us on this topic before the start of this LDRD, although we believed there was strong-but-quiet interest. The LDRD program was deemed the best way to develop and transfer this technology.

To the best of our knowledge, the key goal of this LDRD – obfuscation of integrated circuit function through the use of graphene wiring – has not been addressed by any previous work. There are other obfuscation techniques, of course, but they involve adding complexity in the form of additional circuitry (decoys) or imposing layout constraints that could limit circuit density and performance (camouflage, similar to a uniform sea-of-gates). None of them has the "hide in plain sight" simplicity offered by graphene.

Basic graphene growth techniques already existed at Sandia by 2015, and they had been instrumental in providing material for research programs such as special-purpose field effect transistors and sensitive detectors. But processes needed to be developed in the LDRD program that were more compatible with the CMOS materials and processes used in Sandia's Microelectronics Development Laboratory and MicroFab (collectively called the MESA Facility). Graphene films grown at Sandia or obtained commercially were grown on copper substrates and then transferred to silicon wafers containing test circuits. The graphene layers were then patterned using standard photolithography and plasma etch techniques, completing interconnections that were intentionally omitted in the normal metal wiring. After graphene processing, additional wiring was added to the test circuits to mimic patterns that would be found in standard ICs.

Sandia's MESA facility provided a unique environment for this work. The ability to experiment with novel materials and develop new processes in the context of a trusted, relevant, rad-hard CMOS technology exists nowhere else in the DOE complex, university community, or commercial foundries. In this LDRD project, the lure of graphene was obviously its physical thinness – at only 1 atom thick, it should be extremely difficult to detect. However, that same attribute causes problems in handling, processing, inspection, etc. Challenges were also encountered in materials compatibility, contamination, and process damage to graphene, but they were managed more easily with our laboratory's flexible capabilities and eclectic staff.

Total funding for this LDRD project was approximately $470k ($240k in FY15, $230k in FY16), which is roughly equivalent to one-half of an FTE each year.

General Processing and Integration

Principal Contributor: Terri Hickman

In general, some of the details of the process flow depend on the specific kind of graphene device that is being created. For this LDRD, where graphene is being used only as wiring, the process followed the sequence outlined below.

•Standard silicon wafers, <100> orientation, ~20 Ω-cm resistivity.

•Clean the wafers in SC1, SC2 and hydrofluoric acid to remove particles, organics, metal contaminants, and native oxide.

•Deposit 300 nm of SiO_2 using plasma-enhanced chemical vapor deposition (in the μFab tool called “CVD-2”).

•Create a “zero” layer. This layer has no electrical function, and serves only to provide alignment marks for the subsequent layers. This is necessary because the first electrically active layer, graphene, is nearly invisible and would be very difficult to align to. The “zero” pattern is generated by photolithography on a Karl-Suss MJB aligner using AZ5214 photoresist which is spun at 4 krpm and soft baked at 110°C for 90 seconds prior to being exposed for 2.3 seconds at 20 mW/cm^2. An image reversal bake follows this (100°C for 45 seconds), along with a flood exposure for 45 seconds. The final pattern is developed in MF-319 developer for ~45 seconds.

•To complete the “zero” layer, deposit a layer of metal through e-beam evaporation (using the μFab’s Temescal tool). This metal level consists of layers of 20 nm titanium and 200 nm of gold. To complete the liftoff patterning, we immerse parts in acetone for at least ~2 hours (sometimes overnight) to remove metal in areas exposed earlier, along with the photoresist, leaving the metal patterns that make up the zero alignment level.

•The next process steps add graphene via the “trivial transfer method” (discussed in later sections of this report). The substrate and graphene films are submerged in deionized water, and a graphene sheet is carefully positioned above the substrate. Careful maneuvering while lifting the wafer from the water allows the graphene to adhere to the wafer. The wafer with graphene is allowed to dry in air (elevated-temperature bakes might improve the adhesion). Additionally, an extended soak in acetone is necessary to remove the PMMA “handle” film from the graphene (the handle is applied at the time of graphene growth to allow mechanical handling). This sequence is now being done inside the μFab to reduce contamination.

•Photolithography (PR spin, bake, expose, develop, no image reversal) is used again to place an image of the desired graphene structures on the dried film. The graphene is etched using a plasma ashing tool (oxygen plasma).

•Photolithography is used to create a lift-off pattern (in photoresist) for the first electrically active metal layer (called M1, which contacts the graphene).

•Deposit metal (20 nm titanium and 200 nm of gold), soak in acetone to remove PR and liftoff metal.

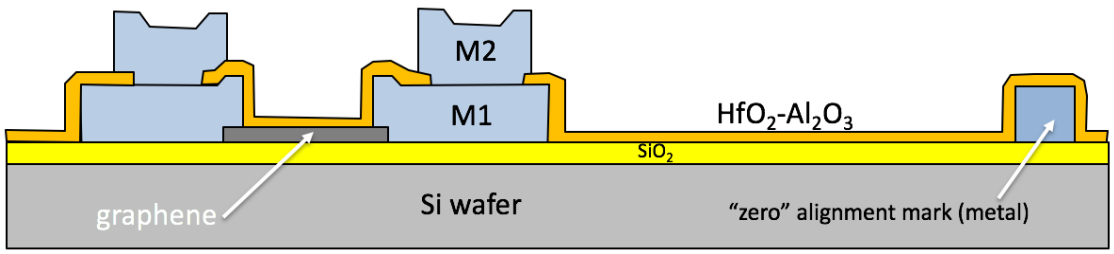
•Because the exposed graphene can be very sensitive to damage – especially from oxygen at high temperatures and/or in plasmas – we've found that it is best to encapsulate it with a thin layer of hafnium oxide. About 1.5 nm of Al_2O_3 is deposited first (aluminum target, e-beam evaporation, with a partial oxygen atmosphere) to promote adhesion. About 50 nm of HfO_2 is deposited using atomic layer deposition equipment at the Center for Integrated Nanotechnologies (CINT).

•Photolithography and chlorine-based plasma etch are used to create openings in the HFO_2/Al_2O_3 insulators for electrical connection to the graphene.

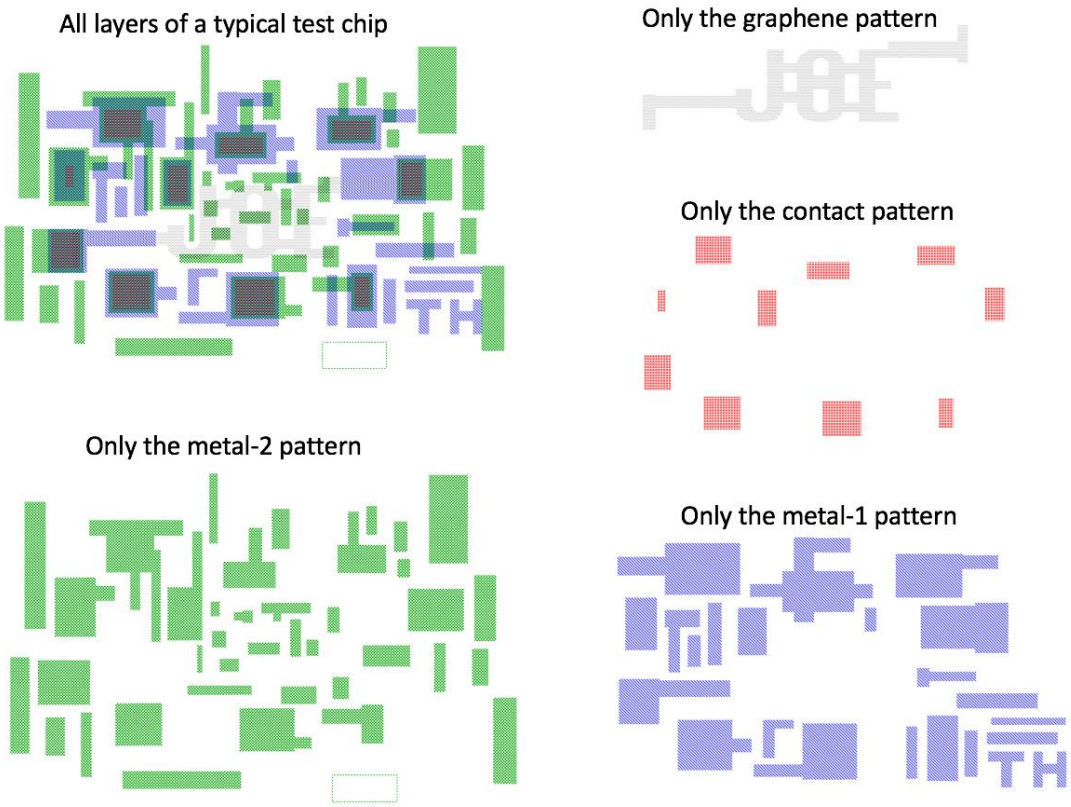
•Then we etch at CINT, in a chlorine-based plasma etch tool.

•The final metal layer (M2) is added by the same lithography, deposition, and liftoff techniques as before. This metal layer provides final interconnections and test pads.

At that point, the part has finished processing and is ready for test.



The next page has diagrams of layer patterns on a typical graphene test chip.



Plan view (from the GDS layout file) of a typical graphene test chip

Chemical Vapor Deposition of Graphene Films

Principal Contributors: Isaac Ruiz, Michael L. Thomas, Stephen W. Howell

At this time, the growth of graphene films by chemical vapor deposition (CVD) is recognized to be the most promising synthesis method of high-quality scalable graphene films, compared to various other popular methods like SiC epitaxial growth and exfoliation/Scotch tape method.[1-4] Although initially the synthesis of graphene through SiC and exfoliation yielded higher quality graphene than CVD graphene, it has always been limited by its scalability for mass manufacturing of electronic grade graphene films.[5] Also, the vast progress made in the CVD growth of graphene over the last 5 years has produced large-area CVD films with comparable carrier mobilities of small exfoliated graphene flakes.[6-8] Thus, here at Sandia National Laboratories, we have begun the transition from SiC epitaxial graphene synthesis to CVD synthesis.

Although there is great promise in CVD graphene, it is also a more involved synthesis method compared to others. Typically, the film is deposited onto a metal catalyst, removed from the catalyst and then transferred onto the preferred substrate. These 3 steps require much care and consideration in order to grow a pristine film and to keep it that way through etching and transfer. The discussion of the growth of CVD graphene will be divided into 3 sections here.

1) The growth mechanism of graphene on metal catalyst, and methods for preparing the metal foil catalyst for growth.
2) The deposition of graphene onto Cu foils.
3) Finally, the removal of the graphene from the metal catalyst and transfer onto the desired substrate.

The three procedures described will demonstrate the complete integration of CVD graphene films onto wafer substrates and ready for device processing and fabrication.

Preparation of Metal Catalyst

There is a myriad of ways to produce graphene by CVD, typically involving varying metal catalysts, precursors, and deposition methods.[9-14] Sandia National Laboratories has decided to focus on graphene deposition onto Cu foil substrates because there are some specific advantages compared to other metals such as Ni, Au, Pt, Rh, or Ir. The massive amount of research on Cu as a metal catalyst has provided a rich amount of information that reveals that high quality, large domain sized films can be produced depending on various growth methods and recipes.[15,16] Cu offers the ability to grow a self-limiting monolayer of graphene compared to Ni, which typically is prone to producing multilayer graphene films.[17] Finally, the cost of Cu compared to some of the other rare earth metals favors future large scale manufacturability for commercial

graphene films, keeping the price per square cm low, especially if the Cu foil can be reused repeatedly, cutting down on waste.

For the growth of graphene films on metals, three things are needed for our synthesis method: A carbon source, a co-catalyst, and a catalyst substrate. In our case, those three are CH_4 gas, H_2 gas, and Cu foil. The copper foil is heated to a high temperature in a tube furnace under the flow of Ar and H_2 gases. Once the growth temperature is reached, CH_4 gas is introduced into the reaction chamber and the deposition of graphene depends. The CH_4 gas decomposes at high temperature and the CH_x adsorbs onto the surface of Cu foil. The H_2 gas also decomposes at the high temperature and single H atoms react with the Cu surface and also further decompose the CH_x molecules on the Cu surface. Films of monolayer/fewlayer CH_x are formed on the surface of the Cu surface which are slowly decomposed down to a hexagonally arranged single layer of carbon.[18,19] The CH_x nucleates on the Cu by reacting with defect sights on the Cu surface. This will form several nucleation sites across the foil surface, where each nucleation site produces a single-orientation graphene crystal as shown in Figure 1. These crystals are randomly oriented and when they coalesce into a single film they produce a polycrystalline film. The carrier mobility in the film decreases as the graphene grain size decreases, so large polycrystalline graphene films or completely single crystal films are preferred for high quality films. Because the nucleation density of the graphene domains is directly a function of the number of defect sites on the Cu foil surface, it is of utmost importance to be able to control the surface morphology of the Cu foil.[20]

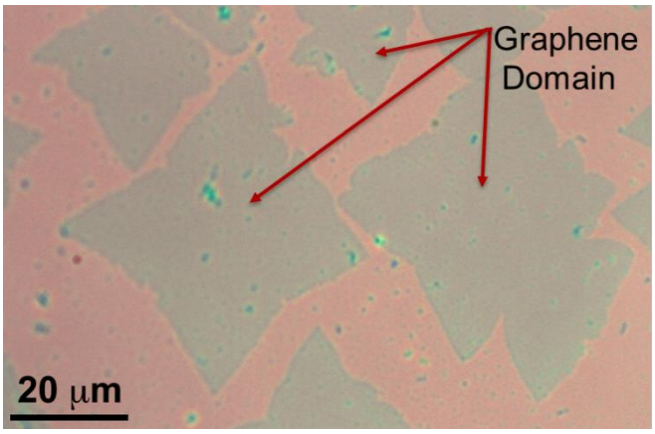


Figure 1: Graphene domains on SiO_2.

Because of the importance of the Cu foil surface in determining the quality of complete graphene films, it is vital to be able to tailor the Cu surface in order to produce the best graphene possible. In our case we have taken two approaches to reducing the number of defect sites on the surface. The first is to treat the commercially purchased Cu foil by a chemical polishing technique. This provides several benefits: it cleans the Cu surface by getting rid of any organic materials or contamination that have been left on the surface from the foil fabrication process, and it gets rid of any oxide layer that may have

formed on the surface of the foil. This chemical polishing leaves behind a pristine Cu surface.

The second approach is a polishing that can lower the number of defects sites on the surface by reducing the surface roughness of the film. Overall, the polishing promotes a self-limiting monolayer film, larger grain sizes, and a reduction in the amount of morphological damage (e.g., wrinkles and tears) that can be induced by the Cu foil during transfer.

The procedure for polishing is very straightforward. Two pieces of Cu foil are cut to similar sizes. They are immersed in an electrochemical solution of H_2O, phosphoric acid, isopropanol, ethanol, and urea. The piece we want to polish is treated as the cathode and the other piece is the anode. They are separated by a few cm and held parallel to each other while a voltage is applied between the samples. Conditions for the polishing can vary depending on the size of the Cu foil; the voltage varies from 2-6 V. Typically, higher voltages are needed for larger Cu samples. The typical setup is shown in Figure 2. Through this method the surface roughness of the Cu foil can be reduced from about 70 nm to 2-3 nm. This greatly reduces the number of defect sites for the graphene to nucleate on. Potentially the number of defect sites can also be controlled by varying the amount of time the foil is polished.

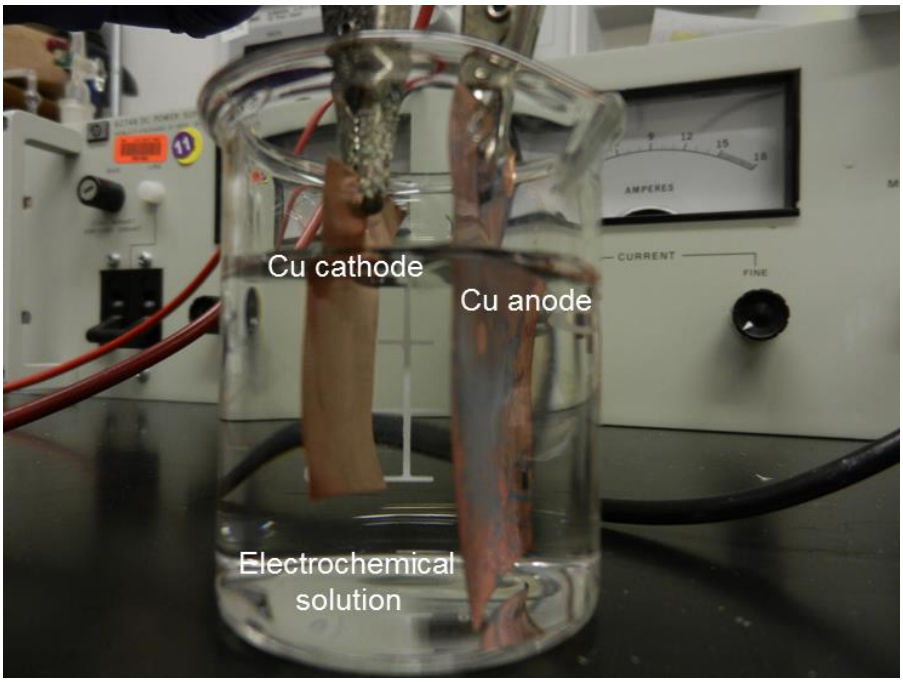


Figure 2: Basic electrochemical polishing setup.

CVD Synthesis of Graphene Films

There are several critical factors to consider when developing growth recipes for CVD graphene. First, further preparation of the Cu foil before the deposition of graphene can be done in a form of an annealing step. Annealing of the foil can further reduce the number of defect sites on the Cu surface by creating larger grain sizes on the Cu foil and by also further reducing the surface roughness of the film. Second, there are many parameters to take into account to customize the graphene growth recipe, including pressure, temperature, gas flow, and growth time. Slight changes in any of these parameters can affect film characteristics such as grain size, continuity, and uniformity. Thus careful control of these parameters is critical in order to grow films of desired characteristics.

Sandia National Laboratories' goal has been to develop our own in-house CVD capabilities in order to transition from the use of commercially purchased graphene. In order for this to happen we need to produce higher-quality films than we are currently purchasing from ACS Materials. In this case, the quality of the film will be judged by 3 main factors: graphene grain size, carrier mobility, and uniformity. Initial experiments were aimed at varying the pressure on a baseline recipe with fixed growth temperature and gas flows. These gas flows were at a ratio of 1:4 of CH_4:H_2 and at a temperature of 1000°C. Although these values are probably not optimal, we know that they can produce graphene films in a relatively short amount of time (<1 hour). The growth time was varied only for the purpose of trying to quantify the graphene domain sizes, because once the graphene domains begin to coalesce they can no longer be measured easily. Therefore, in order to measure the domain size we stopped the growth before it coalesced into a complete film. This allowed us to visually see the domains under an optical microscope. Thus for all intents and purposes, the only parameter that was varied was the pressure. Any results of domain size can be extended to complete films by only increasing the growth time.

Figure 3 shows what a typical commercially-available ACS Materials trivial transfer graphene sheet looks like. Figure 3A shows a trivial transfer film on a SiO_2 substrate. It can be seen that there is a monolayer film with sporadic bilayer and trilayer regions across the film. The Raman mapping of the 2D peak area (Figure 3B) also shows a monolayer region with multilayer regions across the surface. The Raman spectra in Figure 3C also confirm the presence of mono-, bi-, and tri-layers in the film along with showing that the quality is fairly good, as evidenced by the low D peak at ~1350 cm^{-1}. Although it is a difficult process to measure the grain size of these films (due to the presence of the multilayer regions) we can set an upper limit for the average grain size of the film. Because the multilayer regions will form at the same nucleation site that the monolayer region below nucleates, we can assume that the distance between two multilayer grain centers is the size of the monolayer grain. Again, assuming that the nucleation is relatively uniform across the copper we can determine that the average

grain size is the average distance between the multilayer nucleation sites. Because not every nucleation site will form a bilayer region there won't be uniform bilayer regions but there should be a uniform nucleation density (in reality this isn't always the case because the nucleation density can change according to which parts of the Cu foil are exposed to the reaction gases first; thus the nucleation density can vary across the foil). This means that although we can measure the distance between multilayer regions, at best that is the largest grain size possible. There is no guarantee that there is not a smaller monolayer grain in between the multilayer region, but because we cannot tell optically we can only assume the upper limit of the average grain size to be the average distance of the between multilayer grains, with the possibility that they can be smaller. Thus for the ACS graphene presented in Figure 3 the average grain size seems to be between 10 and 20 microns.

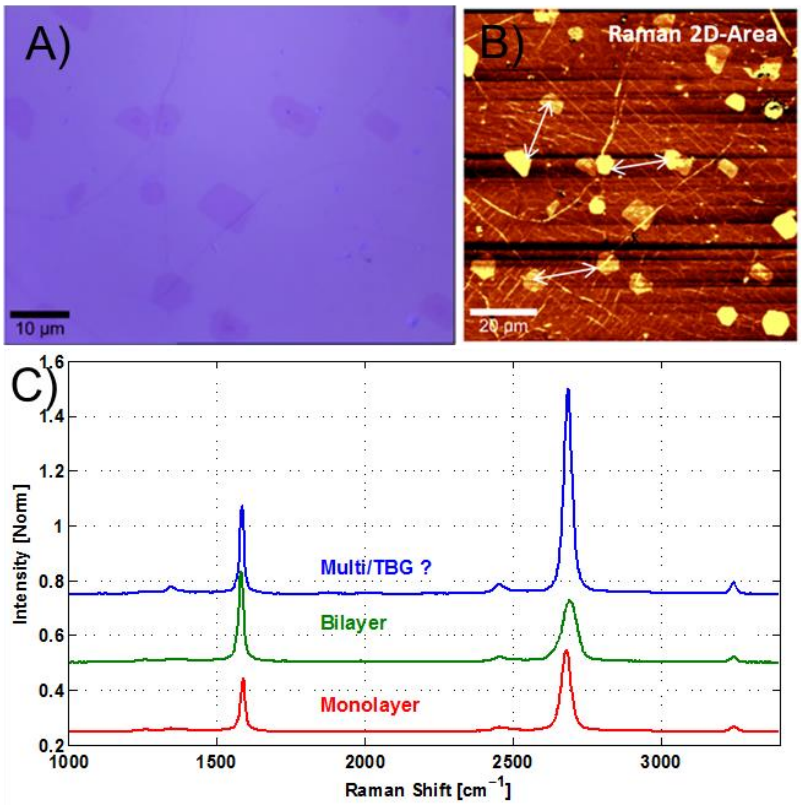


Figure 3: ACS Material's Trivial Transfer graphene sheet. A) Optical image of the transferred graphene film on an SiO_2 substrate. B) 2D peak area Raman maps of the graphene film. C) Raman spectra of various point across the graphene film.

Although the multilayer regions are helpful for determining grain size, they are not good for the film in terms of uniformity. The multilayer regions in the film degrade device performance by acting as scattering sites for charge carriers when a field is applied to the film. Also, as seen in Figure 3B, they provide an enhanced optical contrast that is

contrary to the “obfuscation” element of this LDRD. Therefore, the goal for SNL graphene synthesis is to reduce or completely eliminate the formation of these bilayer regions. As far as carrier mobility of the ACS graphene, previous measurements on the films indicate a value of ~1000 cm^2/Vs. With mobility values reported in publications up to 2 orders of magnitude larger, there is plenty of room for mobility improvement.[15]

Initial experiments to synthesize SNL graphene focused on matching and then exceeding ACS’s graphene in terms of grain size and uniformity. By reducing the pressure, we were able to demonstrate the control of the nucleation density across the Cu foil as shown in Figure 4. All these films were grown for the same time (30 minutes) but at various pressures. It can be seen that as the pressure decreases from 5 Torr

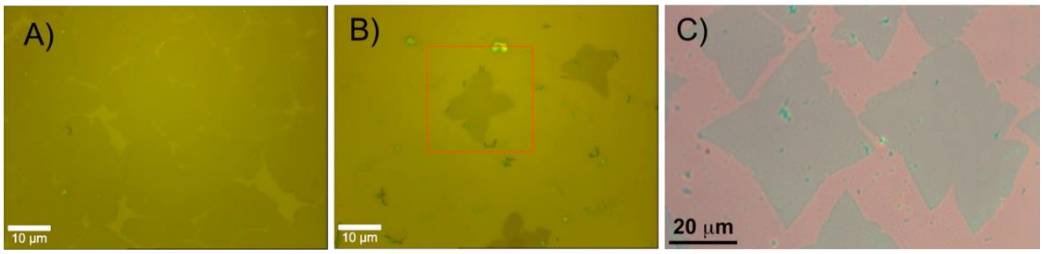


Figure 4: Control of nucleation density of SNL grown CVD graphene. Synthesized at A) 5 Torr, B) 1 Torr, and C) 0.5 Torr.

to 0.5 Torr the nucleation density is reduced, allowing the growth of grain sizes ranging from 10 microns all the way to approximately 60 microns. This already surpasses what we have seen from the commercially available ACS material. Another observation that can be made from Figure 4 concerns the uniformity of the film. Although the graphene has not yet coalesced, it can be seen that no bilayer or multilayer regions are apparent in the graphene. This due to the polishing of the Cu foil done beforehand. Thus we can show that our films are more uniform.

Figure 5 below shows an optical and Raman mapping of an SNL CVD graphene film that is just about to coalesce. Again no multilayer regions are observed in either the optical or Raman map of the 2D peak area. Furthermore, the Raman spectra in Figure 5C shows that the film is of at least the same quality as the ACS material due to the lack of a strong D peak at around 1350 cm^{-1}.

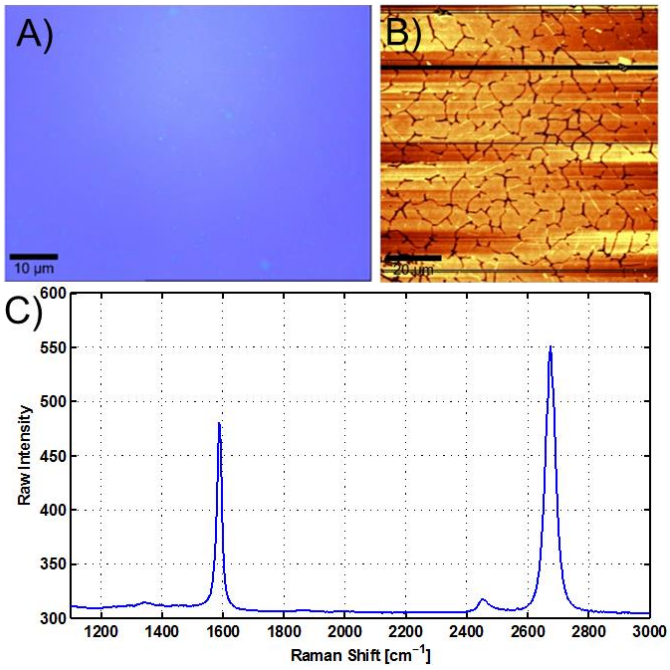


Figure 5: SNL synthesized graphene A) optical image, B) Raman mapping and C) spectra.

Carrier mobility values for the various films have not been measured. Although we have made working FET devices (as part of other programs) we are still optimizing our recipes and transfer techniques in order to produce high-mobility graphene sheets.

Transfer of Graphene Films

Although the graphene film can become contaminated though the CVD process, the biggest source of contamination and damage to the film is the transfer.[21-23] Therefore, careful control of the process needs to be taken in order to reduce any degradation of the graphene film. For the moment we have decided to use wet transfer techniques to remove the graphene and apply it to the desired substrates. We have focused on two different methods. The first method is a wet chemical etch method and the second is an electrochemical delamination method. Both methods begin by applying a thin coat of PMMA onto the graphene/Cu foil. The PMMA acts as protective layer to hold the graphene together. Attempting the transfer without PMMA will result in the destruction of the graphene film.

For the wet etching transfer we suspend the PMMA/graphene/Cu stack on the surface of an etchant such as $FeCl_3$. The $FeCl_3$ etches the Cu, leaving behind a suspended sheet of PMMA/graphene. The sample is then fished out on a glass slide and rinsed with DI water several times to reduce any particle contamination from the etch. The PMMA/graphene is transferred onto a desired substrate (e.g., silicon wafer) and dried.

Once it has dried the PMMA layer can be washed away with acetone and IPA leaving behind a graphene film. The potential pitfalls of this method are that the physical handling of the film can begin to damage it, causing tears and wrinkles. Also, the method is likely to contaminate the graphene film from both the sides. During the etching process, copper, copper chloride, and iron chloride particles can attach to the underside of the graphene, while the PMMA on the top surface can leave behind residue even after having been rinsed off. Both of these contaminations can degrade the quality of the graphene film.

In order to avoid the contamination from the etching process, we switched to an electrochemical delamination method. In this procedure, a negative voltage is applied to the PMMA/graphene side of the foil and the Cu side of the foil. A positive voltage is a then applied to a counter electrode in a solution NaOH. When the PMMA/graphene/Cu stack is submerged in the NaOH, a charge builds on the graphene and Cu foil, and they begin to repel one another. The PMMA/graphene begins to delaminate from the copper foil and then become suspended in the NaOH solution. The steps that follow are the same as in the wet etching process: the PMMA/graphene film is transferred and rinsed in DI water to reduce any Na contamination and then transferred onto a substrate. Again there is a risk of damaging the graphene through this transfer process due to the physical handling of the graphene and foil, so high care must be taken to avoid substantial damage to the film.

In conclusion, we have demonstrated the capability to synthesize graphene by CVD for the first time here at SNL. Processes needed to grow high quality graphene and transfer the materials onto substrates were developed and demonstrated. Also the control of the graphene nucleation density was demonstrated; when compared to the previously utilized commercially available ACS graphene, it was shown that the SNL graphene films are more uniform and composed of larger graphene grains. Going forward, refinement and optimization of the growth parameters will be pursued in order to yield significantly higher-mobility graphene than available from ACS materials.

References

1) Ni, Z. H., W. Chen, X. F. Fan, J. L. Kuo, T. Yu, A. T. S. Wee, and Z. X. Shen. "Raman spectroscopy of epitaxial graphene on a SiC substrate." *Physical Review B* 77, no. 11 (2008): 115416.
2) Virojanadara, Chariya, M. Syväjarvi, Rositsa Yakimova, L. I. Johansson, A. A. Zakharov, and T. Balasubramanian. "Homogeneous large-area graphene layer growth on 6 H-SiC (0001)." *Physical Review B* 78, no. 24 (2008): 245403.
3) Wang, Xiqing, Pasquale F. Fulvio, Gary A. Baker, Gabriel M. Veith, Raymond R. Unocic, Shannon M. Mahurin, Miaofang Chi, and Sheng Dai. "Direct exfoliation of natural graphite into micrometre size few layers graphene sheets using ionic liquids." *Chemical Communications* 46, no. 25 (2010): 4487-4489.

4) Zhu, Jun. "Graphene production: New solutions to a new problem." *Nature nanotechnology* 3, no. 9 (2008): 528-529.
5) Pan, Wei, Stephen W. Howell, Anthony Joseph Ross III, Taisuke Ohta, and Thomas A. Friedmann. "Observation of the integer quantum Hall effect in high quality, uniform wafer-scale epitaxial graphene films." *Applied Physics Letters* 97, no. 25 (2010): 252101.
6) Petrone, Nicholas, Cory R. Dean, Inanc Meric, Arend M. van Der Zande, Pinshane Y. Huang, Lei Wang, David Muller, Kenneth L. Shepard, and James Hone. "Chemical vapor deposition-derived graphene with electrical performance of exfoliated graphene." *Nano letters* 12, no. 6 (2012): 2751-2756.
7) Gannett, W., W. Regan, K. Watanabe, T. Taniguchi, M. F. Crommie, and A. Zettl. "Boron nitride substrates for high mobility chemical vapor deposited graphene." *Applied Physics Letters* 98, no. 24 (2011): 242105.
8) Boyd, D. A., W-H. Lin, C-C. Hsu, M. L. Teague, C-C. Chen, Y-Y. Lo, W-Y. Chan et al. "Single-step deposition of high-mobility graphene at reduced temperatures." *Nature communications* 6 (2015).
9) Coraux, Johann, Martin Engler, Carsten Busse, Dirk Wall, Niemma Buckanie, Frank-J. Meyer Zu Heringdorf, Raoul Van Gastel, Bene Poelsema, and Thomas Michely. "Growth of graphene on Ir (111)." *New Journal of Physics* 11, no. 2 (2009): 023006.
10) Li, Xuesong, Weiwei Cai, Jinho An, Seyoung Kim, Junghyo Nah, Dongxing Yang, Richard Piner et al. "Large-area synthesis of high-quality and uniform graphene films on copper foils." *Science* 324, no. 5932 (2009): 1312-1314.
11) Kondo, Daiyu, Shintaro Sato, Katsunori Yagi, Naoki Harada, Motonobu Sato, Mizuhisa Nihei, and Naoki Yokoyama. "Low-temperature synthesis of graphene and fabrication of top-gated field effect transistors without using transfer processes." *Applied physics express* 3, no. 2 (2010): 025102.
12) Gao, Libo, Wencai Ren, Huilong Xu, Li Jin, Zhenxing Wang, Teng Ma, Lai-Peng Ma et al. "Repeated growth and bubbling transfer of graphene with millimetre-size single-crystal grains using platinum." *Nature communications* 3 (2012): 699.
13) Li, Zhancheng, Ping Wu, Chenxi Wang, Xiaodong Fan, Wenhua Zhang, Xiaofang Zhai, Changgan Zeng, Zhenyu Li, Jinlong Yang, and Jianguo Hou. "Low-temperature growth of graphene by chemical vapor deposition using solid and liquid carbon sources." *ACS nano* 5, no. 4 (2011): 3385-3390.
14) Dato, Albert, Velimir Radmilovic, Zonghoon Lee, Jonathan Phillips, and Michael Frenklach. "Substrate-free gas-phase synthesis of graphene sheets." *Nano letters* 8, no. 7 (2008): 2012-2016.
15) Hao, Yufeng, M. S. Bharathi, Lei Wang, Yuanyue Liu, Hua Chen, Shu Nie, Xiaohan Wang et al. "The role of surface oxygen in the growth of large single-crystal graphene on copper." *Science* 342, no. 6159 (2013): 720-723.
16) Hao, Yufeng, Lei Wang, Yuanyue Liu, Hua Chen, Xiaohan Wang, Cheng Tan, Shu Nie et al. "Oxygen-activated growth and bandgap tunability of large single-crystal bilayer graphene." *Nature nanotechnology* (2016).

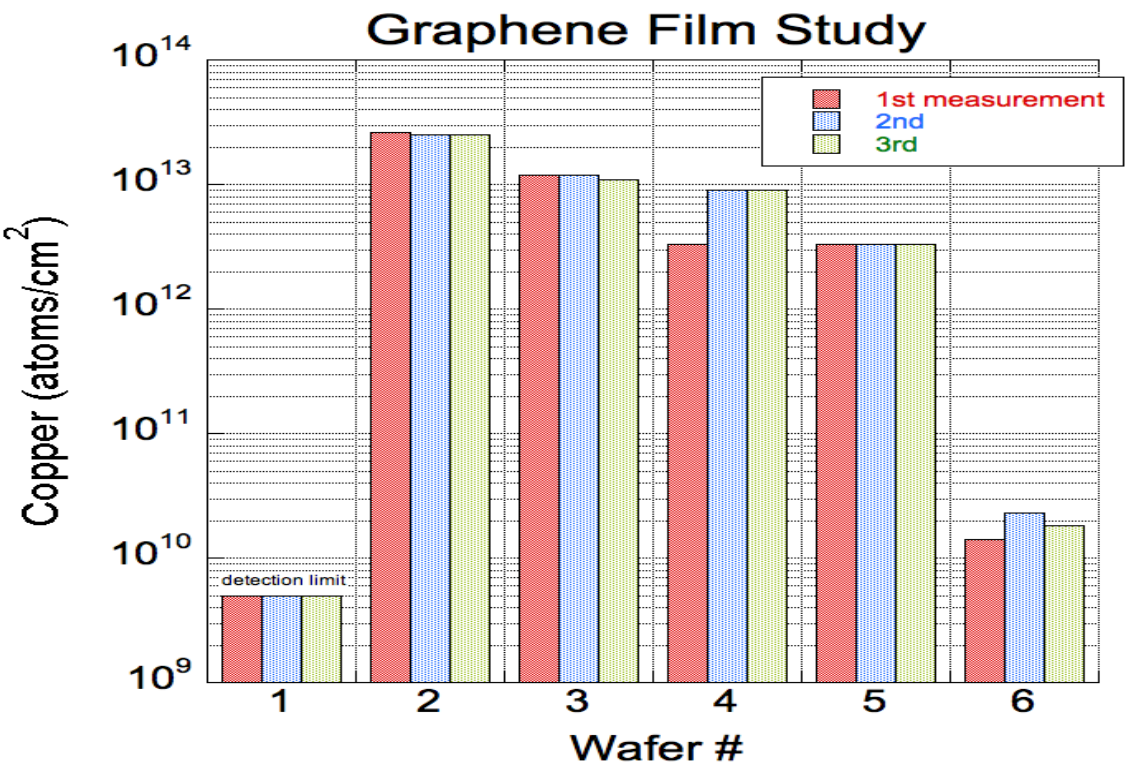
17) Velasco, J. Marquez, S. A. Giamini, N. Kelaidis, P. Tsipas, D. Tsoutsou, G. Kordas, Y. S. Raptis, N. Boukos, and A. Dimoulas. "Reducing the layer number of AB stacked multilayer graphene grown on nickel by annealing at low temperature." *Nanotechnology* 26, no. 40 (2015): 405603.
18) Li, Qiongyu, Harry Chou, Jin-Hui Zhong, Jun-Yang Liu, Andrei Dolocan, Junyan Zhang, Yinghui Zhou, Rodney S. Ruoff, Shanshan Chen, and Weiwei Cai. "Growth of adlayer graphene on Cu studied by carbon isotope labeling." *Nano letters* 13, no. 2 (2013): 486-490.
19) Luo, Zhengtang, Seungchul Kim, Nicole Kawamoto, Andrew M. Rappe, and AT Charlie Johnson. "Growth mechanism of hexagonal-shape graphene flakes with zigzag edges." *Acs Nano* 5, no. 11 (2011): 9154-9160.
20) Li, Xuesong, Luigi Colombo, and Rodney S. Ruoff. "Synthesis of Graphene Films on Copper Foils by Chemical Vapor Deposition." *Advanced Materials* (2016).
21) Ruiz, Isaac, Wei Wang, Aaron George, Cengiz S. Ozkan, and Mihrimah Ozkan. "Silicon oxide contamination of graphene sheets synthesized on copper substrates via chemical vapor deposition." *Advanced Science, Engineering and Medicine* 6, no. 10 (2014): 1070-1075.
22) Staley, N., H. Wang, C. Puls, J. Forster, T. N. Jackson, K. McCarthy, B. Clouser, and Y. Liu. "Lithography-free fabrication of graphene devices." *Applied physics letters* 90, no. 14 (2007): 143518.
23) Joiner, Corey A., Tania Roy, Zohreh Razavi Hesabi, Bhaswar Chakrabarti, and Eric M. Vogel. "Cleaning graphene with a titanium sacrificial layer." *Applied Physics Letters* 104, no. 22 (2014): 223109.

Contamination of Graphene

Graphene would be considered a new material in almost any integrated circuit manufacturing facility, and therefore would be introduced only after very careful consideration. However, carbon itself certainly isn't the problem – the photoresist films that are used dozens of times in a typical IC process flow are, after all, chiefly carbon. Carbon-doped oxides have also made appearances in modern ICs.

The main concern with graphene is the element that is still commonly clinging to its surface after the graphene film is transferred to a silicon wafer – copper. (The processes for growing graphene on a copper foil and then transferring it to a silicon wafer are discussed in other sections of this report.) Copper can be a dangerous actor in silicon, rapidly diffusing through both oxides and silicon and causing electrical problems such as increased leakage currents, reduced breakdown voltages, and lower reliability.

Early in the LDRD project, Total Reflectance X-Ray Fluorescence (TXRF) analysis was performed (by an outside vendor, Cerium Labs) on 6 wafers. One of those was a control wafer (fresh from the box, no processing), but the others either contained commercial graphene films or were exposed to wet processing baths that were shared with graphene-containing wafers. The results, graphically depicted below, show astoundingly large surface concentrations of copper. None of these would be acceptable in a CMOS IC fab (which is why most of our graphene processing was done in Sandia's μFab).



Near the end of the LDRD project when Sandia-grown graphene became available, a second set of samples was sent to Cerium Labs for TXRF analysis. The results are summarized in the table below.

	Sample C2 Bare/clean control wafer (no graphene)	Sample D7 Sandia graphene, delaminated	Sample C4 ACS graphene (commercial)
P	300	1500	2100
S	150	1600	1300
Ca	<10	900	3600
Ti	<1	100	300
Cr	-	200	<100
Fe	<10	1300	1000
Cu	<1	12,500	1300

Surface concentrations are in units of $x10^{10}$ atoms/cm^2

Unfortunately, the “Sandia graphene” sample had about 10 times more copper contamination than the ACS commercial graphene, which was already highly unacceptable. It is clear that much work needs to be done in this area.

Optical Contrast of Graphene Embedded in Dielectrics

Principal Contributors:
Isaac Ruiz, Michael Goldflam, Terri Hickman, Stephen W. Howell

The optical contrast of graphene on dielectrics has been studied extensively in the past for various reasons including optimizing graphene's visibility, accurate layer identification, and for use of metrology of graphene films.[1-4] Through these studies, it has been shown that the optimal SiO_2 thickness in order to make the graphene as high contrast as possible is 247 nm, while the contrast is much lower for other dielectrics such as Si_3N_4, HfO_2, Al_2O_3 and $BaTiO_3$.[5] Here in this study we examine the visibility of graphene that is encapsulated between two dielectrics. We look at optimizing and minimizing the optical contrast of the graphene buried in four different dielectrics, as well as experimentally measuring the contrast of the films buried in SiO_2.

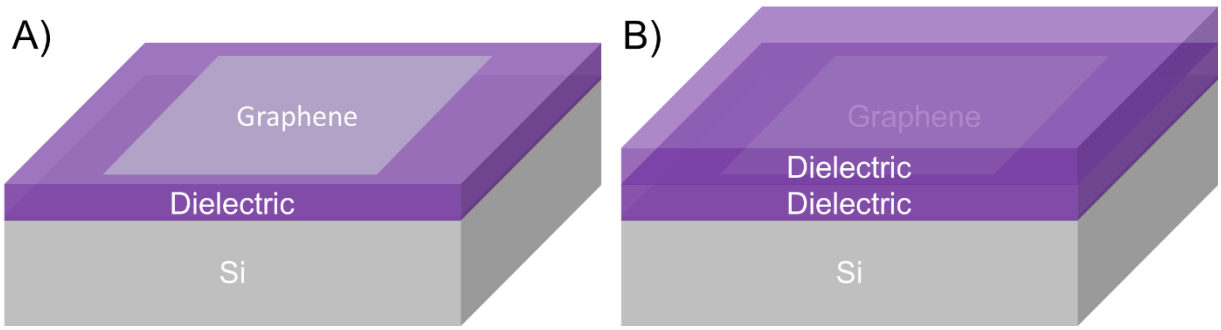


Figure 1: Graphene stacking arrangements. A) Exposed graphene on top of a dielectric and B) graphene buried in a dielectric.

Typically, the contrast studies of graphene have been performed on an exposed dielectric such as shown in Figure 1A. However, in many cases this is not the ideal arrangement. Graphene is highly susceptible to degradation when exposed to the atmosphere and its properties may begin to change over time. Therefore, similar to CMOS processes, a passivation layer is needed on top of the graphene to maintain the integrity of the film as seen in Figure 2B. Simulations have been conducted previously on buried atomically-thin materials to improve the visibility of the films, however there has been very little work in directly measuring the visibility of graphene stacked between two dielectrics.[6] This is likely due to the difficulty of depositing dielectric films onto graphene films, due to wetting problems with the graphene and also the harsh processes required to deposit the films using techniques like plasma-enhanced chemical vapor deposition. In many PECVD processes, the chamber conditions can cause the destruction of the graphene films, by etching or ion bombardment.

In order to model the optical contrast of graphene buried in various dielectric thicknesses, the reflection spectra were calculated using a transfer matrix formalism described in Konti's work.[5] The only difference in this case is that instead of a 4-layer

(air/graphene/dielectric/Si) and a 3-layer system (air/dielectric/Si) to calculate the reflection coefficient and contrast, either a 5-layer (air/dielectric/graphene/dielectric/Si) or a 3-layer (air/dielectric/Si) system is used instead. The simulated light source was the visible range (380-800 nm wavelength) and incident perpendicular to the substrate. The contrast was calculated as done in Simsek's publication[6] as shown in Equation 1,

(1) $C = (R_{ref} - R_g)/R_{ref}$,

where R_{ref} is the reflectivity of the dielectric on the Si, and R_g is the reflectivity of the dielectric/graphene/dielectric/Si stack. Figure 2 shows the results of the simulation of the contrast for the top and bottom dielectric thicknesses ranging from 0-1000 nm. It is interesting to note that for SiO_2 and Al_2O_3, as the bottom dielectric thickness increases, the contrast has a periodic nature while also generally decreasing. However, as the top dielectric layer increases the contrast does not fluctuate appreciably. In the case of Si_3N_4 and HfO_2 the reflectivity changes periodically when either the bottom or top dielectric increases in thickness. (Highest contrast is indicated by the dark red and

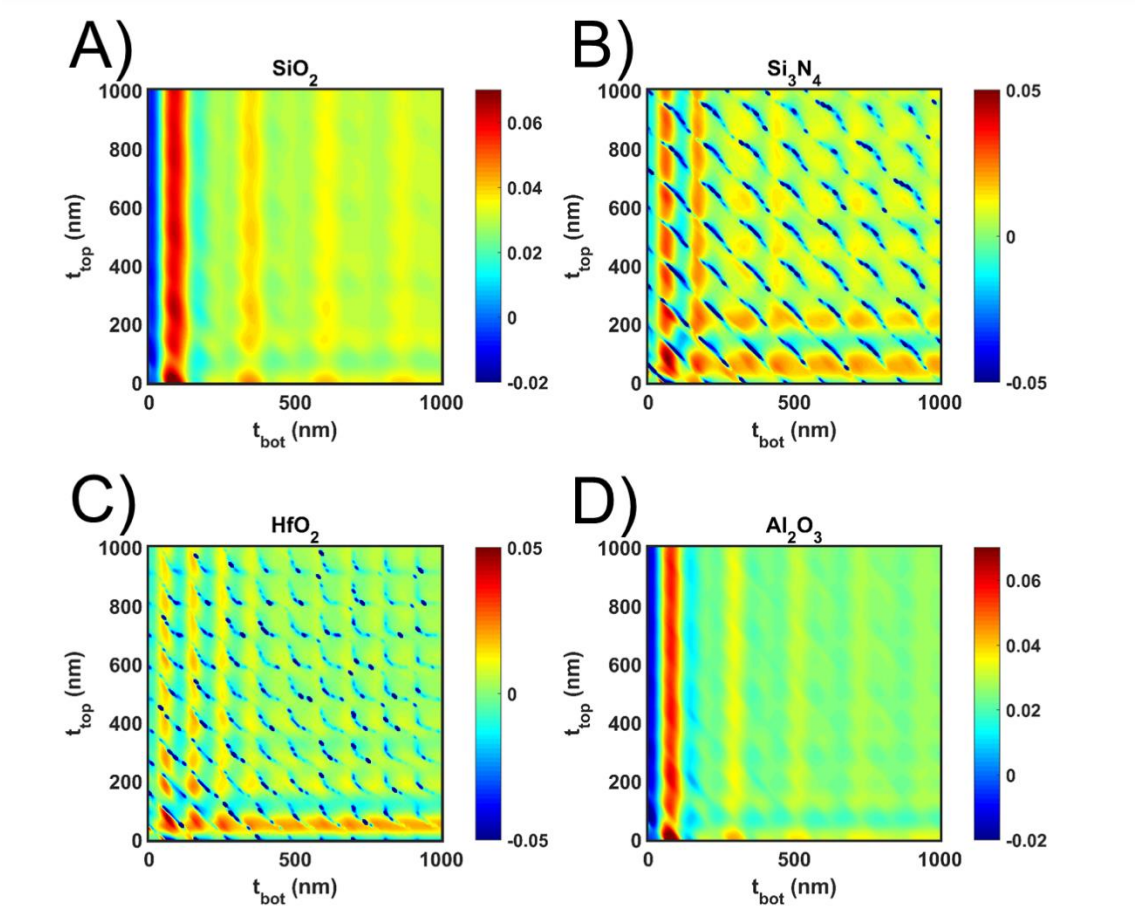


Figure 2: Contrast of graphene films buried in varying thicknesses of a) SiO_2, B) Si_3N_4, C) HfO_2 and Al_2O_3.

dark blue regions on the plots.) In order to *minimize* the contrast, the regions closest to 0 need to be determined (coded as yellow, green, and light blue in the plots). For the case of SiO_2 and Al_2O_3 this means to minimize the contrast there are only very specific thickness for the bottom layers that can be utilized. However, for the HfO_2 and Si_3N_4 the periodicity of the contrast allows for many different values of top and bottom thicknesses to be utilized when designing the dielectric stack.

In order to experimentally measure the contrast of a graphene film between two dielectric stacks, three dielectric stack configurations were fabricated. Using SiO_2 as the base dielectric material, three thicknesses were chosen: 200 nm, 500 nm and 1000 nm. The top layers where increased from 0 nm to 174 nm, in approximately 25 nm increments. In order to deposit the top layer without damaging the graphene during the PECVD process, a thin layer of Al_2O_3 was first deposited through e-beam evaporation to help with the adhesion onto the graphene, and then a 5 nm layer of HfO_2 was deposited by ALD in order to help isolate the graphene from the processing reactions in the PECVD chamber. Sketches of the film stacks are displayed in Figure 3.

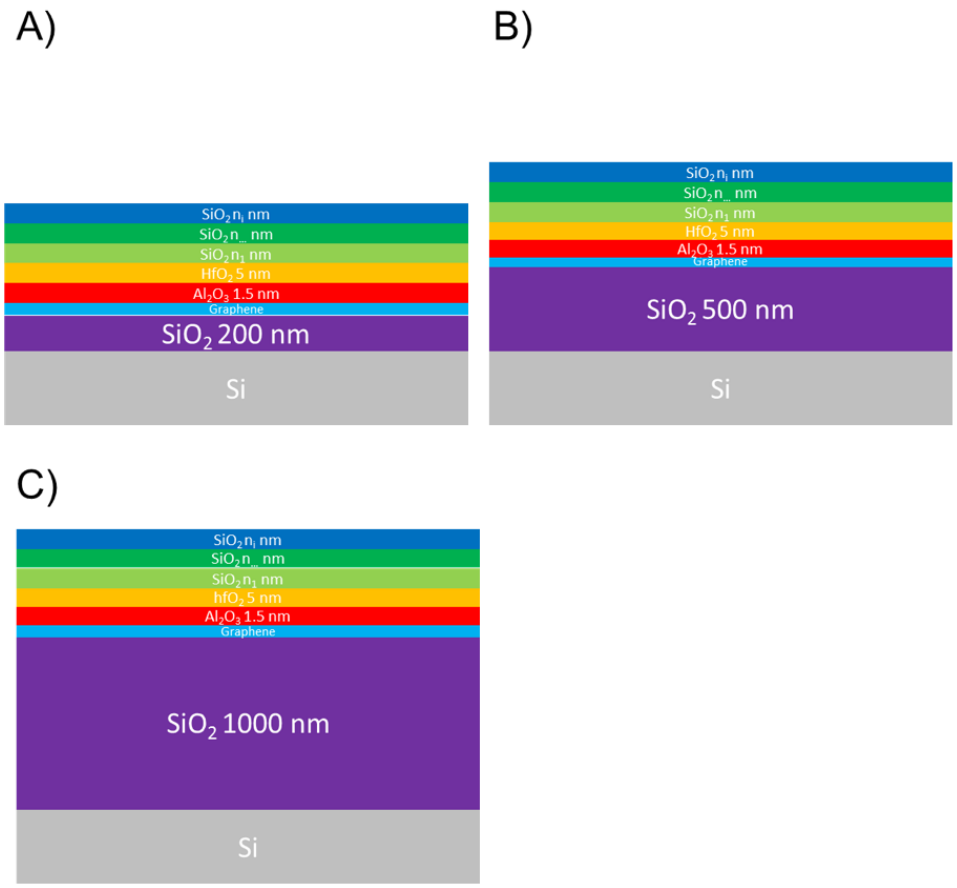


Figure 3: Experimentally fabricated dielectric stacks. Fixed A) 200nm, B) 500nm and C) 1000nm base SiO_2 thicknesses, with incrementally increasing top SiO_2 layers.

The optical images of the graphene/dielectric stacks were taken with an Olympus MX80 microscope using an LMPlanFL 5X objective lens with a numerical aperture of 0.13. CVD graphene was used in all of the stacks. The images of the results are displayed in Figure 4. It can be seen that not only are there dramatic changes among the different base thicknesses, but also as the top layer dielectric thickness is increased. Along with variations in contrast, the color of the stack also changes due to the refraction within the different SiO_2 thicknesses.[7] Compared to modeled results in Figure 2A, it can be seen that experimentally the contrast begins to go down slightly as the base layer thickness is increased, just as predicted by the model. Also there are some slight variations in the

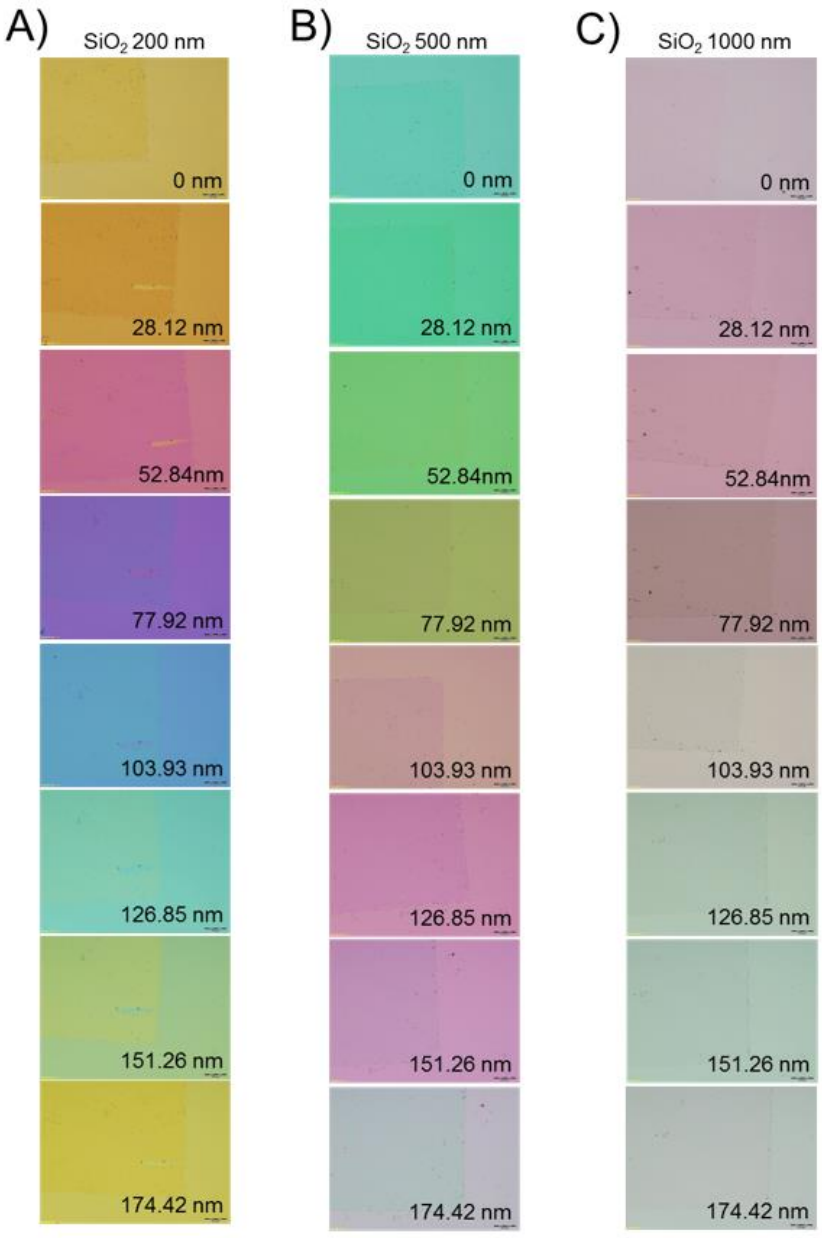


Figure 4: Optical images of varying SiO_2 top dielectric thicknesses on fixed A) 200 nm, B) 500 nm and C) 1000 nm SiO_2 based thicknesses.

contrast as the top dielectric film thickness is increased. By comparing all these configurations, it is obvious that certain colored substrates make the graphene contrast greater or lower. Thicknesses that give the stack a purple or dark pink color make the graphene stand out much more, while thicknesses that yield a green colored substrate make the contrast between the graphene and SiO_2 very low. Thus, the contrast can be controlled accurately by fine tuning the thicknesses towards these different colors.

Finally, the contrast was measured in these samples. Figure 5 shows the measured average contrast of the samples from Figure 4. Figure 5 shows that the contrast can vary greatly and even between positive and negative.

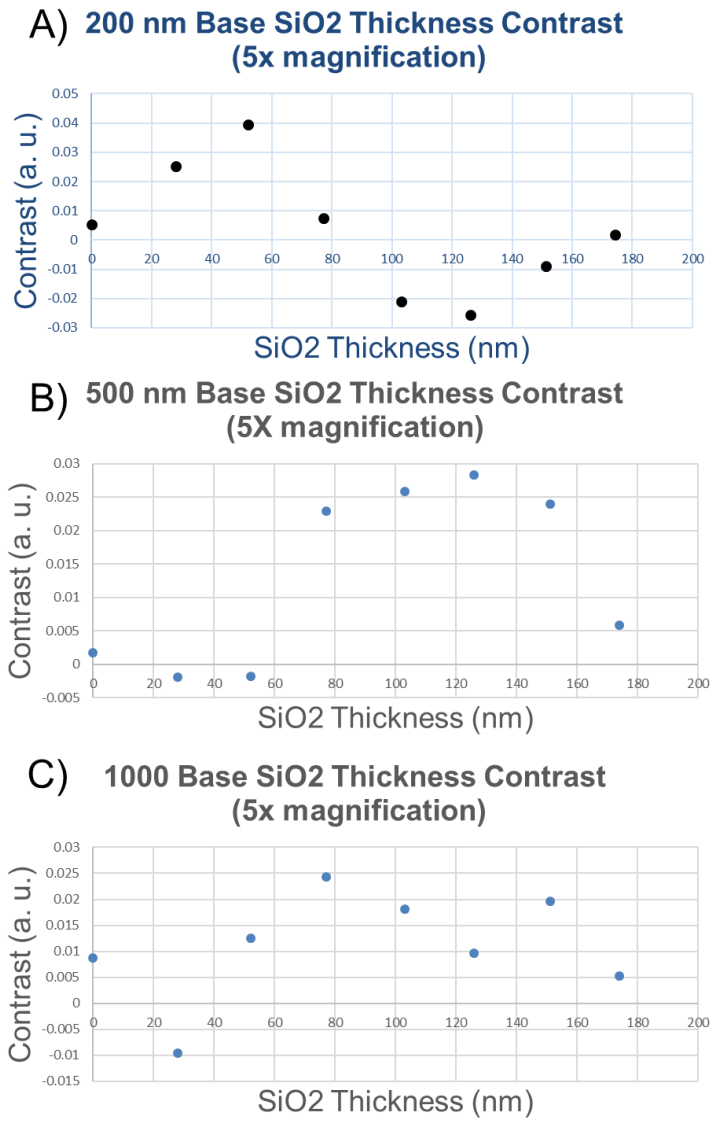


Figure 5: Average values of the contrast for fixed based oxide thickness A) 200 nm, B) 500 nm, and C) 1000 nm, as the top oxide thickness varies between 0 and 174 nm.

In conclusion, we were able to create a model to describe the contrast for graphene buried in various dielectric thicknesses. We were then able to fabricate test structures and measure the contrast across 3 different base thicknesses, with top thicknesses varying between 0 and 174 nm. The contrast was seen to vary between positive and negative, meaning with careful selection of the dielectric thicknesses the graphene can be made to be more or less visible. Future work should refine the models by comparing them to experimental data for all the dielectrics discussed here and not just SiO_2, especially some of the dielectrics like HfO_2 and Si_3N_4, which had very interesting contrast maps.

References

1) Ni, Z. H., H. M. Wang, J. Kasim, H. M. Fan, T. Yu, Y. H. Wu, Y. P. Feng, and Z. X. Shen. "Graphene thickness determination using reflection and contrast spectroscopy." Nano letters 7, no. 9 (2007): 2758-2763.
2) Jung, Inhwa, Matthew Pelton, Richard Piner, Dmitriy A. Dikin, Sasha Stankovich, Supinda Watcharotone, Martina Hausner, and Rodney S. Ruoff. "Simple approach for high-contrast optical imaging and characterization of graphene-based sheets." Nano Letters 7, no. 12 (2007): 3569-3575.
3) Blake, P., E. W. Hill, AH Castro Neto, K. S. Novoselov, D. Jiang, R. Yang, T. J. Booth, and A. K. Geim. "Making graphene visible." Applied Physics Letters 91, no. 6 (2007): 063124.
4) Kyle, Jennifer Reiber, Ali Guvenc, Wei Wang, Maziar Ghazinejad, Jian Lin, Shirui Guo, Cengiz S. Ozkan, and Mihrimah Ozkan. "Centimeter-Scale High-Resolution Metrology of Entire CVD-Grown Graphene Sheets." small 7, no. 18 (2011): 2599-2606.
5) Kontis, Christopher, Marcel R. Mueller, Christian Kuechenmeister, Klaus T. Kallis, and Joachim Knoch. "Optimizing the identification of mono-and bilayer graphene on multilayer substrates." Applied optics 51, no. 3 (2012): 385-389.
6) Simsek, Ergun, and Bablu Mukherjee. "Visibility of atomically-thin layered materials buried in silicon dioxide." Nanotechnology 26, no. 45 (2015): 455701.
7) Henrie, Justin, Spencer Kellis, Stephen Schultz, and Aaron Hawkins. "Electronic color charts for dielectric films on silicon." Optics express 12, no. 7 (2004): 1464-1469.

Design and Layout of Circuits for Obfuscation

Principal Contributors: Liam Claus and Marcos Sanchez

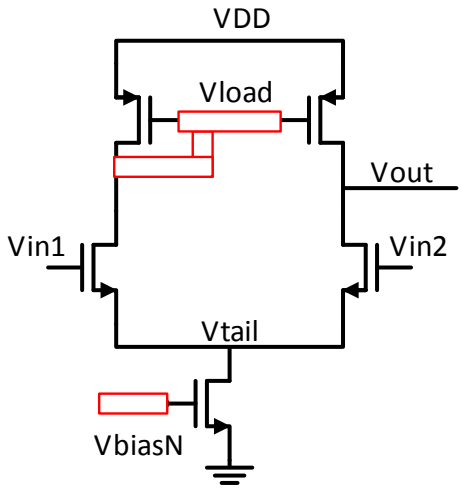
An exercise was proposed to analog and digital IC designers: In what locations could "invisible" graphene be used to obfuscate circuit function? The text and graphics below summarize their thoughts.

For both digital and analog functions, the electrical resistance of graphene is an important consideration. Although its *resistivity* (a basic geometry-independent material property) is low, the film is extremely thin and its total resistance can be significantly higher than that of the aluminum, copper, or polysilicon films that it replaces. A typical monolayer graphene film can have sheet resistance of about 300 Ohms per square, hundreds of times greater than aluminum and copper, for example. Therefore, graphene should be used only for connections that are physically short, and only in locations in the circuit that are tolerant of high resistances. It turns out that these constraints are not overly restrictive.

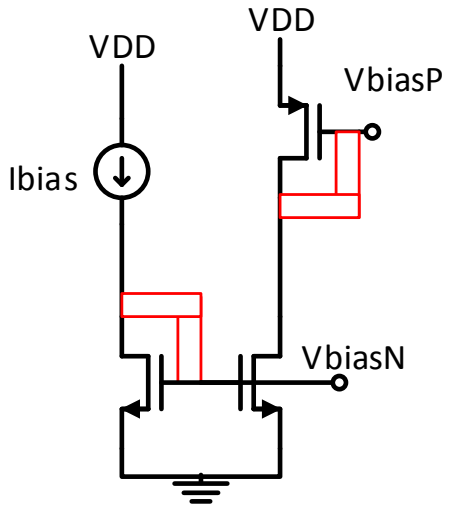
Analog Applications

In general, graphene interconnect should be used at high-Z nodes. Diode-connect nodes and bias distribution seem to be good potential candidates for graphene insertion.

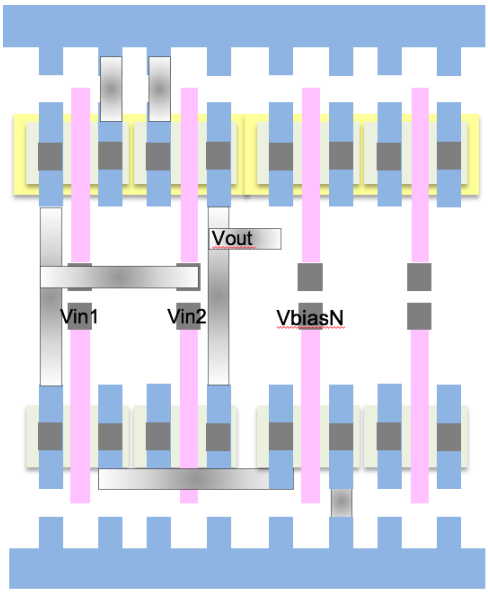
Graphene in differential amplifiers might be of limited use (for obfuscation) because these circuits tend to be recognizable by their transistor configuration, not the wiring patterns. Nevertheless, here's one possible configuration (graphene is in red, and replaces metal wiring):



Current sources, often used to generate the differential amplifier tail current bias, could also use graphene (shown below). Again, the benefit might be small because current sources are often recognizable by their transistor configuration instead of wiring patterns.



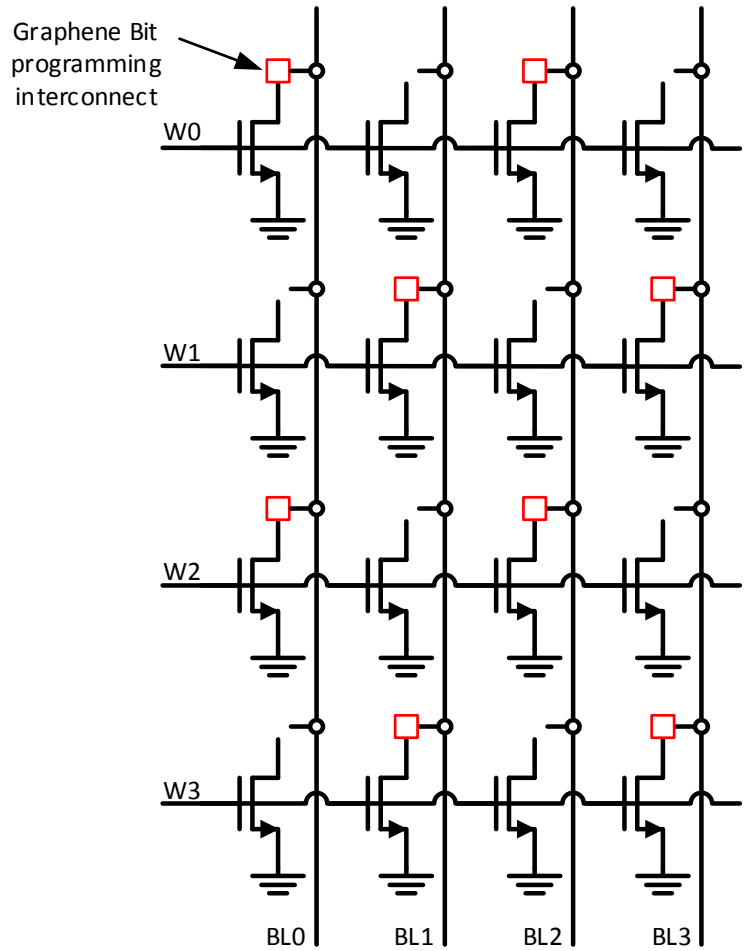
In an interesting twist, two *digital* cells can be reconfigured to create an operational amplifier, leading to the possibility of covertly creating (using graphene wiring) an analog amplifier sitting inside a sea of digital gates (graphene is shown in grey):



Higher-level blocks (DACs, ADCs, PLLs, etc.) are often recognizable because of their transistor placement, so using graphene to replace some of the wiring would probably be of little benefit.

Digital Applications

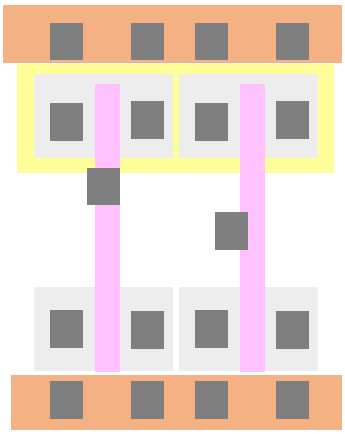
Read-Only Memory (ROM) can be used to store programming, configuration data, and other important items, but it is usually very easy to decipher the contents by examining the connections made to the transistors. If graphene were used to hide the connections, however, some degree of obfuscation is possible. In effect, all bits of the memory would appear to be unprogrammed and it would be difficult to identify 1s and 0s by casual inspection. The high resistance of the graphene should not affect the pull-up or pull-down nature of the ROM programming:



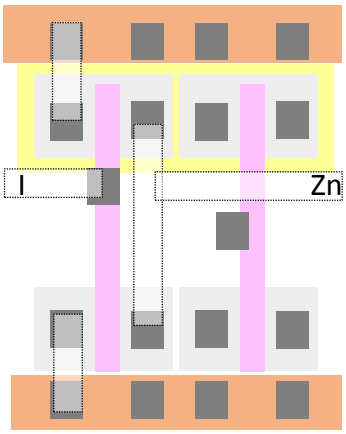
In common practice, standard digital cells can share the same “base cell” transistor layout. In essence, the physical layout of the transistors of all cells are exactly the same, and the function (inverter, NOR, NAND, etc.) is determined by the wiring. In one possible use of graphene, some connections between transistors could be made with graphene to disguise the intended digital function. All other transistors in the layout could wired on (or off) to maintain consistent power between cells. Some examples are

shown below (graphene is depicted as white rectangles). Because the graphene lines would be very difficult to detect, these four circuits would appear identical to each other – yet they would perform very different functions.

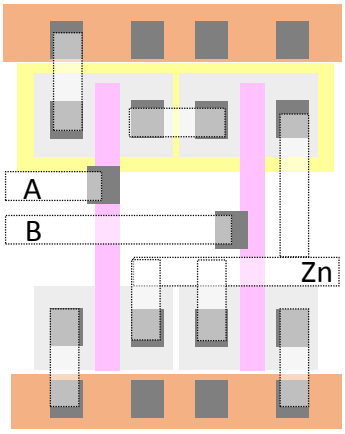
BASE CELL



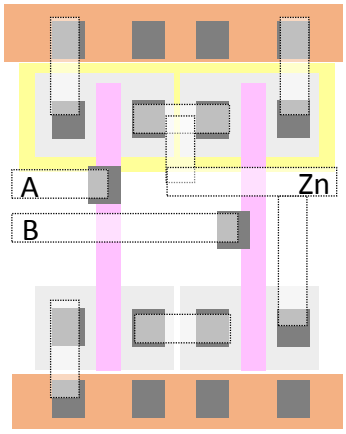
INVERTER



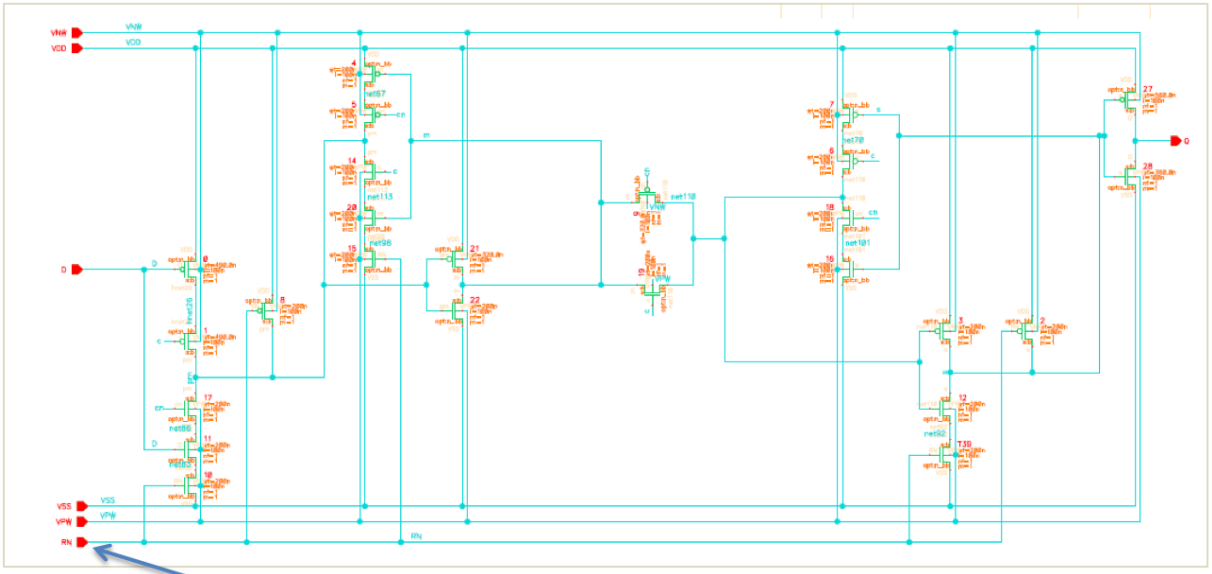
NOR



NAND



Finally, a graphene activated transistor could be used to pull up (or down) internal storage nodes of transistors (to clear or pre-set flip flops, for example). The schematic on the next page illustrates that approach.


VNW
VDD
D
VSS
VPW
RN
Q
Graphene driven node

Analysis/Discovery Techniques

Principal Contributors: Mary Miller, Darlene Udoni, and Paul Kotula

Finished test chips containing graphene and common wiring elements were subjected to a wide variety of analytical techniques to assess the difficulty of detecting the graphene. The results from this part of the LDRD project are contained in a classified addendum that will be available from the PI or PM (Bruce Draper, Brad Gabel).

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