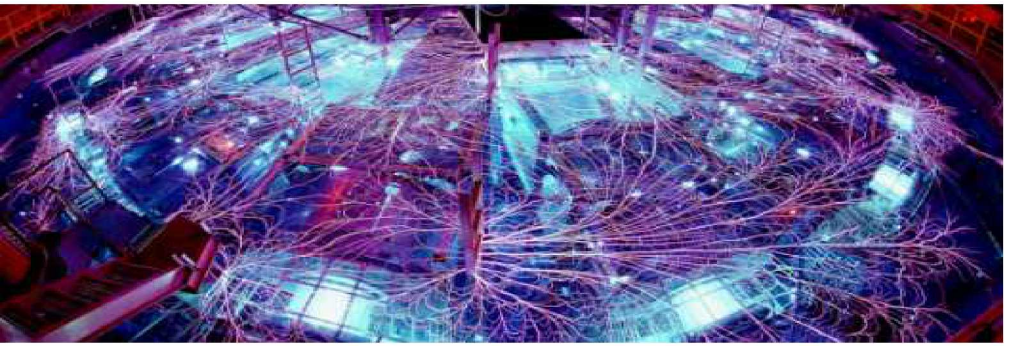
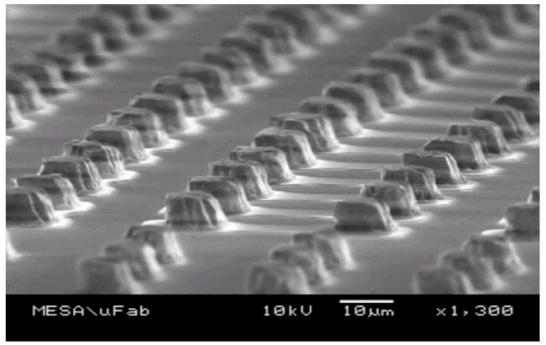
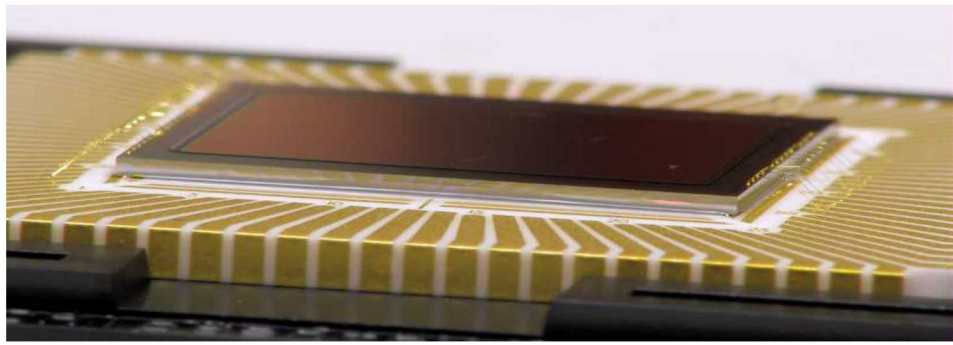
SAND2019-1043PE







GaAs Detector Arrays for hCMOS Cameras

Quinn Looker, Michael Wood

hCMOS Workshop 1/17/2019

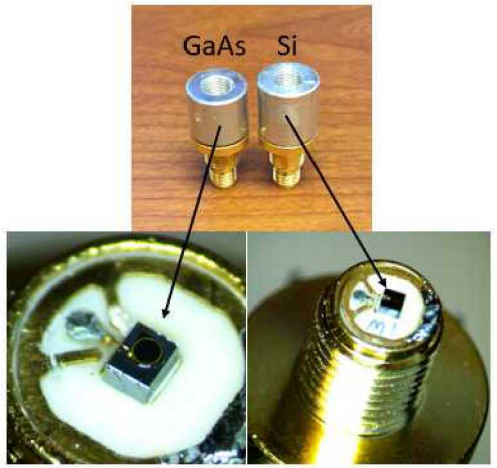
Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

Project Goals

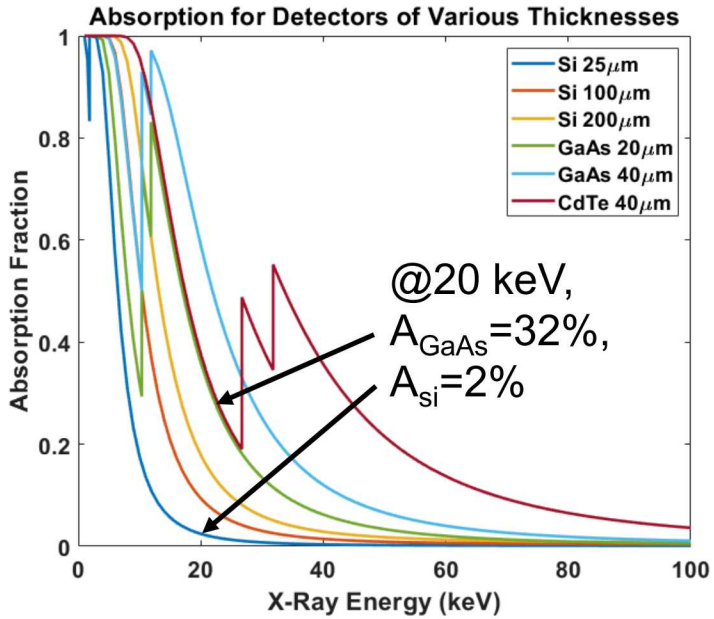
1. Deliver functional UXI sensor with ~15x sensitivity to 20 keV x-rays, while maintaining similar time gate profile
   a. Fabricate GaAs diode arrays with 25 µm pixel pitch (3x3 up to 36x36)
   b. Deliver test results on estimated defect rate, leakage current, inherent pixel time response, and cross-talk
   c. Deliver functional multi-frame, x-ray sensitive sensor using existing ROIC and a GaAs detector array

Key LDRD Results

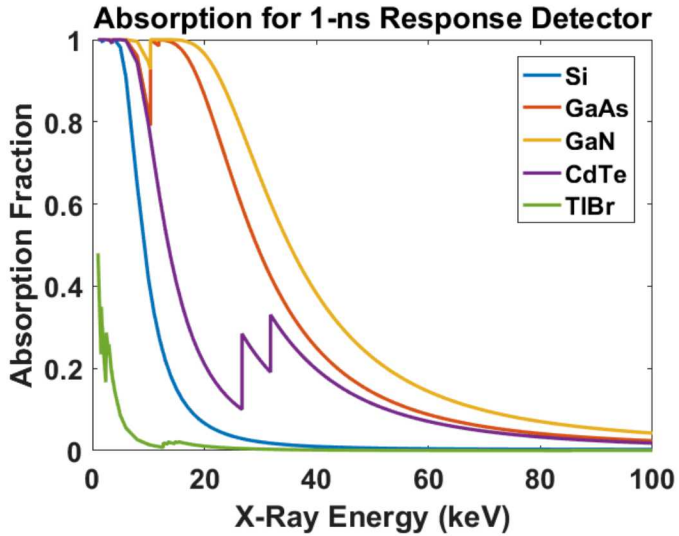
LDRD Goal: Demonstrate higher Z (>14) detectors with increased hard x-ray absorption and similar time response to Si detectors



Similar package and readout



Photoelectric absorption scales as ~Z^4



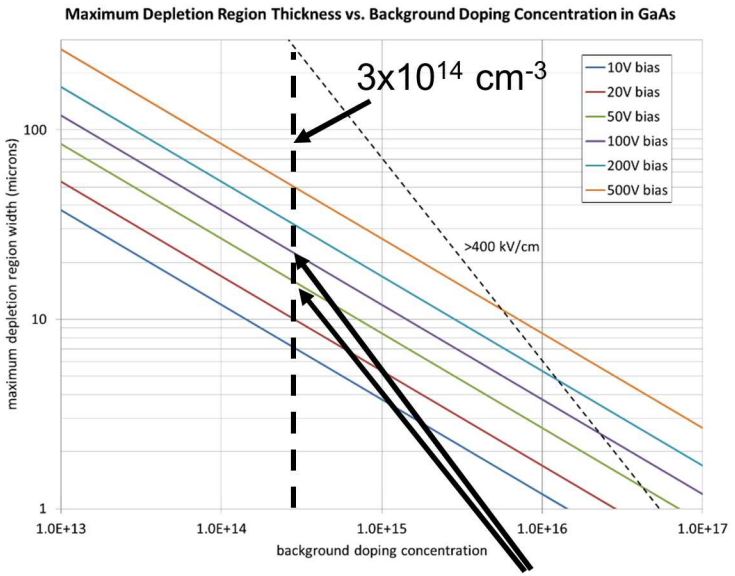
Increasing detector thickness directly conflicts with preserving speed

Key LDRD Results

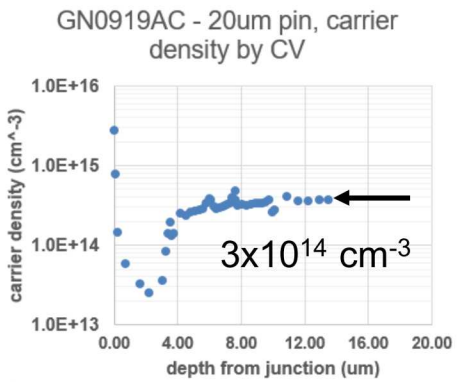
1. Demonstrated MBE growth of GaAs up to 40 µm thickness with sufficiently low background impurity concentration to deplete at a usable bias voltage

$$x_d = \sqrt{\frac{2\varepsilon V}{qN_d}}$$

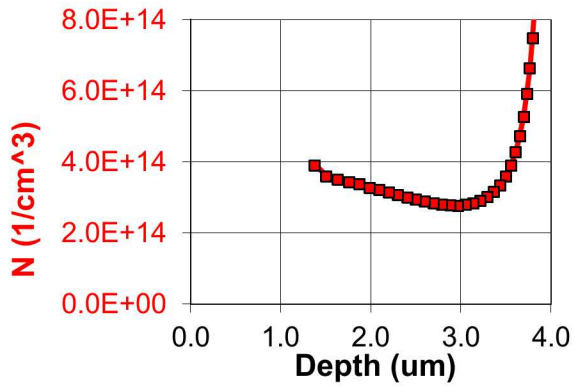
x_d: Depletion depth (cm)
ε: Dielectric constant (F/cm)
V: Applied bias (V)
q: electronic charge (C)
N_d: Dopant concentration (cm^{-3})



Sandia-grown GaAs epi



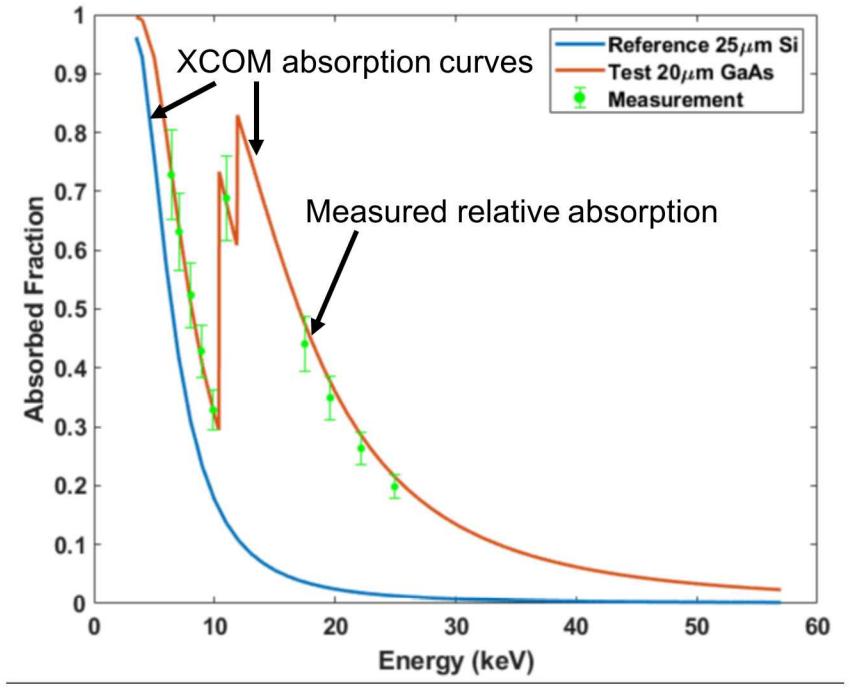
Commercially-grown GaAs epi



10 µm thickness can use 50 V supply
20 µm thickness can use 100 V supply

Key LDRD Results

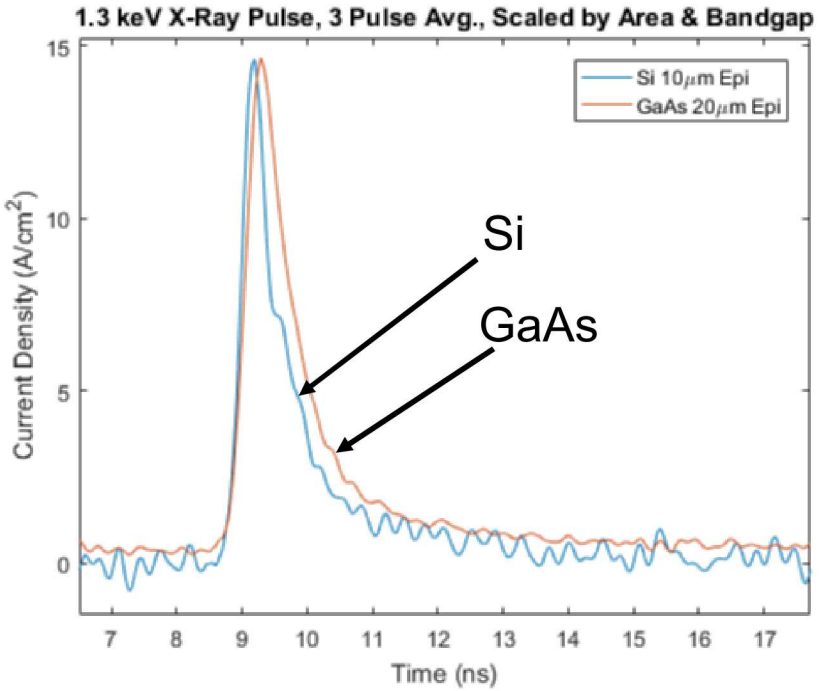
2. Demonstrated expected absorption at selected x-ray energies



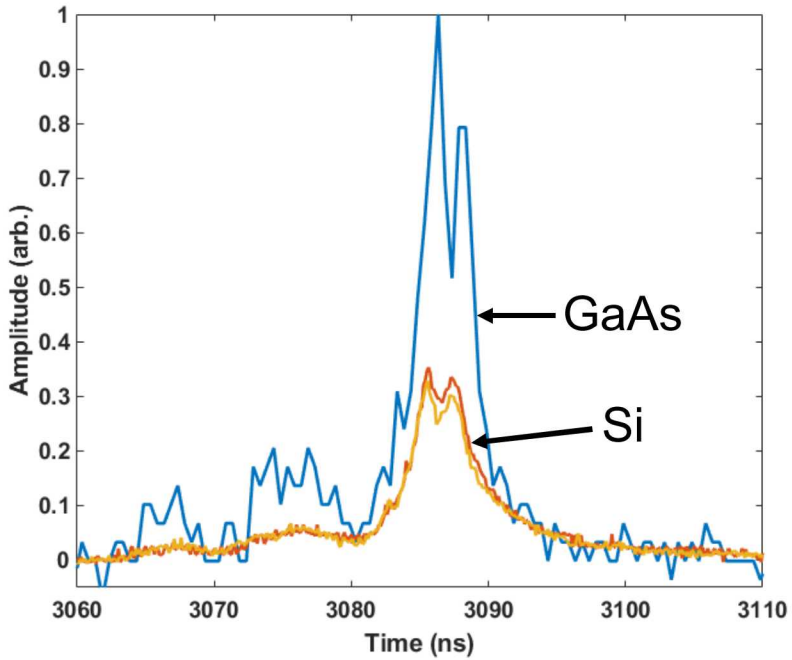
Key LDRD Results

3. Demonstrated equivalent speed to Si detectors

Soft x-rays (100% absorption in Si and GaAs)



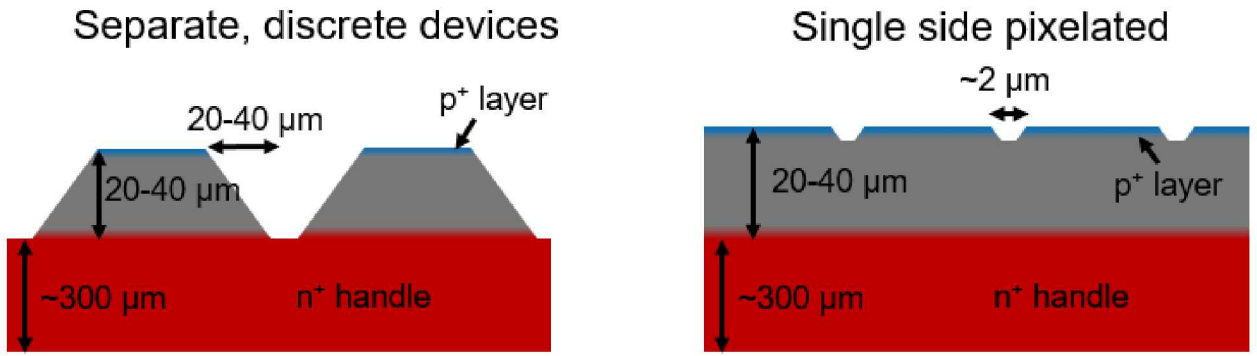
Hard x-rays (Incomplete absorption)



GaAs on UXI – Main Tasks

1. Backside-Illuminated Detector Process Development

Significant move from mesa-etched, frontside-illuminated devices used in LDRD to backside-illuminated small pixels for UXI designs



May require multiple design->fab->test iterations

2. Pixel Design

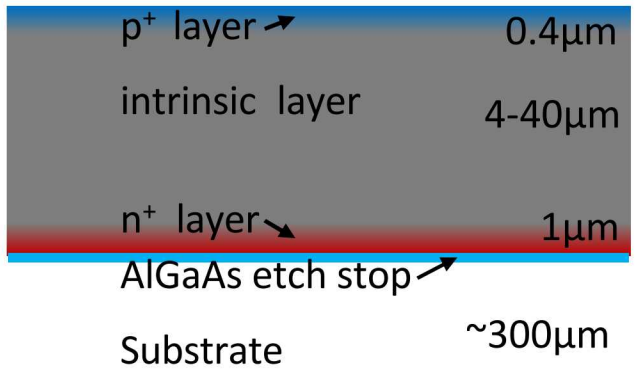
Mask layout of 25 µm pitch pixels – electrical isolation, channel stop, backside metal

3. Flip Chip Bonding Process Development

Team has experience with similar products, but application specific issues may appear

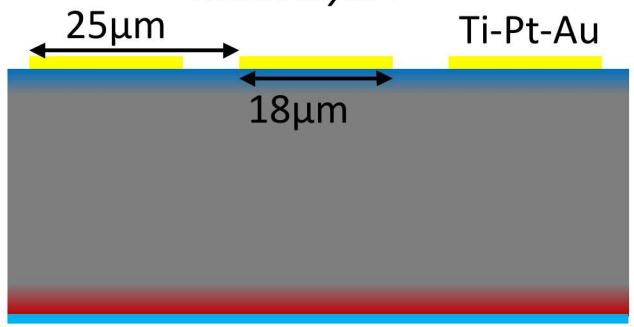
GaAs Array Process Plan

0. Starting Material: GaAs epi on GaAs substrate



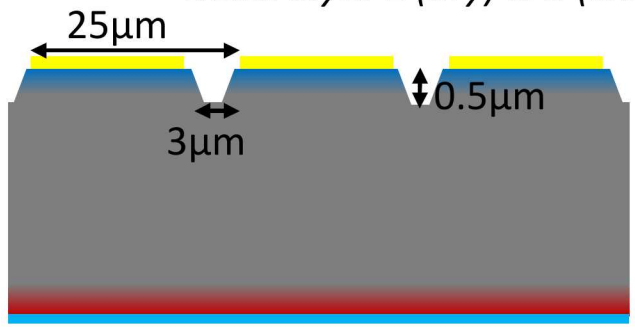
1. Create pixel metal contacts

Mask layer 1



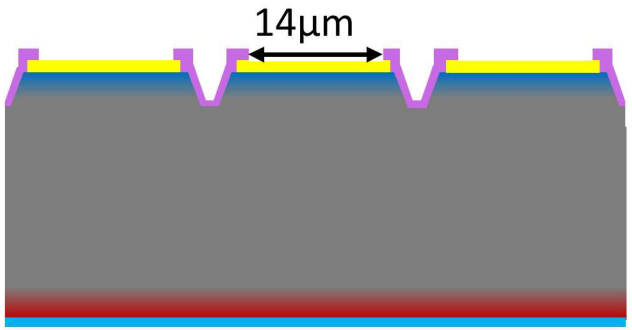
2. Etch pixel isolation trench

Mask layer 2 (dry) & 3 (wet)



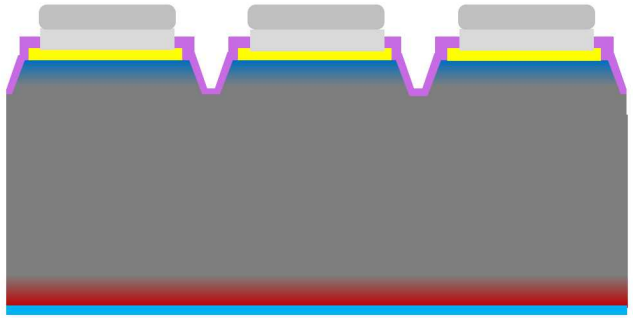
3. Deposit and etch nitride passivation

Mask layer 5

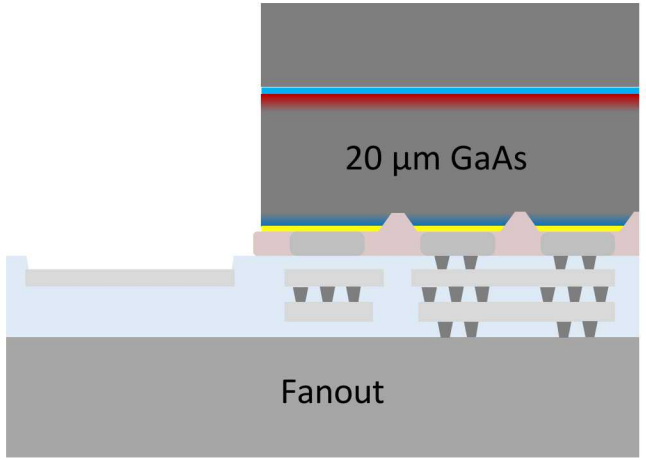


4. UBM/Indium dep and liftoff

Mask layer 6

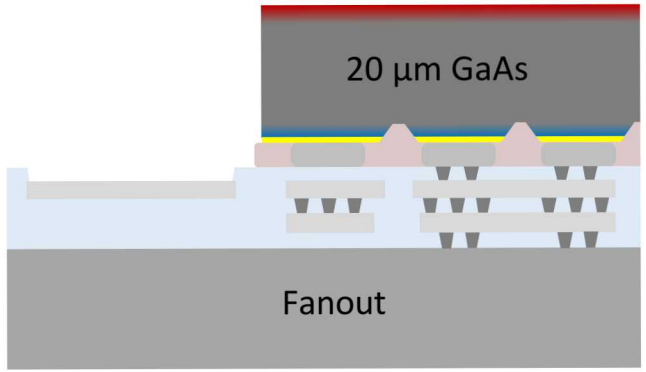


5. Scribe and break die segments.
6. Indium hybridization.

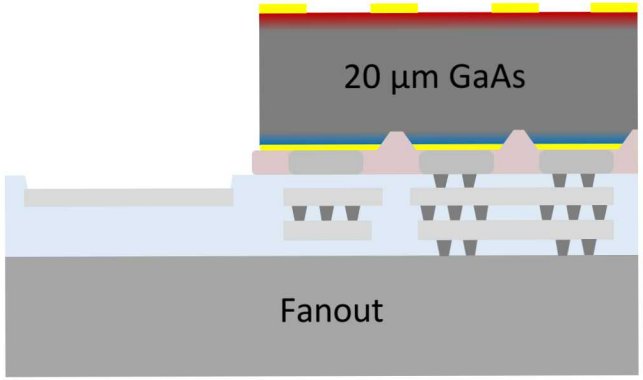


GaAs Array Process Plan Part 2

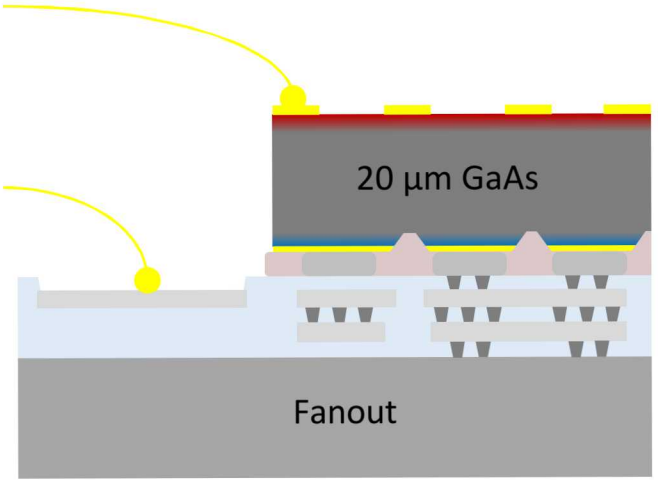
7. Substrate removal



8. Backside contact dep and pattern *Mask layer 7*



9. Packaging and testing



Task 1: GaAs wafer growth

Goals for initial MBE campaign (11/05/18-12/20/18)

1. Grow process development wafers
2. Build a stock of 20 µm PIN wafers for FY19/20 program goals
3. Growth of 40 µm PIN wafers for initial testing and FY20+ goals
4. Test ability to finely control background doping levels to reduce bias voltage for full depletion

Device description	Number of wafers	Wafer #s
Process development structure	2	GN1563, GN1564
Standard structure, X = 4,000 nm	2	GN1565, GN1566
Standard structure, X = 20,000 nm	4	GN1571, GN1572, GN1573, GN1578
Standard structure, X = 40,000 nm	1	GN1579
Hall test structure	1	GN1582
Standard structure, X = 20,000 nm Background: 1E14/cm3 p-type	1	GN1583*, GN1585
Standard structure, X = 20,000 nm Background: 5E13/cm3 p-type	1	GN1584
Standard structure, X = 20,000 nm Background: 1E13/cm3 p-type	1	GN1587
Hall test structure	1	GN1586
Standard structure, X = 40,000 nm Background: 1E13/cm3 p-type	1	GN1588

PIN diode epitaxial structure:

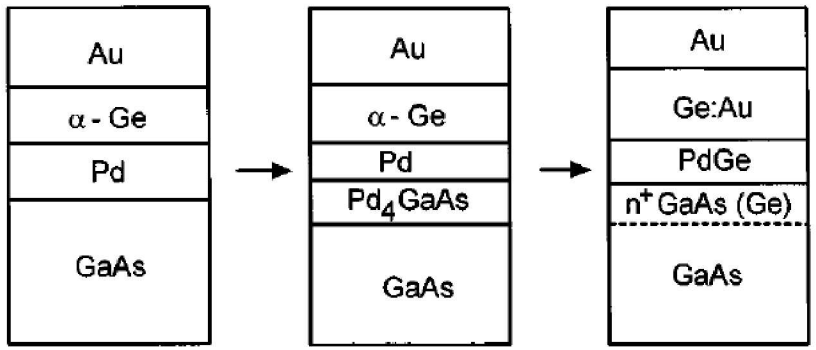
Task 2: Develop low-T ohmic n^+ contacts

Background:

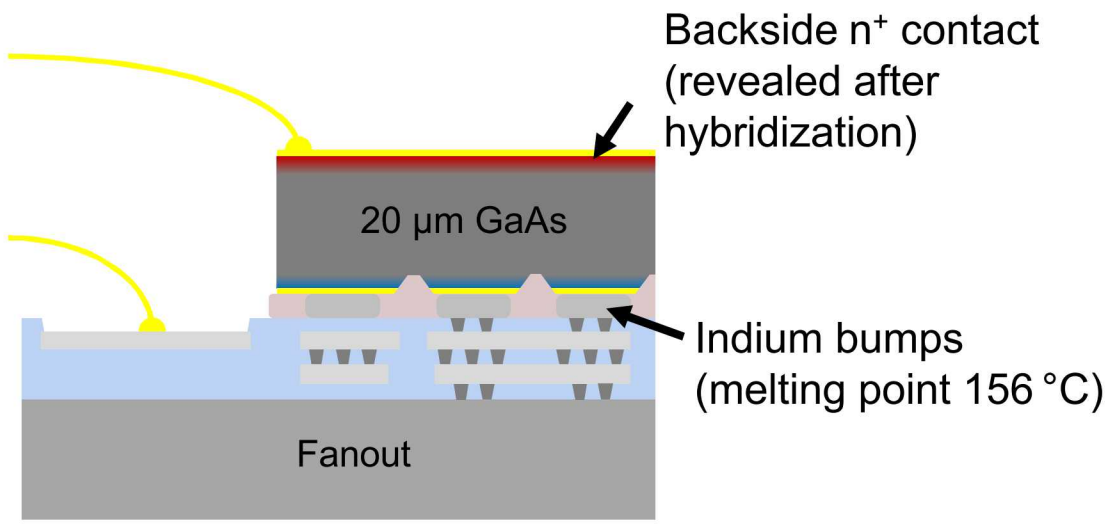
- Current ROIC design requires an n-type backside contact formed after hybridization
- For non-hybridized devices we use a 400 °C alloying process to form an Ohmic n^+ contact
- High temperature would melt In bumps and likely damage underfill epoxy

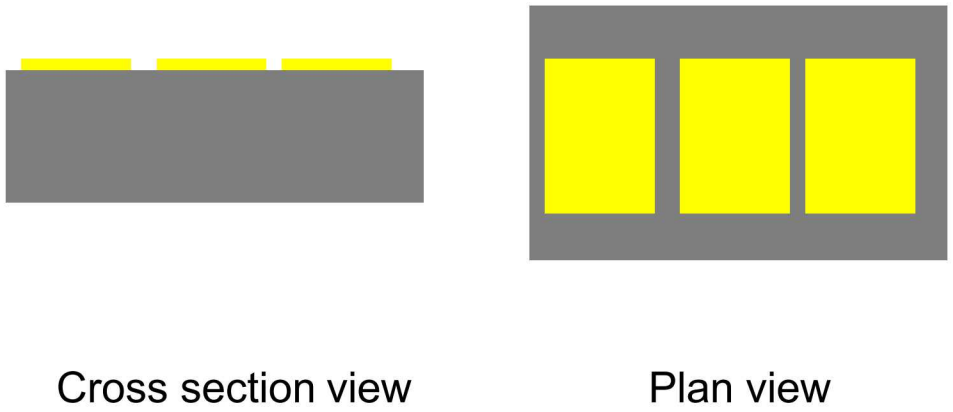
Recent results:

- Literature study pointed to Pd/Ge/Au stack as compatible with low-temperature n-contacts to GaAs
- Process demonstrated with existing mask set from XRD LDRD
- Results show contact resistance <15 Ω/pixel



L. Wang, J. Appl. Phys. **79**(8) 1996





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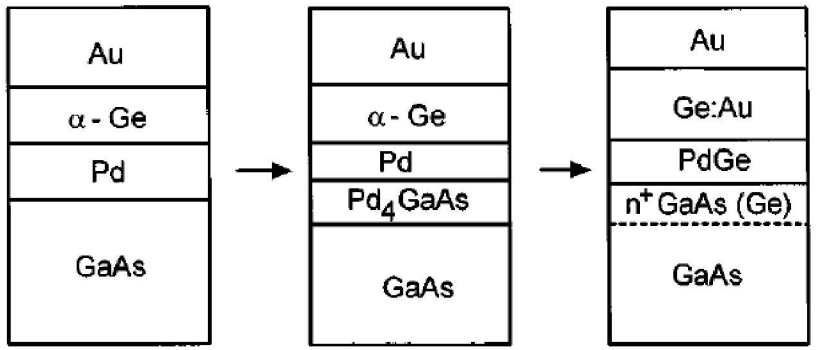

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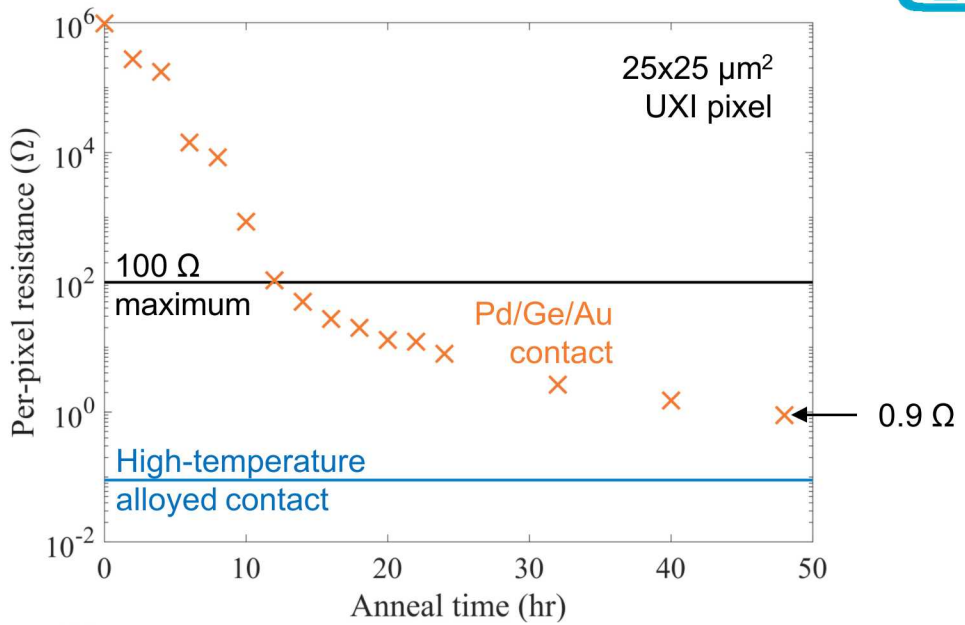
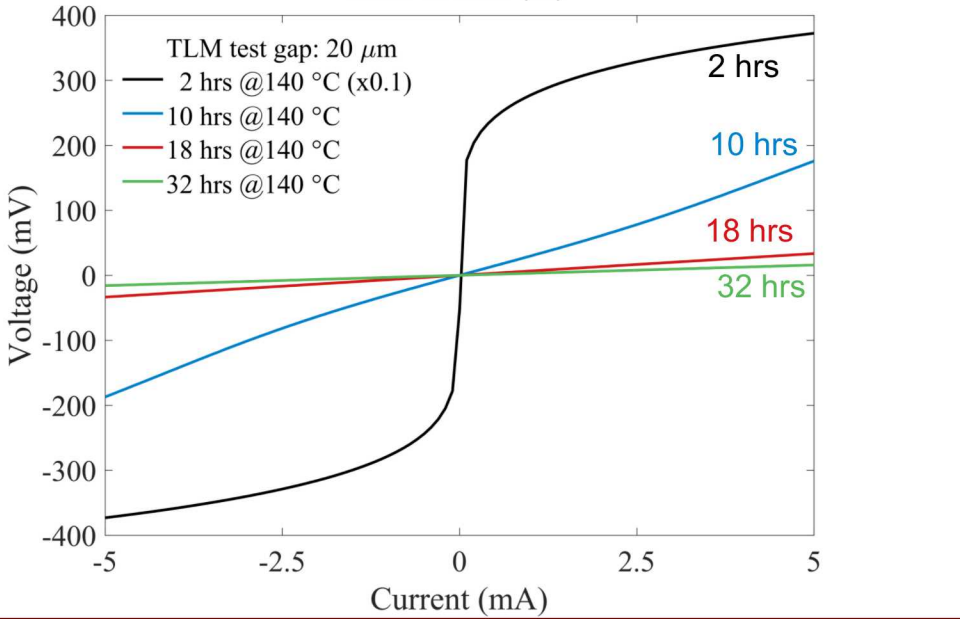




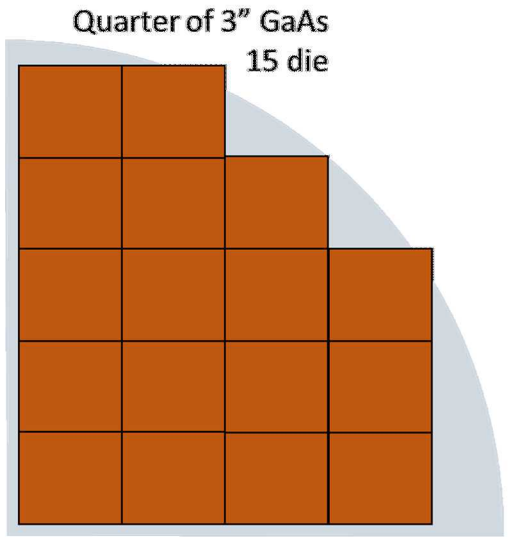
Task 3: Mask design

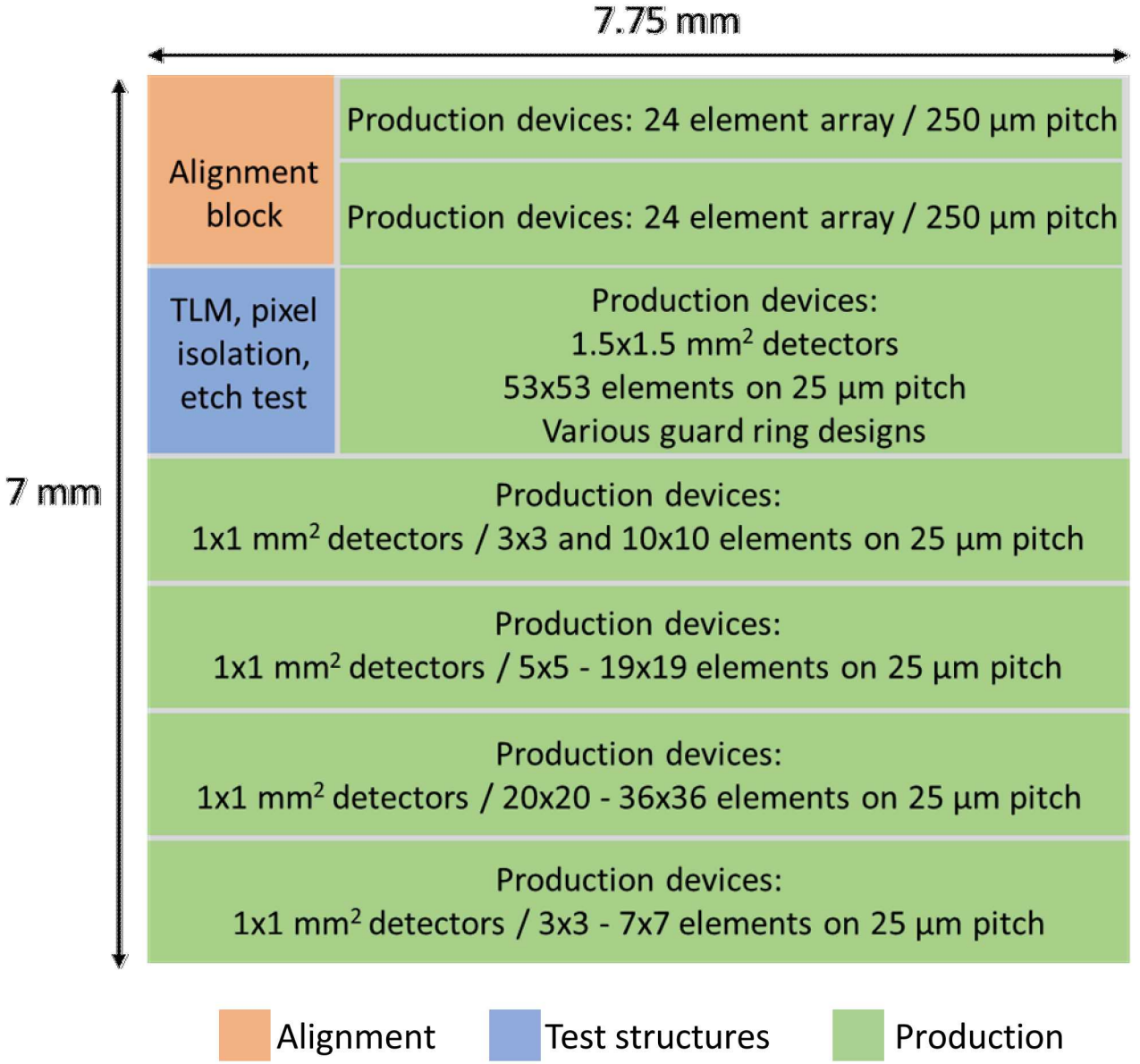
Background:

- Need a dedicated mask set to hybridize and test 25 µm GaAs pixels
- Mating Si fanout chips already fabricated and tested
- Key measurements: pixel time response and cross-talk

Recent results:

- Target test arrays identified on Si fanout mask
- Currently laying out five-layer mask design and writing corresponding fabrication plan based on recent process development results





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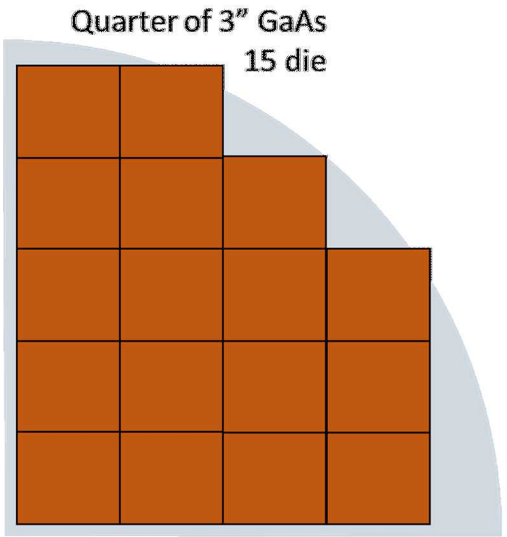

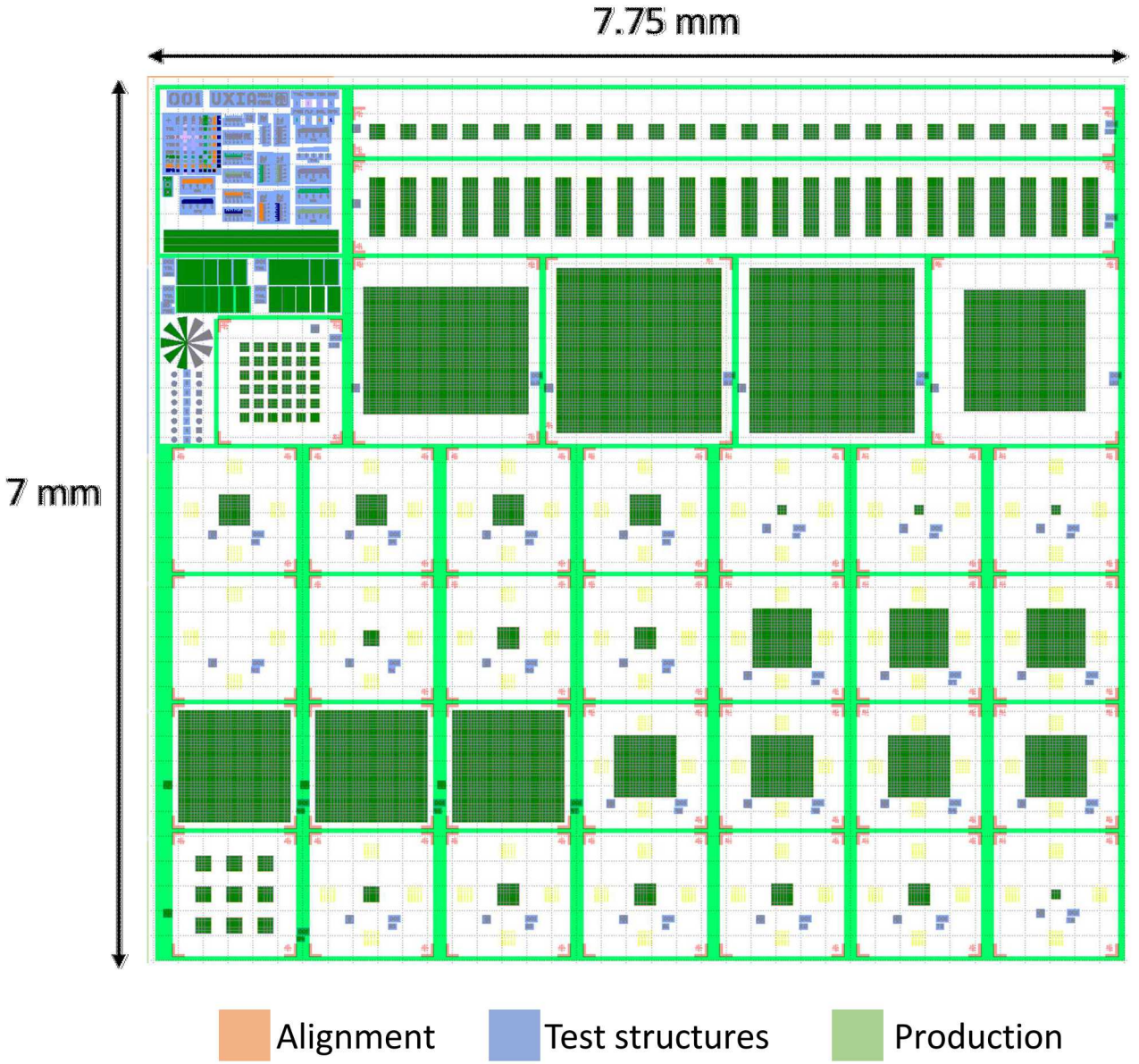

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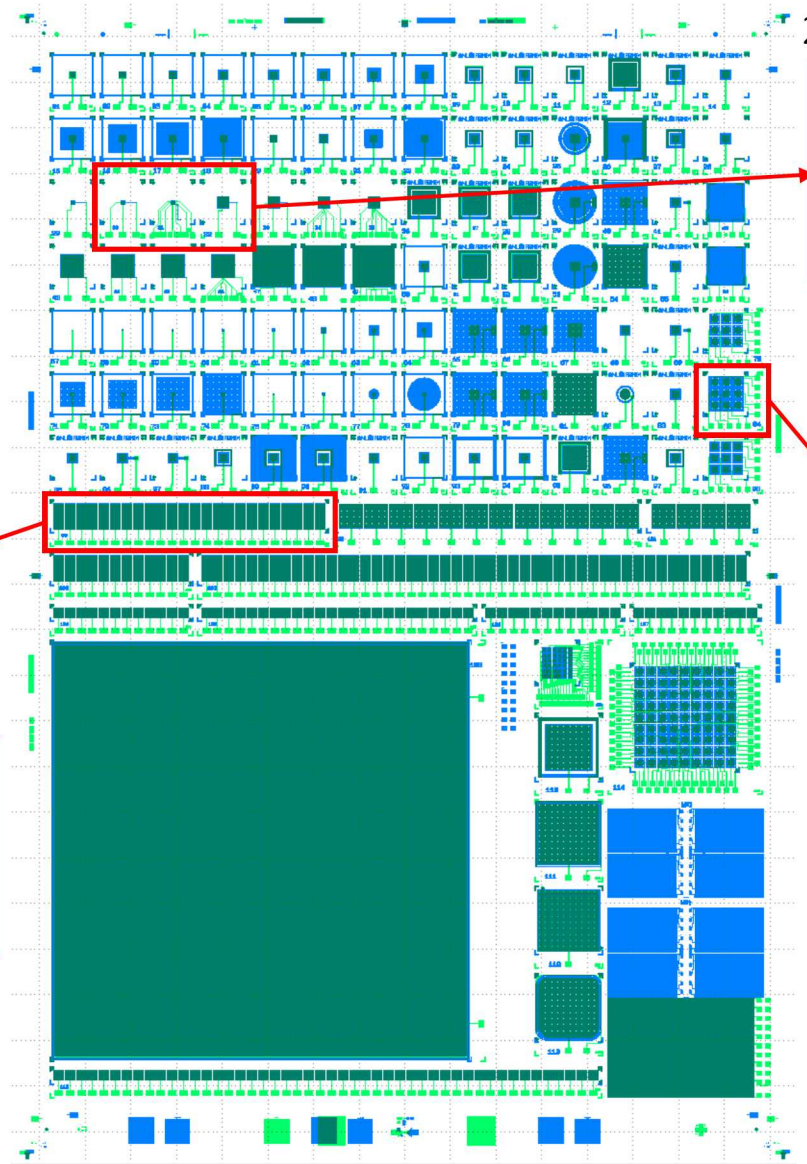
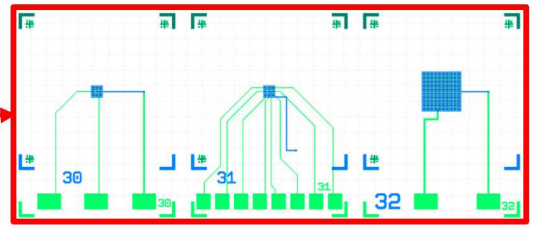
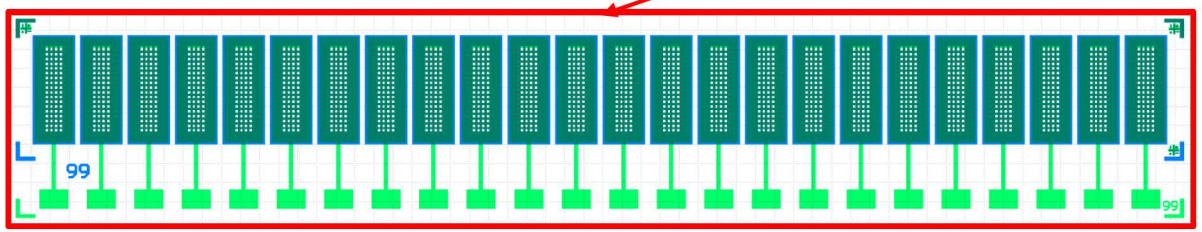
Si fanout chip:

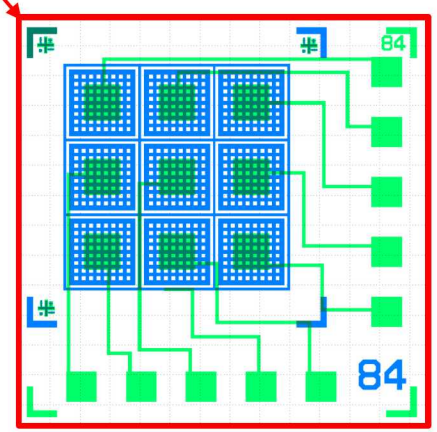


25 µm pitch, 3x3 and 10x10





24-element array, 250µm pitch

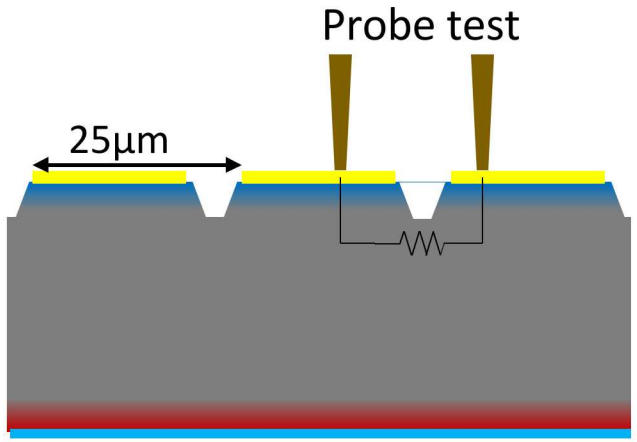


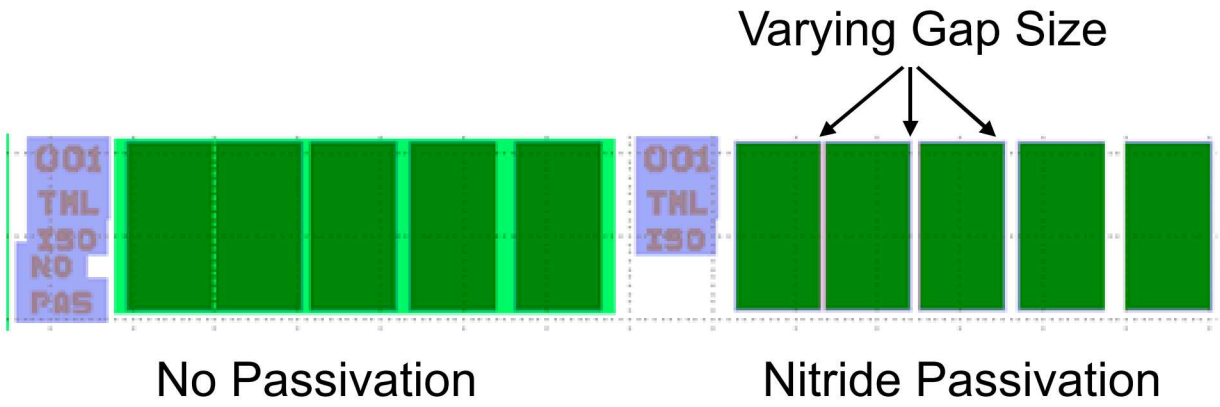
250µm pitch, full readout

Task 4: Process Development

Background: General process development is needed. Trench isolation of pixels is a significant departure from the current method of ion-implanted channel stop in Si. We need to test electrical isolation of pixels, which can be done on-wafer during fab.

Development task: Iterate on all fab steps. Following step 2 and 3 in the fab process, probe test on-wafer to determine electrical isolation of pixels. Will dictate whether wider or deeper trenches are needed, or a new method is needed.
I-V at various steps to ensure dark current is within acceptable limits.



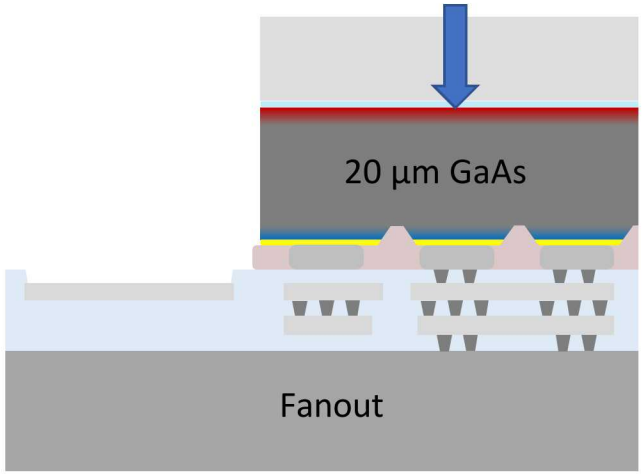


Task 5: Hybridization Development

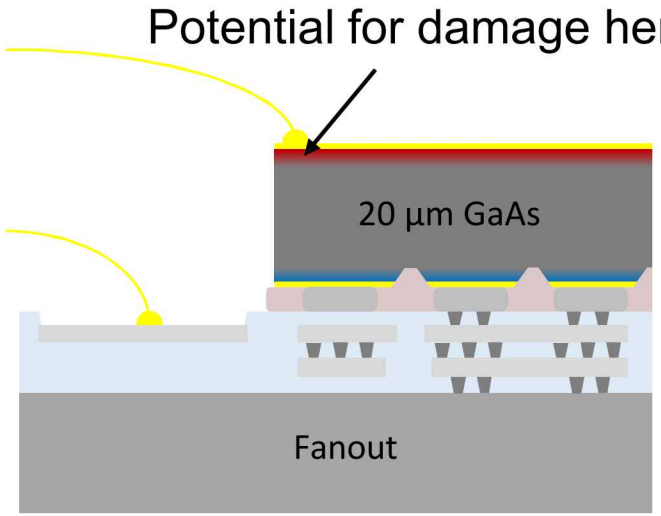
Background: Indium bump bonding of small die is low risk, but handling small die may be challenging. Die thinning may be difficult with small, narrow die. Full UXI arrays may be easier to handle.

Development task: Need to develop bump bonding, epoxy fill, and die thinning process. Die may break or chip.

Test substrate removal of bonded die



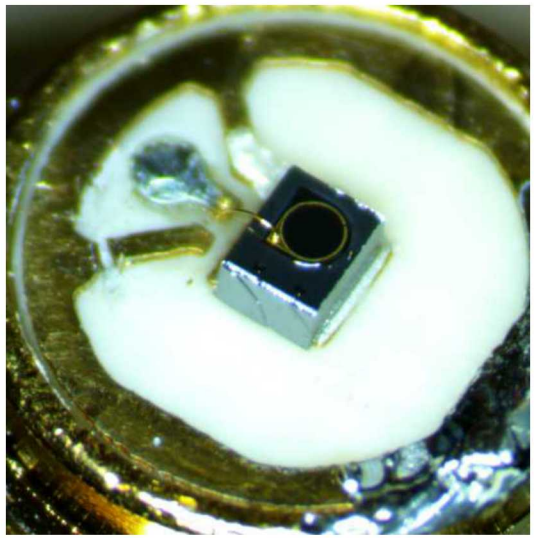
Task 6: Packaging Development

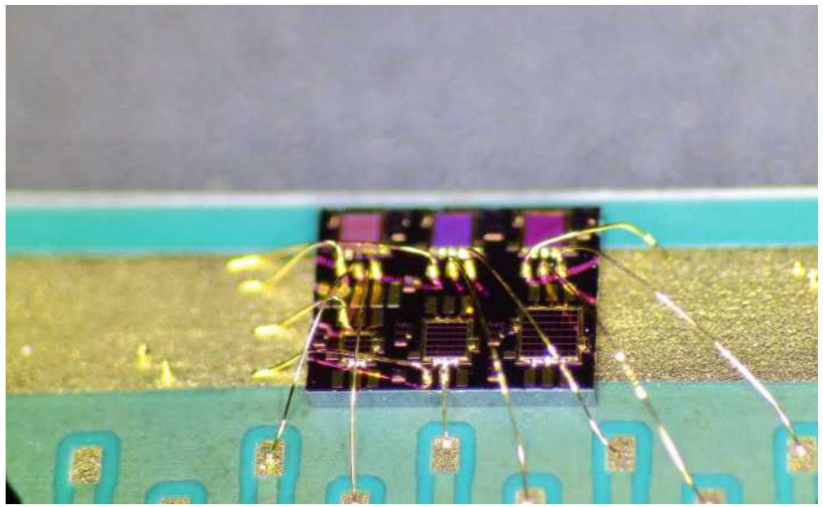


Background: Unknown whether wire bonding to back side will be successful on small, indium hybridized die. This has been successful on bump bonded Icarus parts and will likely succeed on full size GaAs arrays, but small test arrays may be a special challenge.

Development task: Design test board for die arrays. May be able to re-use those developed for Si diode arrays. Develop wire bonding process to backside metal.

Frontside-illuminated GaAs examples





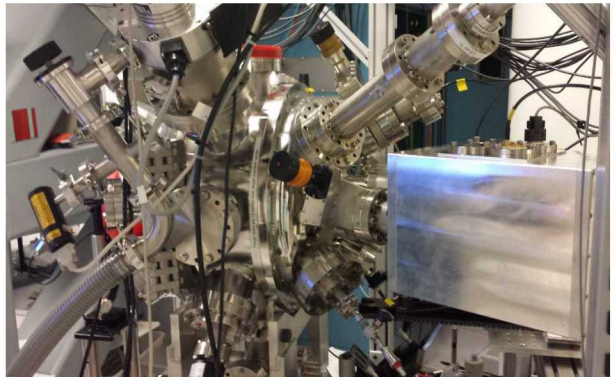
Task 7: Testing

Background: The small test arrays provide us with a unique opportunity to test individual pixel sensitivity, temporal response, and pixel-to-pixel crosstalk. We should demonstrate x-ray sensitive pixel detectors.

Development task: Sub-ns green laser illumination for pixel time response; SEM and apertured laser illumination for cross-talk; Chaco x-ray illumination for x-ray response; possible TruFocus CW x-ray source for responsivity, hard x-ray cross-talk.

X-Ray QE

Pulsed X-Ray



SEM

Pulsed Laser

Multi-Year Timeline and Focus

- FY19:
  - Design, build, and test a ~3x3 and ~36x36 pixelated GaAs array at a thickness of 20-40 microns bonded to a fanout.
  - Design a 0.5 MP GaAs array for bonding to Daedalus
- FY20:
  - Build and test a 0.5 MP GaAs array bonded to Daedalus
  - Design a High Energy ROIC and/or diode array with charge handling capabilities for photon energies up to ~40 keV.
- FY21:
  - Deliver GaAs-Daedalus sensors for use on Z and NIF
  - Build and test a High Energy UXI ROIC and/or diode array for photon energies up to ~40 keV
- FY22:
  - Deliver High Energy UXI sensors for use on Z and NIF

FY19 Timeline