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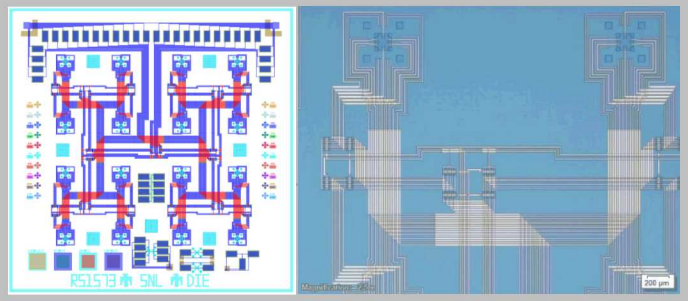

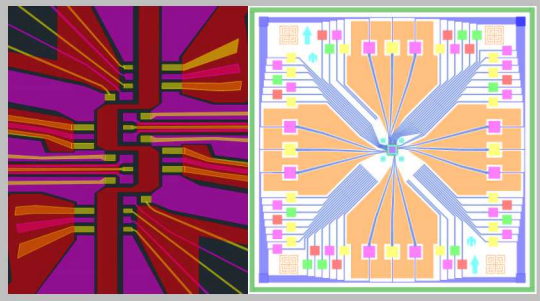

Option 1: Qubits in Gate-Defined Silicon Quantum Dots
UW/Delft/Harvard/SNL Collaboration

Dan Ward

Program Review, Jan. 27th, 2020

U.S. DEPARTMENT OF ENERGY | NNSA National Nuclear Security Administration

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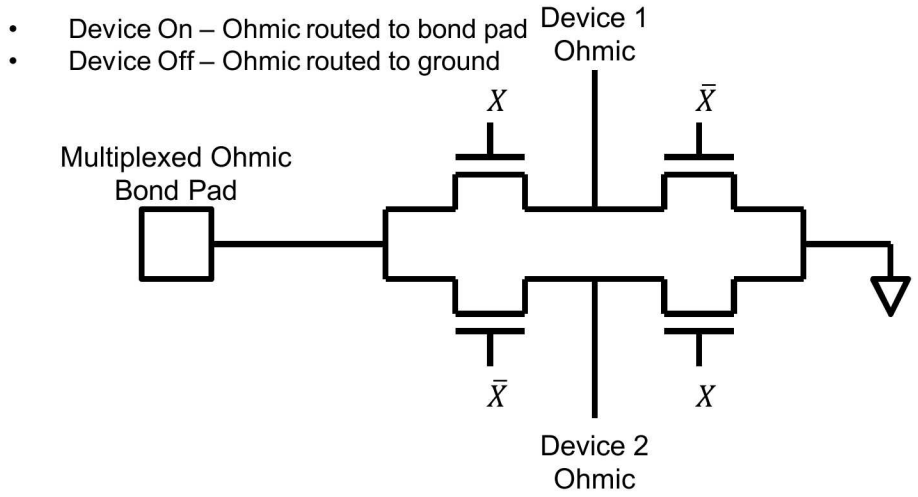
SNL Tasks

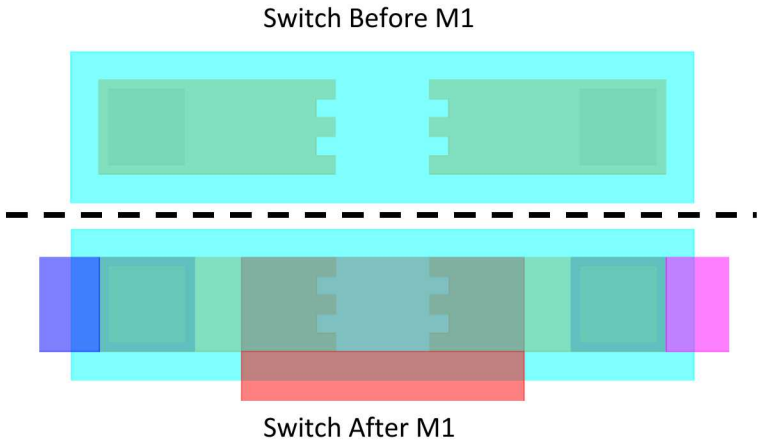
Sandia National Laboratories

1. Charge noise measurement platform
   - Comparison of Hall and charge noise for different cap thicknesses and dielectric films
   - Resolving aluminum gate issues
2. Octuple quantum dot fabrication
   - Towards 4 qubit project goal
   - Gate design from Wisconsin
   - RF PCB Design included in work

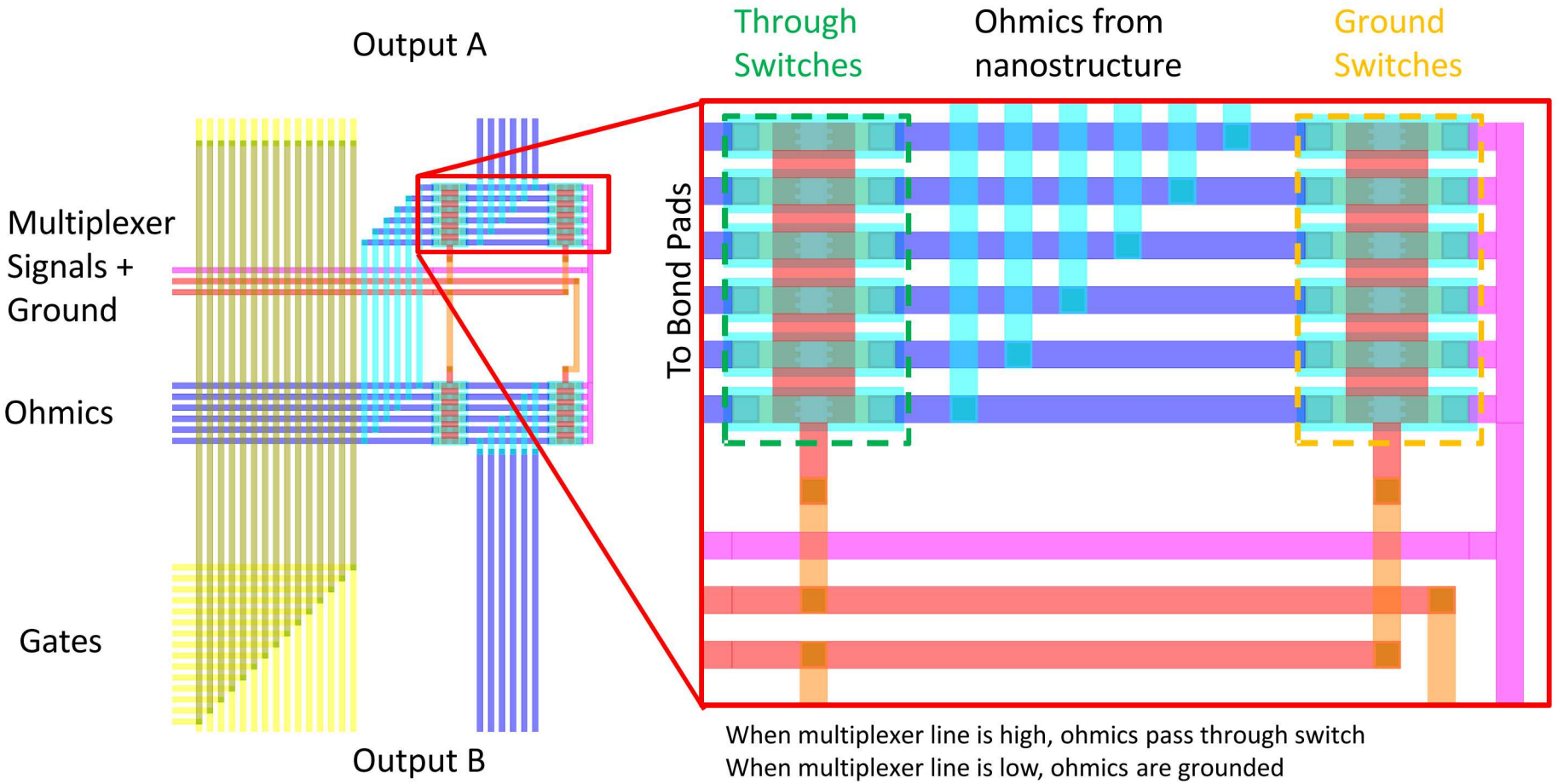
Charge Noise Platform

- Goal: Multiple (32) charge noise measurements on a single die to assess variability
- Approach: Implement on-chip multiplexing to enable measuring 16 different double QD systems (double QD = 2x charge noise measurements)
  - Verify multiplexing operation with Hall bars
    - Decreases yield requirements
    - Mobility across die is also interesting
    - Devices delivered at end of CY19
  - Double QD systems ready for nanostructures
    - Resolving aluminum gate issues
    - Aluminum gate issues must be resolved for 8-QD devices as well
    - Expect to deliver in March

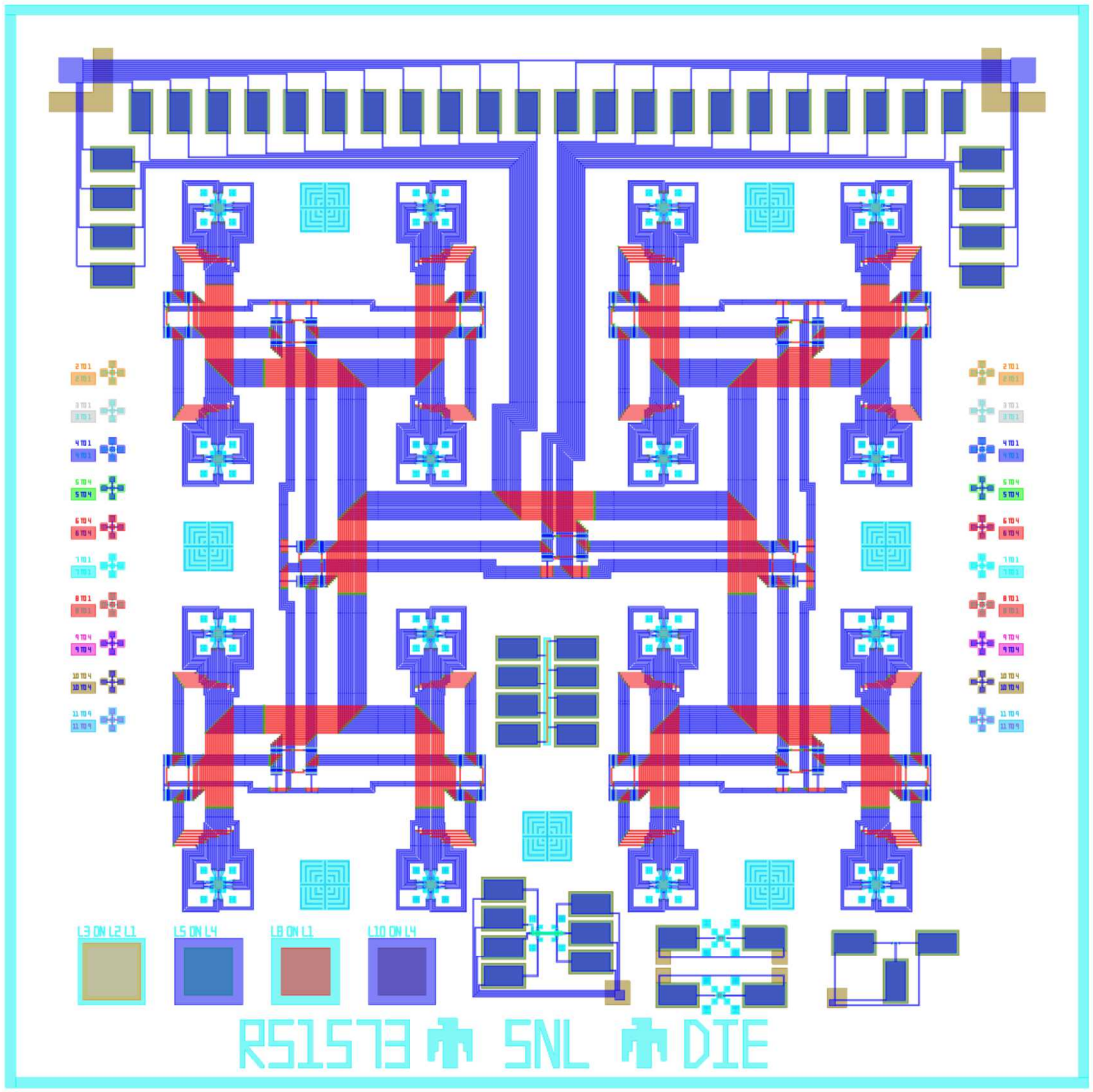




Multiplexer routing

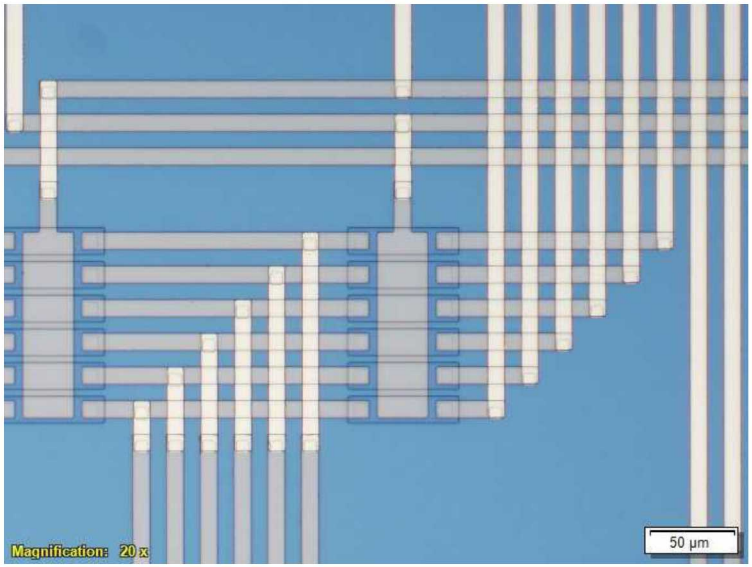


Full design

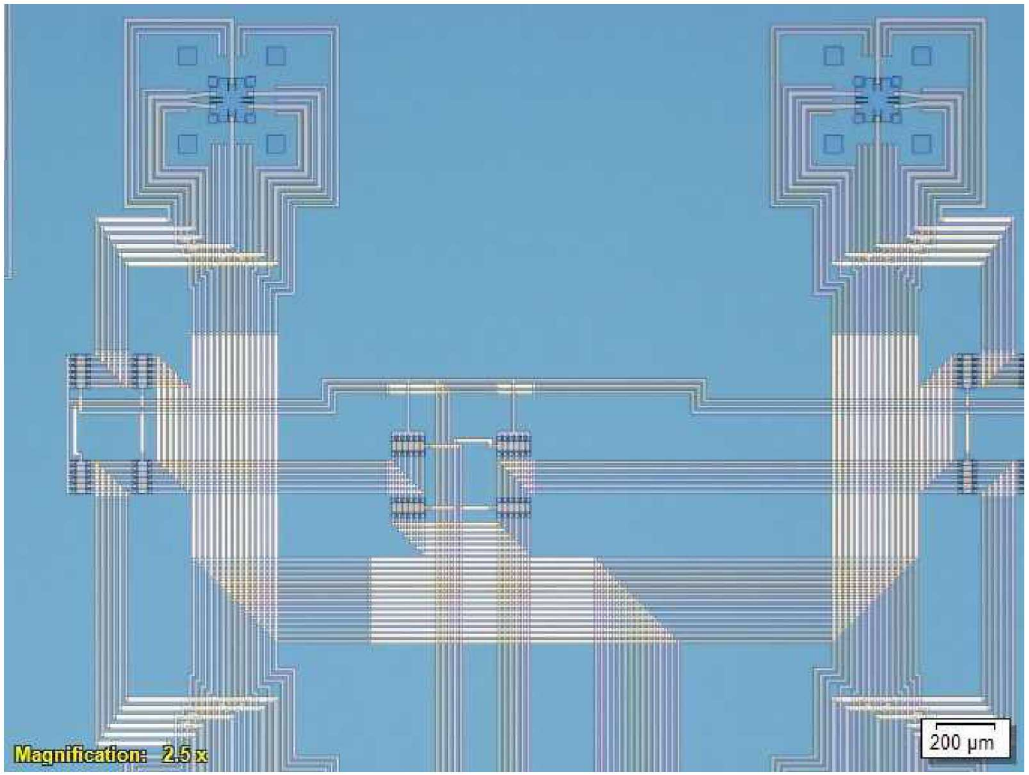


- 10x10 mm die
- 16 DQD devices
- 11 mask levels + EBL
- 2 metal routing layers (blue,red)
- 360 routing switches
- Diagnostics
  - Ohmic conduction
  - Gate isolation
  - Hall
  - Switch isolation

Fabrication in process

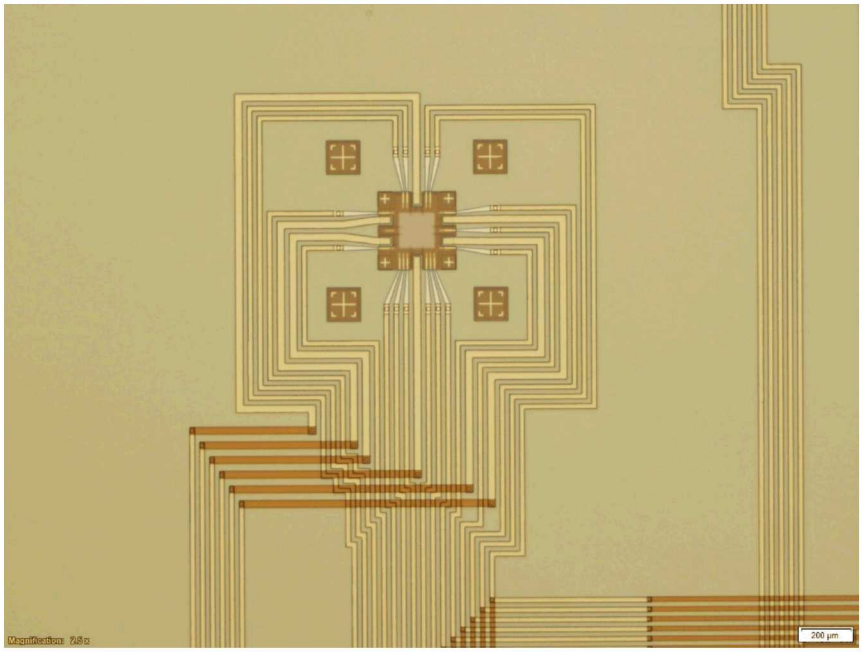


Switch Block after M2



Construction zones after M2

Completed die without nanostructure

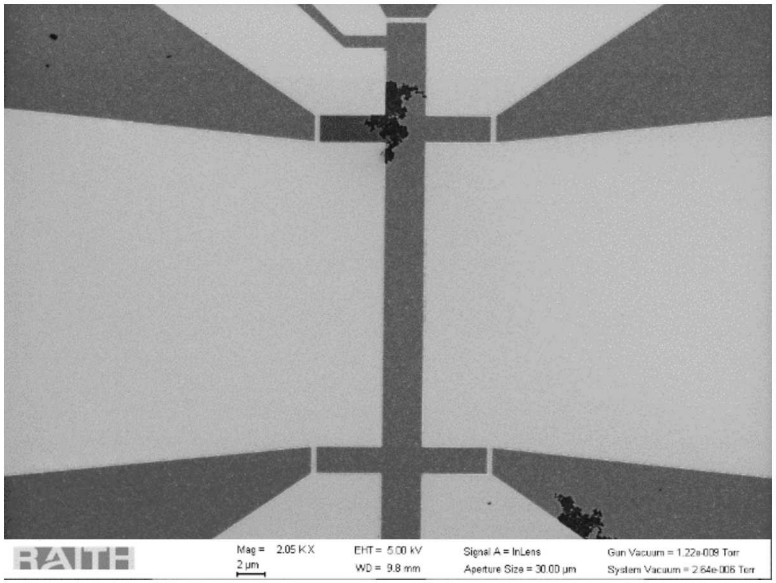


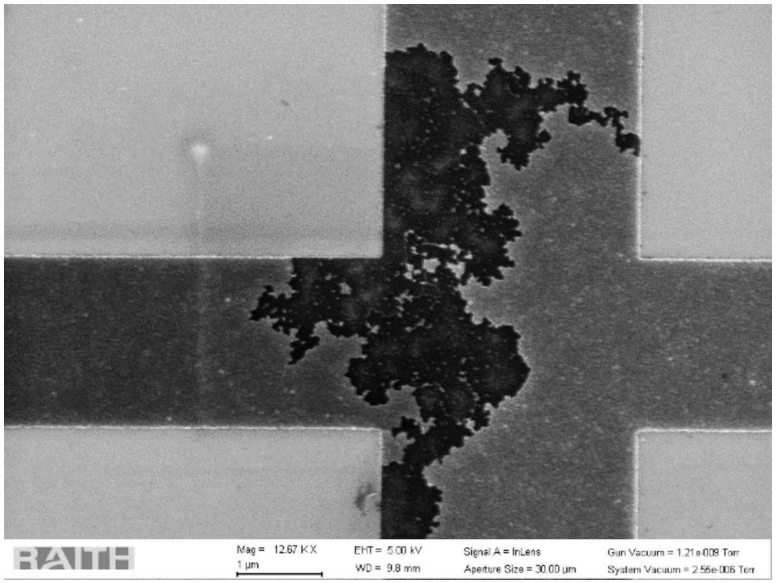
Next steps

- Add nanostructures
  - Validate switch performance - UW
  - Fabricate with DQD
    - Improve yield by changing number of devices patterned per die
    - Working aluminum gate issue

Aluminum gate issue

- Random patches of aluminum in gates is fully oxidizing
- Suspicion is that background pressure of oxygen is causing issues
- Tentative solution: Titanium gettering evaporation + high growth rate Aluminum deposition at -180C
  - Initial testers complete





Example of aluminum oxidation issue

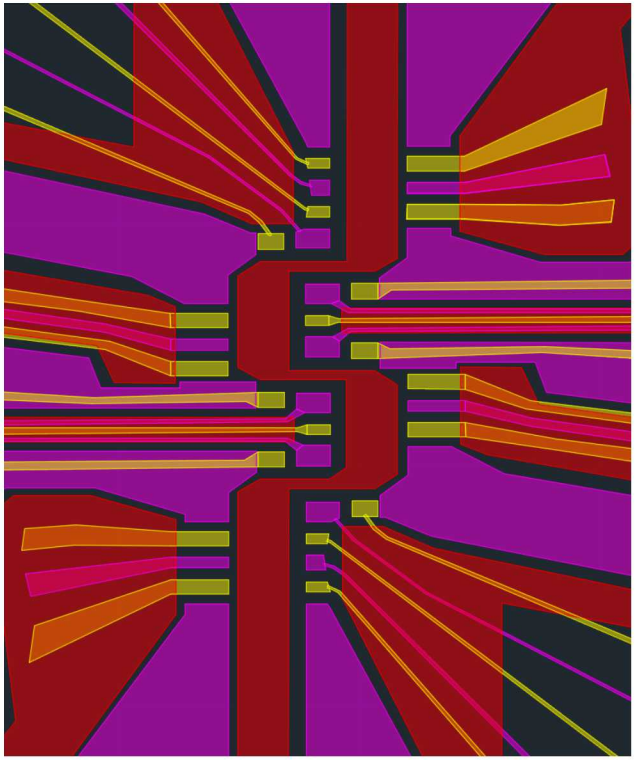
Octuple Quantum Dots

Sandia National Laboratories

- Goal: Build devices with 8QDs with consideration for minimizing RF cross talk
- Approach:
  - UW nanostructure design
  - RF wave guiding on chip (SNL design)
  - Developing PCB design tailored to chip layout

8 dot devices

- Squiggle dot design from UW
- 4 capacitively coupled double QDs with opposing charge sensors
- SNL is designing die and PCB compatible with design



Cartoon Schematic of 8 dot device

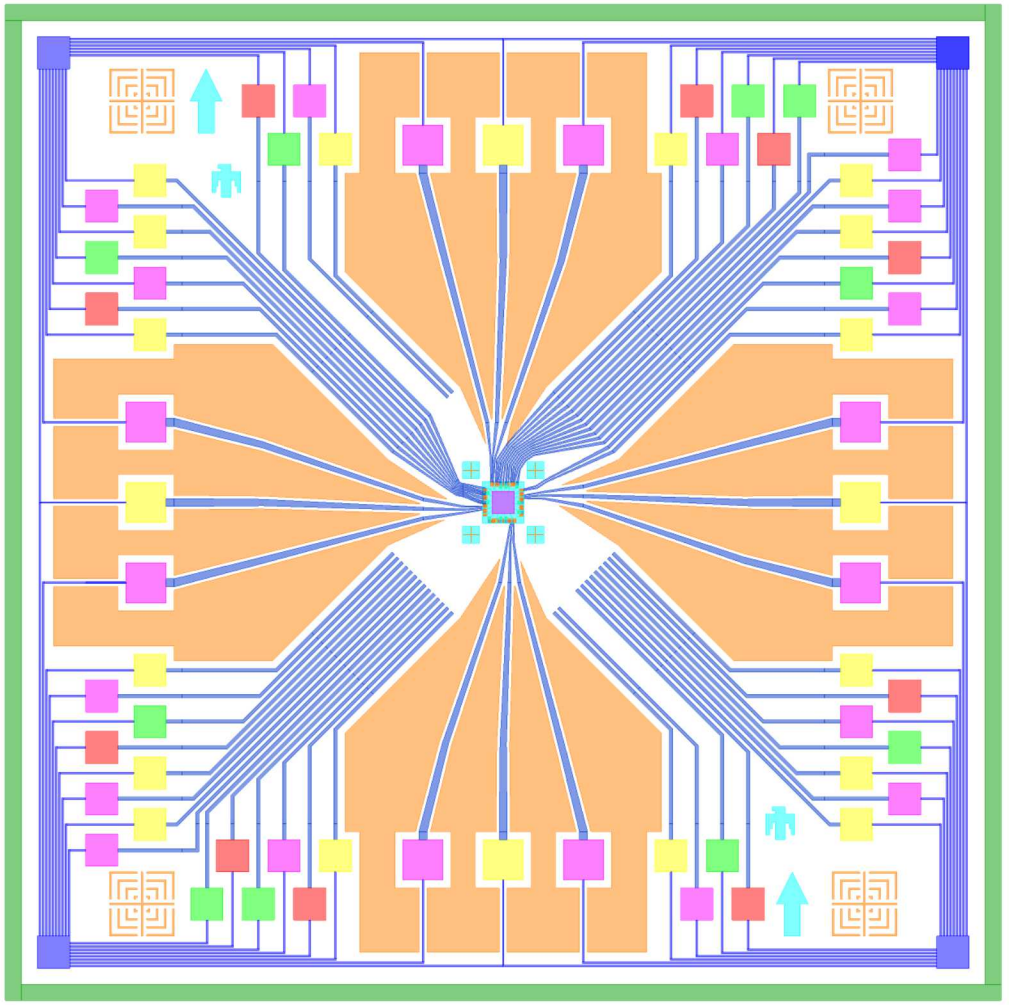
Isolation

Accumulation

Tunnel barrier

8 dot device

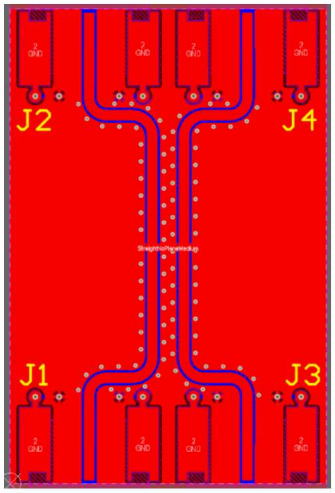
- 52 gates (yellow, magenta, red)
- 12 waveguided gates (orange ground plane)
- 10 ohmics (green)
- In progress
  - Multiple iterations with UW
  - Compatibility across fabs
  - Incorporate up to the minute learning
  - Test fabrication run nearly complete
- Delivery
  - May timeframe



PCB Work

- What level of PCB complexity is needed?
- Built PCBs with and without extra ground planes (adjusting waveguides as needed)
- Experimentally no improvement in crosstalk using more complicated ground plane scheme
- Will test at 4K
- Informing 8QD PCB design

Single ground plane



Extra ground plane