Sandia National Laboratories

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# ESD Tutorial

PRESENTED BY

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# Outline

- Introduction
- I/O and Power Supplies
- ESD Qualification
  - Human Body Model
  - Charged Device Model
  - TLP
- Rail-Based Protection
- Results
- Conclusions

# Introduction

- What is ESD?
  - Known since the early years of Greek philosophy
  - Although many processes in our body are controlled by electricity, our experience of strong electrostatic fields is limited to raised hair.
  - Benjamin Franklin's Kite
  - Albuquerque – Low Humidity
  - ~4000V to produce a visible charge
- Examples
  - Humidity ranges from

| Humidity ranges from | 10%-20% | 65% to 90% |
|---|---|---|
| Walking on carpet | 35,000V | 1,500V |
| Vinyl envelope | 7,000V | 600V |
| Picking up a plastic bag from a table | 20,000V | 1,200V |
| Walking on a vinyl floor | 12,000V | 150V |

# Introduction

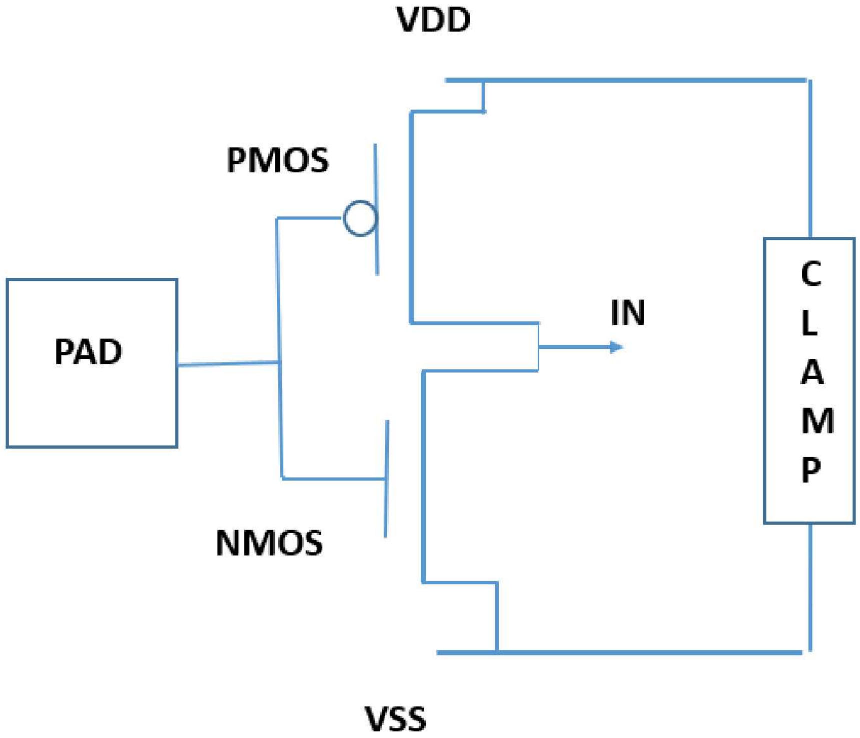
- ESD and Integrated Circuits
  - By definition, ESD interactions associated with ICs are assumed to occur on unpowered parts at room temperature.
  - These events are transient
  - For other situations, electrical overstress (EOS) is the term used to describe damage due to steady over-voltages on powered parts.
  - ESD damage can occur during:
    - IC fabrication
    - Wafer testing
    - Packaging
    - Testing after packaging
    - Handling of the packages
    - Assembly on to Boards
    - Testing of systems
  - ICs are customarily designed to provide a certain level of protection from the hazards that the devices are expected to experience. ESD protection level is only as good as the weakest pin.
  - As in most situations, compromise between chip area, circuit performance, ESD capability and radiation effects must be considered.
  - With each process generation, resulting in smaller geometries, thinner gate oxides, lower breakdown voltages, larger pin counts, etc., it becomes more difficult to provide good ESD protection.
  - Reference: Amerasekera and Duvvury, **ESD in Silicon Integrated Circuits**, 2nd Ed, Wiley, 2002.

# I/O and Power Supplies

- ESD damage that occurs during IC processing is healed during the thermal process steps that are used in the process flow until the final metal and passivation are completed.
- Connections to the outside world
  - Power Ground Inputs Outputs
- Zapping between any pair of pads with either polarity can result in ESD damage. **It only takes one weak pad**.
- Inducing charge into the die and discharging through a single pin can also cause ESD damage. **Again, it only takes one weak pad**.
- All of the Input and Output pads and the Power and Ground pads have circuitry to protect the pads from ESD events.

# I/O and Power Supplies

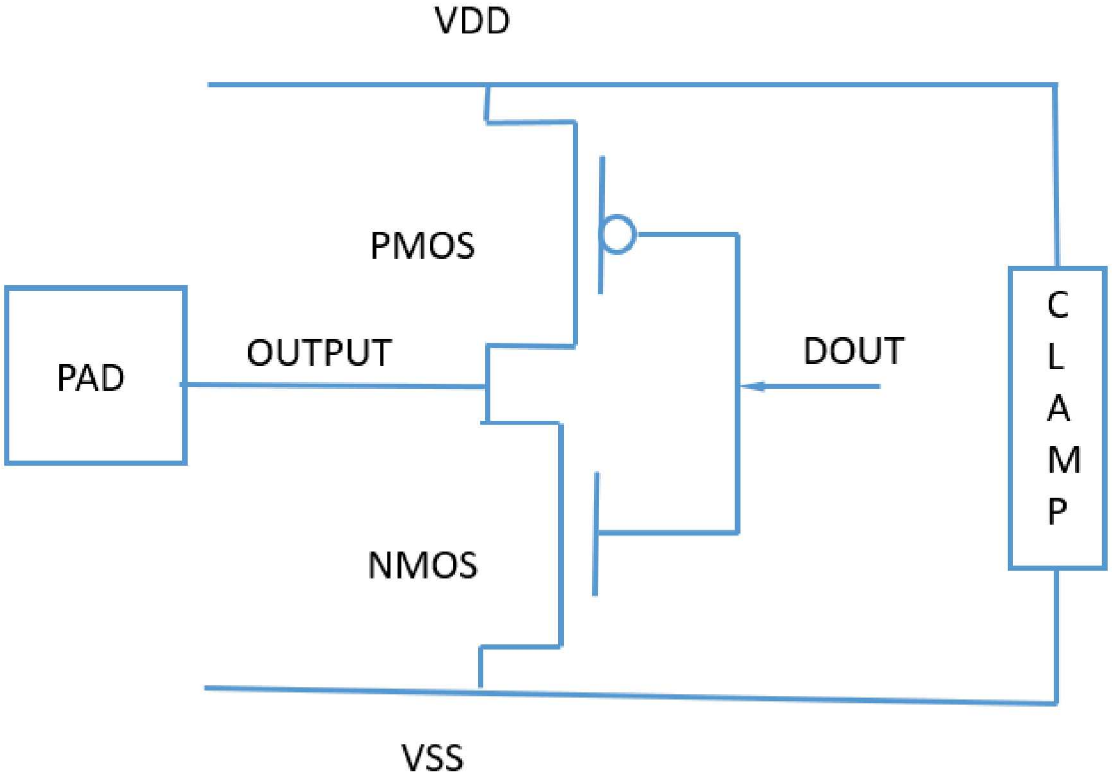
- What components are susceptible to ESD?
  - Input Circuit




A voltage applied between either the PAD and VSS or VDD places a stress across the gate oxide that can breakdown the oxide. That oxide breakdown is a function of the process flow.

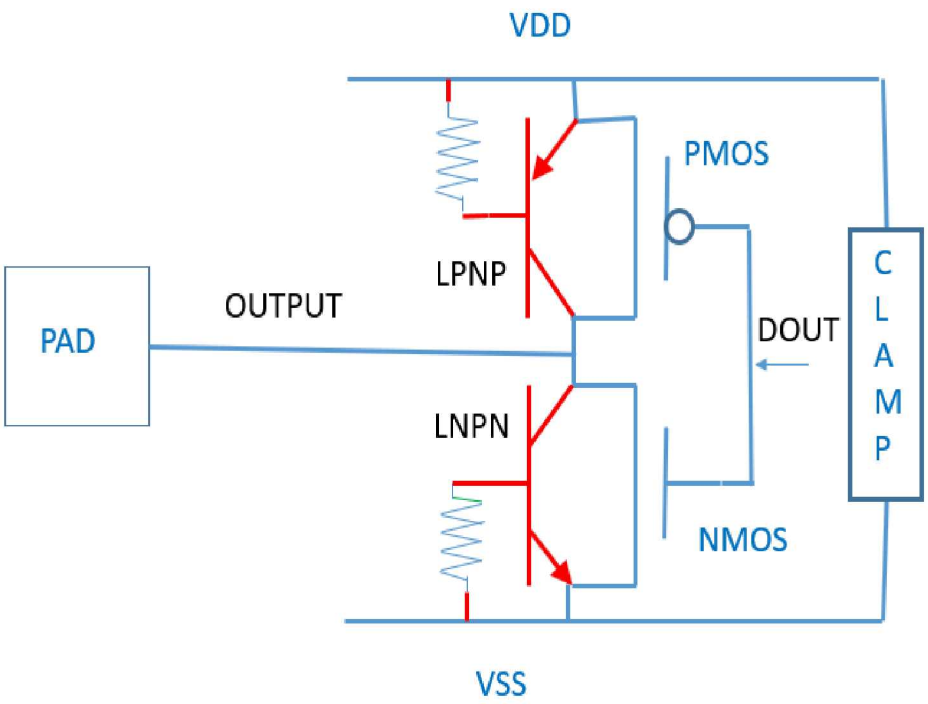
# I/O and Power Supplies

- Output Pad




A voltage stress from PAD to VSS can result in a failure of the NMOS pull-down and a voltage stress from PAD to VSS can result in a failure of the PMOS pull-up.

# I/O and Power Supplies



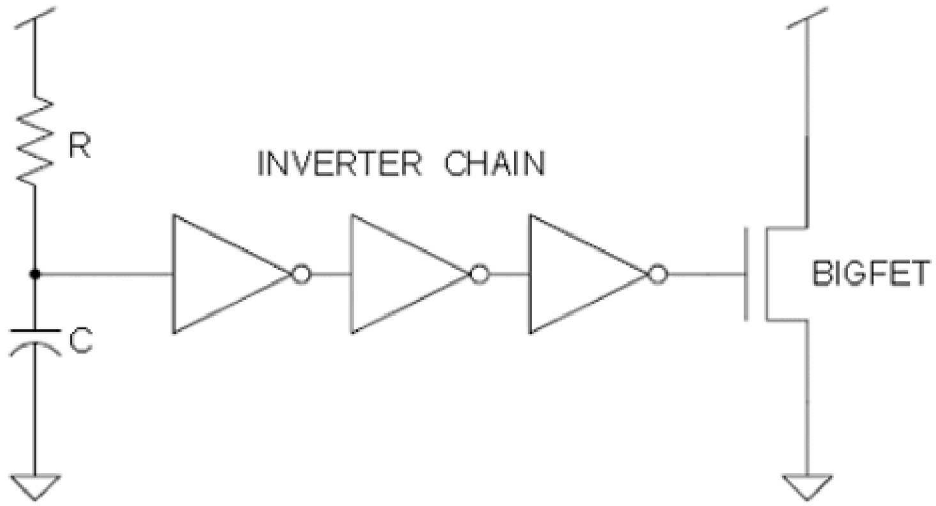

Output Pad with parasitic bipolar transistors.

# I/O and Power Supplies

- Power Supply Clamps prevent the destruction of the internal core circuitry.
- In digital CMOS integrated circuits, most of the logic consists of PMOS and NMOS transistors with one conducting and the other blocking.
- Most of the power Supply clamps make use of large NMOS BigFETs distributed around the die (typically a total of 4000µm wide with a minimum channel length) that are triggered during ESD events and are turned off after the event is completed.

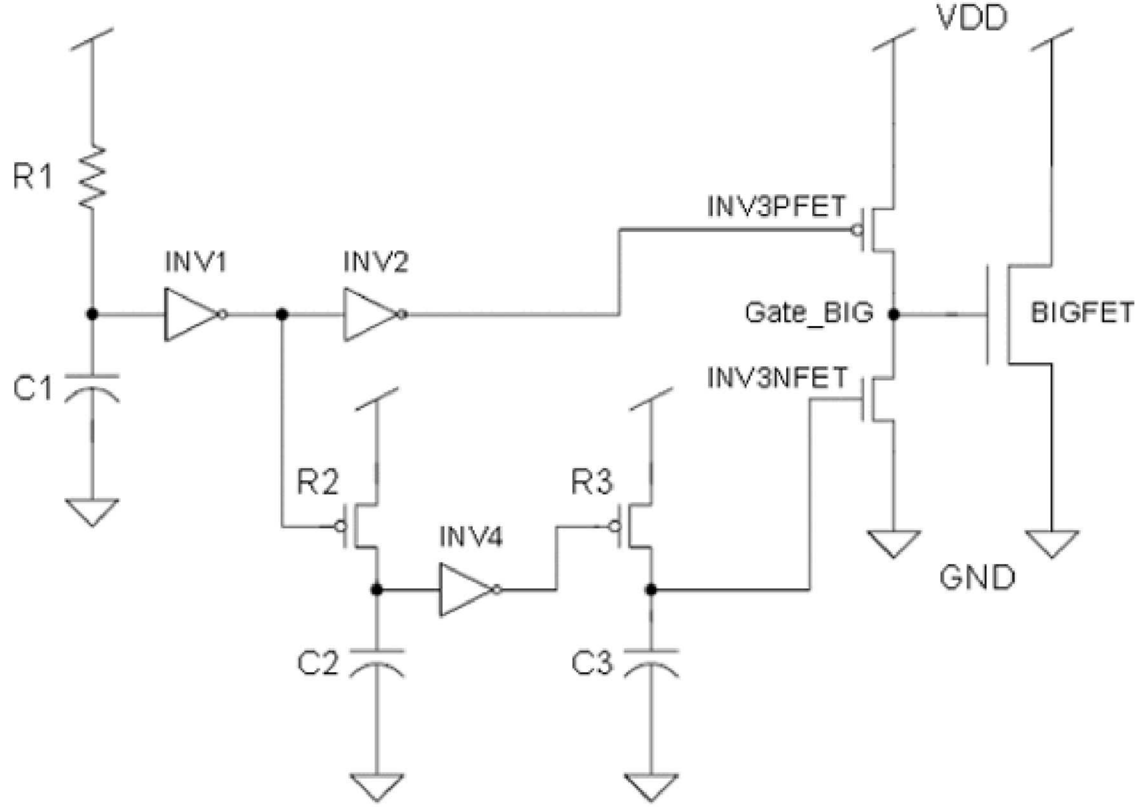
# I/O and Power Supplies

Basic clamp



# I/O and Power Supplies

Multi-RC-Triggered Clamp designed to prevent false triggering during rapid power supply ramps.



# I/O and Power Supplies

- For complex integrated circuits, multiple power domains are common. The individual domains may have different voltages and separate ground connections. Each domain must be protected with 4000µm wide BigFETs and preferred paths to make sure that all of the possible combinations can be safely zapped. Sometimes, when you have multiple grounds, you can provide anti-parallel diode blocks between the various grounds.

# ESD Qualification HBM

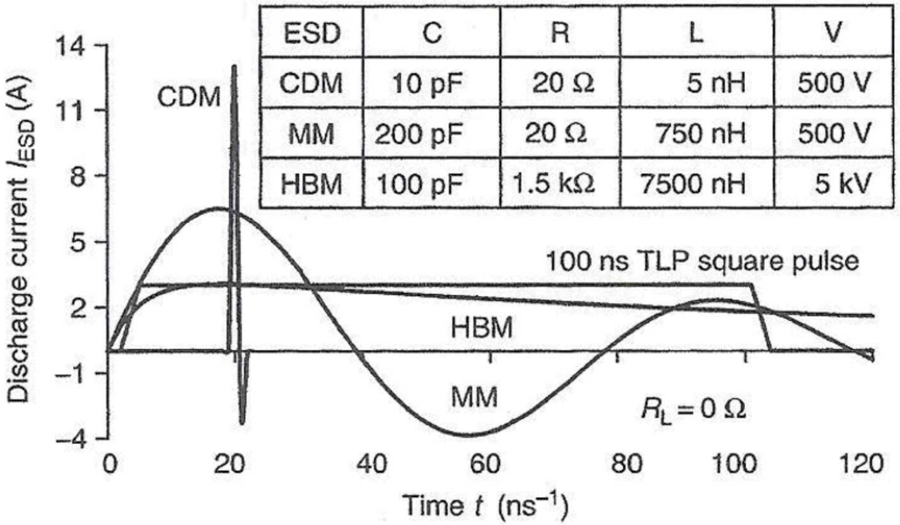
- Sometime in the 1980s, integrated circuit manufactures realized that it was relatively easy to destroy their products.
- In addition to changing the environments where the ICs were made and assembled, they decided to include protection on the individual dice.
- There were two general categories
  - Electrical Over Stress (EOS)
  - Electrostatic Discharge (ESD)
- After some experimenting, they concluded that a “human body model” (HBM) would be a 100pF capacitor charged to a specific voltage would be discharged through a 1.5kΩ resistor with a 10ns rise time (controlled by a 7500nH Inductor).

# ESD Qualification HBM

- Of course, they had to make a whole set of standards and got the MIL Spec issued.
- Back in those days, with 14 pin DIP, they said you have to zap three times with both polarities each VDD to VSS, each I/O to each VDD and each VSS, and each I/O to the other I/Os with the VDD and VSS floating.
- They assumed that 3 samples should be sufficient at each voltage and started to hope that they could go up to 2kV.
- Again of course, there were no machines set up to do these tests, so 3 or 4 companies set up to make "standard" machines. Relays entered the situation, and a variety of IC companies started to compare the results on the different machines.

# ESD Qualification

- 41 years ago, the EOS/ESD Symposium was initiated.
- Papers through the years have helped to determine which machines are best, and the specifications now include waveform specs.
- Since then, we have generated some new qualification types.




| ESD | C | R | L | V |
|---|---|---|---|---|
| CDM | 10 pF | 20 Ω | 5 nH | 500 V |
| MM | 200 pF | 20 Ω | 750 nH | 500 V |
| HBM | 100 pF | 1.5 kΩ | 7500 nH | 5 kV |

# ESD Qualification        CDM

- The Machine Model (MM) was introduced by the Japanese, but it has gradually disappeared, since the type of failures was proven to be similar to HBM.
- The Charged Device Model (CDM) represents an entirely different type of failure, and is now becoming the most important qualification.

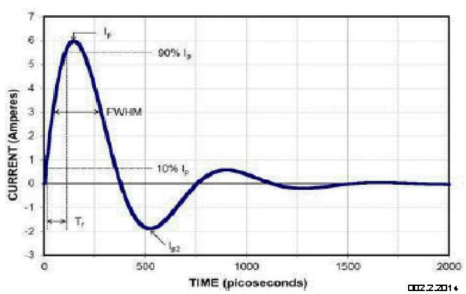
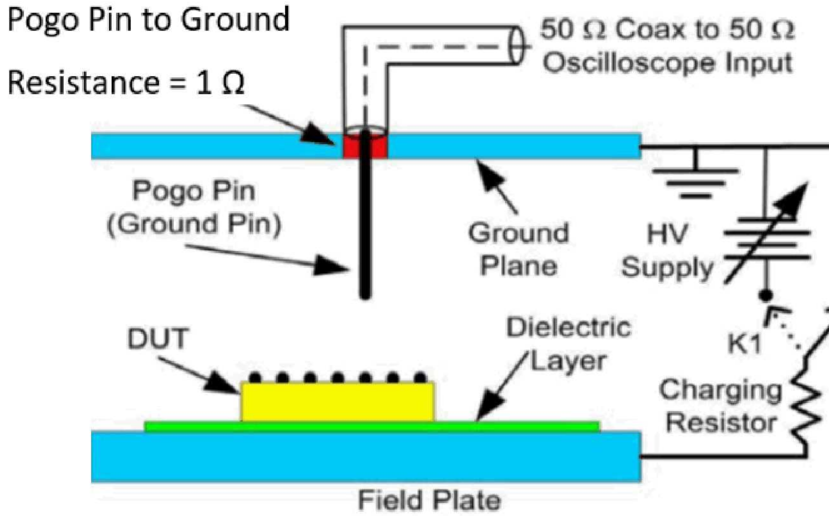



*Figure 2: CDM Characteristic Waveform and Parameters*

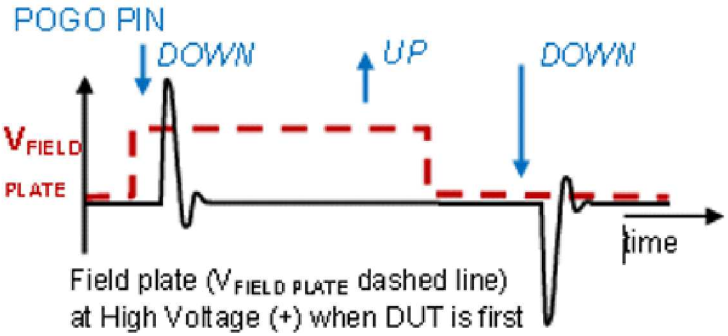


# ESD Qualification CDM

- Charged Device Model (CDM) (the Dead Bug)
  - The CDM stress is a relatively new test.
  - There were a number debates over the Dead Bug vs. the socketed CDM, but the official standard is the Dead Bug.
  - In this case the packaged part is placed with the pins facing upward on a plate that is raised to a specific voltage, then each pin is discharged through a "pogo pin" to ground (positive and negative) through a 1 Ω cylindrical resistor.
  - It is important to recognize that the CDM performance is related to the die area and the package. The same die will perform differently in a different package.

# ESD Qualification CDM

- CDM current pulse is on the order of 500 ps and has a much higher peak value than HBM
- The procedure for getting both polarity pulses from a single induced voltage is shown in the figure.
- Each pin is zapped in both polarities, even if there are multiple pins tied together (like 65 VSS pins on Eiger.)




Field plate ($V_{FIELD\ PLATE}$ dashed line) at High Voltage (+) when DUT is first contacted by pogo pin, and at Zero when contacted the second time.

# ESD Qualification HBM

- HBM Range
  - Typical products will pass 500V HBM, 1kV HBM, and 2kV HBM (Class 2)
  - We Stress three parts each at 500V HBM, 1kV HBM, 1.5kV HBM, and 2kV HBM to ensure that our parts are at least Class 1C
  - Automotive applications require at least 4kV HBM
  - Note: The lowest level at which a single pin fails determines the Class
  - Failure is defined as Pass/Fail on the final test

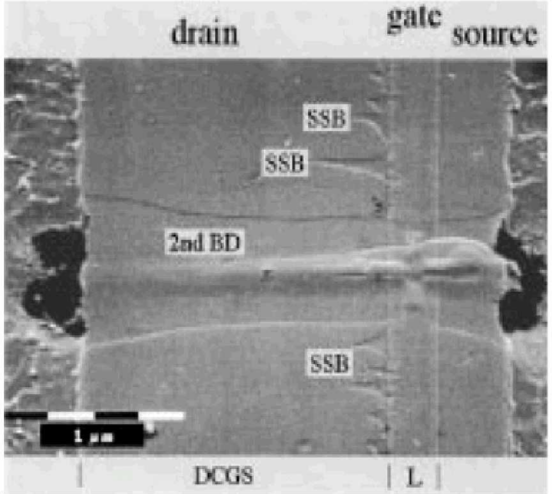



Figure I I-4. FMA SEM picture of HBM ESD tested gg-nMOSts showing sub-surface breakdown (SSB) and second breakdown (second BD) silicon melt signatures. DCGS stands for drain-contact-to-gate spacing.

# ESD Qualification CDM

Table 3. CDM ESDS Device Classification Levels

| Classification Level (see Note 1) | Classification Test Condition (in Volts) (See Note 2) |
|---|---|
| C0a | < 125 |
| C0b | 125 to < 250 |
| C1 | 250 to < 500 |
| C2a | 500 to < 750 |
| C2b | 750 to < 1000 |
| C3 | ≥ 1000 (see Note 3) |

NOTE 1: Use the "C" prefix to indicate a CDM classification level.

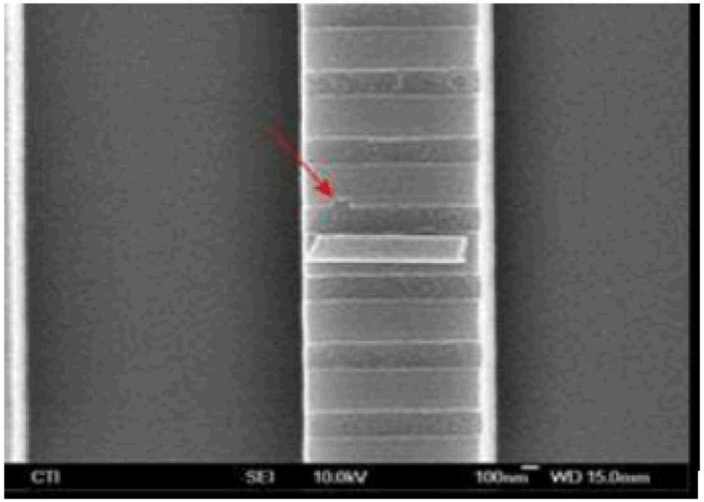



Figure III-6. The SEM micrograph of the FAR depicts a pin hole in a gate oxide. This failure picture is classified as typical CDM-type fail.

# ESD Qualification

- The term "Qualification" should be recognized as a way of comparing your product to similar products from your competition.
- Your customer will determine whether or not to accept your product.
- Note that different designs made on the same process may have different levels of HBM and CDM.

- CDM in particular is package dependent.

# ESD Qualification TLP

- The most useful technique for developing ESD protection structures is the Transmission Line Pulse (TLP).
- This plot is for a grounded gate NMOS transistor. Each point on the black line is an individual pulse. The quasi-IV plot looks like a real IV plot. The leakage scale is logarithmic across the top of the graph. The red plot does not show each individual point, but they are all included. The TLP can be used at either wafer level or package level.

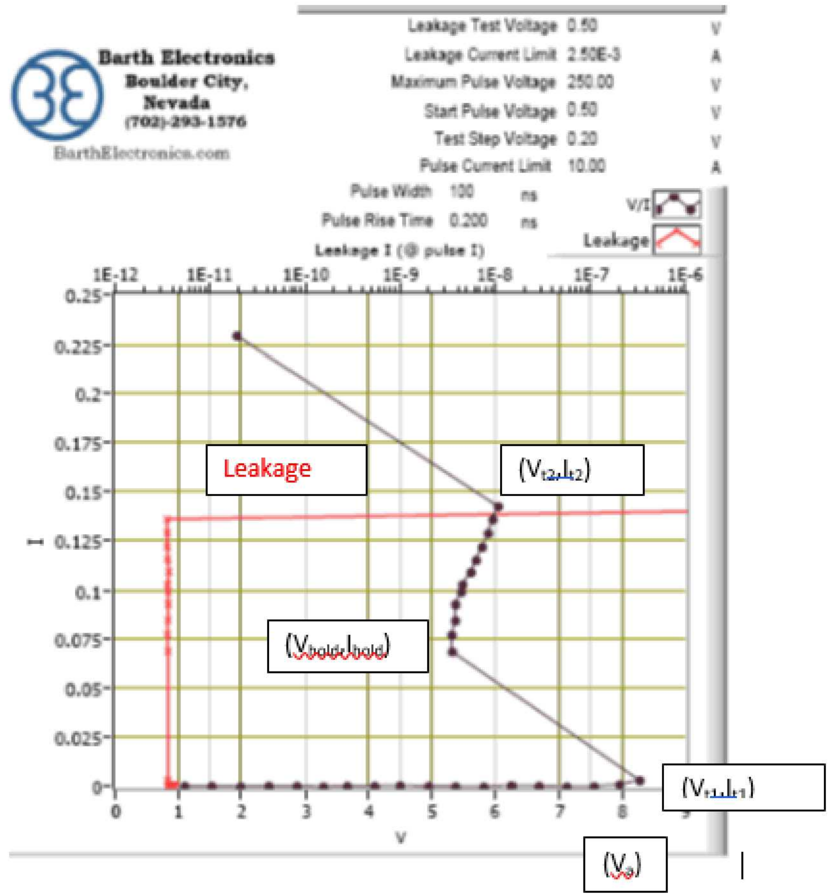


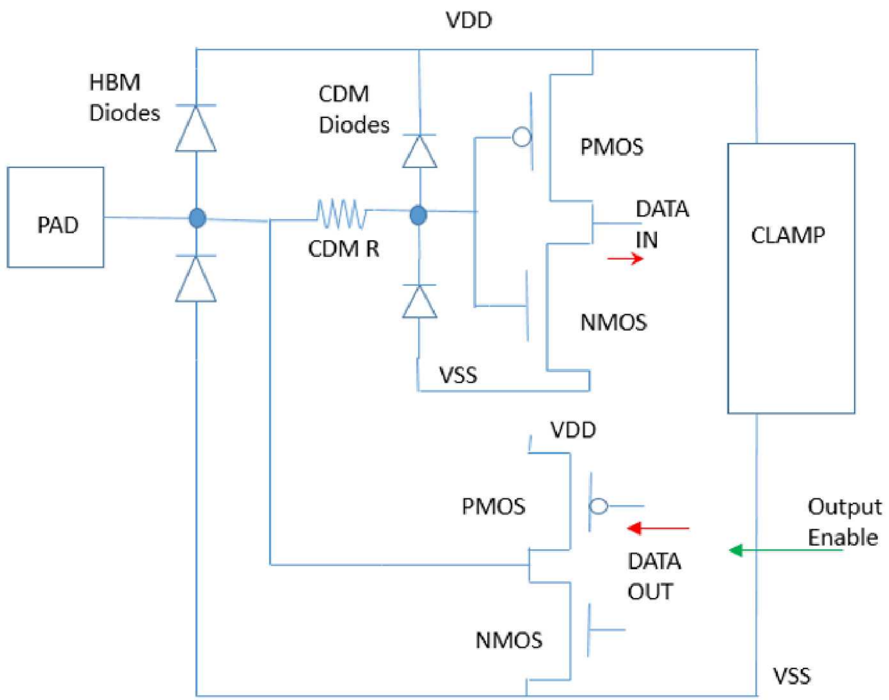

Figure V-5. TLP of a ggNMOS.

# Rail-Based Protection

- ESD protection on CMOS Silicon-on-Insulator (SOI) has some differences compared to bulk silicon CMOS.
  - SOI prevents the formation of PNPN devices which result in Latch-Up in bulk silicon. It is possible to form PNPN switches in SOI but it requires special designs.
  - Bulk silicon has an advantage in providing thermal paths from the devices that are blocked by the buried oxide in SOI.
  - Bulk silicon has direct connections to the substrate which provides paths for CDM stresses.
- Rail-based protections are useful in both SOI and bulk silicon.
- All OUTPUT and INPUT Pads have an Up-Diode from the pad to the VDD and a Down-Diode from VSS to the pad.
- There is a Power Supply Clamp from VDD to VSS in each Power Domain.

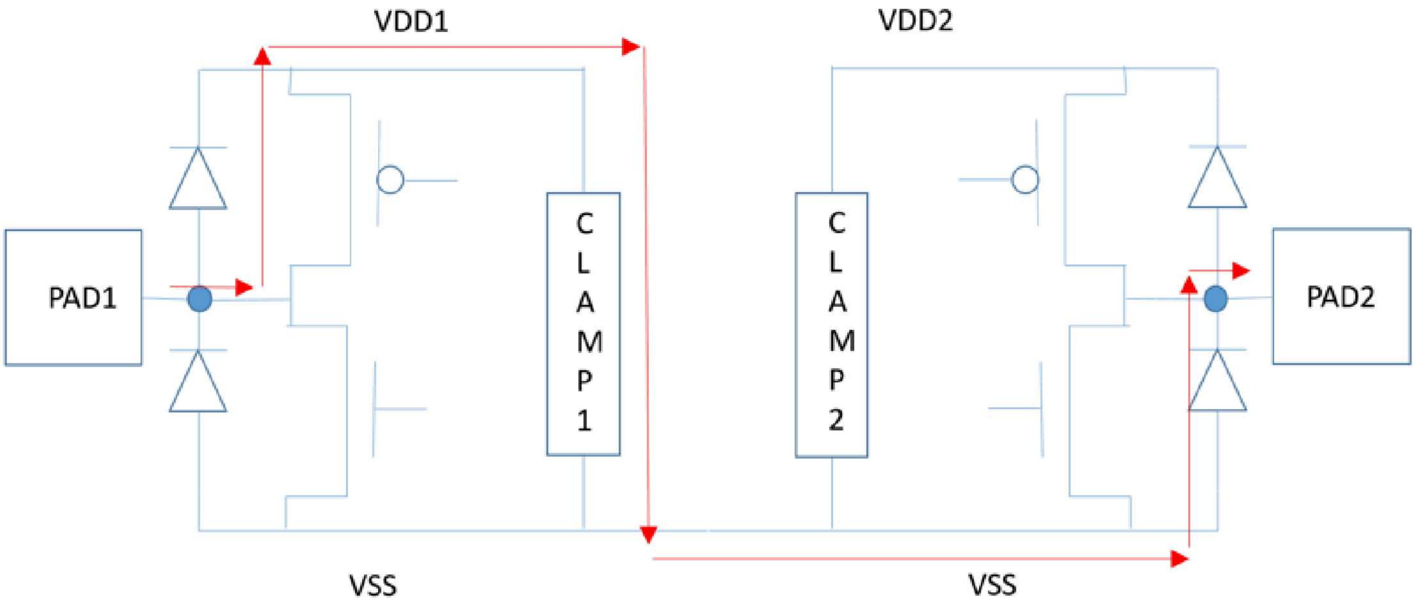
# Rail-Based Protection

- All OUTPUT and INPUT Pads have an Up-Diode from the pad to the VDD and a Down-Diode from VSS to the pad.
- INPUT Pads have an additional pair of diodes and a CDM resistor
- There is a Power Supply Clamp from VDD to VSS in each Power Domain.



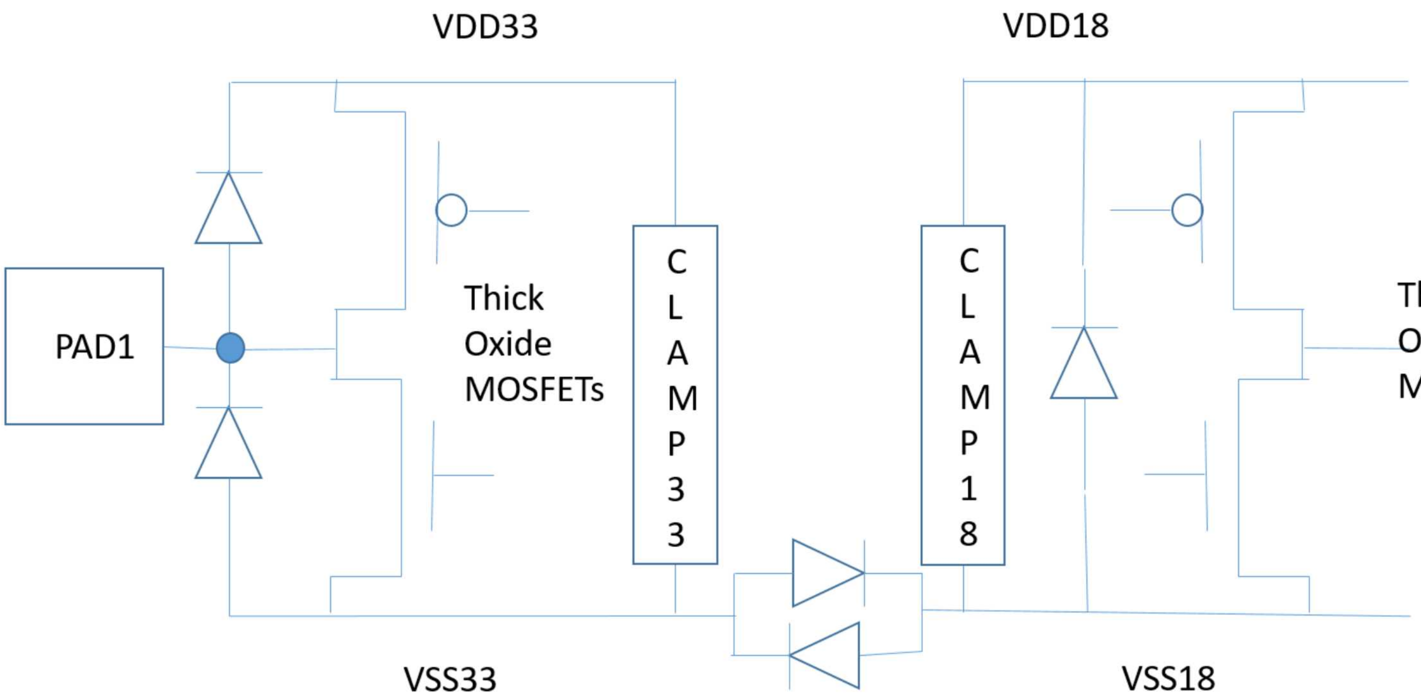
# Rail-Based Protection

- Rail-Based Protection for Multiple Power Domains with common ground



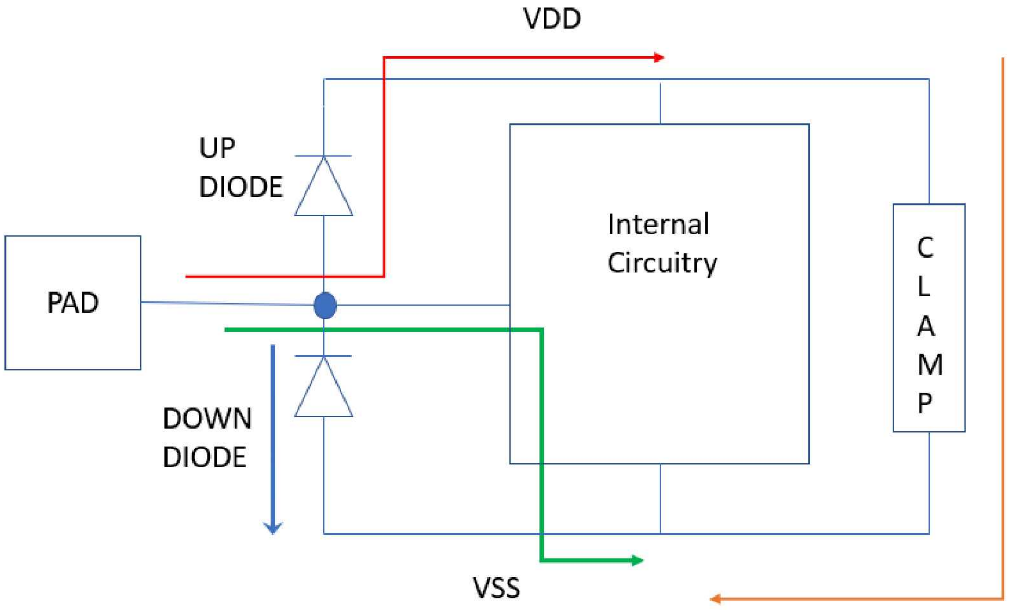
# Rail-Based Protection

Rail-Based Protection for Multiple Power Domains with separate grounds and different power supplies (HBM zap from PAD1 to VSS18 or VDD18)

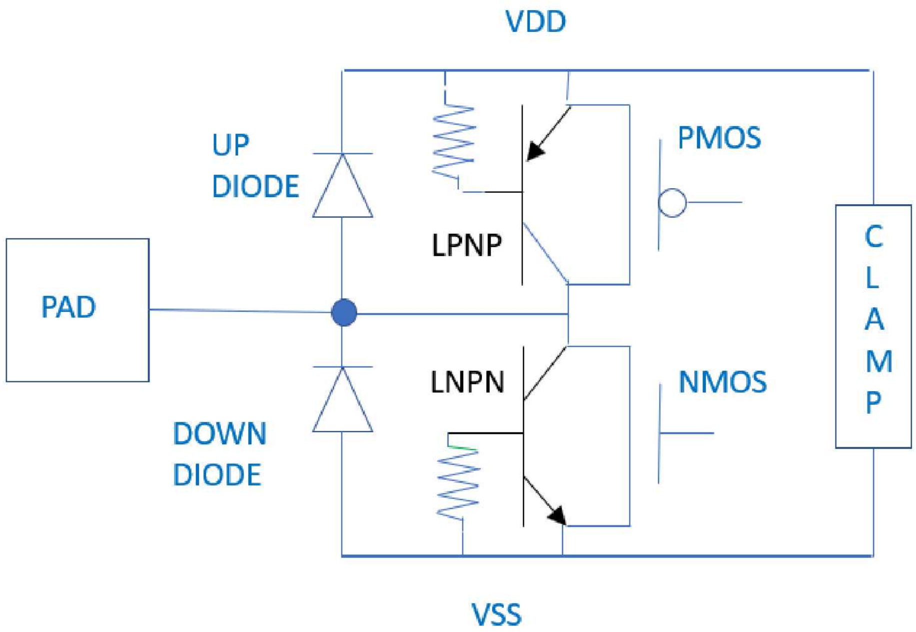


# Rail-Based Protection

- Preferred path
- Undesired path if the diode breakdown occurs
- Undesired path if internal circuitry is on or turns on because the power supply is charged during the ESD event.



# Rail-Based Protection OUTPUTs



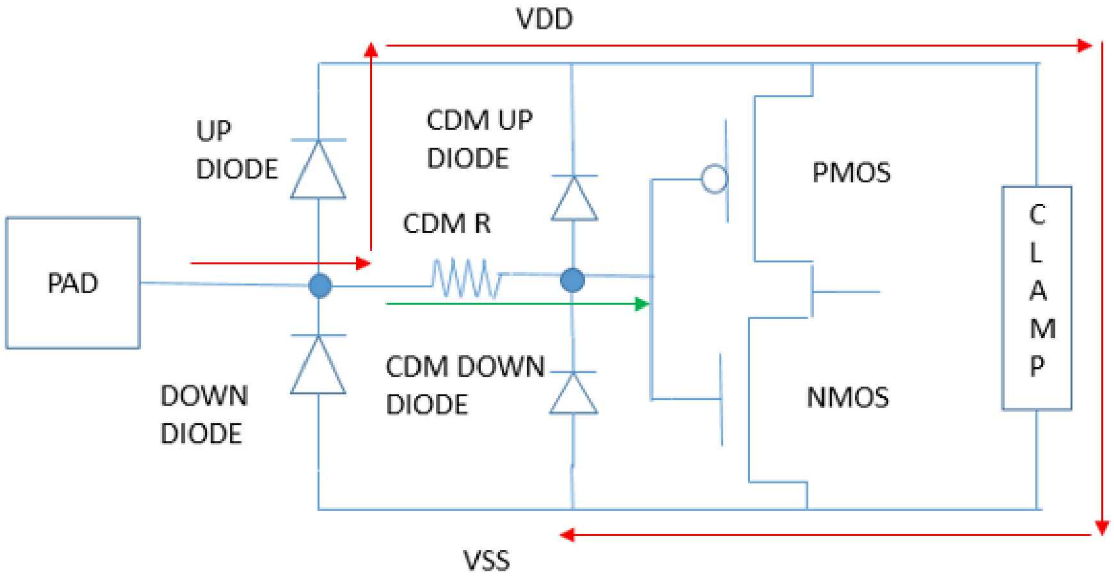

Rail-based protection for an OUTPUT Pad including the parasitic lateral bipolar transistors in parallel with the PMOSFET and NMOSFET.

The weak link is the LNPN with a large Snap-Back compared to the LPNP due to a much higher β in the LNPN.

A positive HBM zap from Pad to VDD will go through the forward-biased Up Diode.
A positive HBM zap from VSS to Pad is protected by the forward-biased Down Diode.
A positive HBM zap from Pad to VSS can go through the forward-biased Up Diode and through the Clamp, but it can also go through the reverse-biased Down Diode or through the LNPN which can go into Snap-Back and destroy the circuit. In a similar situation, a positive HBM zap from VDD to the Pad could go through the LPNP.

# Rail-Based Protection INPUTs

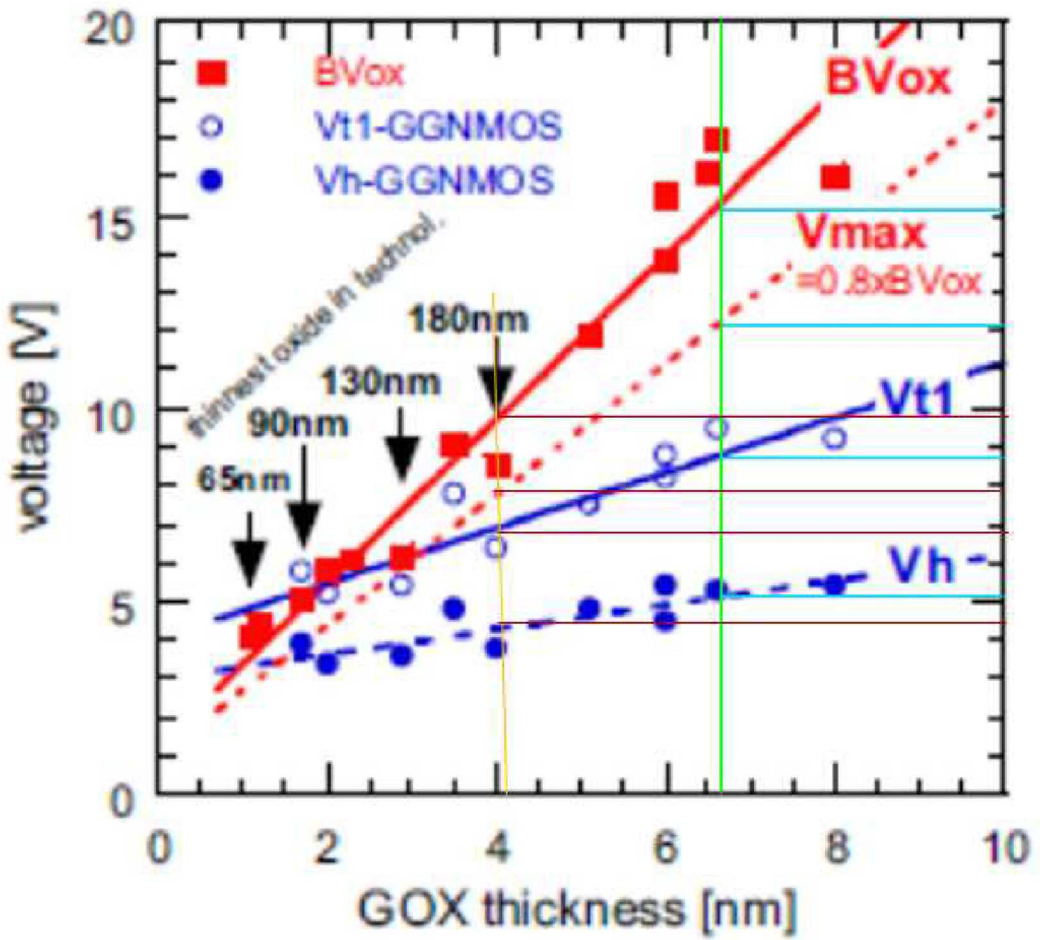
Rail-Based protection for INPUTs must provide both HBM and CDM protection. The preferred path for HBM is shown in red. If the green path occurs, the gate oxide will breakdown.




The CDM Resistor and the CDM UP and DOWN Diodes are selected to limit the voltage across the gate oxides during CDM events. The CDM UP and DOWN Diodes are typically 1/3 the size of the UP and DOWN HBM Diodes. In most cases, CDM R is between 200 and 300 Ω.

# Rail-Based Protection INPUTs

- Transient breakdown of NMOS GOX (area <40µm²) as a function of GOX Thickness in various bulk CMOS technologies (180nm to 65nm). Green is 350nm and Orange is 180nm.

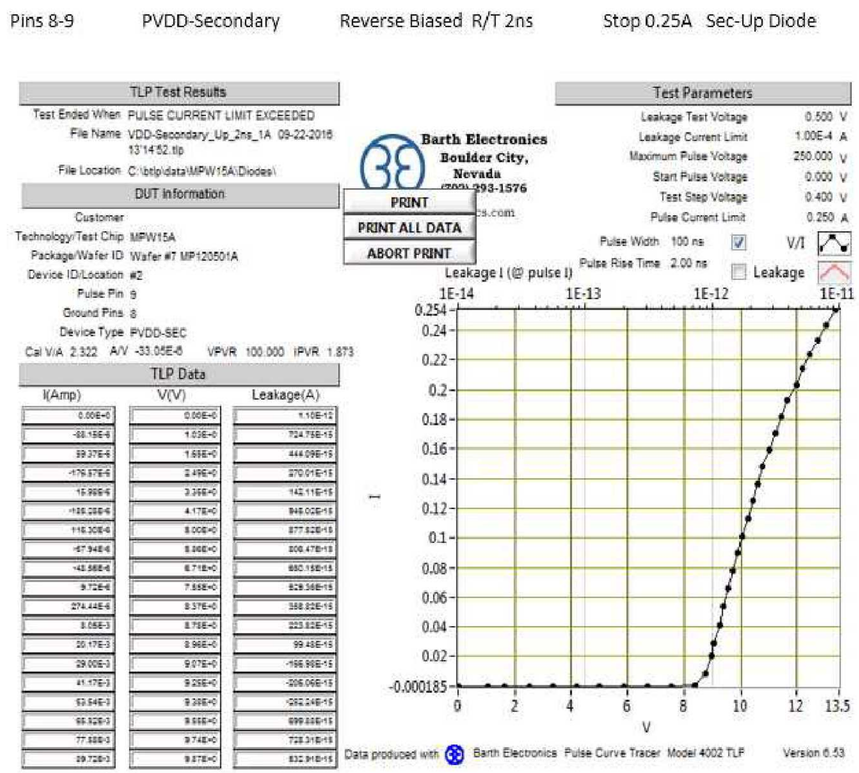


# Rail-Based Protection ANALOG

- ESD protection of ANALOG Pads is not as well defined as ESD protection of digital pads.
- In general, the same diodes are used to protect both digital and analog pads.
- The ANALOG pads can be either inputs or outputs.
- Resistors can have an impact on the performance of analog circuitry.
  - Some analog pads have the HBM UP and DOWN diodes and go directly to internal circuitry. That internal circuitry determines the ESD performance.
  - Some ANALOG pads are bare wires (no resistors and no diodes)
  - Choose your own resistor size rather than trying to make a standard.

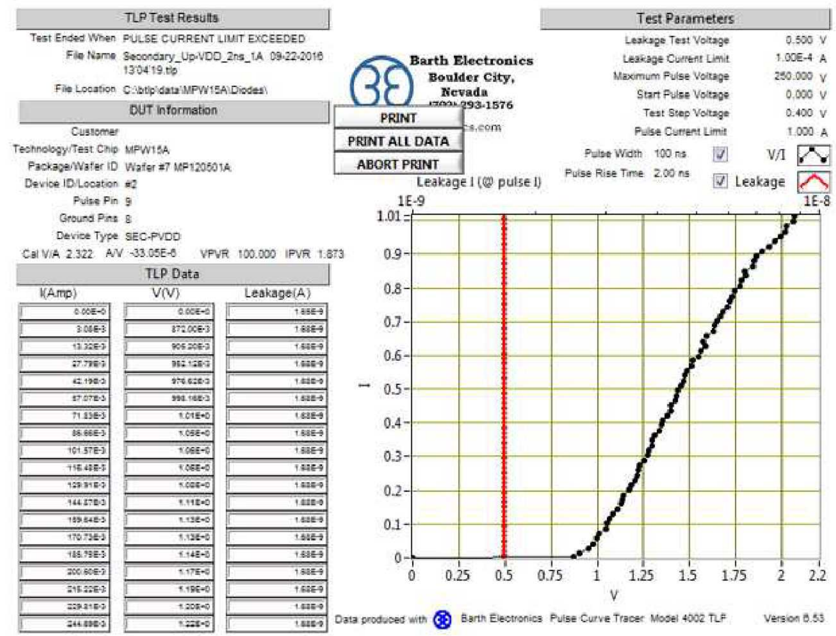
# Results DIODEs

- The diodes used in Pad Cells are special devices. They must be large enough to withstand a reverse breakdown voltage that appears to be an avalanche breakdown with a resistor in series.
- This diode fails at 0.25A and 13.5V



# Results   DIODEs

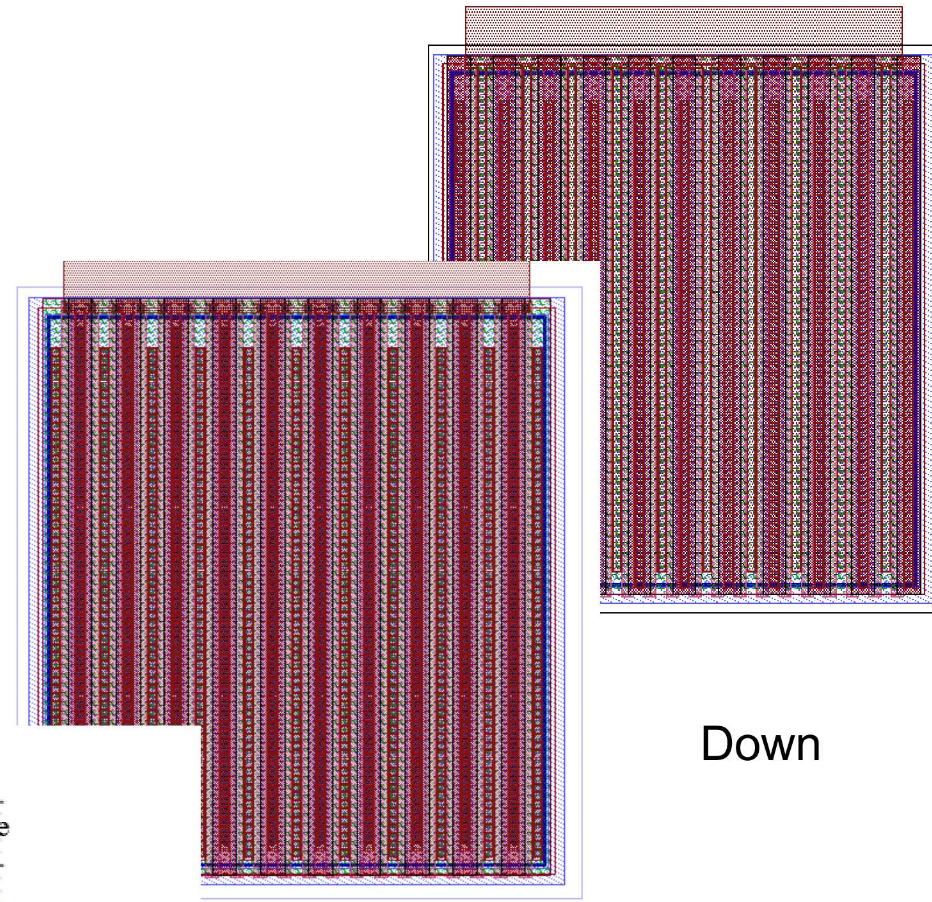
- In the forward direction, these diodes are expected to carry HBM currents in excess of 1A.  The device starts to conduct at approximately 0.8V, and has an effective resistance near 1Ω as the current rises to 1A with a voltage of 2V.



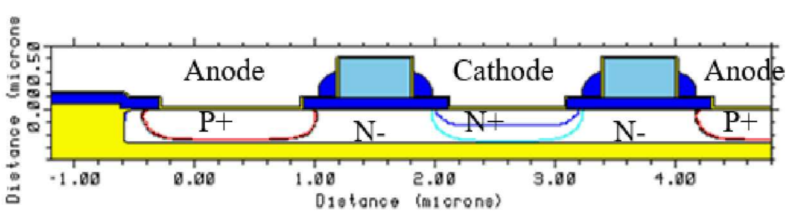
# Results DIODEs

- The dominant ESD Diodes are “poly-bound” structures with multiple fingers. Both UP and DOWN diodes are P+/N-/N+ devices, but they are laid out in different ways, to make it more convenient for connections.

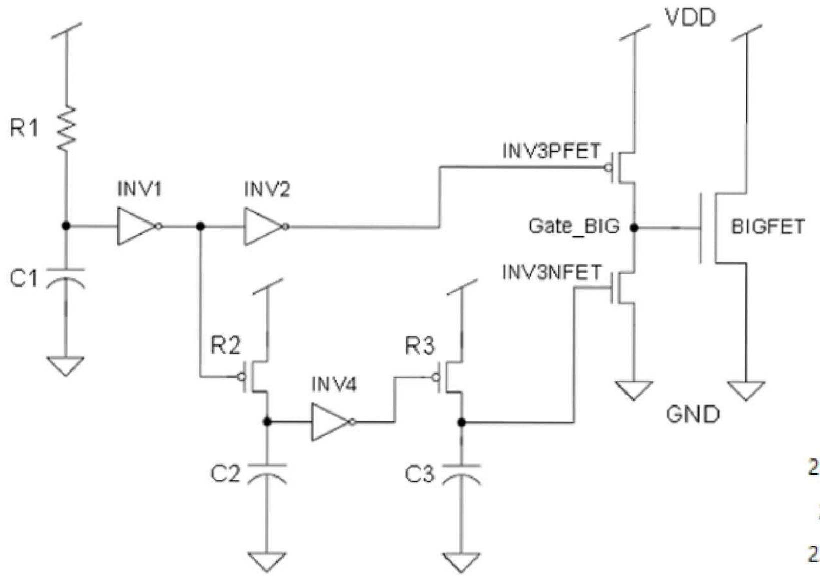
Up



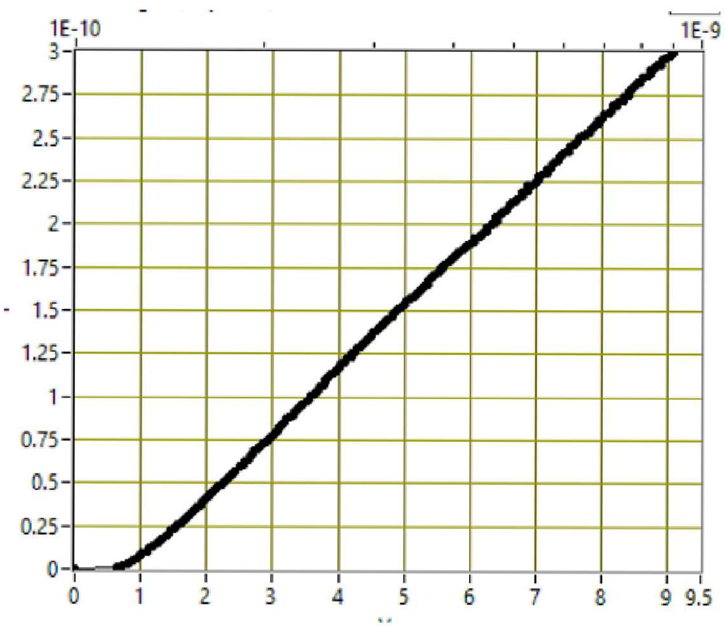
Down



# Results Power Supply Clamps

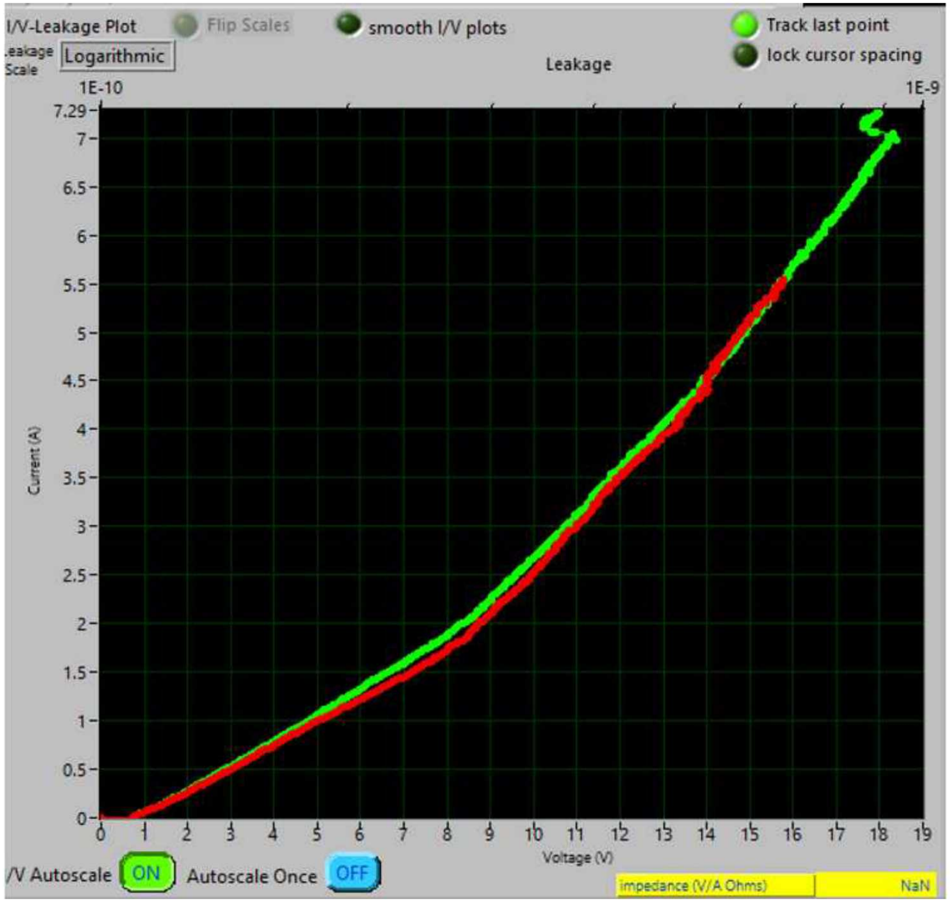



Device width 4000µm

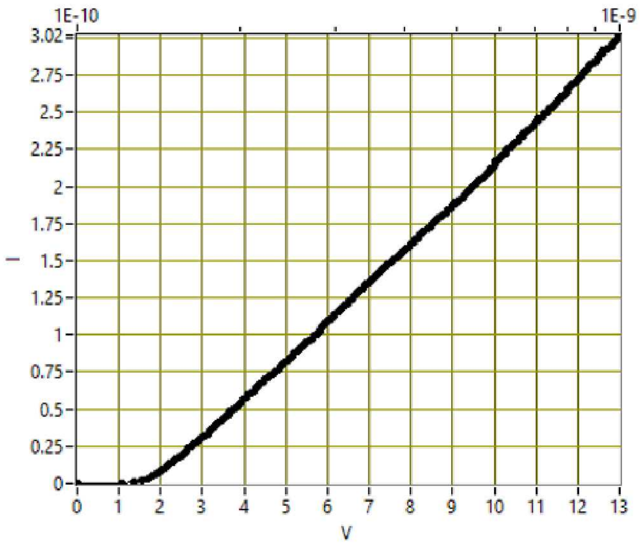


# Results Power Supply Clamps

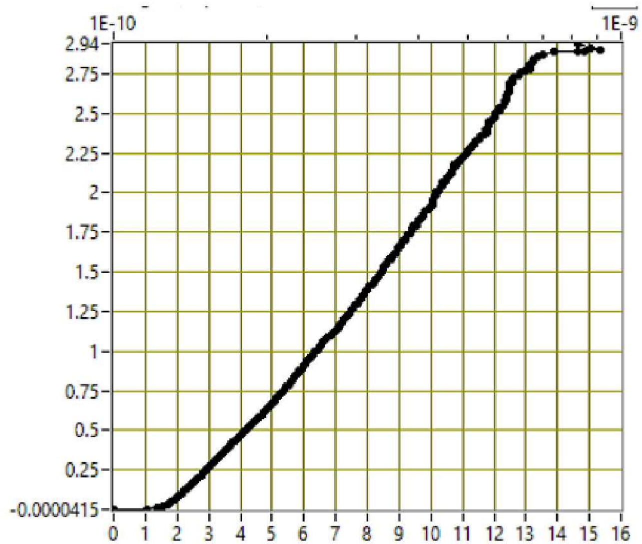
- Distributed Power Supply Clamps on 500 Pad product
- 8x500µm wide clamps comparing two locations on the wafer. Over stressed to failure.



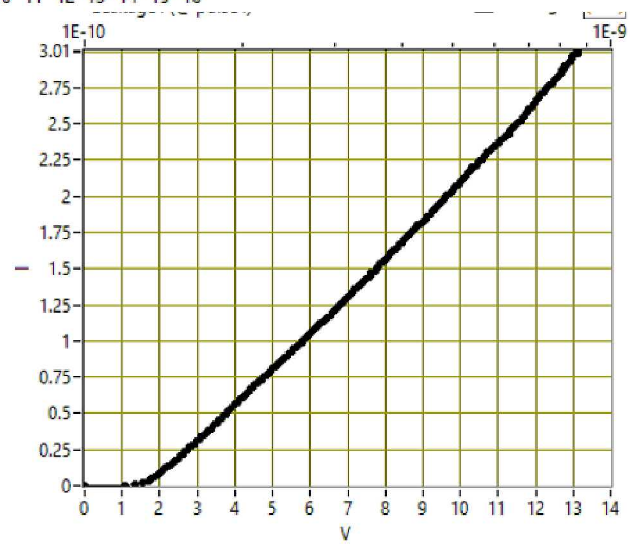
# Results INPUT




Input

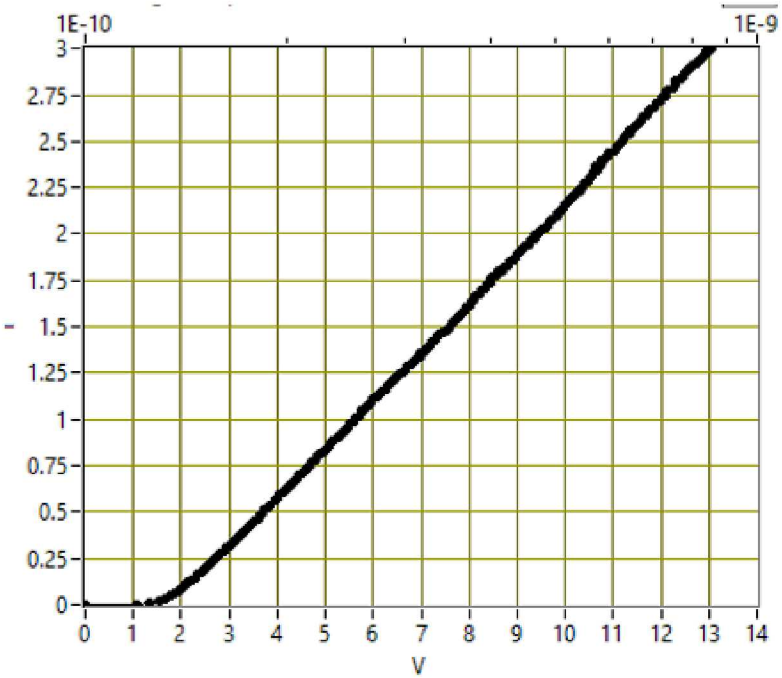



Input with Hysteresis

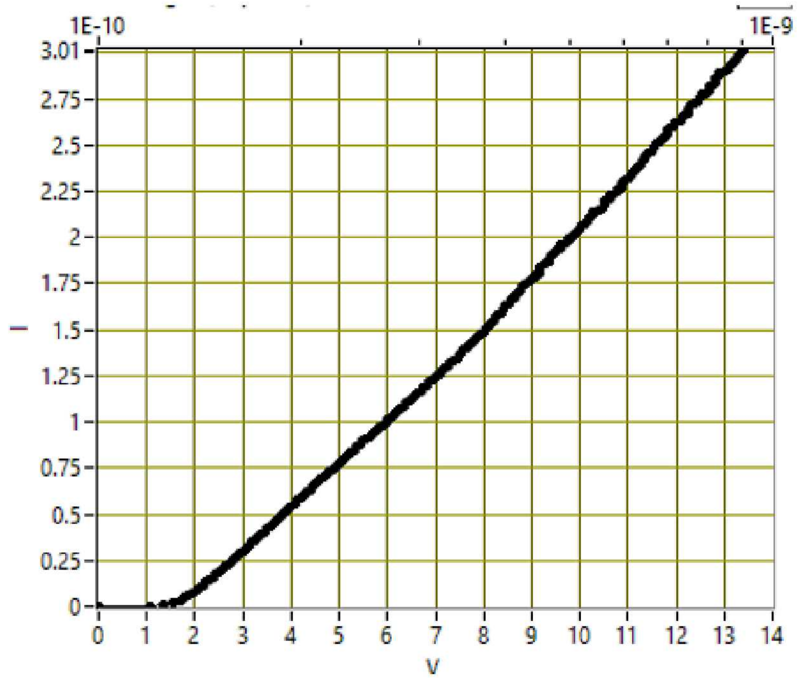



Input with Hysteresis and Bus Holder

# Results OUTPUT




4mA Fast Output




12mA Slow Output

# Conclusions

- Specifications have been developed that allow us to compare products under two types of ESD stress, HBM and CDM.
- These are not the only types of ESD stress, but they provide a good example of radically different stresses with different types of failures.
- The TLP is an effective tool for developing new processes and suggesting ways of improving our products.
- All products must be “ESD qualified”.
- Come and see me if you are doing something “different”, early in the product development.