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IIRW 2018 DISCUSSION GROUP: Product reliability for Low-Volume, High-Consequence Integrated-Circuits Fabrication

Discussion leader: Gaddi S. Haase, Sandia National Laboratories

Participants:

Mark	Andres	Tom	Kopley
Gennadi	Bersuker	Pat	Lenahan
Brad	Bittel	Daniel	Lichtenwalner
Pavel	Bolshakov	Deborah	Noble
Soong	Chang	Matt	Ring
Nate	Damon	Riddhi	Shah
Elias	Fantz	Roberta	Stradiotto
Matthew	Hogan	Ryan	Waskiewizz
Shu-Hab	Hsu	Chadwin	Yang
Tobias	Kemmer		

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Low-Volume, High-Consequence Integrated-Circuits

- Low-Volume high-consequence IC products may be installed in critical circuits of a life-support system, an aerospace application, or a self driving vehicle.

- The IC may be built in a specialized low-volume fab, or fabricated one wafer-lot at a time in a large foundry for a low-volume company.

Product Reliability Assurance consists of two main parts:

1. Screen out the defective, infant-mortality population.
2. Verify that the remaining parts meet a **specified reliability** (i.e. the fraction of parts that keeps functioning as specified, after a specified field life-time at specified operating conditions).

Product reliability part 1: Screen out the defective, infant-mortality population

1. 100% of all parts
2. Burn In: Stress the parts at a higher temperature, supply voltage, clock rate, etc. Test again to verify that all functions of the IC operate per specification.
3. Alternatively, add a stress period (usually elevated supply voltage) and repeat test. Is this a cost saving alternative?
4. The stress should remove defective parts effectively, but not weaken good parts.
   - How to determine that enough stress was applied?
   - How to avoid pre-mature aging of good parts? This is especially difficult for technology nodes of low dimensions (say under 32nm), where variations may result in loss of reliability.
5. What to test after application of stress:
   1. Verify that the IC still functions according to specifications, - or:
   2. Look at parameters (such as Iddq and Fmax) change after stress per part.

Product reliability part 2: Verify final product reliability

1. Life-Test: A destructive stress test, to be performed on a sample of parts only
   - Low-volume translates to small sample size. How to compensate for small sample size and still maintain statistical significance?
   - Are we only limited to the determination of the confidence level by which we can state that the product meets or exceeds the specified reliability?
   - If we assume that early failures are driven by defects + design/process marginalities, can we fit a time-to-fail distribution to observed failures in order to extract reliability forecasts? What distribution has a physics-based reasoning for fitting early failures?

2. Life-Test Stress:
   - Use stress levels that do NOT open new degradation mechanisms. Can we verify that?
   - How to chose stress that ages all the sub-circuits and components of the IC equally? Is it at all possible?
   - What is the total acceleration factor? It is required to evaluate the stress-time needed to meet one customer-defined life-time at use-conditions. Do we have to use the upper-most use conditions (voltage, temperature, etc.)?
   - If the IC is operated with an external clock, what's the effect of using a faster or slower clock rate?