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## **Radiation and Self Heating Effects in Hetero-Junction Bipolar Transistors: FY2019 L2 MileStone 6723 Report**

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## **Abstract**

Hetero-Junction Bipolar Transistors (HBT) have several advantages over Silicon Bipolar Junction Transistors (BJT) in radiation environments. One advantage is an intrinsic hardness to displacement damage causing radiation. The generally smaller size of HBTs compared to BJTs also means that less photocurrent is generated by these devices. A disadvantage of the smaller size is less ability to dissipate heat due to smaller surface areas and contacts. This report describes simulations intended to study the initial heating of HBT transistors due to ionizing radiation events and the subsequent heating caused by feedback in the devices when responding to these events.

# 1 Acknowledgments

The explorations in this document are done with software tools. Although the major TCAD software tool is commercial, the remaining tools are implementations of active research.

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## 2 Preface

This report describes the development and progress of two distinct simulation campaigns to investigate the interaction of radiation and self heating in compound semiconductor devices. The first of these efforts is focused at the fundamental device physics level and is conducted with the Technology Computer Aided Design (TCAD) tools in the Silvaco semiconductor simulation suite. Multiple tools are utilized which range from device creation (either with a process simulator like Athena or Victoryprocess and/or direct creation in the device simulators) to device simulation in tools like Atlas or Victorydevice.

The second of these efforts is a study to investigate issues of translating the physical effects established at the fundamental device level to compact device models that can be utilized in a circuit solver environment. Most of this effort is directed at assessing the viability of the approximations in the compact model implementations for use in evaluative studies of device survivability in radiation environments. In this work, no fundamental problems appear to stand in the way of performing radiation induced self heating simulations at the circuit solver level.

### 3 Summary

This work is focused on establishing the relationship between radiation exposure and thermal responses of compound semiconductor devices during operation. Achieving this understanding requires physics based study of compound devices and their associated packaging from an electrical and thermal standpoint. Although this understanding is rooted at the fundamental physics level of these devices and is of interest for academic objectives, there are practical and pressing reasons for pursuing this work in order to accomplish insertion of compound semiconductor devices into systems required to operate in radiation environments. While the details of these reasons are not included in this report to maintain an emphasis on general results, this work will nevertheless contribute to design and qualification activities in the near and far terms for systems with potential radiation exposure.

The approach taken is to use simulation as the core of the work and work towards reproducing key characteristics seen in experimental measurements as validation of the simulations. Of course, all of the information generated by simulation does not lend itself to experimental validation because some quantities are experimentally inaccessible. However, agreement between simulation and experiment over a limited subset will enhance confidence in the broader range of simulation results. TCAD calculations using commercial tools and Sandia National Laboratories' (SNL) Charon tool can produce results concerning macroscopic quantities of temperature and current that can be related in the simulations to microscopic quantities of charge carrier densities and internal device fields. The result are predictions of device behavior due to radiation coupling with self heating and insights as to internal device mechanisms that drive these predictive results. Examples of this coupling include semiconductor device calculations that include radiation (e-h pair generation in material) and self heating through joule heating of the lattice by charge carrier (e-h pairs) scattering.

High Fidelity TCAD calculations are suited for discoveries at the device level but consequences of a device interaction with radiation and its performance in a circuit are better addressed in simulations conducted with circuit solvers. In order to perform these studies, it is important to embed sufficient physics in the compact models to capture relevant mechanisms. In such a scenario, it then becomes possible to use the compact device models in isolation to explore ramifications of the embedded physics as a function of bias, temperature, radiation level, and other parameters. The compact model can thus supplement the TCAD studies with much faster runtimes and more possible variations of conditions.

A large determinant in self heating effects in semiconductor devices is the ability of the electronic packaging to absorb and conduct heat away from the semiconductor system. Commercial semiconductor device simulators are limited to treating package effects as approximations formulated as simple thermal circuits. COMSOL (*Computer Solution*) calculations on the other hand are true multi-physics simulations that that can simultaneously probe the conduction of heat through a finite element model of a chip in the package as well as perform simple TCAD simulations of semiconductor device behavior as a function of bias. Ultimately, the calculations covered in this work will be ported to a COMSOL simulation and environment. Such a calculation is presented in [29].

## 4 Nomenclature

AIMSPICE Automatic Integrated Circuit Modeling SPICE

A Amperes - fundamental unit measure of current

BC Base-Collector

BE Base-Emitter

BEOL Back End of the Line

BJT Bipolar Junction Transistor

Charon Sandia National Laboratory developed TCAD code

COMSOL Computer Solution multi-physics software package

DOE Department of Energy

Dose Rate Ionizing radiation at high rate generating electron hole pairs in significant densities

DRCCS Dose Rate Controlled Current Source

ECAD Electronic Computer Aided Design

FEOL Front End of the Line

FET Field Effect Transistor

FWHM Full Width Half Max - measure of pulse duration in time, usually a Gaussian pulse

GaAs Gallium Arsenide

GHz Giga Hertz frequency range

Gummel Curve I-V of a transistor where collector and base currents are plotted against  $V_{BE}$

HBT Hetero Junction Bipolar Transistor

HEXFET Hexagonal Field Effect Transistor - refers to the layout of the transistor

I-V current voltage usually referring to a device characteristic

III-V Refers to compound semiconductors consisting of elements from third and fifth groups in periodic table

$I_C$  collector current

$I_B$  base current

$I_E$  emitter current

Mesh, Meshpoints grid of nodes where TCAD calculations are conducted

MOSFET Metal Oxide Semiconductor Field Effect Transistor

mA milli-Amp, 1 A = 1000 mA

mV milli-Volt, 1 V = 1000 mV

NPN Bipolar transistor consisting of N-type emitter, P-type base, N-type collector

PN P-type N-type semiconductor junction

Self Heating Refers to heating of a device caused by the operation of the device due to the currents in the device

SOA Safe Operating Area - bias levels and radiation levels below thresholds of damage to semiconductor devices

SNL Sandia National Laboratories

2D Two Dimensions

3D Three Dimensions

TCAD Technology Computer Aided Design

Thermal Runaway condition of semiconductor device with thermal energy positive feedback

TF Tor Fjeldly model

V Volts - fundamental unit measure of potential

$V_{BE}$  forward voltage applied between emitter and base

$V_{BC}$  reverse (in forward active operation) voltage applied between collector and base

$V_{CE}$  voltage between emitter and collector

VBIC Vertical Bipolar Inter-Company Model

Xyce Sandia National Laboratory developed circuit simulator tool



## 5 Introduction to Thermal and Radiation Effects In Hetero Junction Bipolar Transistors

Radiation Effects in semiconductor transistors depend on the type (particle or wave) and spectrum of radiation and the make-up of the transistor. In recent years, III-V transistors have generated interest due to their small size and intrinsic hardness to particle radiation induced displacement damage. The small size of these devices stems partially from fabrication techniques and these same techniques also reduce the effects of displacement damage from radiation. Additionally, the magnitudes of generated photocurrent from ionizing radiation are reduced by the small vertical dimensions of these transistors. Other advantages of the smaller size are reduced power requirements and higher switching speeds. However, associated with these advantages is the disadvantage of reduced heat transmission and dissipation capabilities. In some cases, these disadvantages lead to significant impacts on these devices and correspondingly fuels demand for further study on this topic.

### 5.1 Existing Work and References

Studies of heating and thermal runaway in semiconductor devices have a rich and deep history with a corresponding broad span of topics. The work can be predominantly divided into the categories of experimental exploration and mathematical modeling. This later category can be further sectioned into analytic descriptions and TCAD or Electronic Computed Aided Design (ECAD) modeling of the phenomena. The following list of references includes instances of these three categories.

Initially, the uncertainties surrounding the specifics of secondary breakdown in BJTs were large and early work centered on the establishing the role of dissipated energy [1] and thermal properties of the transistors. This work included experimentally examining the breakdown as a function of thermal conductivities and as a function of the resistances attached to the device [4]. Mathematical models were developed describing self heating effects leading to descriptions of turning points in  $I_C$  versus  $V_{CE}$  curves that are related to thermal runaway in transistors [6]. These ideas coalesced by 1977 into the concept of safe operating areas (SOA) in an IV plane for device operation and geometric constraints on device sizes and

layouts [7]. The mathematical descriptions of turning point behavior continued to evolve with multiple solutions of a relation used to describe transistor operation [8]. As more attention was applied to thermal responses of structured devices, important differences emerged between single and multiple finger BJTs and HBTs. An example of these differences include the collapse of current gain due to thermal instabilities in single finger HBTs [13]. Several different additional phenomena also contribute to different responses between single and multiple fingered devices. As another example, temperature gradients in multiple finger HBT devices have been found to lead to corresponding nonuniform current distributions and the resulting feedback effects result in hot spots in emitter fingers [14].

By the 2000s enough progress had been realized so that comprehensive overviews of the mathematical modeling with a resulting overlying theory could be summarized [20]. This has allowed further mathematical explorations into the interactions between the transistors and the surrounding resistances [21] including studying the ramifications of the Kirk effect. Follow-on work included a more detailed examination at the SOA boundary and particular instabilities resulting from transitioning between different thermal runaway mechanisms [24]. Finally, more recent work in normal environments leads to predictive capabilities that detail the SOA boundaries with respect to device sizes. This work is comprised of measurements, analytically modeling of the electrical behavior, and separate thermal modeling of the transistor structure and includes all mechanisms such as avalanche, avalanche interactions with the Kirk effect, current collapse, and thermal breakdowns [22].

These references are only a small sample of the available literature on these topics. In summary, the self heating and thermal breakdown field in normal environments has well established topic areas and clear directions for additional study.

In contrast, relating heating and thermal runaway to radiation effects is a relatively narrower field of study with less predecessor work. The early work in this field is concentrated on experimental studies of circuits in dose rate radiation that use power MOSFET devices. It is easy to understand this focus as power MOSFET devices are designed to switch and carry high currents and this potentially introduces vulnerabilities from high current self heating. Additional current from dose rate events will exacerbate this vulnerability. Correspondingly, an early reference is concerned with measurement of the response of a power supply using HEXFET power MOSFETs. [9]. Follow-on work investigated the device as a stand alone component so the radiation induced runaway of single MOSFETs was characterized. [11]. The present work is concerned with new applications



of III-V HBTs and started with time dependent simulation studies [28]. Associated TCAD level work is concerned with establishing fundamental thermal related mechanisms affecting performance in these devices. [30].

This last work bears comparison to previous high fidelity simulations that have provided detailed examination of device behavior at the SOA boundary [25]. Specifically, this work has compared the impact ionization consequences at high currents and low fields in the presence of the Kirk effect with the self heating present at high voltages and lower currents. These TCAD results show distinct differences in the electrical behavior of the device in these scenarios, based on analysis of the simulation results. These efforts provide the foundation for ongoing studies (including this report) of these effects with the additional element of time included.

This field is less studied because of the narrower interest in radiation effects and the time dependent characteristic of radiation events. As will be seen, responses to radiation in devices of interest often exhibit a delayed response and the radiation event itself may not occur instantaneously. The subsequent heating of a device that does not experience immediate thermal runaway also can have a relatively long time constant and this last factor makes this a particularly difficult field of study that requires additional attention.

## **5.2 The Present Work**

In keeping with the needs mentioned in the summary. this report studies the relationship between ionizing radiation exposures in III-V transistors and related heating effects through simulation and experiment. The simulations and results are described here and the experiments will be reported in a later report. The simulations utilize Technology Computer Aided Design (TCAD) methodologies and are extended with compact models based on analytic expressions of the relevant physics. The primary thrust of the study is to develop simulations of HBT transistors that reflect thermal generation and dissipation effects suggested by characterization data. With suitable models and calibrations, the impacts of these devices on circuits and systems through thermal runaway can be studied.

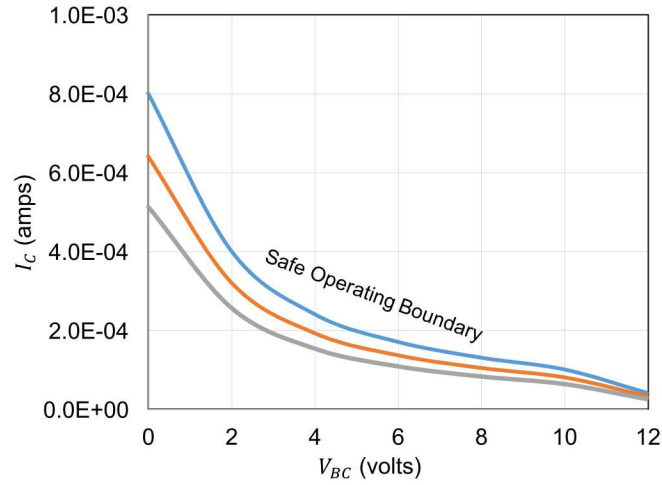
The investigation begins with analysis of thermal behaviors in normal environments (no radiation, room temperature). In the simulations, under normal environment conditions, the transistors can be operated so that thermal runaway is

duplicated for any particular  $V_{BC}$  value at large overdrive levels. Curves of the thermal runaway current versus base emitter voltage have been established and form the basis of calibrating the models. Such a simulation campaign aids in the understanding of the elements that contribute to thermal runaway. The understanding of the fundamental precursors to thermal runaway allows for determining suitability of particular devices for radiation environments as well as useful design information. With insight, devices can be modified at the technology level, the geometry level, and the interaction with packaging level to change device capabilities with regards to heating.

This thermal analysis is complemented with the addition of ionizing radiation in the simulations. The introduction of charge carriers from the radiation and the ensuing increase in device currents increase the rate of Joule heating during device operation. This additional heating challenges the ability of the device and package to dissipate heat leading to radiation augmented or induced thermal runaway. The combination of simulated thermal runaways with the radiation responses of the devices leads to the definition of operational boundaries of these devices under a range of environments and operating conditions. It is expected that doserates above critical levels will shift these boundaries so that thermal runaways occur at lower values of device bias or temperature. Therefore, the simulations enable the construction of a series of curves such as shown in Figure 1. These curves are a notional representation of operational boundaries in the I-V space where I refers to collector current and V refers to  $V_{BC}$  or  $V_{CE}$ . The uppermost curve is based upon simulation results from simulations that yield transistors experiencing thermal runaway in normal (no radiation) environments.

For the devices under study, the I-V plane is divided into the region above the curve and the region below the curve. All simulations with conditions that correspond to the region above the curve will experience thermal runaway and simulations with conditions that correspond to below the curve will not experience thermal runaway. The lower curves are translated versions of the upper curve and indicate that with the addition of radiation or high temperatures, thermal runaway will occur at lower current magnitudes.

The TCAD simulations detailed in this report are therefore used to define points of thermal runaway on the lower two curves in Figure 1. Further simulations add to these runaway data points and fill in the remainder of the curves in Figure 1 to have greater calculation based confidence in the operational range of these devices.



**Figure 1.** I-V curves that define boundaries of thermal runaway in the NPN transistor simulations. The uppermost curve is the curve under normal environment conditions. Lower curves reflect the addition of some environmental stress that causes the device to thermally runaway at lower operating current values.

It should be stressed that the present efforts are not directed towards an accurate quantification of the conditions and boundaries of thermal runaway, rather an understanding and the ability to predict the general behavior of devices. The intent is to investigate the performance of devices at these boundaries and to verify and initially validate the modeling results with independent data. An initial goal is to develop a consistent understanding of the interaction between radiation and self heating, and thus suitability of devices for radiation missions can be assessed.

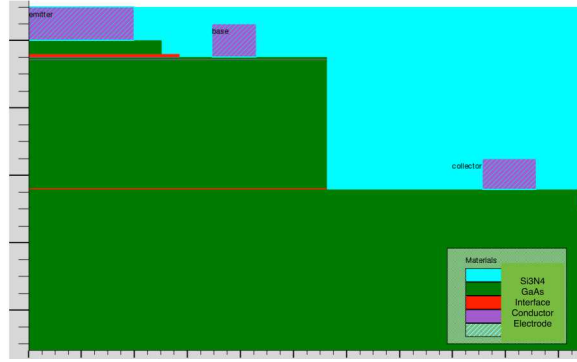
## 6 HBT TCAD Calculations including Self Heating and Photocurrent

### 6.1 Setup of the TCAD Calculations

The high fidelity device simulations are implemented in the device simulators Atlas or Victory Device [31] by Silvaco. The simulation is a two dimension (2D) replication of a cross section of a single emitter III-V HBT. The device can be configured as a single emitter 'finger' or as multiple emitter 'fingers' in parallel. The cross section is intended to stand in for a larger device that is extended into the third dimension. In addition, the device is partially represented as a half slice in the simulation and the modeled device reflected around the  $x=0$  axis is the complete representation of the actual device. For this analysis, two dimensions are considered sufficient but temperature related current constriction in III-V devices is a concern so that follow-on simulation work may move to three dimensions (3D). [14]

Because this is a III-V heterojunction transistor, there are bandgap discontinuities at the interfaces between the regions of the device. The resulting potential wells or barriers require fine meshes to resolve the charge carrier behavior in the vicinity of the junctions. In addition to this fine mesh requirement, thermal boundary conditions are required in order to calculate thermal effects of normal operation or radiation exposure. These boundary conditions are most naturally applied to the contacts. Figure 2 is example of the transistor simulation structure with the contacts delineated. In this figure, one half of a single emitter is shown in 2D cross section.

With the thermal contacts specified, simple thermal analysis can be performed via simulation under operational conditions. The maximum temperature of the transistor can be specified as the temperature in the hottest region where the operational currents drive the temperature rise. These regions heat faster than other regions because the calculations determine that heat is added to the regions faster than it can be removed by conduction through the transistor to the contacts which are held at a defined temperature. The calculations rely on archived thermal property values that are default values for the code and these values determine the conductivity of the structure. Unfortunately, this transistor representation is only a small section of an actual transistor and therefore additional thermal elements



**Figure 2.** Two dimensional representation of HBT device with emitter, base, and collector terminals shown. This device, used in the TCAD calculations is an NPN transistor.

are required in the calculation to duplicate the thermal effects of the remainder of the transistor structure that cannot be included in this calculation. The reason for the exclusion is the limit on the number of mesh points that the calculation and/or machinery is capable of supporting.

The most simple additional thermal elements in this system are added thermal resistances [15] between the contacts and the rest of the structure to duplicate the flow of heat in a realistic transistor structure and its surroundings. This approach is known as a lumped thermal model and the addition of these elements should allow the thermal calculations to duplicate the performance of a transistor using this model. Of course these elements require a calibration effort in order to produce a calculation with usable accuracy.

## 6.2 Joule Heating and the Lattice Heat Flow Formulation

Most TCAD calculations solve the drift - diffusion equations of the charge carriers and Poissons equation for self consistency. Because these are the common underpinings of TCAD calculations, this formalism is not covered in this report. This problem, however, adds the importance of heat which means that some mathematical formulation is necessary for computing and tracking heat in the device. The tracking is enabled with the addition of a heat flow equation 1 [31]. This equation is solved at every node in the computational lattice along with the Poisson, continuity, and transport equations. Unfortunately, the computational burden with

the addition of this equation is large and slows the calculation considerably.

$$C \frac{\delta T_L}{\delta t} = \nabla \cdot (\kappa \nabla T_L) + H \quad (1)$$

where

- $C$  is the heat capacity per unit volume
- $\kappa$  is the thermal conductivity
- $H$  is the heat generation rate, and
- $T_L$  is the local lattice temperature

Both  $H$  (as will be shown) and  $T_L$  are position dependent quantities.

Heat generation can consists of multiple effects but of most interest in this problem is the Joule heating effect resulting from the the pulse of dose rate induced induced carriers flowing through the device. The Joule heating can be expressed as:

$$H = \left( \frac{J_n \cdot J_n}{qn\mu_n} + \frac{J_p \cdot J_p}{qp\mu_p} \right) \quad (2)$$

where

- $J_n$  is the electron current density
- $J_p$  is the hole current density
- $q$  is the fundamental charge
- $n$  is the electron density at a given position
- $p$  is the hole density at a given position
- $\mu_n$  is the electron mobility, and
- $\mu_p$  is the hole mobility

The relationship is a statement of Joule's law or a reformulation of

$$P = I^2 R \quad (3)$$

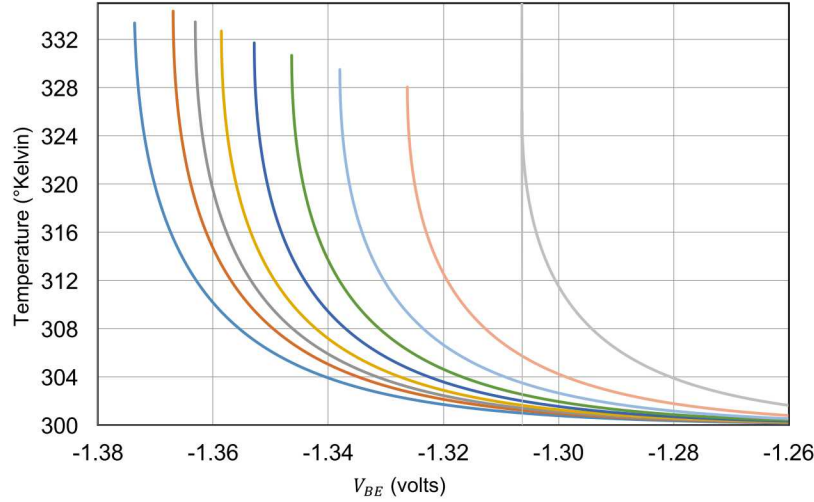


Obviously, the current densities and the carrier densities are local which means that the expression is position dependent. Again, equation 1 is solved at every position node in the calculation.

### 6.3 Thermal Run Away Calibration

The calibration process is initiated by utilizing simulations of Gummel curves for the modeled transistor. During the generation of a Gummel curve, the base and collector currents  $I_B, I_C$  are monitored as the driving base-emitter voltage  $V_{BE}$  is ramped. The base-collector voltage  $V_{BC}$  is held at a fixed voltage. At low  $V_{BC}$  voltages, the simulations can be driven to high  $V_{BE}$  voltages and the device experiences an approximate exponential increase in current with the characteristics of a single exponential function. As  $V_{BC}$  is increased, the device can be driven up to threshold  $V_{BE}$  voltages beyond which, the device begins to experience a runaway super-exponential current increase due to thermal effects. This is the self-heating of the transistor. At higher  $V_{BC}$  voltages, these threshold voltages in  $V_{BE}$  occur at lower values. In other words, the transistor thermally runs away as a function of  $V_{BE}$  and this runaway point can be lowered by raising  $V_{BC}$ . Setting aside for the moment a discussion of the physics of this runaway, the simulation of these threshold voltages can also be affected by the thermal model chosen for the transistor.

As an example, the thermal resistances connecting the thermal contacts to the body of the semiconductor device can be varied to affect the runaway threshold voltage value. The larger the thermal resistance, the less heat is transferred to the contacts and the device is more prone to self-heating effects. Figure 3 is a representation of several studies where  $V_{BE}$  is ramped to a thermal runaway point for different values of the thermal resistances. In all of these studies,  $V_{BC}$  is held at 4 volts. On this plot the emitter voltage is ramped negatively so the base-emitter junction of the NPN is forward biased and this is expressed as a negative  $V_{BE}$ . The plot shows the increase in temperature of the device as  $V_{BE}$  is ramped to higher magnitude negative values. Along each curve, the temperature of the device increases up to a point where the curve turns vertical and the calculation fails. This means that the next temperature step associated with the subsequent voltage step is too large for the calculation tolerance. The curves are arranged so that the leftmost curve with the largest negative values of  $V_{BE}$  is the lowest thermal resistance curve



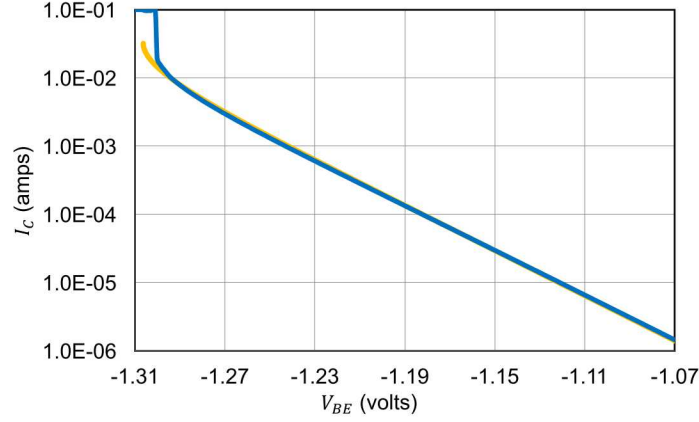
**Figure 3.** Temperature versus  $V_{BE}$  curves for TCAD simulations of the transistor structure. Each curve uses a different value of the thermal resistance in the calculation with the thermal resistance increasing in the curves left to right. The rightmost curve represents a thermal runaway at lower values of  $V_{BE}$ .

and the rightmost curve has the highest thermal resistance. The thermal resistance is thusly varied in the simulations to match the type of data found in Figure 4.

Figure 4 shows collector current data of measured Gummel curves for a base-collector voltage  $V_{BC}$  of 4 volts. Also shown is a simulated curve of collector current which approximately matches the measured collector current values. It is easier in the simulations to match the collector currents in contrast to the base currents because the base currents require close approximations for the defect species in the transistor in order to match the measurements.

For the purposes of this study, the important feature in the curves is the thermal runaway displayed at the highest  $V_{BE}$  values. This runaway occurs in both the base and collector current curves. The match between the simulated collector current curve and the measured curve is not exact but it is calibrated to occur at the approximate same value of  $V_{BE}$ . The discrepancy in shape is the result of the heat dissipation in the model not replicating all of the breakdown characteristics of the actual device. However, the most important parameter for this study is magnitude of the runaway threshold  $V_{BE}$ . The matching of the simulation in this plot and the measured data therefore determines the value of the thermal resistances to be used in subsequent calculations.





**Figure 4.** Measured (blue) and simulated (orange) collector current curves for the actual transistor and the corresponding simulation model. The thermal runaway at high  $V_{BE}$  in both the measured and simulated curves is used to calibrate the values of thermal resistances in the high fidelity TCAD simulations.

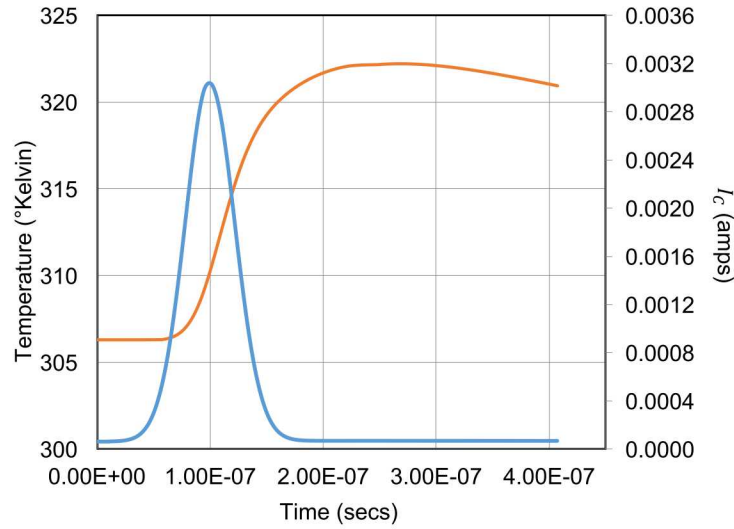
## 6.4 Defining Behaviors in Short Time Calculations

With the calibration effort described in the previous section, it is believed that an electrical and thermal model of the transistor incorporates sufficient fidelity so that it can be used for studies of the transistor under various environmental conditions and that the qualitative response of the transistor can be predicted via simulation. The condition of interest for this study is simulating the effects of relevant magnitude pulses of ionizing radiation, typically at an ambient temperature of 300 degrees Kelvin. These pulses are simulated in TCAD calculations by adding a specified density of electron-hole pairs as a function of time that is commensurate with the time dependence of measured pulses. Although the measured pulse is not a simple analytic function of time, a pulse that is Gaussian in time can elicit useful response information for this study and the present work has examined pulses that range in full width at half max (FWHM) from 6 to 60 nanoseconds. The longer pulse widths comprise the bulk of the studies because they naturally produce greater heating and the bulk of measured pulses are long ( $>40$  nanoseconds).

The method of the thermal runaway simulations proceeds as follows. The simulations start by incrementally advancing  $V_{BE}$  voltage, thus delineating a Gummel curve from negative values of  $V_{BE}$  up to the desired  $V_{BE}$  voltage at which a Gaus-

sian ionizing radiation event will be applied to the device. The desired voltage level is one where the device might operate in forward active mode at a fairly high current so that the device is potentially susceptible to heating effects. This ramp in voltage is necessary because the calculations incorporate self-heating effects in the form of solving for the lattice temperature as a function of history and current. Consequently, because of the inclusion of lattice heating, the calculations are less stable and require this systematic (and small) stepping in voltage to achieve the target  $V_{BE}$ . Once the target voltage is reached, the device is powered in this manner for a transient time dependent calculation and a radiation pulse is applied as a function of time. Figure 5 represents time dependent simulation results of both the applied radiation pulse as represented by the collector current (blue) and the temperature response (red) of the transistor. Note that the time scale here is on the order of the radiation pulse (100s of nanoseconds) and is a fraction of the more complete simulations presented later in this report.

In the figure, the time dependent shape of the radiation pulse is followed by



**Figure 5.** Plot showing the generated photocurrent (simulated) from an ionizing radiation pulse and the increase in the lattice temperature of the transistor that results from the ionizing radiation event. Left vertical axis shows temperature and right vertical axis shows photocurrent measured at the collector terminal.

the collector current since a component of the collector current is the generated charge in the device. The displayed current is the sum of the operating current of the transistor and the generated photocurrent from the radiation. The generated

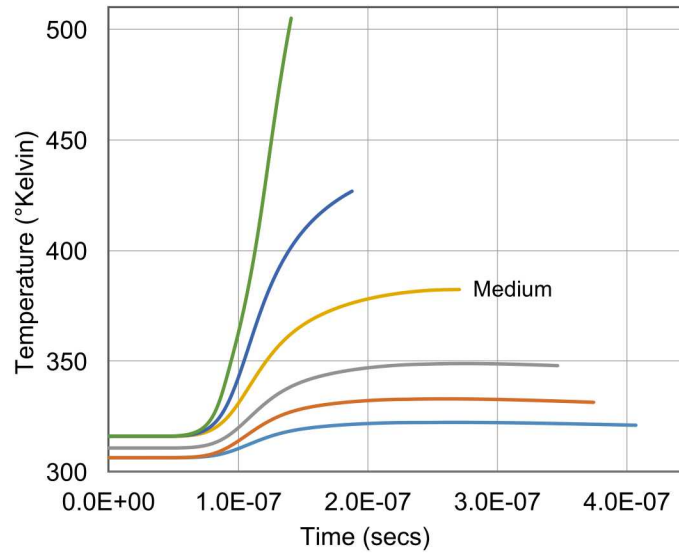
photocurrent contributes the Gaussian characteristic and begins at approximately 10 nanoseconds and lasts until approximately 200 nanoseconds. Preceding, during and after this period, the device is passing the normal operating current for the applied bias conditions. As the transistor experiences the radiation pulse and the ensuing charge carrier pulse, its lattice temperature increases due to an increase in scattering. This also leads to an increase of the normal operating current of the devices which is a function of temperature. Therefore, this operating current is not constant and displays a ramp like characteristic after the pulse.

The figure shows a relatively modest rise in temperature of about  $16^{\circ}\text{K}$ . It also shows that after the peak rise in temperature, the transistor begins to cool. The thermal time constant for the rise in temperature is on the order of 80 nanoseconds for these relatively low radiation levels. Simulations show that the thermal time constant varies as a function of dose rate and at higher dose rates, the heating takes longer to peak before cooling. At highest dose rates where the device proceeds directly to thermal runaway, the runaway occurs earlier in time than these temperature peaks. These results are discussed and illustrated in the next two sections of this report.

It is expected that the cooling shown in the figure will eventually return the device to the ambient temperature and that the photocurrent induced rise in temperature is transitory. The rise in temperature is due to the energy deposited in the semiconductor from the radiation and the self heating caused by the increased current from the initial rise in temperature. This figure shows a system that is heated in this manner and responds by achieving a maximum temperature and then slowly begins to cool. At higher dose rates, the elevated current level may reach a magnitude such that the transistor can not cool and thermal runaway occurs in a similar fashion as the runaways experienced in the Gummel curves with high  $V_{BC}$ s.

Figure 6 shows the temperature responses of a series of simulations conducted with different  $V_{BC}$  values and different applied dose rates. The resulting curves show a variety of responses which range from early time thermal runaway to late time cooling of the device. Because of the different  $V_{BC}$  values, the simulations are ramped (via  $V_{BE}$ ) to several different values of collector current prior to the steady state bias conditions held throughout the radiation pulse. The different collector current levels are seen in the spread of the curves at early times such as  $0.5 \times 10^{-7}$  seconds. These collector current curves also indicate that the simulations are starting at several different starting temperatures which reflect the different  $V_{BE}$  conditions.

All of these simulations are performed with a 60 nanosecond FWHM Gaus-

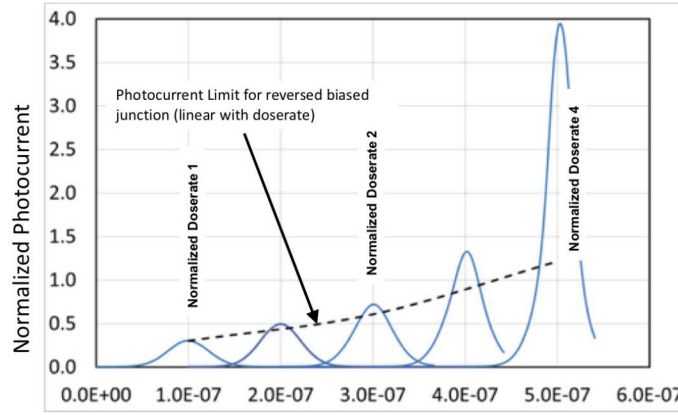


**Figure 6.** Transient simulated temperatures of HBTs exposed to Gaussian ionizing radiation pulses. Lowest curve represent low  $V_{BC}$  and low doserate conditions and higher curves represent higher  $V_{BC}$  and higher doserate conditions.

sian pulse centered at 100 nanoseconds. Therefore the rise in temperature occurs at the same time for all of the pulses but the magnitude differs between pulses. The amount of temperature rise increases as the pulse magnitude increases but at a faster than linear rate. This is due to the devices operating in a forward active mode so the generated photocurrents from the pulses are amplified by the transistor action of the devices. This is a demonstration of the 'secondary photocurrent' that transistors experience in operational modes [3]. Fig. 7 illustrates this nonlinear increase of photocurrent with a notional plot of nonlinear photocurrent as a function of dose rate for the HBT device. It is important to make this distinction for forward active transistors from operating configurations (emitter and base electrically tied together) where photocurrent increases linearly with doserate. This nonlinearity is one of the significant contributors to thermal runaway and as such is a factor in the simulations detailed in this report.

Considering Fig 6 again, the curve labeled Medium shows a temperature rise of approximately 60 °K. This transistor prior to the pulse operates at a current below a threshold current level that would lead to runaway conditions. This curve is notable because after the pulse, the sustaining operating current through the device may at long times operate at the threshold current level which produces thermal





**Figure 7.** Generated photocurrent is added to the operation of the transistor and is amplified via transistor action. The total photocurrent increases super linearly with doserate and thus adds to the joule heating caused by the current.

runaway in normal environment conditions. The implication is that for transistors subject to higher  $V_{BC}$ ,  $V_{BE}$ , and doserate values than this curve should experience thermal runaway. Transistors operating at less than the threshold values for  $V_{BC}$ ,  $V_{BE}$ , and doserate should experience a finite temperature increase followed by a normal cooling. Therefore, the operating and environmental conditions for this scenario represent a threshold case where the device is operating at a borderline static condition. It is one of the goals of this report to identify this boundary curve and if possible to quantify it accurately for this device.

## 6.5 Multiple Time Scale Thermal Runaway Calculations

In the course of conducting the thermal runaway simulations, scenarios leading to early time runaway were studied as well as late time runaway scenarios. Several aspects of the simulation were examined in detail to better understand the physics implications of the time dependent behavior and the time to failures (both numerical failure and the associated implied device failure) for the calculations.

The scenarios shown in Figs 5 and 6 are early time calculations of temperature changes in the HBT device due to irradiation effects. A systematic survey of radiation levels,  $V_{BC}$ , and  $V_{BE}$  values shows that distinct behaviors are realized at multiple time scales ranging from early time (on the order of the radiation pulse)

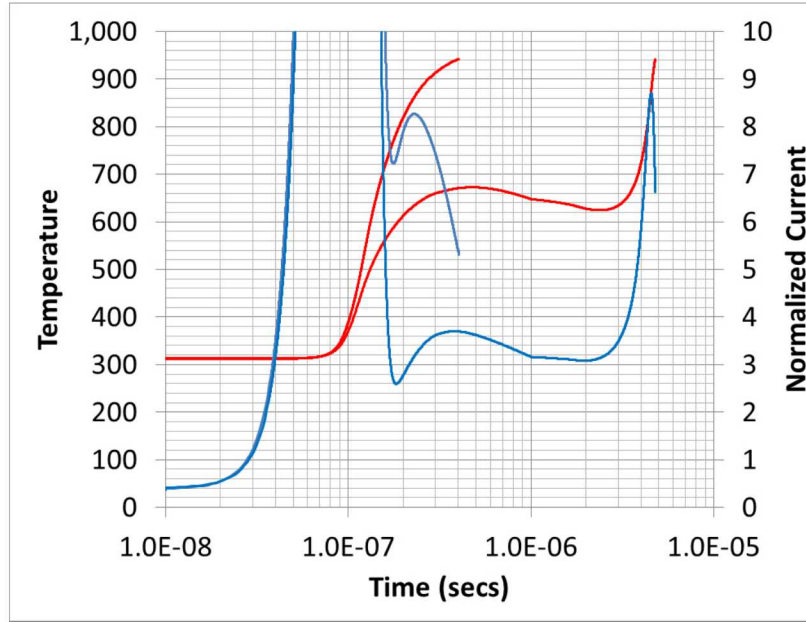
to later time (up to 2 orders of magnitude longer than the radiation pulse).

### 6.5.1 Transistor Failure at High Temperatures

Figure 8 illustrates the types of different time scale behaviors with two distinctly different scenarios. In the figure, the two scenarios are presented where the red curves represent the temperatures and the blue curves represent the collector currents as a function of time. Centered roughly at  $1.0 \times 10^{-7}$  seconds is the 60 nanosecond radiation pulse which is reflected in the behavior of the collector current in both scenarios. In both cases the current pulse due to the photocurrent is off the scale of the plot and reaches a peak at approximately  $1.0 \times 10^{-7}$  seconds and is mostly decayed by  $2.0 \times 10^{-7}$  seconds.

In the case corresponding to the higher radiation level and the higher collector current pulse, the device temperature begins rising during the pulse and continues increasing after the pulse. Although the rate of increase begins to drop in this case, the temperatures rise to a point above 800 degrees Kelvin where the intrinsic carrier density  $n_i$  begins to match the doping levels in the transistor. Under these circumstances, the device is no longer able to function as a transistor and current amplification begins to decrease. The collector current which decays after the radiation pulse, increases again by  $2.0 \times 10^{-7}$  seconds driven by the corresponding rise in device temperature. However as the temperature passes 800 degrees Kelvin, the collector current plateaus and then begins to fall. As the calculation surpasses the 900 degree Kelvin point the calculation becomes unstable and fails.

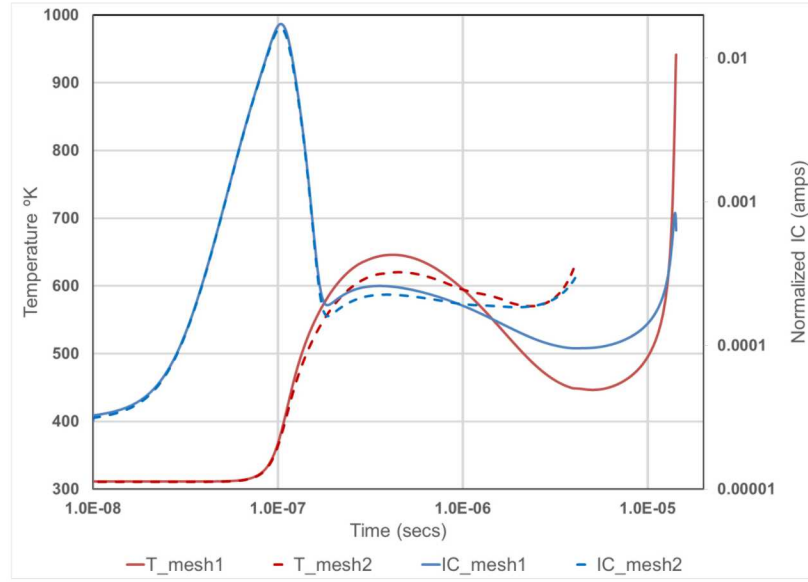
The lower radiation case does not show this direct to thermal runaway behavior initiated during the radiation pulse. The temperature starts to rise during the pulse and the collector current decays to its post pulse low after the pulse at approximately  $2.0 \times 10^{-7}$  seconds. From this point, the collector current rises to a peak and then begins to fall. Shortly thereafter, the temperature of the device peaks and also then begins to fall. This behavior on a longer time scale would probably lead to the device eventually cooling from the radiation pulse to ambient (defined by operating conditions  $V_{BE}$  and  $V_{BC}$ ) temperatures. However, this cooling acts only on a very short time scale and most importantly, the collector current does not drop below a threshold level that leads to eventual cooling. Instead, it remains above a threshold and continues to add heat to the device through joule heating. This is seen after  $2.0 \times 10^{-6}$  seconds where the collector current starts



**Figure 8.** TCAD simulations showing temperature (red) and current (blue) versus time for two simulation cases. The earlier runaway case (simulation stops at  $4.0 \times 10^{-7}$  seconds) has more challenging  $V_{BE}$  and radiation levels compared to the later runaway case. (simulation stops at  $5.0 \times 10^{-6}$  seconds).

rising again and is followed by the temperature which leads to more collector current which raises the device temperature and ultimately leads to thermal runaway at approximately  $5.0 \times 10^{-6}$  seconds. It is interesting to note that in the course of approaching thermal runaway, the same behavior of the current peaking and falling and the temperature rising in a monotonic fashion to greater than 900 degrees Kelvin occurs similar to the higher radiation scenario.

These two situations represent a calculation becoming unstable (equivalent to thermal runaway) at 400ns in one case and 5  $\mu$ seconds in the other case, a difference consisting of a factor of ten. The defining characteristic in both cases is the persistence of the collector current above the critical level to prevent cooling and thus leading to runaway in both situations.



**Figure 9.** TCAD simulations showing temperature (red) and collector current (blue) versus time for two simulation meshes. The solid lines represent a more refined mesh and the dotted lines represent a coarser mesh.

### 6.5.2 Effects of Mesh Density on the Calculations

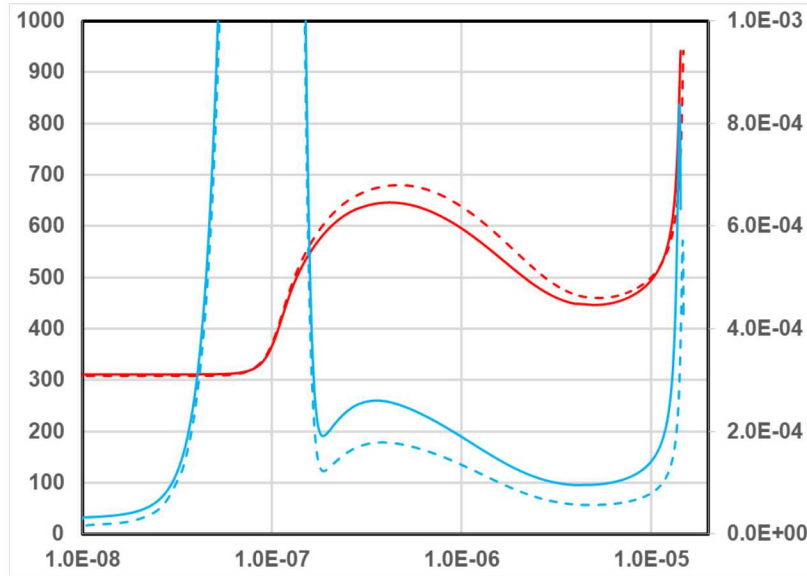
The scenarios described depend partially on the thermal characteristics (thermal resistors, material constants) representing the ability of the package and device to dissipate heat. It is obvious that changing these parameters will change the timescales or even the occurrence of the thermal runaways. Less obvious is the effect of the mesh used in the calculation. Therefore it is important to investigate this with a study that compares the results using different mesh densities. This was done primarily as a means to find a mesh density to reduce the total run times of the calculations but it raises interesting question concerning the accuracy of the simulations. For the most part the compared meshes are similar in the the semiconductor portion of the structure. However, the less dense mesh is significantly less dense in the passivation nitride part of the structure that lies atop the base and collector regions. This nitride should not contribute to the currents in the device but the mesh density in this region may affect the ability of the device to dissipate heat through this region. A reduced capacity for heat dissipation should lead to earlier thermal runaways and this is exactly what Fig. 9 shows for identical bias and radiation conditions.. The dotted lines representing the mesh with reduced



number of nitride meshpoints does indeed runaway earlier than the solid lines representing the denser mesh. The  $V_{BC}$  for both of these simulations is 18 volts.

These two mesh configurations exhibit a large difference in the thermal runaway times of the device. However, the qualitative time dependent behavior of the approach to runaway and eventual runaway is similar in both configurations. At this stage, the work is less focused on quantifying these behaviors and more directed at understanding the qualitative behaviors associated with the radiation and heating mechanisms. Therefore, from the standpoint of this work, both of these results have value in that they most likely represent the same fundamental mechanisms and the simulations using either mesh configuration can be useful to study.

### 6.5.3 Physical Mechanisms and Thermal Runaway



**Figure 10.** TCAD simulations showing temperature (red) and collector current (blue) versus time for two  $V_{BC}$  bias conditions. Dotted lines represent low  $V_{BC}$  bias (non-avalanche) and solid lines represent high  $V_{BC}$  bias (avalanche).

Despite the conclusion that simulations using the two meshes probably exhibit the same physical mechanisms, the question remains whether calculation scenarios using the same mesh but resulting in different runaway times are exhibiting

the same physical mechanisms. One method to study this question is to turn the query around and determine what time dependent differences exists for different physical mechanisms contributing to thermal runaways at the same time.

As an example, a simulation comparison can be used to address the question of whether the approach to thermal runaway is influenced by the presence or absence of avalanche current. At high  $V_{BC}$  values of 28 volts or above, avalanche current is present in the base-collector region and is incorporated in the calculations. Fig. 10 shows two calculations where the dotted line represent a low  $V_{BC}$  condition (18 volts) and the high  $V_{BC}$  condition (28 volts) is represented by solid lines. In both bases the thermal runaway occurs at 12  $\mu$ secs. Red represents temperature and blue represents collector current. To be clear, the dose rate has been adjusted in these calculations to yield the thermal runaways at the same time for both bias cases. The dose rate is higher for the  $V_{BC}=18$  volts case, thus causing the transistor to fail at the same time as the  $V_{BC}=28$  volts case.

The important conclusion to draw from this plot is that there appears to be no significant difference in the time dependent behavior between the two situations. This forces the conclusion that thermal runaway behavior is probably dominated by small set of factors that lead to similar behavior over a range of scenarios. This set of factors is most likely dominated by package thermal characteristics and the presence or absence of avalanche current does not seem to influence the qualitative runaway behavior.

#### 6.5.4 Radiation Upper Limits on Thermal Runaway

It is important to interpret simulation results such as shown here with regards to included and excluded elements of the calculations. In other words, to understand the results requires consideration of the included physics as well as any absent but essential components. For example, it is not unreasonable to exclude from a calculation a systematic bias which is definitely present but its magnitude is unknown. This uncertainty regarding the magnitude introduces difficulties in direct incorporation into the calculation and therefore the ramifications of the bias can be included in subsequent analysis of the results by regarding it as an *epistemic* uncertainty.

In the present case there are several elements that are excluded from the calcu-

lations because of lack of models or computational resources. It has been noted previously that the thermal characteristics of the packaging is approximated by simple thermal resistances attached to the contacts of the transistor in the TCAD calculations. However, no attempt has been made to describe what happens to these attachments at elevated temperatures. In reality, the thermal behavior of the semiconductor contacts or the package at high temperatures may dictate the failure limits of the transistor to a greater degree than the behavior of the bulk semiconductor.

The highest temperatures in semiconductor fabrication occurs in the processing of bulk semiconductor structures such as implants and passivations. These are typically referred to as front end of the line process steps or FEOL. The processing of the contacts, vias, and connective metallurgy takes place at lower temperatures and are called BEOL process steps. In fact, the BEOL structures in a semiconductor device would be unstable at the temperatures required to process the FEOL structures. Therefore, it is reasonable to conclude that the self heating limitations of a given semiconductor device may be due to the BEOL fragilities. Again, functional failures due to BEOL structures stressed by high temperatures are outside the scope of the present modeling. Rather, in these calculations, the emphasis has been placed on the bulk semiconductor behavior in the FEOL structures because this is the generation source of the heat.

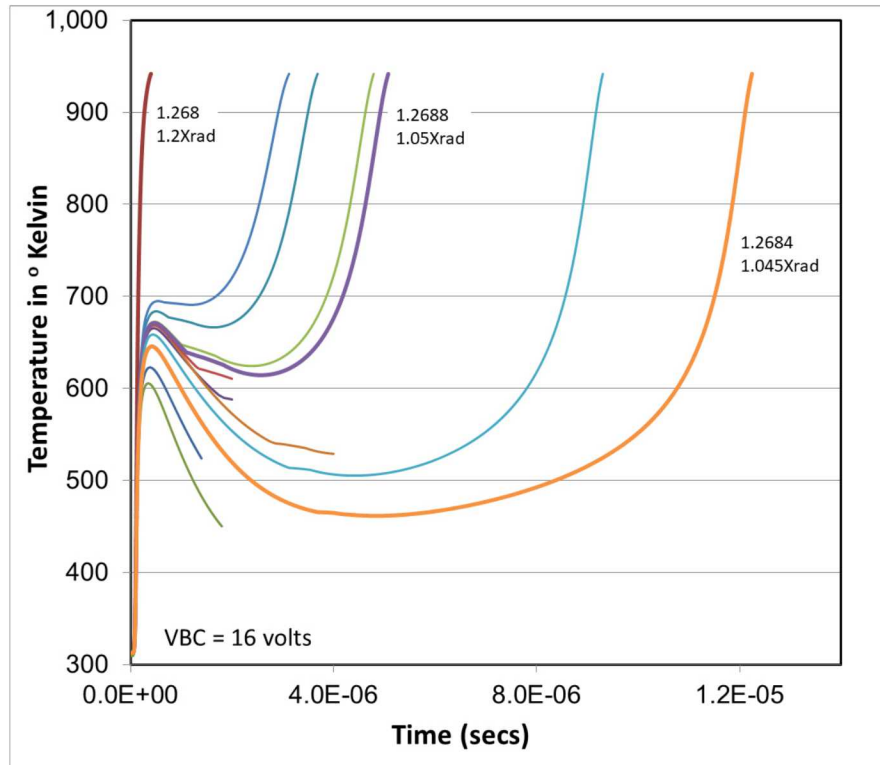
Transistor failure data suggests that the dominant failure modes may be independent of the semiconductor structure and may occur at lower radiation values than the current simulations suggests. [34] Thus the simulation results presented here for phenomena in the FEOL structures may systematically overestimate the dose rate induced temperatures resulting from self heating runaways.

## 6.6 Dense Mesh Extended Time Calculations

Previous sections have detailed the setup to the TCAD calculations and the types of analysis enabled by these calculations. In this section are shown results from the long term calculations and conclusions drawn from these results. These long term calculations demonstrate the time dependent thermal response of the HBT device for various radiation and  $V_{BE}$  levels. Each plot shows multiple instances of these values and the plots are grouped according to the value of  $V_{BC}$ .

This series of studies was performed with Silvaco TCAD using the mesh with the denser mesh in the nitride region. The longest of these simulations requires over 3400 hours of wall clock time to complete. Because of this computational burden, this series of simulation campaigns consumed over a year to complete. These computational details are noted here as a guidepost for future explorations in this field.

Although some of the computations were exercised at lower  $V_{BC}$  than 16 volts,



**Figure 11.** TCAD simulations showing temperature versus time for various  $V_{BE}$  and dose rate values, all with  $V_{BC}=16$ .

the value of  $V_{BC}=16$  voltage is the lowest shown in this report. Recall that the

trade off between field and current exists in these calculations so lower  $V_{BC}$  voltage should be able to support higher values of  $V_{BE}$  and higher radiation exposure values. In Figure 11, multiple trajectories of maximum device temperature as a function of time are shown, all with  $V_{BC}=16$  volts. Three of the trajectories are labeled with  $V_{BE}$  bias and radiation exposure number pairs in the calculation. The radiation exposure numbers are normalized to a estimated reference value of the radiation that causes the transistor to self heat and to continue into thermal runaway. This reference value was determined from a preliminary set of calculations intended partially to bracket self heating effects.

The shortest time to thermal runaway in the figure is the curve which reaches over  $900^{\circ}\text{K}$  in less than 500 ns. This is driven by the 20% over value of the reference radiation exposure. The curve which is 4.5% over the reference radiation values takes  $12\mu\text{secs}$  to proceed to thermal runaway and does so with higher collector currents due to a higher  $V_{BE}$  value.

All of these curves include a significant amount of self heating from the current pulse generated by the radiation pulse. In the curves of longer duration than 500 ns, self heating is followed by a cooling period before the device experiences thermal runaway. The  $12\mu\text{second}$  curve has a predicted rise in temperature of  $350^{\circ}\text{K}$  followed by an almost  $200^{\circ}\text{K}$  cooling before self heating. These are values from a computation that includes no failure mechanisms external to the bulk silicon such as contact heating or package degradation. Because of this, it should be noted that these high temperature and large cooling predictions should be regarded as the upper range of these phenomena.

One of the goals of this series of campaigns is the identification of the critical long term operational collector current that determines the runaway/no-runaway boundary. The longest duration curve in this figure ( $12\mu\text{seconds}$ ) is an estimate of approximately 4% above the reference radiation level which causes this critical threshold current. As part of this goal, mapping the radiation level of a set behavior (e.g. thermal runaway at  $12\mu\text{seconds}$ ) to  $V_{BC}$  or  $V_{BE}$  value is of interest in characterizing this boundary or the region around the boundary. Thus a 'standard' runaway time can be compared between different sets of  $V_{BC}$  and dose rate level calculations. Hypothetically, given a full matrix of calculation conditions, these standard curves (runaway at 8, 10, 12, etc.  $\mu\text{seconds}$ ) could be compared and one can be chosen as the SOA boundary definition. A difficulty arises due to the lengthy nature of some of the TCAD calculations and this is motivation for the compact model calculations.

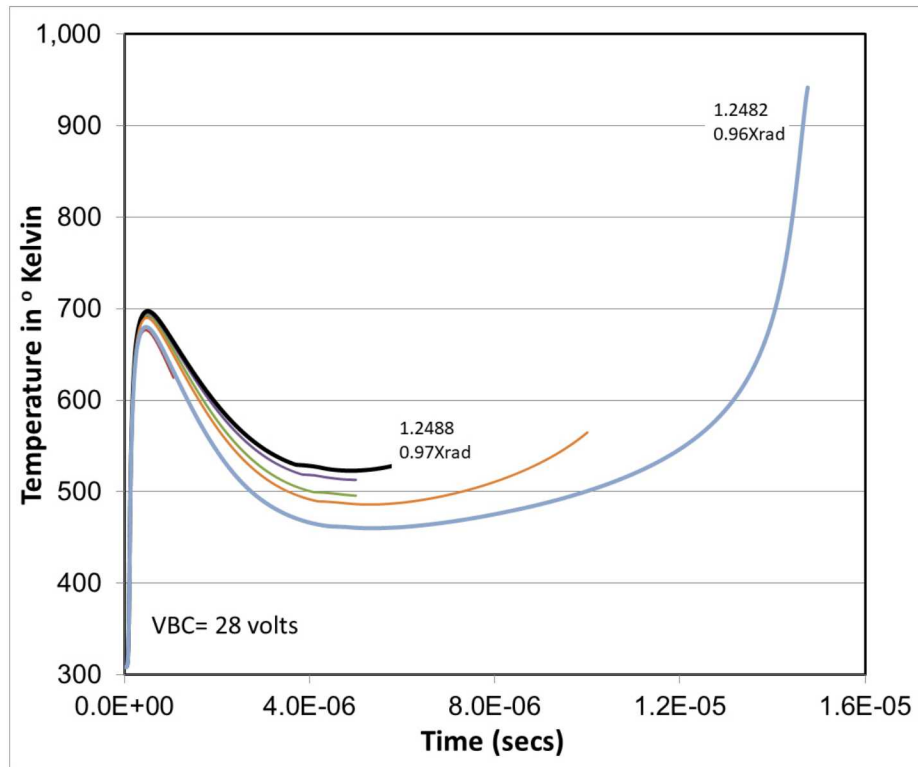


In line with the discussion in section 6.5.4, it is likely that the runaways calculated here are probably overestimates in terms of radiation magnitudes or time to failures. Recognizing that these standard curves are most likely upper boundaries allows some freedom in the choosing of the SOA boundary definition.

Since  $V_{BC}=16$  volts is considered a relatively low voltage with no avalanche effects, it is interesting to compare calculations at this scenario to a larger  $V_{BC}$  voltage such as 28 volts. This is shown in Figure 12 where it is immediately clear that there are less calculation results than at  $V_{BC}=16$  volts. The inclusion of avalanche effects at this higher voltage slows the calculation speeds considerably since each current calculation includes additional components of generated current. Consequently, there are less complete calculations at the longer runaway times because these calculations are the most lengthy of all the calculations in this report.

Nevertheless, there are important similarities and differences seen in these results compared to the lower voltage calculations. It appears that the initial heating and subsequent cooling deltas are slightly larger than the  $V_{BC}=16$  volt case. Although, the long runaway time curve in Figure 12 extends to 14  $\mu$ seconds, the fundamental shape of the curve seems to be similar to the time dependent shape of the 12  $\mu$ second curve in Figure 11. Again, it can be concluded that the addition of the avalanche current does not alter the mechanism of the advance to failure of the thermal runaway. A significant difference from the  $V_{BC}=16$  volt case is the smaller radiation levels shown in the Figure and the smaller  $V_{BE}$  biases of the scenarios.

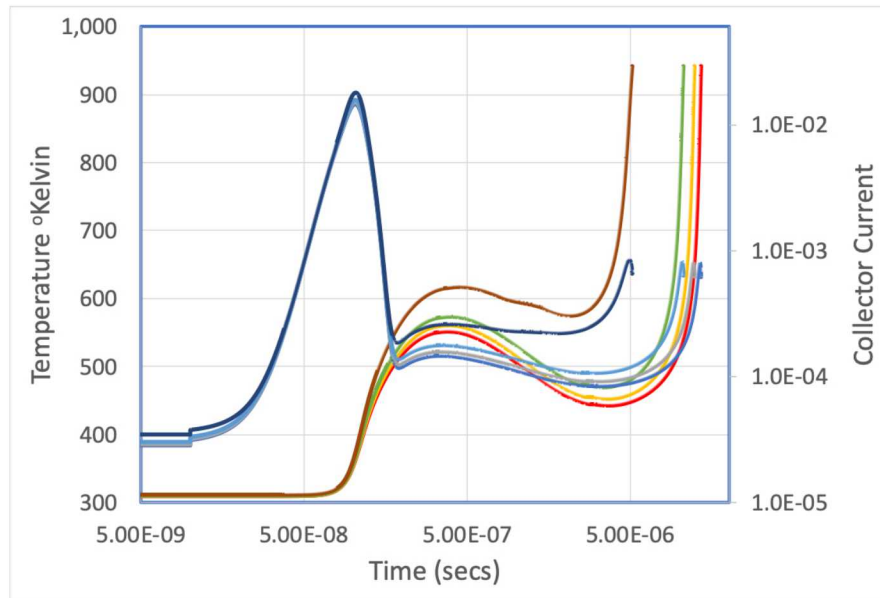
Additional  $V_{BC}$  voltage cases are shown in appendix A for completeness. Because of the computational burden of these calculations, the less refined mesh is used to extend these calculations to longer runaway times. Again, the ultimate goal is to find the defined reference radiation levels and  $V_{BE}$  values for each  $V_{BC}$  case and study the resulting SOA boundary.



**Figure 12.** TCAD simulations showing temperature versus time for various  $V_{BE}$  and doserate values, all with  $V_{BC}=28$ . This plot shows more partially completed simulations than the other plots because these simulations have an avalanche current component which is lacking in the other simulations. This makes the simulation much slower and thus more time is required for a finish. Due to machine uptime limitations, many of the simulations could not finish in allotted times.

## 6.7 Coarse Mesh Extended Time Calculations

Section 6.5.2 references studies with differing mesh node densities for the purpose of accelerating the lengthy TCAD calculations. The coarse mesh referenced in this section is the mesh used in ongoing work to establish the general SOA boundaries via the TCAD calculations. Although the ultimate aim of these calculations requires sufficient accuracy for predictive calculations, the more important capability at this stage is reproduction of the effects of the important physical mechanisms. The coarser mesh is considered adequate for this reproduction and the resulting calculations are considered valid examples of long term thermal runaway behaviors. Thus the SOA boundary derived from these calculations will be useful to study this system. Despite the differences (predictions of thermal runaways at



**Figure 13.** TCAD simulations showing collector currents and temperatures versus time for various  $V_{BE}$  and dose rate values, all with  $V_{BC}=16$ .

slightly lower radiation levels) the results from the coarser mesh can be compared to the dense mesh calculation. For example, figure 13 (coarse mesh calculations) should be compared to Figure 11 (dense mesh calculations). For convenience in the case of displaying both temperature and current in Figure 13, the time scale has been adjusted to a logarithmic scale. This enables the display of the X-Ray pulse (as reflected in the collector current) and the delayed response of the temperature.

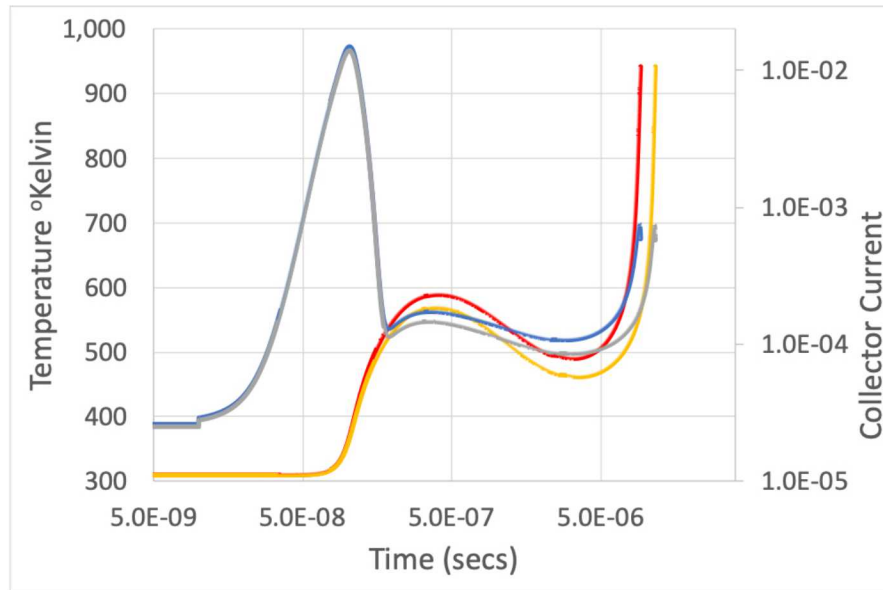
In the figure, both collector currents and maximum device temperatures are



shown as a function of time for several different pairs of  $V_{BE}$  bias and radiation magnitude. For comparison, the rightmost calculation in the figure proceeds to thermal runaway with a  $V_{BE}$  bias of 1.265 volts and a radiation pulse magnitude of 0.99Xrad. The thermal runaway occurs at 13.5  $\mu$ seconds. In Figure 11 the thermal runaway at 12  $\mu$ seconds occurs at 1.2684 volts and 1.045Xrad radiation pulse magnitude.

As anticipated, the radiation and bias levels are slightly lower for the coarse mesh results that are similar to the dense mesh results. The similarities outweigh the differences, however, and add credibility to the coarse mesh results. These similarities include the extended cooling period preceding the final increase to thermal runaway and the sudden drop in collector current as the maximum device temperature approaches its maximum value.

Similar characteristics are shown in Figure 14 which displays temperatures and



**Figure 14.** TCAD simulations showing collector currents and temperatures versus time for various  $V_{BE}$  and dose rate values, all with  $V_{BC}=18$ .

currents like Figure 13 but with  $V_{BC}=18$  volts. All of these plots show that the increasing characteristics of the collector current precede the temperature increase both in the case of the post pulse maximum and the final increase to device failure. This again points to the concept that the SOA boundary might be best defined in terms of a critical current in the collector.

Figure B.6 in appendix B shows similar calculations with  $V_{BC}=28$  volts.

## 7 Compact HBT Thermal and Photocurrent Models

The TCAD results in the first part of this work provide new insight into the physics of the lead up to thermal runaway induced by photocurrent in HBTs. A difficulty in using TCAD in these calculations is the computation burden and the corresponding lengthy time periods required for results. As stated previously, some calculations require multi-thousand hour run times. Thus any method to obtain these results in a more timely manner is highly desired. This leads naturally to a consideration of embedding the relevant physics into a compact model formulation and using compact model calculations to perform necessary studies. Given that sufficient fidelity can be introduced to the compact modeling, the ability to embed these calculations into circuits becomes a possibility and opens new avenues for research.

As will be seen, introducing realistic thermal physics into a compact model with dose rate radiation awareness requires several advances over existing models. In short, both the existing thermal models and photocurrent models possess shortcomings which limit their usefulness in this application. Much detail is covered in Robertson [29] as to the motivation and refinements needed for the compact thermal models.

Robertson's report describes the historical mathematical basis for thermal models applicable to crystalline semiconductor substrates. Specifically, the non-linear thermal conductivity found in GaAs substrates and related III-V materials used in GaAs HBTs is noted and discussed. The thermal properties of GaAs have been recognized as being the source of self-heating decades before similar self-heating problems became an issue for MOSFETs. Additionally, applications having frequencies in the GHz range commonly have to deal with high power dissipations in small volumes and the ensuing rapid rise in device operating temperatures.

Moreover, the use of GaAs based substrate material compared to silicon based substrates brings other non-linearities that must be modeled accurately. GaAs thermal conductivity is one third that of silicon and in the case of the typical heterojunction device the heat is generated in very small volumes scattered across the die. This leads to large thermal gradients from device junction through the substrate to the thermal sink. The device temperature can rise quickly, even when used in pulsed power applications, and if self-heating is not taken into account during a transient simulation, this can lead to considerably inaccurate solutions. The junction temperature of a GaAs HBT can quickly exceed 150C greater than the

surrounding die temperature. Inaccurate temperature estimate results in dramatic junction temperature error and can lead to convergence issues. The simulation need is to accurately predict the channel/junction temperature in order to predict reliability and radiation effects on the device. Again, the realization of an accurate thermal model compact model coupled with a photocurrent model in a circuit solver such as Xyce enables research opportunities but also the ability to impact design decisions early in the development process.

## 7.1 Essential Elements of Thermal Modeling in Compact Models

As mentioned above, for the reasons of size, application, material properties, and strong temperature dependence of thermal conductivity, GaAs devices can experience problematic self heating. All of these issues contribute to difficulties in obtaining accurate simulation results of GaAs HBTs operating even under nominal conditions. To illustrate the thermal conductivity issues, thermal conductivities of several selected materials are shown in Table 1 [17]. The values are given in Watts per meter Kelvin [W/mK] and are quoted at given reference temperature, typically  $T_{ref} = 300\text{K}$ . The thermal conductivity parameters for a number of other materials such as Aluminum and Silicon have been included for comparison. Throughout this report, the thermal conductivity at 300K for GaAs is assumed to be 46 W/mK from [17]. It should be noted that the thermal conductivity value of 44 W/mK for GaAs in earlier references such as [10] has been included in the table for completeness. The values in the table makes clear that GaAs is at a disadvantage when it comes to transferring heat compared to other materials making up semiconductor structures.

Heat transfer from a region of higher temperature to a region of lower temperature is accomplished by one of three methods depending on the geometry; Conduction, Convection, Radiation. For the purposes of the studies here, we focus on conduction as this is the mechanism used in the TCAD calculations and assumed in the compact model. The heat is carried through a pure semiconductor in the temperature range 0-600K by phonons (atomic vibrations) [5]. Interactions between atoms in a crystalline solid such as GaAs, can be considered as truly elastic, collectively producing displacement waves through the material. In an ideal, infinite crystal lattice, the thermal energy of the solid is expressed in terms of the

**Table 1.** Thermal Conductivity for Various Materials

Material	$\kappa [W/mK]$	$\alpha$	References
air	0.026		15
Silicon (Si)	148	1.3	9
Copper (Cu)	399		5
Aluminium (Al)	205	1.3	16
Gallium Arsenide (GaAs)	46	1.25	16
GaAs Earlier Values	44		16
Aluminium Arsenide (AlAs)	80	1.37	16
Indium Phosphide (InP)	68	1.4	16
Galium Nitride (GaN)	130	1.4	16
Gallium Phosphide (GaP)	77	1.4	16

collective harmonic motion of the atoms in the lattice. In a real material, the motion of the atoms is not harmonic. Because of the nature of and the dominance of this phonon mediated conduction mechanism, it is reasonable to assume that the conduction mechanism changes as the motion of the lattice changes. In other words, it has a strong dependence on temperature.

For example, in silicon at 0K, there is no motion in the lattice, thus the thermal conductivity is 0 W/mK. The thermal conductivity rises approximately exponentially with rise in temperature to a maximum near  $20^\circ K$  and then falls at a rate greater than  $1/T$  to around  $500^\circ K$ . The thermal conductivity flattens out approaching a limit as the temperature rises above  $1000^\circ K$ . The subject is covered in detail in [5] where the reader can find a graphical representation of the temperature dependence of thermal conductivity of Silicon in Figure 1.

Therefore, the thermal behaviors to be captured in a model include not only the effect of low thermal conductivity in GaAs to begin with but also the effects of power dissipation on the currents in a device. In addition, the dependence on temperature of these effects must be included.

## 7.2 Elements of Photocurrent Compact Models in Semiconductors

In the high fidelity TCAD calculations, dose rate effects are introduced through the time dependent addition of charge carriers into the semiconductor materials. At every node point in the simulation structure, the current continuity equations

account for the drift induced and diffusion induced motion of these carriers. In addition, the Joule's law based heating contribution of these carriers is calculated and influences the lattice temperature at every node. This schema ensures that a direct connection exists between the current in the device and the temperature of the device. Note that the Joule's law formulation accounts for carrier contribution to heat from all carriers, both from normal operation of the device and the excess carriers introduced by radiation. Therefore, the increased temperature will increase the number of device operation carriers which will contribute to an increased temperature and so on. It is conceptually straightforward to understand that thermal runaway modeling is an intrinsic feature of the TCAD modeling.

The calculation scheme is different in the compact models. It is important to realize that the normal environment operation model of the device is a stand alone code module that can be independent of the code describing the photocurrent response and also is independent of the calculation that determines the temperature of the device as a function of the current flowing through it. Various models can be used to describe the normal environment device operation and these models include the Ebers-Moll, Gummel-Poon, or Vertical Bipolar Inter-Company (VBIC) models. Here, the VBIC model is used and calibrated to describe the HBT device under study in this work. Additionally, there exists several generations of dose rate effects models (of which Wirth-Rogers is the first [2, 3]) but this study uses the Tor Fjeldly (TF) model [16].

The Tor Fjeldly model is a compact model which is applied at every biased PN junction in the device. The model considers the contributions to photocurrent at a PN junction as originating in three regions about the PN junction. The regions consists of the depletion region and the two quasi-neutral region on either side of the depletion region. The quasi neutral regions are defined by the minority carrier lifetimes or the diffusion lengths of the carriers in the region. The model calculates the depletion region volume as a function of the applied bias and the quasi neutral region volume as a function of the carrier diffusion lengths. The total dose rate generated charge is calculated dependent on the magnitude of the dose rate and the volume of the regions. This total charge is then added to the device currents at internal terminal nodes of the device.

In the Tor Fjeldly modeling scheme, each PN junction in a transistor (the emitter-base and the base-collector) is represented by a current source attached between the respective terminals. The currents thus generated must be integrated into the thermal model in order to influence the device temperature. Without the



addition of a thermal model, the excess photocurrents have no influence on the temperature of the device in the model. The implementation of the Tor Fjeldly model in this manner does fail to reproduce some of the dose rate induced behaviors of a transistor in terms of current magnitudes and this and other details are discussed in section 7.3.4.

### **7.3 HBT Self Heating and Radiation Compact Model Research Elements**

Sections 7.1 and 7.2 briefly outline the important elements of implementing the thermal and photocurrent models and their application with the HBT compact device model. Each of these models were developed separately to pair with the normal environment device model and consequently require modification to work together. The following sections provide some detail on the research developments that are required to make these models compatible with each other and to match the computational physics capabilities of the TCAD high fidelity modeling. The topics are presented roughly in order of implementation in this study although work continues on refinements in each of these areas. The results presented here are preliminary and will be refined as developments occur.

#### **7.3.1 Improved Heating Expression**

Work has concentrated on basing the modeled heat dissipation in a device on physically reasonable processes and encapsulating a description into a mathematical formulation that can be included in a compact model. An essential element of this description is the inclusion of the thermal resistance increase as the temperature of the device increases. Including this positive feedback effect in the model allows the model to predict the thermal runaway behavior observed in measured devices. Another important aspect to capture is the correct geometry of the heat spread. It is this geometry that determines the magnitude of retained and transferred heat from the device. Finally, in regard to capturing the realistic behavior of a device in thermal runaway, it is desirable to control the calculation and restrict it from numerically unstable regimes by constraining the calculation within phys-



ically reasonable limits of temperature or current. The intent is to replace the too simple self heating DT node and RC circuit methodology present in the VBIC and other compact device models with a more accurate and less approximate formulation.

By convention in the electronics industry, the relation of heat flow in a device and the change in temperature of the device is given by the expression representing an equivalent thermal circuit.

$$\Delta T = Pwr_{diss} \cdot R_{therm} \quad (4)$$

where  $Pwr_{diss}$  is the power dissipated in the electronic device and  $R_{therm}$  is given by

$$R_{therm} = A \cdot (C_1 + C_2 \cdot T + C_3 \cdot T^2) \quad (5)$$

This thermal resistance relationship comes from Robertson [29]. The term encapsulates the nonlinear behavior of the thermal resistance with temperature and the temperature behavior of the correct geometric sourcing of the heat. This relationship is to be regarded as an analog of Ohm's law where the voltage represents a difference in temperature and the dissipated power is a current.  $C_1$  is usually referenced as the ambient temperature and  $C_2, C_3$  are calibration constants.

The rate of energy transfer for an electronic device with voltage drop  $V$  and current  $i$  is

$$dE/dt = V \cdot i \quad (6)$$

Where  $dE/dt$  is the the same as  $Pwr_{diss}$ . As a first pass expression without regard for device geometry it is reasonable for a three terminal transistor with two semiconductor junctions to write

$$dE/dt = Pwr_{diss} = abs(V_{BE} \cdot i_{emit}) + abs(V_{BC} \cdot i_{coll}) \quad (7)$$

This expression assumes no voltage drops to the base contact or in either the emitter or collector regions. In actually, these exist but are of low magnitude and are ignorable. This expression is usable for a large geometry transistor where the self

heating of the device may occur separately for the two junctions and two 'hot spots' may exist in the device.

In a transistor with smaller vertical dimensions, these two regions of heating may act as a single region. In practice, the calculation of heat in a device is important when the structure or part of the structure is susceptible to damage or change from the dissipated heat. In most devices, the semiconductor lattice is relatively hardened to heating effects but the contacts and contact metallurgy are more fragile and are fabricated at lower temperatures. With this regard, the emitter contact is the contact that is typically in proximity to the most heated region of the transistor and therefore is the structure of interest. By this argument, it is reasonable to consider only the heat generated close to the emitter contact and the dissipated power may be written as

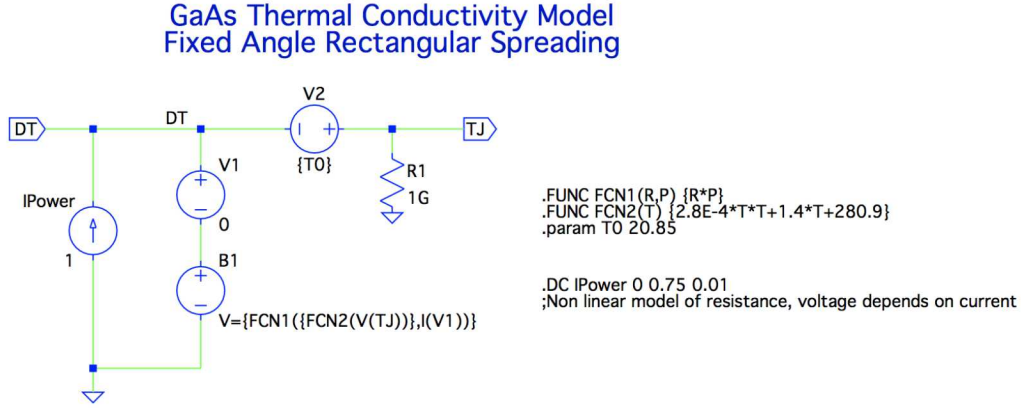
$$dE/dt = Pwr_{diss} = abs(V_{BE} \cdot i_{emit}) \quad (8)$$

This is sometimes written as

$$dE/dt = Pwr_{diss} = abs(V_{BE} \cdot i_{coll}) + abs(V_{BE} \cdot i_{base}) \quad (9)$$

where this makes it explicit that the emitter current is nominally the sum of the collector and base currents. Another argument for writing it this way is that the collector can sometimes contribute more current than the emitter during a photocurrent generating event because of the relative volumes of the regions.

Figure 15 shows how the thermal model is applied to the VBIC compact model. This figure is a schematic where the thermal model is represented as an electrical circuit. In this circuit, the thermal resistance is internal to the voltage source (B1) and the current in the circuit is the dissipated power. Voltages in this circuit are equivalent to temperature differences. This thermal circuit includes a node (DT) which takes the applied voltage at this node and uses it to set the operating temperature of the device in any simulation using the model. In the VBIC model, this node was initially defined to couple with a calibrated thermal resistance which is replaced in the current work with the expression in equation 5. Thus, the dissipated power (current) flowing through either the calibrated resistance or this improved expression sets a voltage which defines the temperature of the device. Note that total dissipated power here includes both operational and any dose rate induced dissipated power.



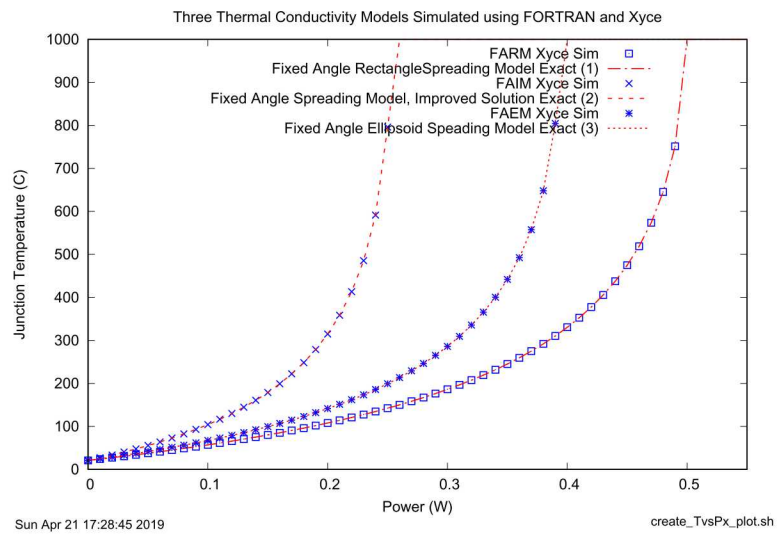
**Figure 15.** Schematic of expression applied to the DT node of a HBT device to capture nonlinear thermal resistivity and self heating effects

The total temperature change of the transistor undergoing self heating is then given by the populated expression for equation 4 using the expression that is a function of temperature to represent the resistance multiplied with the dissipated power (current) of the device.

$$\Delta T = [abs(V_{BE} \cdot i_{coll}) + abs(V_{BE} \cdot i_{base})] \cdot A \cdot (C_1 + C_2 \cdot T + C_3 \cdot T^2) \quad (10)$$

Equation 10 represents the change in temperature of the device in terms of the current flowing through the device and the temperature of the device. With appropriate calibrations to the constants, it should represent the self heating behavior of an actual HBT device. This model is demonstrated in Figure 16 with the junction temperature shown as a function of the power through the device. Three different behaviors are shown to exhibit the calibration range of the model.

This expression is a starting point in implementing a more realistic thermal treatment in a compact model HBT description. It will be coupled with the other research thrusts in this study to realize the compact model description of device behavior in the presence of radiation. However, as will be seen in the next section, this nonlinear thermal resistance results in more complex behavior of the transistor model at higher currents and higher power dissipations.



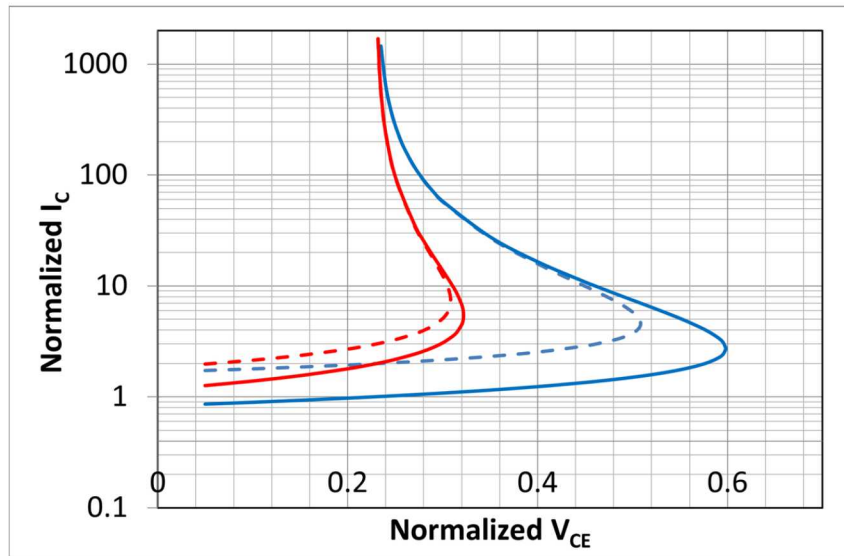
**Figure 16.** Plot of the expression in Fig. 15 and in equation 10 with three different sets of model parameters.

### 7.3.2 Operation at a Safe Operating Area Boundary

Adding self heating calculations to the functional device compact model results in a mathematical system where multiple solutions may exist for ranges of the independent variable. For example, quantities such as collector currents that depend on the collector emitter voltage possess multiple solutions in certain ranges of voltages. This leads to numerical ambiguities in current solutions for particular independent variable values and hence unstable systems. In actual performance of some electronic devices and model descriptions, this gives rise to flyback or turning point behaviors.

In operation, these turning points represent significant transition points between different regions of device operation. A device may experience nominal operation at voltages below a threshold collector emitter voltage and experience unpredictable behavior at voltages above this threshold. In practice, these thresholds or turning points can be equated to the safe operating boundaries of the devices.

The ability to explore mathematical solutions around the turning points is a



**Figure 17.** Turning point behavior as exhibited by collector currents in analytic calculation. The dotted lines represent the collector currents with the addition of radiation induced photocurrent.

necessary capability to map out the SOA of the device in normal environments. As a calculation strategy, the pursuit of modeling runaway behavior begins at this boundary and is then extended to regions enclosed within the safe operating area.

The working demonstration of a radiation induced thermal runaway in the model at this boundary is proof that such a model can be constructed. It then becomes an extension to an existing model system to induce thermal runaways at higher levels of radiation and at points removed from the SOA boundary. In principle, minor perturbations to the system (or model) at this boundary should induce significant changes to the possible solutions and this is what we seek to demonstrate the potential of the compact modeling.

To begin the analysis, turning points for collector current can be represented with an analytic expression and the effects of radiation can also be incorporated into the same expression. Exercising this analytic expression provides insight to the follow-on analysis with numerical models, both high fidelity and circuit solver level. The following expression for collector current contains a term for electrothermal feedback which leads to multiple solutions.

$$I_C = I_0 \cdot e^{\left[\frac{q}{kT}(V_{BE} - R_E I_E - R_B I_B + R_{th} \phi I_C V_{CE})\right]} \quad (11)$$

Where  $\phi$  is the electrothermal feedback coefficient. Adding photocurrent to the collector can be expressed in a straightforward fashion as an additional term if secondary photocurrent is excluded:

$$I_C = I_0 \cdot e^{\left[\frac{q}{kT}(V_{BE} - R_E I_E - R_B I_B + R_{th} \phi I_C V_{CE})\right]} + I_{photo} \quad (12)$$

Photocurrent can be expressed in steady state conditions via a Wirth-Rogers formulation [2]:

$$I_{photo} = I_{SS} = aAG(W_t + L_p + L_n) \quad (13)$$

Secondary photocurrent across a forward biased junction can be expressed as a modification of forward bias:

$$I_{photo} + I_{operation} = I_0 e^{\left[\frac{q}{kT} V'_{BE}\right]} \quad (14)$$

These equations can be normalized and approximated by an equation of the form.

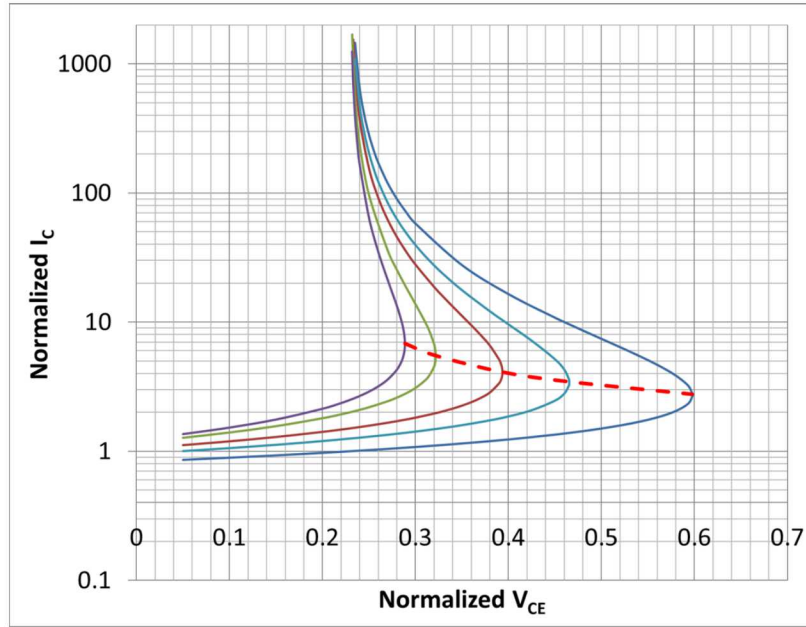
$$i = c_2 e^{(c_2 i (v - c_1))} \quad (15)$$



Modifications to this equation allow an exploration of parameters that influence the voltage location of a turning point as well as the current level. Figure 17 is an example of this. The solid curves in the figure represent the collector currents as a function of  $V_{CE}$  and the two curves represent the calculation at two different values of  $V_{BE}$ . Note that the red curve implies a turning point at higher current than the blue curve but at a lower value of  $V_{CE}$ .

These curves are mathematical representations of device behavior but measured devices most likely will not show the retrograde  $V_{CE}$  characteristic. Instead, a measured device most likely will exhibit a runaway increase in current at the turning point with no change in  $V_{CE}$  of the device. This behavior corresponds to the nominal operation up to the turning point and unpredictable behavior at higher voltages.

However, these curves do illustrate the trade off between current through the

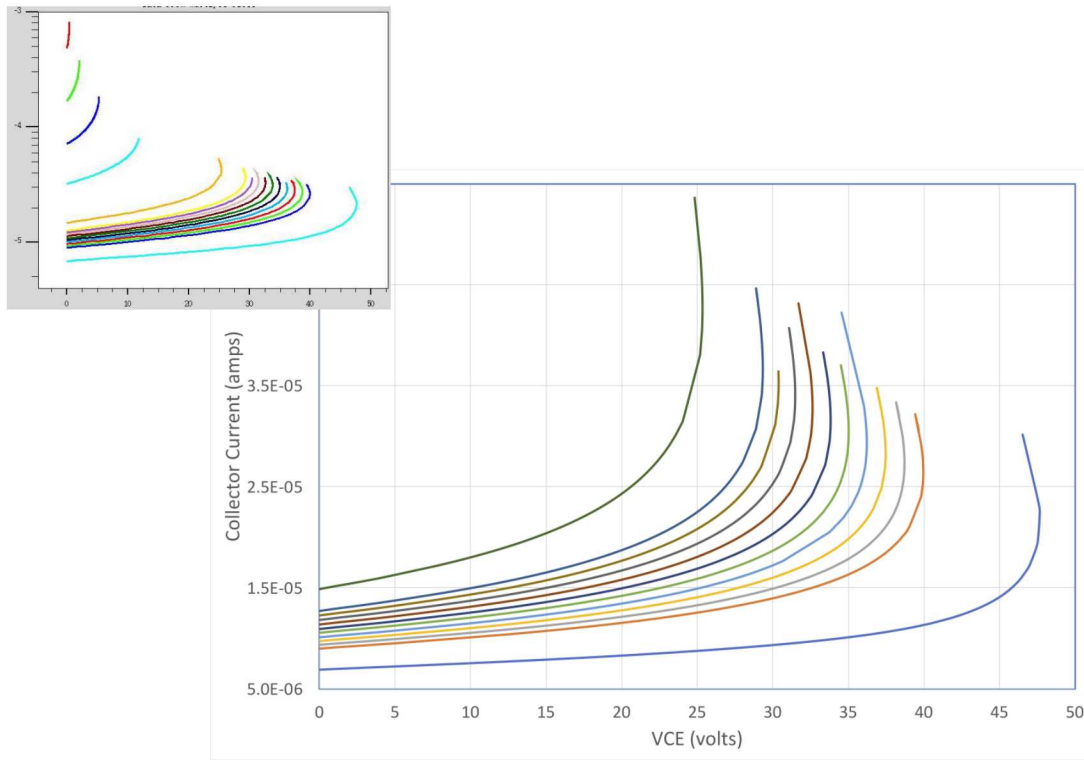


**Figure 18.** Turning points from several analytic collector current curves linked together into a safe operating area boundary.

device and electric field at the base collector at each of the turning points. As a further illustration, the dotted curves show the evolution of the curves when a constant amount of generated photocurrent is added to the system. These curves are generated by the addition of a constant to equation 15. Again, the additional photocurrent adds to the current at each of the turning points but the points correspondingly move to the left in the plot implying that the turning point will occur

at lower  $V_{CE}$  (lower base-collector fields) values in the presence of radiation.

Stitching together the turning points from several curves such as the ones in Figure 17 allows the construction of a complete curve. In the case shown in Figure 18, this is the SOA curve under normal operating conditions with no radiation applied. Each curve in Figure 18 represents different base currents or a different base-emitter bias. In principle, this curve could be used to define limits to operate the device so that thermal runaway is not experienced. However, the purpose of the exploration of the SOA with analytic representation is to understand the concepts and to conduct a preliminary exploration of behaviors with the addition of radiation. The generated curves illustrate the general concepts of the trade offs along the SOA between electric fields and current. Despite the insights provided by this calculation, the analytic treatment includes no expectation of a quantitative description.



**Figure 19.** TCAD generated  $I_C$  vs  $V_{CE}$  curves calculated to low current turning points and beyond to calculation failure. Linking the turning points together forms a safe operating area boundary in normal environments. Inserts show turning points calculated both at low voltages, high currents and high voltages, low currents

In order to explore the SOA boundary more quantitatively, it is desirable to be able to reproduce these behaviors with simulations at the high fidelity device level or the device model in a circuit solver. In both cases, some type of continuity techniques are required in order to map the current curves in the vicinity of the turning points. For the high fidelity case some information can be found in the curvetrace technique detailed in [32]. A demonstration of the TCAD calculations with continuity techniques applied in a similar configuration as in Fig. 18 is shown in Fig. 19. TCAD calculations of device currents are conducted as a function of a  $V_{CE}$  ramp up to the  $V_{CE}$  value where the calculation reaches a turning point and then to the point where the calculation fails. Without a specific curve-continuity technique employed, the calculation fails at the turning point and is unable to continue. These calculations are adequate to establish the definitive turning points and thus produce the boundary points of a normal environment SOA curve like in Fig. 18.

Each curve represents a device with differing magnitudes of current injected across the emitter base junction. The leftmost curve represents a device operated at a high forward emitter base bias of 1.26 volts and the rightmost curve represents a device operated at a lower 1.24 volt forward bias. The curves in between are obviously intermediate biases.

Since these curves are generated by a high fidelity simulation of the HBT device under study, it is possible to rely on these curves for a quantitative assessment of the SOA boundaries. It should be borne in mind however that each of these curves is a TCAD calculation that requires a computational cost, in this case about an hour per curve. The time spent generating these curves is therefore considerable. Another aspect to consider is whether radiation could be added to these computations as it was in Figure 17 with the goal of generating radiation aware SOA boundaries. The analysis in Section 6.4 and following sections shows that there is a time dependence to the buildup of heat in the devices and the runaway curve cannot be adequately delineated statically. Thus the radiation aware SOAs are most accurately calculated with time dependent TCAD calculations as detailed in previous sections.

As seen in these previous TCAD calculations, it is not necessary to operate the TCAD calculations on the normal environment SOA boundary to allow the simulated devices to proceed to thermal runaway. Due to the inclusion of the relevant physics, the TCAD calculations are able to show runaway behaviors at biases and currents not on the normal environment SOA boundary but rather in the interior

of the regions enclosed by the SOA boundary. Due to the lengthy computational burden of these calculations, the present effort seeks to incorporate the same capabilities in the compact modeling description of these devices.

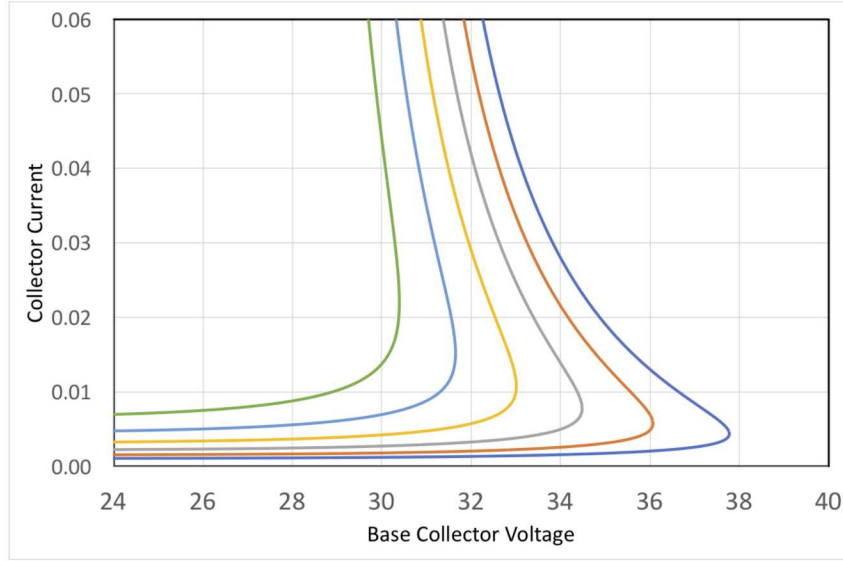
Therefore, more relevant to compact model investigations are turning points in device characteristics generated by a device model in a circuit simulation. Since the system of equations in compact HBT models is different than the TCAD calculations, the method of arc-length continuations requires a custom implementation. New algorithms are added to Xyce (arc-length homotopy) to allow solutions up to and beyond the turning points. Continuation Algorithms are the general sets of algorithms to enable these calculations. The algorithms in Xyce are based on The Library of Continuation Algorithms (LOCA) created in 2002 at Sandia National Laboratories. [18] This library is aimed at the tracking of solution branches as a function of a system parameter and the direct tracking of bifurcation points. A good reference for a graphical representation of arc length methods is Vasios [26]. The Xyce implementation allows for the computations to proceed to and beyond turning points.

Fig. 20 is an illustration of the VBIC device model coupled with the improved thermal model and used to calculate collector current turning points as a function of  $V_{CE}$ . In this case, arc-length homotopy is used to obtain solutions at higher currents than the turning point and the calculation is able to proceed along the curve to multiple solutions.

This figure is a circuit solver calculation but the calculation focus is similar to the analytic results of Fig. 18. Whereas the analytic curves are hypothetical, these curves are results from a model that has been calibrated for normal device operation and also calibrated for thermal behavior. Instead of normalized currents and voltages, the values in Fig. 20 are realistic and sufficiently accurate to form a rough SOA boundary as an operating guideline. As an example, the rightmost turning point is at almost 38 volts  $V_{BC}$  and with a corresponding collector current of  $\sim 5$  ma. The leftmost curve contains a turning point that is 4X higher in current but only supports a  $V_{BC}$  that is almost 8 volts less than the lower current case.

There are multiple mechanisms that interact to reduce the supportable  $V_{BC}$  and it is clear that higher accelerating fields at the base collector reduces the current carrying capacity for a given temperature. Or in other words, at high currents, the accelerating voltages must be lowered to keep the device within a temperature range. Correspondingly, the operating currents must be lowered if the device is to be operated at a high  $V_{BC}$  voltage.



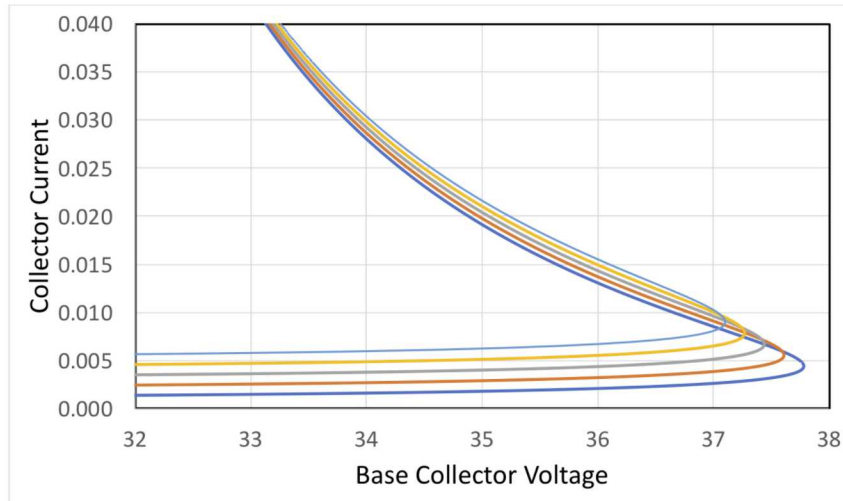


**Figure 20.** Turning points in collector currents as a function of  $V_{CE}$  as calculated in Xyce. Left most curve corresponds to  $V_{BE}=1.30$  and rightmost curve corresponds to  $V_{BE}=1.25$

The fundamental mechanism responsible for these limits is Joule heating of the lattice caused by the current. (See equation 2.) At high fields, the avalanche mechanism is a component of the limiting currents as well. The important point to keep in mind is that the simple expression (equation 10) captures the temperature response as a function of current and is calibrated to reflect the correct response. The expression is versatile and can describe HBT's in general but must be recalibrated for each device and the particular mixture of mechanisms in each device.

The analytic exercise displayed in Fig. 17 can also be duplicated using the compact model numerical system. In Fig. 21 is shown a similar scenario where in this case the steady state constant photocurrent is added as a constant current through the base collector junction implemented with a current source. The analytic model exercised in Fig. 17 is an behavioral expression for collector current from an analytic description of a device. The numerical device calculation in Fig. 21 represents an additional collector current component that is comprised only of base-collector addition current. Despite this difference, some of the features in both figures show similar behavior.

As in the high fidelity TCAD case, this analysis can yield insight with certain limitations. Again, the issue of time dependent dissipated power heating of the device plays a significant role in advancing the transistor towards thermal runaway



**Figure 21.** Turning points in collector currents as a function of  $V_{CE}$  as calculated in Xyce. Incremental magnitudes of dose rate induced photocurrent have been added to each curve. Left curve = max photocurrent, rightmost curve = 0 photocurrent.

and is not addressed in these static calculations. It is desired to include these elements in a compact model description of the process and the following sections outline some of the approaches to accomplish this.



### 7.3.3 Adding Time Dependence Through a Thermal Mass Term

Preliminary work with coupling the thermal and the photocurrent compact models has shown that the resulting approach to thermal runaway is rapid (10s of nanoseconds) and binary (absolute boundary in dose rate magnitude between simulations that experience thermal runaway and ones that do not) in initial calculations with no additional included physics. This is considered unrealistic as the time constants seen in TCAD calculations and experimental data are usually much longer than this tens of nanosecond timescale.

The standard thermal modeling approach in compact models utilizes an R or an RC circuit attached to the device node (DT) that defines the temperature. The RC circuit enables some variation in determining the rate of temperature change but a more customizable method will most likely be required for matching data. It is expected that heating and cooling descriptions will be matched with a pre-factor term to modify the rate of temperature change in the device model. It needs to be stressed that the heating and cooling pre-factor terms should be different and separate to reflect the different geometries of heating (centralized) and cooling (distributed). Simulation experiments to further define this pre-factor are underway.

It is anticipated that a possible form of the pre-factor is:

$$M_{therm} = (1e^{-(\alpha \cdot t)}) \quad (16)$$

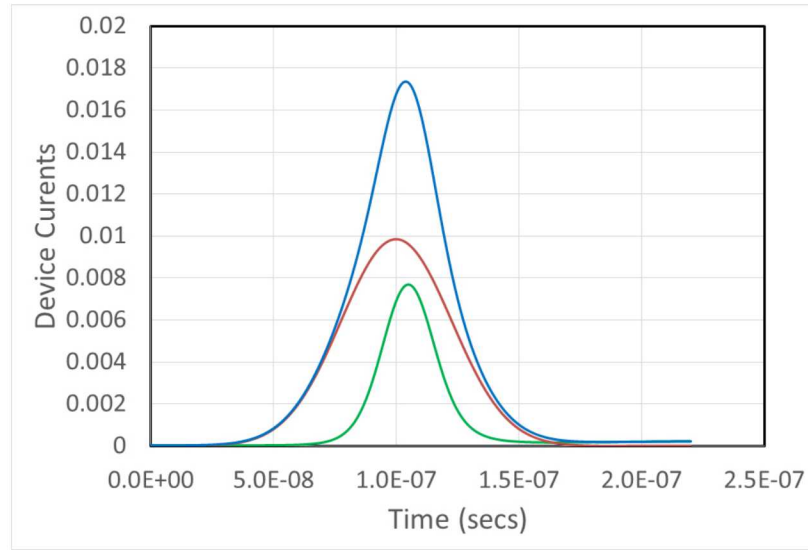
Where  $\alpha$  is an adjustable decay constant

### 7.3.4 Two Terminal Current Sources Applied to Three Terminal Devices

TCAD modeling indicates that all forward active HBT terminal currents increase in magnitude under irradiation by an X-Ray or  $\gamma$  ray pulses. In some cases this current is sufficient to induce joule heating as the carriers drift due to electric field and undergo scattering with the lattice. In this situation, the amount of current increase is amplified because of the increase in temperature and the resultant rise in intrinsic carrier density ( $n_i$ ). This feedback is one of the physical mechanisms that lead to thermal runaway. Intuitively, this situation is unsurprising as the additional carriers should lead to additional currents throughout the device.

As a demonstration of this expectation, Figure 22 shows the increase in magnitude of all of the terminal currents of an HBT during a dose rate radiation event as simulated in a TCAD simulation. Note that the figure shows the absolute values of the device currents.

Recreating the results of Fig. 22 with compact models requires careful im-



**Figure 22.** Absolute values of time dependent currents at three terminals of an HBT during a photocurrent inducing radiation event.

plementation because of the limitations of the compact models. In the ideal case, dose rate controlled current sources (DRCCS) can be added to the junctions of the device at the same level of code that incorporates the device functional model such as the VBIC model. In the SNL circuit solver Xyce, this is the approach taken to describe photocurrents in a BJT whose functional behavior is described by the

Gummel-Poon model under normal environment operation. This treatment follows the approach taken by Tor Fjeldly as originally implemented in AIMSPICE. For convention, this configuration can be referred to as the 'encoded TF' as in encoded Tor Fjeldly. In the encoded TF, the DRCCSs have geometry dependence built into the calculation of the prompt dose rate current generated in the depletion region as does the contribution to the currents from the quasi-neutral regions surrounding the junctions. In principle, the photo generated currents in the device at one junction of a two junction device can be transported through the device to be counted as current at the other junction. This linking of the currents between the junctions mimics the architecture of the Ebers-Moll model which is carried through to the Gummel-Poon model. This schema has been tested and verified to yield qualitative correct results (as verified by TCAD) in both saturation and forward active modes.

This device level encoding of the photo currents in an HBT does not exist for the current work so a more approximate approach is used instead. This approach uses two separate DRCCSs that are applied to the terminals of the HBT at the netlist level and this leads to several potential problems.

The first of these problems is associated with the application of 2 separate 2 terminal DRCCS applied to a three terminal device which may preclude interaction between junctions and moreover lead to reduced current at one terminal. This latter situation arises if the terminal has net opposite polarity current than the current contributed by the DRCCS and the DRCCS currents are of the same magnitude as the transistor operating currents. TCAD simulations have shown that a dose rate induced photocurrent can reverse the base current of a device under specific circumstances but the concern with the compact model extends to more general situations.

A second difficulty is that the shared base region in a 3 terminal transistor must be split between and correctly dimensioned in each of the 2 separate DRCCSs. An incorrect specification for these dimensions may prohibit the 2 DRCCS calculation from matching exactly the encoded TF formulation at all biases. [33] It could be the case that when the biases are such that both junctions have huge depletion regions (that basically penetrate almost all the way across the base), the simulation with externally applied DRCCSs will differ significantly from the encoded TF calculation.

The reason is that in the implementation of the two photocurrent sources buried inside the encoded TF code, the delayed photocurrent terms involving the base are

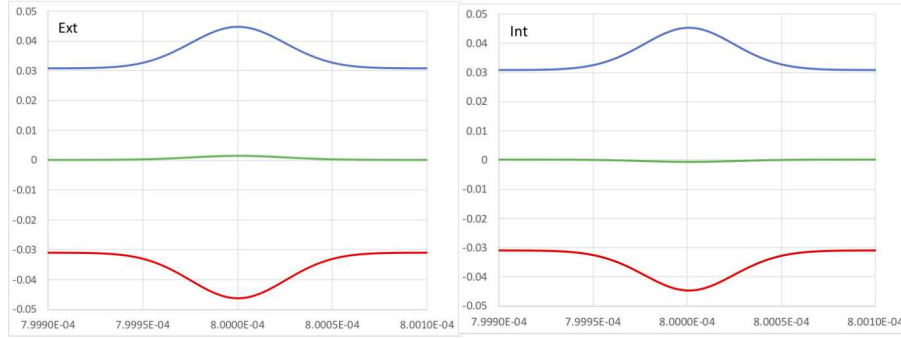
not strictly independent. This is in contrast to the situation with two externally applied DRCCS where each current source behaves independently. The first step of computing the photocurrent in the DRCCS is to determine the depletion region width and its penetration into the N and P sides of the junction. The depletion width itself determines the prompt photocurrent (which is basically just proportional to the volume of the depletion region times the generation rate, on the assumption that all pairs that get created in that volume are instantly swept out by the high fields). But the penetrations into the P and N regions are also used to compute the quasi-neutral part of those regions — that is, the part outside of the depletion region. The delayed photocurrent depends on the size of the quasi-neutral regions.

The encoded TF computes the BE and BC depletion widths and how far they extend away from the junctions in each material, so the quasi-neutral base width is the the base width given in the model card less the part of the BE depletion region that lies in the base, less the part of the BC depletion region that lies in the base. The quasi-neutral base width is used in the computation of two components of the delayed photocurrent. There are quasi-neutral emitter and quasi-neutral collector widths computed as well, which impact other delayed photocurrent terms. The external DRCCS does the same sort of computation to compute the quasi-neutral P-region width and quasi-neutral N-region width that are used in the same manner in the delayed photocurrent terms. This is why the two can't agree completely: there is no way for the two external photocurrent sources to know what fraction of their P material is already part of the other's depletion region, so the width of the quasi-neutral part (and therefore the delayed photocurrent) is computed incorrectly.

Finally, use of externally applied DRCCSs produces different results depending on whether the application of the DRCCS is to the external transistor terminals or the internal terminals of the device. The important differences in the results depends on the values of the terminal resistances and if the photo current magnitudes are sufficient to change the net voltage applied to the terminals. In the case of the SNL HBT, the terminal resistances are on the same order as the terminal resistances of an industry standard 2N2222 device,  $\sim 1\ \Omega$  for the collector,  $\sim 10\ \Omega$ s for the base and  $< 1\ \Omega$  for the emitter.

These values do produce voltage drops of sufficient magnitudes to create differences in calculation results dependent upon the configuration of the external DRCCS connections. These differences can be minimized by applying the DRCCSs with the correct polarity. In general it is recommended to use the internal





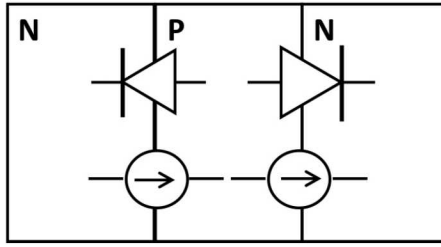
**Figure 23.** Calculated currents with DRCCS external.

**Figure 24.** Calculated currents with DRCCS internal.

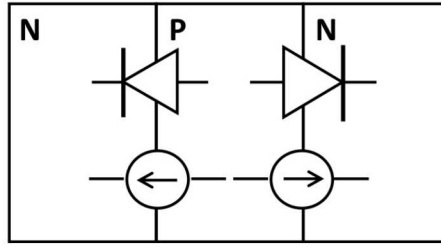
terminals of the device and bypass the terminal resistances in transporting the photo currents into the interior of the device. However, Figures 23 and 24 show that the collector (blue) and emitter (red) currents can be made to exhibit correct polarities during a current pulse depending on the orientation of the DRCCS. The base currents (green) show opposing polarities but the currents are small and the important currents for the calculation of self heating effects are the emitter and collector currents.

Figures 23 and 24 are obtained by orienting the DRCCSs in the configurations shown in Figures 25 and 26. In these diagrams, the box represents an NPN transistor with the emitter, base, and collector shown left to right. The upper row of diode icons represent the diodes formed by the doping of the regions and the lower row of current source icons represent the DRCCSs with the anode corresponding to the tail of the arrow and the cathode corresponding to the head of the arrow. Note that the application of the DRCCS to the internal device terminals have polarities that correspond to the doping of the device whereas the DRCCS applied to the external terminals of the device has polarities that correspond to the major current flow in the transistor. Since the current flow direction can change with bias but the doping direction is invariant, it is recommended that the internal terminal configuration be used in applying the model. However, the results shown in Figures 27 through 29 are obtained with the model exercised in the external terminal configuration since this configuration was used initially.

As a possible circumvention of the limitations of using externally applied DRCCSs, it is not uncommon to model a 3 terminal device with a 2 terminal parasitic photocurrent inducing device connected to 2 of the terminals. This approach



**Figure 25.** Diode and I source external.



**Figure 26.** Diode and I source internal.

to modeling parallels experimental practices because devices are frequently tested in this manner. A typical 3 terminal BJT device may be radiation tested with the emitter and base terminals shorted together electrically and the collector attached to a second terminal. The typical base-collector junction area is much larger than the emitter-base junction area so as a testing and modeling strategy, the emitter-base junction can be ignored as it is the minor photocurrent producer. Adding to this argument is the depth of the depletion region for the base-collector junction is also much larger than the depletion region depth of the emitter-base depletion region. In addition, some devices such as power MOSFETs have the source and the body shorted together as part of fabrication. Thus, the power MOSFET with 3 semiconductor terminals really only uses 2 semiconductor terminals and therefore is another case where a device can be tested and modeled using a 2 terminal parasitic photocurrent device.

Because of the need to account for total power dissipation, it is clear that the total current induced by dose rate must be included in compact models and use of the total currents will more closely approximate the results of TCAD modeling. This total current consists of current from the depletion regions, the two quasi-neutral regions, and the semiconductor regions adjacent to the terminals that do not contribute to current crossing the depletion region but contribute to current at the terminals through diffusion. The first two sources of current are included in the current implementations of the compact photocurrent models but the third source of current is not modeled. Further study is required to determine the relative importances of all current sources (both TCAD and compact models) in order to refine the self heating simulations. This accounting for all currents arising from the dose rate generated carriers may require encoding at the three terminal device code level and it is notable that this is a change to the photocurrent compact mod-



eling methodology that uses independent DRCCSs.

### 7.3.5 Device Compact Model Coupled with Thermal and Photocurrent Models

In order to duplicate behavior and predict the self heating of a compound semiconductor device in a radiation environment, it is essential to synergistically model device operation, heating, cooling, and radiation interaction. A common compact model approach is to superimpose separate models for these effects with single or few shared quantities between models. One goal of this effort is to determine if this approach can reproduce qualitatively the highly nonlinear interactions of radiation and self heating seen in tested devices (and TCAD simulations) and if so, establish the degree of quantitative accuracy. Determining the extent of these capabilities and limiting factors are desired outcomes of this work.

As shown in the cooling term subsection 7.3.6, the superposition of various models into one compact model calculation does produce a physically reasonable result. In this section, the threshold between thermal runaway and return to thermal ambient is discussed by way of demonstrating these behaviors.

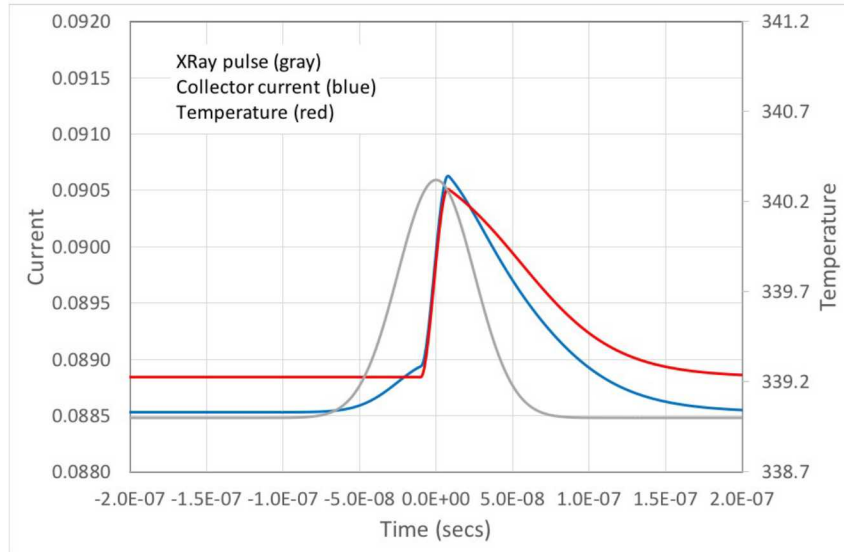
Fig. 27 shows the result of a calculation combining the thermal model and photocurrent model using aligned polarity (Figure 25) photodiodes across both the emitter-base and base-collector junctions. The photocurrent pulse is shown and the collector current response and the temperature rise as calculated by the thermal model is also shown. Note that the temperature rise is measurable but small at less than 2 degrees Kelvin.

It is important to note in the results of the calculation that the temperature rise (red curve) follows and lags the collector current rise (blue curve) in the model by a considerable amount of time ( $\sim 40$ ns). The temperature is defined in the model as dependent upon the emitter current (Equation 8) and the emitter current (not shown) rises at the same time as the temperature which is consistent. The lag time between the start of the emitter current rise and the collector current rise is due to the emitter current consisting of the sum of the base and collector currents. This aspect of the temperature definition is part of the current and future thermal model research.

The rise in temperature and collector current shown in Fig. 27 is rapid with respect to the pulse time characteristics, but is not instantaneous. This rise time may

be determined in the model by internal capacitances tied to the terminals. This rise and the interaction with the device thermal run away is a component of the modeling that may require calibration as discussed in the thermal mass discussion above. From the Figure, it is clear that both the location in time of the thermal rise and the rate of the rise have the same importance as the magnitude of the rise.

The compact models exercised in this fashion are non calibrated and of limited



**Figure 27.** Simulated photocurrent pulse (gray) and the device response (collector current blue and temperature red). The thermal and photocurrent models are employed in this calculation. In this case, the device responds and then returns to nominal conditions after the pulse peak occurs.

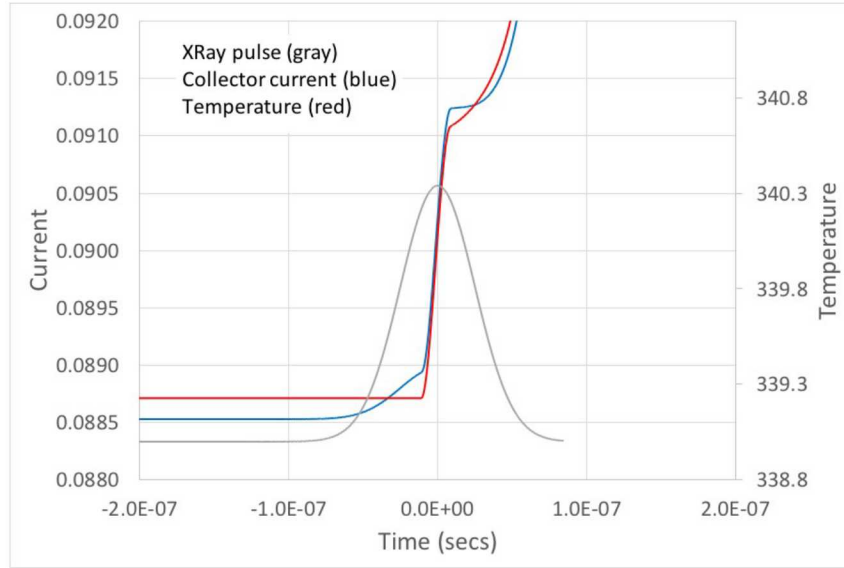
use as far as determining threshold magnitudes of dose rates and biases for thermal run away. Nevertheless, with the models at this stage, it is instructive to accumulate information on levels of critical currents where the device will no longer cool to ambient temperatures as shown in this case.

Fig. 28 shows an additional result of a thermal runaway calculation with the thermal and photocurrent models superimposed. Although the qualitative behavior is quite different, this scenario is very close to the biasing and dose rate as the scenario in Fig 27, with the exception of a slightly higher dose rate. The small increase in dose rate provides sufficient extra charge carriers so that the joule heating is increased and the overall behavior is different.

It is of interest to examine the relative time occurrences of device responses as in the previous scenario. Again, the temperature rise and the emitter current

rise lags the increase in collector current in time. Also the initial peak of collector current and temperature follows the midpoint of the photocurrent pulse by a small ( $< 10ns$ ) time period. However, this initial peak is followed by a short duration plateau and then proceeds to a runaway conditions. The magnitudes of the final current and temperature increases are much larger than the increases due only to carrier generation in the photocurrent pulse.

Because of the runaway conditions, the calculation is fragile and does not



**Figure 28.** Device response to a photocurrent pulse at a slightly higher dose rate than in Fig. 27. In this case, the device responds to the pulse and momentarily ceases heating after the peak of the pulse passes. However, the heat from the current increase is above the threshold for runaway and the device currents and temperature proceed to runaway.

proceed significantly beyond the 50ns point. Both the currents and temperature do experience large gains up to the point of calculation failure with no recovery predicted by the model.

This result with simulations that include only the thermal and photocurrent models is a promising start for compact modeling but lacks some of the important physical features found in the TCAD modeling results. The difference between Figs. 27 and 28 is a sharp transition between scenarios. A real physical system is expected to exhibit hybrid behaviors in a range of dose rates about the threshold dose rate. In fact, this is the behavior predicted by the TCAD modeling, and these

predictions can be analyzed to determine SOA boundaries. At a minimum, the compact model should be able to represent these same behaviors and at a more refined level, be able to describe them to achieve a predictive capability.

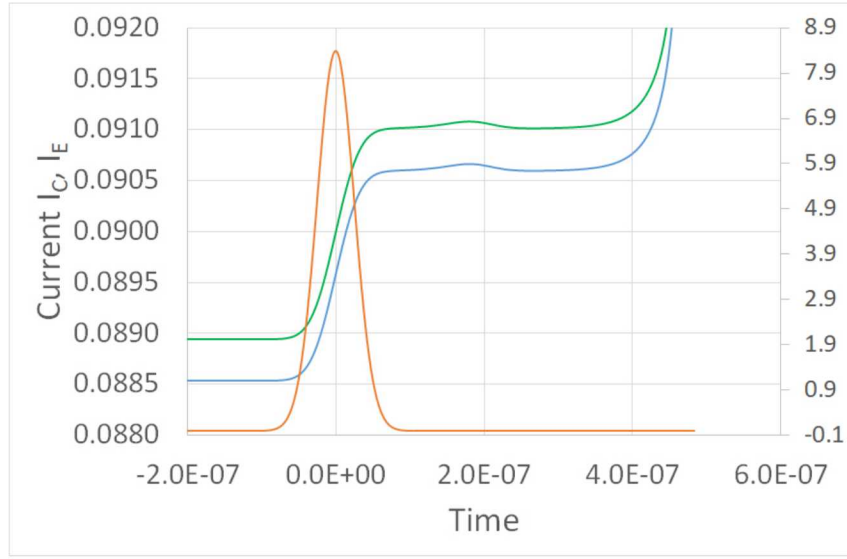
### 7.3.6 Delayed Runaway with a Cooling Term

Radiation test results with individual MOSFETs, HBTs, and HBTs embedded in systems suggest that within a range of radiation magnitudes, the trajectory to thermal runaway is not immediate in time and not necessarily monotonic. TCAD simulations confirm that cooling effects potentially significantly extend the time constants associated with thermal runaway. This implies that a complete description of device thermal behaviors must include independent cooling term(s) to account for the separate and independent sources of heating and cooling. In the compact modeling work, experiments with a cooling term as a function of time have demonstrated the ability to control and delay thermal runaway behavior. It is planned to extend these experiments to also include a dependence on temperature for this term.

Fig. 29 shows the simulated (with Xyce compact models including a cooling term) time dependence of collector and emitter currents during and after the radiation pulse. The dose rate pulse (shown in orange) begins at approximately -80ns and lasts until +80ns. The FWHM of this pulse is 60ns. Sometime after the beginning of the pulse, the collector and emitter currents rise and reach a plateau. From previous simulations shown in section 7.3.5, currents higher than this plateau lead immediately to thermal runaway in the simulation. Because of the cooling term, the simulated currents stay roughly at the level of the plateau for several hundred nano seconds and then proceed to runaway after the cooling term has dropped in magnitude. The time dependent shape of the cooling term in this case is a simple Gaussian function. It is anticipated (and will be shown with Equation 17) that a more complicated cooling term can extend the time before the calculation runs away and moreover duplicate the runaway behavior of the TCAD simulations.

These results are obtained with the DRCCSs applied to the external terminals of the transistor, therefore the aligned DRCCS (Figure 25) configuration is used. This is the reason that the photocurrent pulse does not appear in the tabulated collector and emitter currents since they are calculated internal to the device.





**Figure 29.** Time dependence of collector (blue) and emitter (green) currents in a Xyce simulation using a thermal model with cooling term in conjunction with a photocurrent model. Photocurrent pulse shown in orange. Refer to the model coupling section for a complete discussion of the coupling details.

The radiation level in Fig. 29 is sufficient to send the device into runaway immediately without the cooling term. At lower radiation levels, the simulation may exist on the threshold of runaway. In this case, the cooling term may cause the simulated currents to rise to a plateau and then fall to levels prior to the radiation pulse. With the correct form and magnitude of the cooling term, this decay to ambient temperatures can be tailored to match the higher fidelity TCAD results.

As a demonstration of the first assertion, an artificial function (Equation 17) was created to duplicate the situation of a dose rate pulse with sufficient magnitude to drive the transistor to overheat moderated with a cooling pulse to delay thermal run away. This is similar to the scenario in Figure 29 except that this simulation utilizes the DRCCSs applied to the interior terminals of the device and thus reflects the pulse in the collector current. The artificial function is built using a basis set of three Gaussian pulses of varying magnitudes and sigmas. In turn, these functions could be constructed from more fundamental functions such as sines and cosines.

$$Pulse(t)_{photo} - F(t)_{cooling} = PH_1 \cdot e^{-(\sigma_1 \cdot t^2)} + PH_2 \cdot e^{-(\sigma_2 \cdot t^2)} + PH_3 \cdot e^{-(\sigma_3 \cdot t^2)} \quad (17)$$

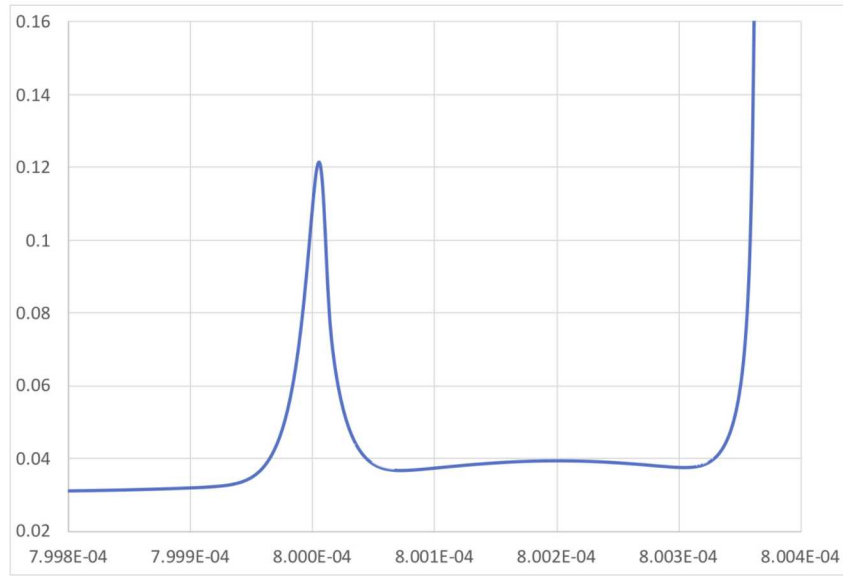
In this expression the coefficients are labeled PH for photo pulses.

The results of this artificial function applied to a simulation configuration with two external DRCCSs connected to the internal terminals of a transistor are shown in Figure 30. The compact model collector current behavior shows the effects of the dose rate generated current followed by a drop to a current level reflecting the pre pulse current plus additional currents due to rise in temperature. This reaction is followed by self heating, cooling, and then thermal runaway in the response of the collector current.

It should be noted that this artificial function was applied as a direct substitution of the power dissipation term in the thermal model rather than in the source term of the photo current. The artificial function is applied at the level of Equation 10 rather than influencing the currents in the power dissipation term. In contrast, the scenario in Fig. 29 is constructed by utilizing both the power dissipation term and the modification of the currents generated by the dose rate source term. This course of study was dictated by time limitations to the overall project and will be followed by a more comprehensive study conducted with realistic dose rate pulses and cooling terms applied to the respective models.

The similarity of Figure 30 to the TCAD results shown in Figure 14 is indicative of the potential of the compact model contributions to this field of study. As of the publication of this report (Fall 2019), the compact modeling is in a development stage and is slated for refinement in follow-on years.



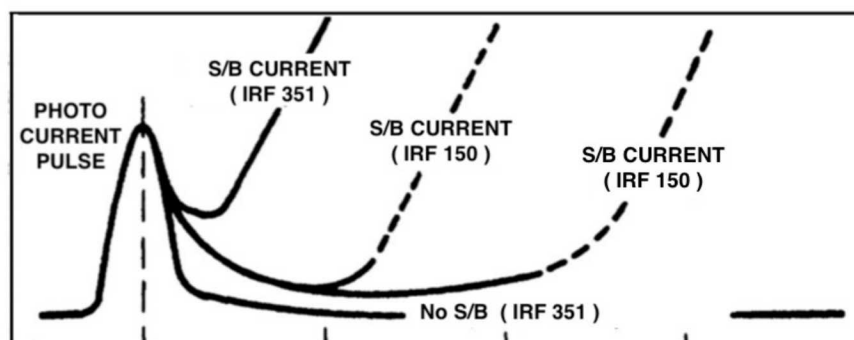


**Figure 30.** Time dependence of collector current in a Xyce simulation using a thermal model, photocurrent model, and a synthetic function to represent both heating and cooling effects. This figure differs from Figure 29 in the reflection of the photocurrent pulse in the collector current.

## 8 Experimental Corroboration of Simulation Predicted Behaviors

In the reference from Volmerange and Witteles [11] photocurrent burnout in power MOS devices resulting from secondary breakdown from the source to the drain is shown in Fig. 31. The photocurrent pulses in these failures were 45ns in duration. Two different types of MOS HEXFET devices were tested and both exhibited failures.

The secondary breakdown current in this situation can be considered equivalent to the collector breakdown current explored in this report with the HBT devices. The duration of the delayed secondary breakdowns shown in this data is on the order of  $\mu\text{secs}$  which is roughly the same timescales exhibited by the HBTs in the simulations in this work. Therefore this work is the direct experimental predecessor work to the current work. The existence of these experimental results



**Figure 31.** From [11] Figure 6. Thermal run away induced by photocurrent pulse in Hex power MOSFETS. The vertical axis is current and each tickmark on the horizontal axis is 1  $\mu\text{sec}$ .

motivates similar investigations with the current generation HBT devices studied in this report. Test campaigns have taken place in 2019 and the data corroborates the simulation predictions at early times during and immediately after the pulse. This work is summarized in [34]. The results are not reported here in order to allow wide distribution of this report.

## 9 Conclusions and Future Work

There are many additional TCAD calculations that could be performed on this system and many issues can be addressed with these calculations. Correspondingly, there are many additions that can be made to the compact models to incorporate the relevant physics as identified by the TCAD calculations.

- TCAD - develop restart capability for lengthy calculations
- TCAD - explore additional parallelization techniques to increase calculation speed
- TCAD - continue calculations to explore SOA boundary
- TCAD - develop temperature dependent contact resistance
- TCAD - reproduce current and future results in SNL Charon tool.
- compact model - refine cooling term for higher fidelity to TCAD calculations
- compact model - explore thermal capacitance-delay term and incorporate into thermal mass term
- compact model - recast cooling and delay terms in formulations of physical models
- compact model - enhance portability of the modeling approach to other circuit solvers.

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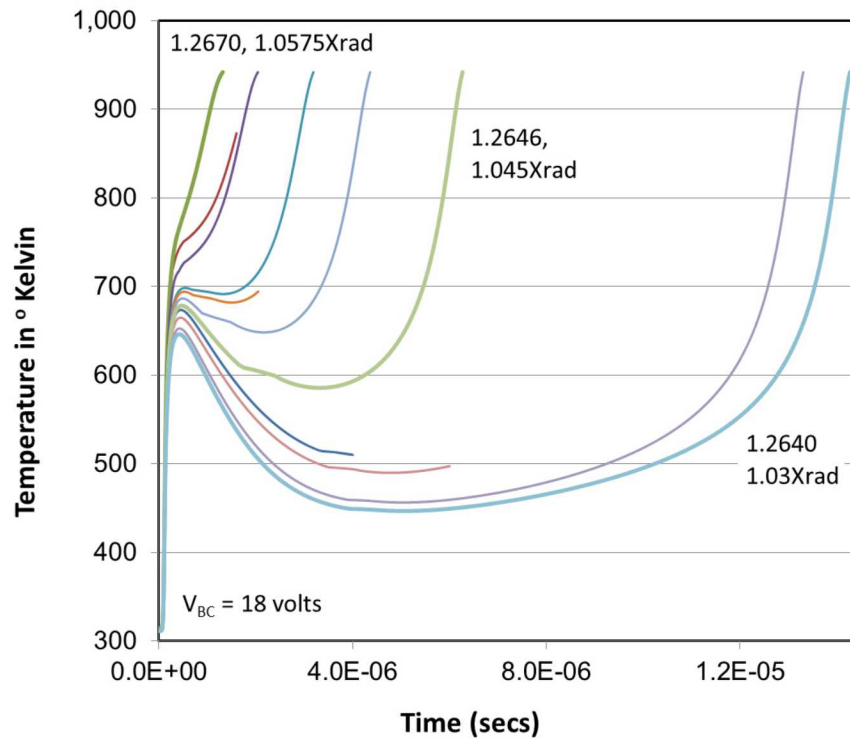
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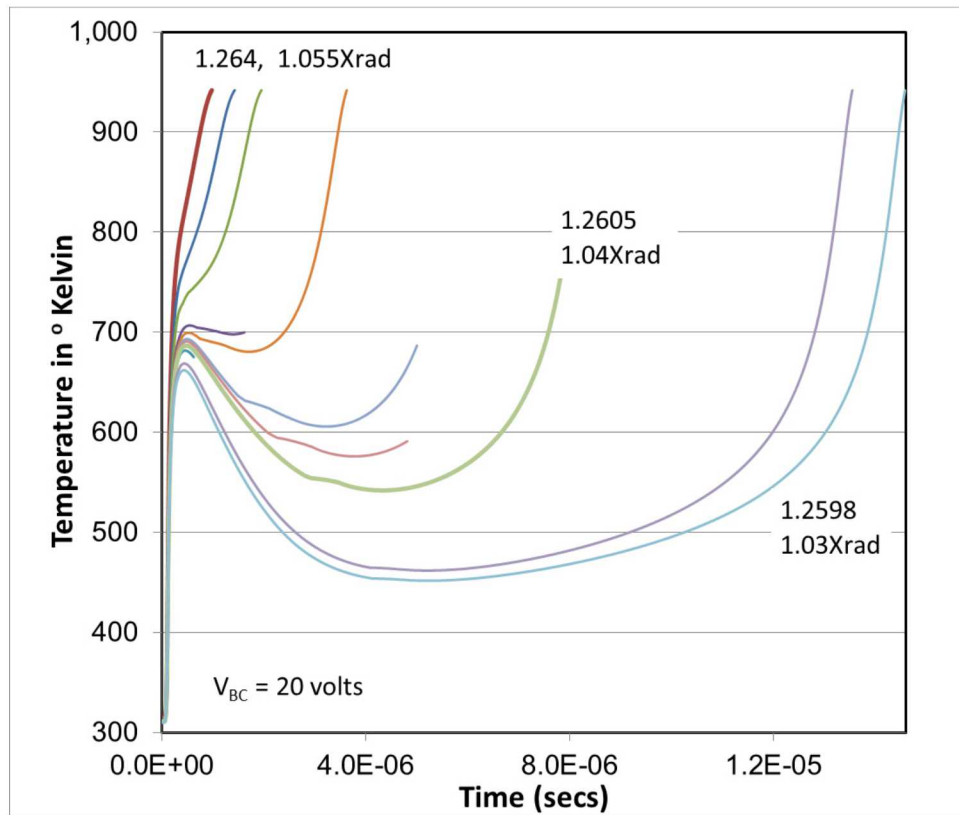
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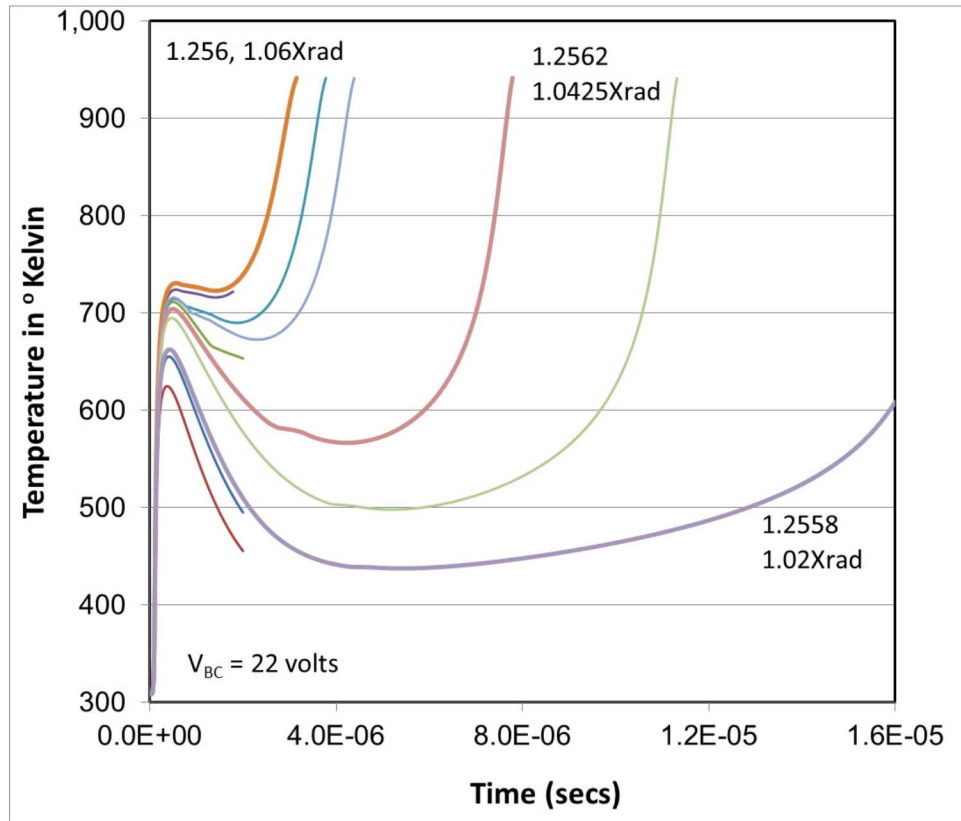
## A Additional TCAD temperature versus time results with dense mesh: Various $V_{BC}$



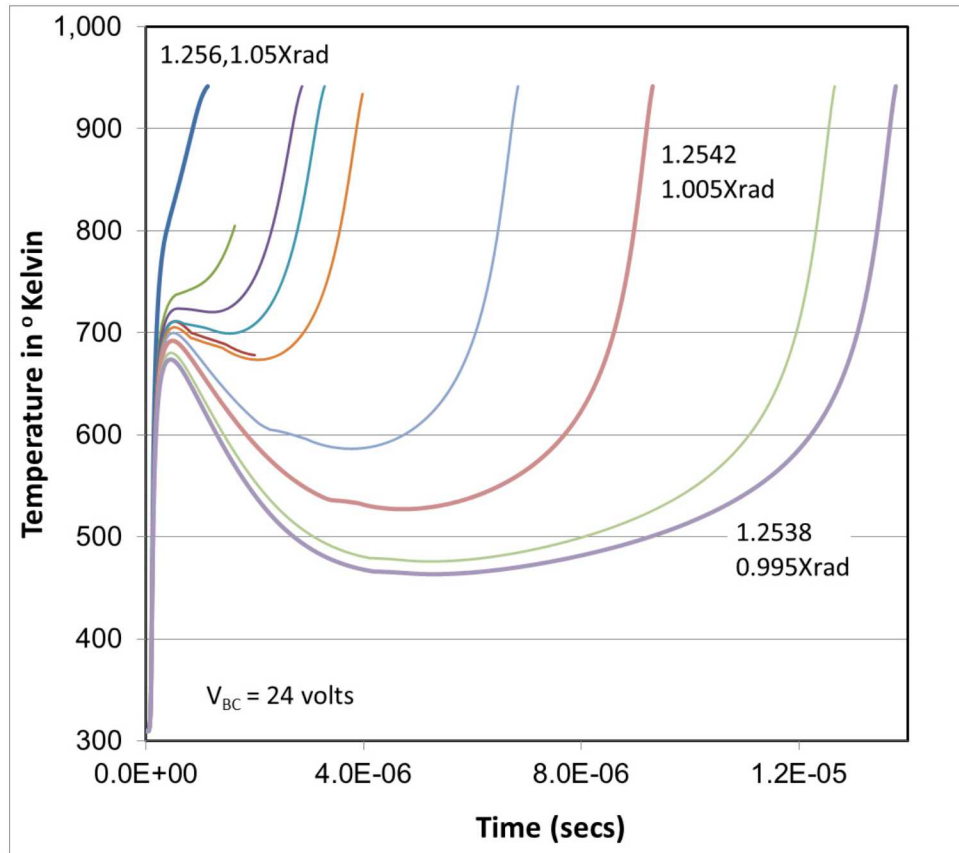
**Figure A.1.** TCAD simulations showing temperature versus time for various  $V_{BE}$  and dose rate values, all with  $V_{BC}=18$ .



**Figure A.2.** TCAD simulations showing temperature versus time for various  $V_{BE}$  and dose rate values, all with  $V_{BC}=20$ .

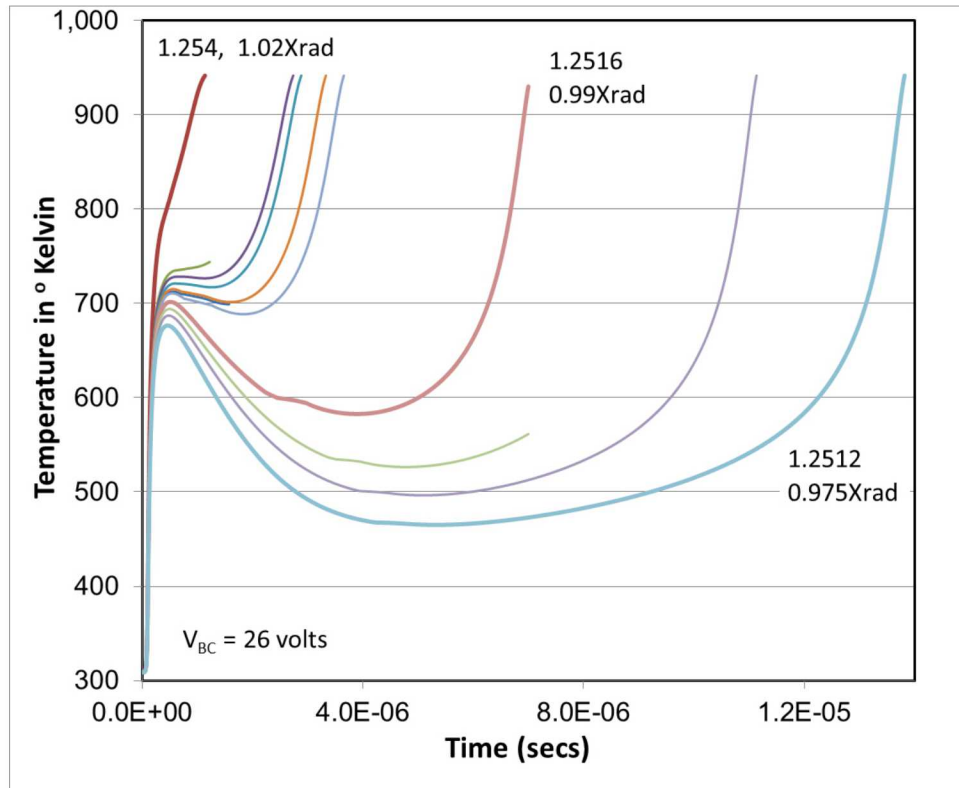


**Figure A.3.** TCAD simulations showing temperature versus time for various  $V_{BE}$  and dose rate values, all with  $V_{BC}=22$ .



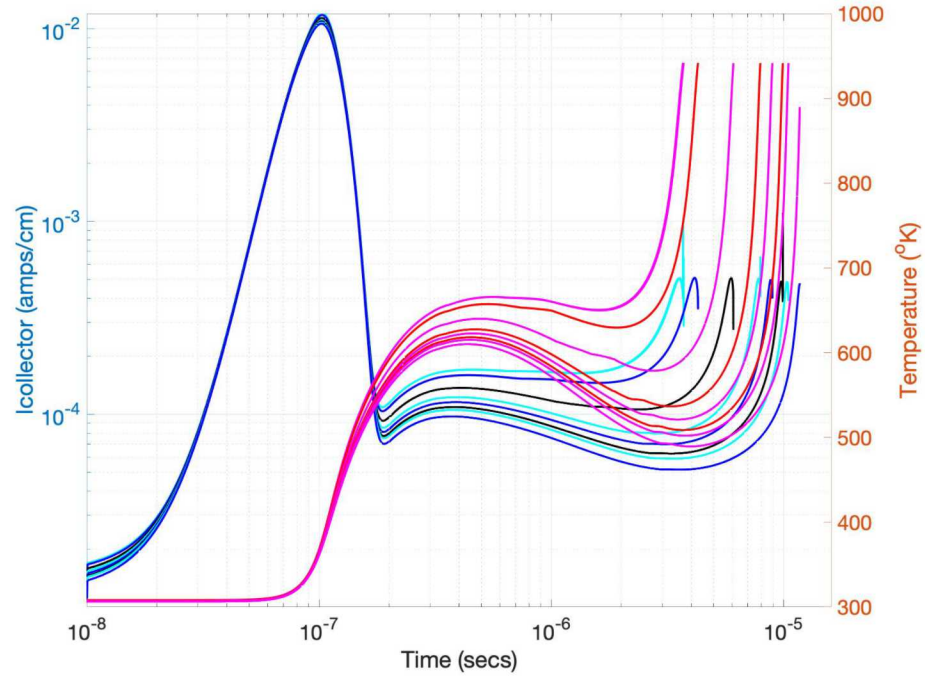
**Figure A.4.** TCAD simulations showing temperature versus time for various  $V_{BE}$  and dose rate values, all with  $V_{BC}=24$ .





**Figure A.5.** TCAD simulations showing temperature versus time for various  $V_{BE}$  and dose rate values, all with  $V_{BC}=26$ .

## B Additional TCAD temperature versus time results with coarse mesh: $V_{BC}=28$



**Figure B.6.** TCAD simulations showing collector currents (blue, cyan, black) and temperature (red, magenta) versus time for various  $V_{BE}$  and doserate values, all with  $V_{BC}=28$ .

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