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Xyce: Open Source Simulation for Large-Scale Circuits

Jason Verley, Eric Keiter, Tom Russo, Heidi Thornquist, Ting Mei, Pete Sholander and Aadithya Karthik

Introduction

Analog circuit simulation has historically been an important capability in the design and verification of Analog and Mixed Signal systems. With the advent of digitally-assisted analog/RF, and System On a Chip (SOC) technologies, the need for fast and accurate analog simulation has increased. While FastSpice methods allow for large-scale simulations, they sacrifice the fidelity of "true SPICE" simulation.

Xyce is a SPICE-compatible analog simulator designed for the accurate simulation of a wide range of circuit sizes, ranging from a few elements to millions of components. It achieves this scaling through Message Passing Parallelism (the method of choice in High Performance Computing). Recent and near-term development in Xyce is focused on compatibility with commercial tools, the simulation of modern technology nodes, frequency-domain simulations, and improved performance.

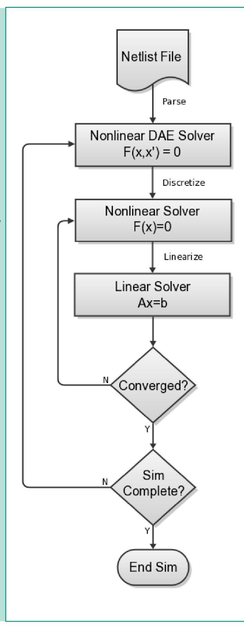
Analog Simulation

Traditional analog circuit simulators, such as SPICE, solve a coupled set of nonlinear differential-algebraic equations (DAEs):

$$f(x(t)) + \frac{d}{dt} q(x(t)) - b(t) = 0.$$

The solution approach follows the flow on the right. The *nonlinear solver* evaluates the output of each device (typically current) based on an input (typically nodal voltages). A Newton iteration step is taken, where the *linear solver* solves the resulting matrix equation. This process is continued until convergence, and the next step in the analysis is taken.

The traditional approaches do not scale well beyond tens of thousands of unknowns due to the reliance on a large single matrix that is treated by *direct matrix solvers*. As a result, the analog runtime scales super-linearly with increasing circuit size. For RF simulation, the scalability can be worse than for transient, because harmonic balance (HB) analysis generates larger, less sparse matrices.



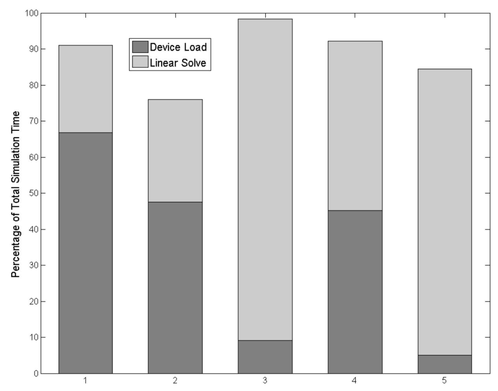
Xyce Parallel Simulation

Xyce has been designed to use distributed memory parallelism to address the scalability issues inherent to solving large nonlinear DAEs. From the beginning, the focus of Xyce development has been to provide scalable, numerically accurate analog simulation for large-scale circuits through the development and improvement of the algorithms at the core of SPICE-style simulation. Furthermore, Xyce has been designed to have a modular framework for integrating device models and developing state-of-the-art continuation algorithms, analysis methods, preconditioned linear solvers, and parallel partitioning techniques.

For optimal parallel execution speedup, Xyce can parallelize both the device evaluation and the linear system solve. The two modes can be invoked together or separately. In smaller problems, the device evaluation tends to dominate; but as the problem size gets larger, the matrix solve dominates the solve time. For large problems, Xyce uses specialized matrix preconditioners and iterative linear solvers for good scalability. The linear system solve is even more important in the frequency-domain due to the much larger matrices.

CIRCUITS: MATRIX SIZE(N), CAPACITORS(C), MOSFETS(M), RESISTORS(R), VOLTAGE SOURCES(V), DIODES (D).

Circuit	N	C	M	R	V	D
ckt1	15622	7507	10173	11057	29	0
ckt2	25187	0	71097	0	264	0
ckt3	116247	52552	69085	76079	137	0
ckt4	688838	93	222481	176	75	291761
ckt5	1944792	400234	211486	795827	36100	199992



References

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Xyce Capabilities

- Typical capabilities: DC, transient, AC, noise, expressions, functions, parameterizations…
- Analog Behavioral Modeling
- Post-processing:
  - Fourier transform of transient output (.FOUR)
  - Post-simulation calculation of simulation metrics (.MEASURE)
- Output: Text Files (tab or comma delimited), Probe, Gnuplot, TecPlot, RAW
- Harmonic Balance Analysis (.HB)
  - Steady state solution of nonlinear circuits in the frequency domain
- Random Sampling Analysis
  - Executes the primary analysis (.DC, .AC, .TRAN, etc.) inside a loop over randomly distributed parameters.
- Sensitivities (DC or Transient)
  - Computes sensitivities for a user-specified objective function with respect to a user-specified list of circuit parameters ($\partial O/\partial p$…); e.g., an output voltage's dependence on a capacitance.

Xyce Release 6.10

- Available soon: `https://xyce.sandia.gov`

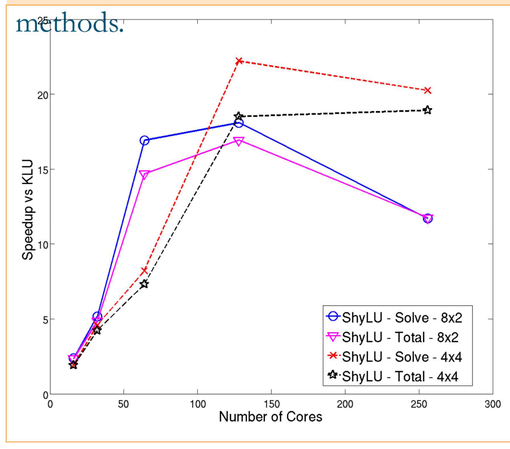
Open Source

- Xyce is released under the Gnu Public License, Version 3

Scaling Example

The default solver in Xyce for serial and small parallel simulations is KLU, a serial, sparse direct solver. The table demonstrates the robustness of KLU for very large circuits compared to other sparse direct solvers; "ckt5" has **1.6 million devices** with **1.9 million unknowns**.

The plot demonstrates a strong scaling study of a parallel solver, called ShyLU, that is under active development. ShyLU is a hybrid solver in both the parallel programming sense—using MPI and threads—and in the mathematical sense—using features from direct and iterative methods. The speedup in the simulation of "ckt5" for different computational configurations is plotted on the left. The optimal configuration in this case uses 128 cores, which results in a **16–23×** speedup.



COMPARISON OF TOTAL LINEAR SOLVE TIME (SEC.) OF VARIOUS SPARSE DIRECT SOLVERS FOR OUR TEST CIRCUITS; (-) INDICATES SIMULATION FAILED TO COMPLETE.

	ckt1	ckt2	ckt3	ckt4	ckt5
KLU	**80.8**	162.2	9381.3	7060.8	**14222.7**
PARDISO (16)	128.6	**105.3**	**715.0**	**6690.5**	-
SuperLU	-	10294.1	-	-	72176.8
SuperLU_Dist (16)	-	-	-	-	-

Near-Term Development Focus

Compatibility with Commercial Simulators

- Working on both netlist compatibility (easier) and feature compatibility
- PSPICE netlist conversion tool (Sandia-only at the moment)
- HSPICE compatibility: under development (netlist and feature)
- Spectre compatibility: targeted for future development

PDK Support

- Strongly tied to simulator compatibility (HSPICE is the focus)
- Initially targeting Global Foundries 14 nm

Mixed-signal support (Verilog via VPI, VHDL via VHPI)

- Initial linking to a discrete event simulator for circuits based on asynchronous logic

S-parameter analysis implementation

Performance Improvements

- Making speed improvements to Industry Standard Compact Models, particularly BSIM-CMG. This will initially be done by improving the Xyce Verilog-A compiler, which is based on ADMS.
- Improving solver performance for circuits of interest, with a focus on improving the parallel solvers, and better selection of default simulation parameters.

Build system moving to CMake

We wish to acknowledge the Advanced Simulation and Computing (ASC) Project under the National Nuclear and Security Administration (NNSA), and the DARPA Posh Open Source Hardware (POSH) Project for funding the development of Xyce.

Xyce™ PARALLEL ELECTRONIC SIMULATOR

U.S. DEPARTMENT OF ENERGY
NNSA National Nuclear Security Administration

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