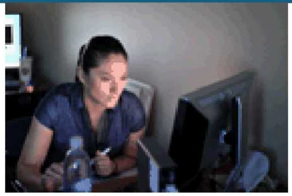
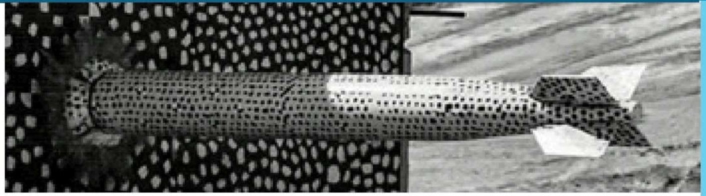
SAND2018-10584PE

Parallel Simulation Capabilities in Xyce





PRESENTED BY

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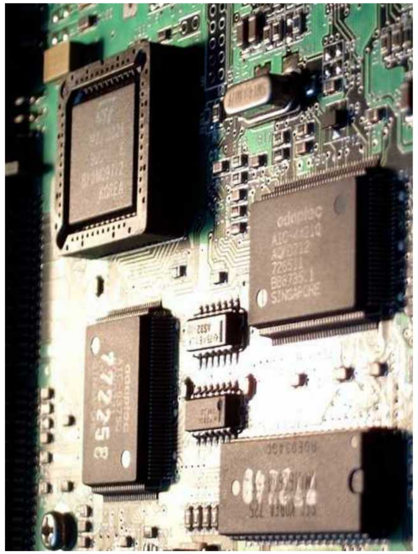
Xyce Circuit Simulation Challenges

- Need to efficiently and seamlessly simulate circuits that have a wide range of devices (10-10^6) and complexity
  - Advanced preconditioning techniques for iterative solvers
    - NW Design teams (5200, 2600)
  - Must support direct solvers for smaller circuits
    - ASC Enhanced Surveillance (9434)
- Stockpile-focused simulation efforts inspired many of the past and current advancements for circuit simulation
- Now DARPA will push that simulation boundary further …



RHP Multiplier (2000) → CMOS6 PA1 (2003) → CMOS7 PA2 (2006) → CMOS7 Eiger (2008) → CMOS7 Shasta 2x2 (2011)

RHP Multiplier (2000)	CMOS6 PA1 (2003)	CMOS7 PA2 (2006)	CMOS7 Eiger (2008)	CMOS7 Shasta 2x2 (2011)
~25K unknowns	~600K unknowns*	~680K unknowns	~430K unknowns	~2M unknowns

Parallel Circuit Simulation Challenges

Analog simulation models network(s) of devices coupled via Kirchoff's current and voltage laws

$$f(x(t)) + \frac{dq(x(t))}{dt} = b(t)$$

Network Connectivity

- Hierarchical structure rather than spatial topology
- Densely connected nodes: O(n)

Badly Scaled DAEs

- Compact models designed by engineers, not numerical analysts!
- Steady-state (DCOP) matrices are often ill-conditioned

Non-Symmetric

- Not elliptic and/or globally SPD

Load Balancing / Partitioning

- Balancing cost of loading Jacobian values unrelated to matrix partitioning for solves

Xyce Simulation Flow

Parsing

- Convert netlist file syntax to equivalent devices and network/circuit connectivity
- Distribute devices over multiple processors
- Determine global ordering and communication

Device Evaluation

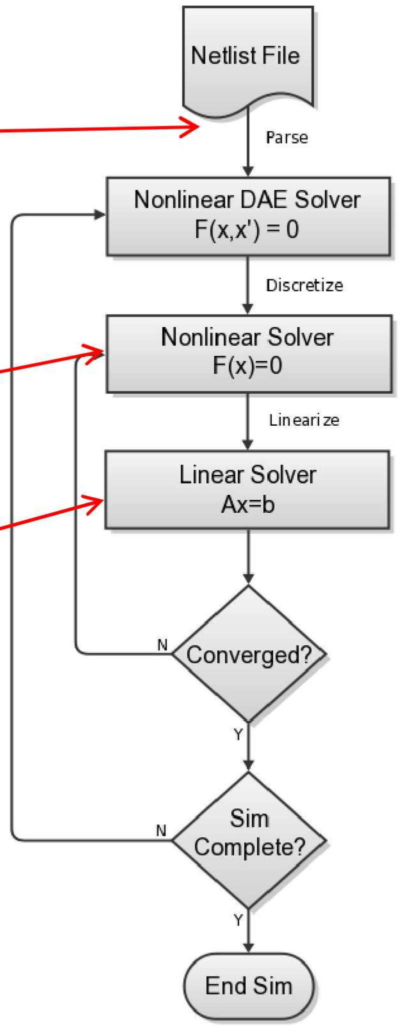
- Loop through all devices for state evaluation and matrix loading

Linear Solve

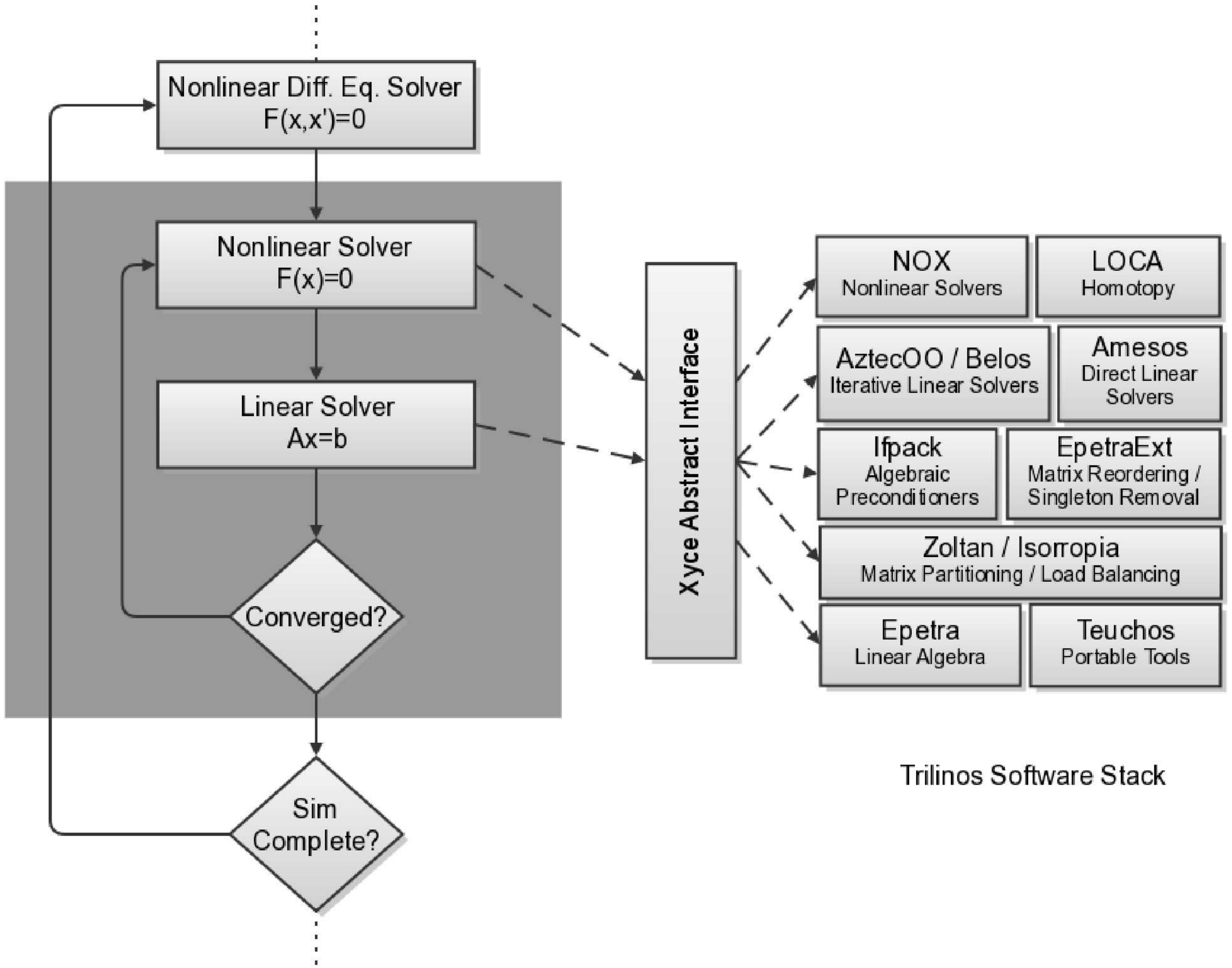
- Sparse linear algebra and solvers used to solve linearized system

Advanced Analysis Methods

- Sampling: Monte Carlo, LHS (DAKOTA)



Xyce Simulation Flow - Trilinos Solver Stack



Trilinos Software Stack

- Parallel linear algebra
- Advanced partitioning
- Parallel solvers
- Preconditioners
- Nonlinear methods (homotopy, continuation)
- Automatic Differentiation
- Stochastic UQ

Past Simulation Advancements (Shasta 2x2)

Removed inefficiencies that prevented parasitic extracted (pex) netlist parsing

- Multiple data storage
- Inefficient searches of long subcircuit lines

Addressed inefficiencies in topology setup

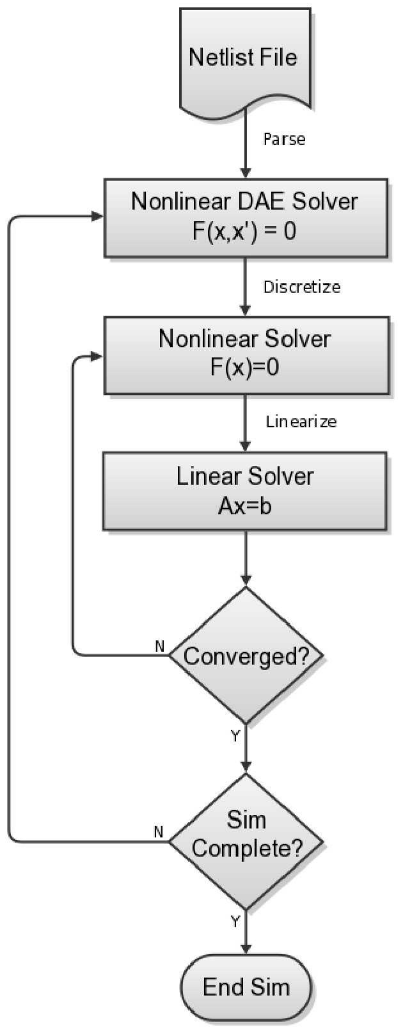
- Preprocess strange connectivity given by extraction tools, where resistors have zero resistance (supernoding)

```
R1 a b 0
```

- Rewrite breadth-first traversal ordering for the graph

Developed new scalable solver approach based on unique matrix structure

- Available preconditioned linear solvers were ineffective for enabling the simulation of this circuit



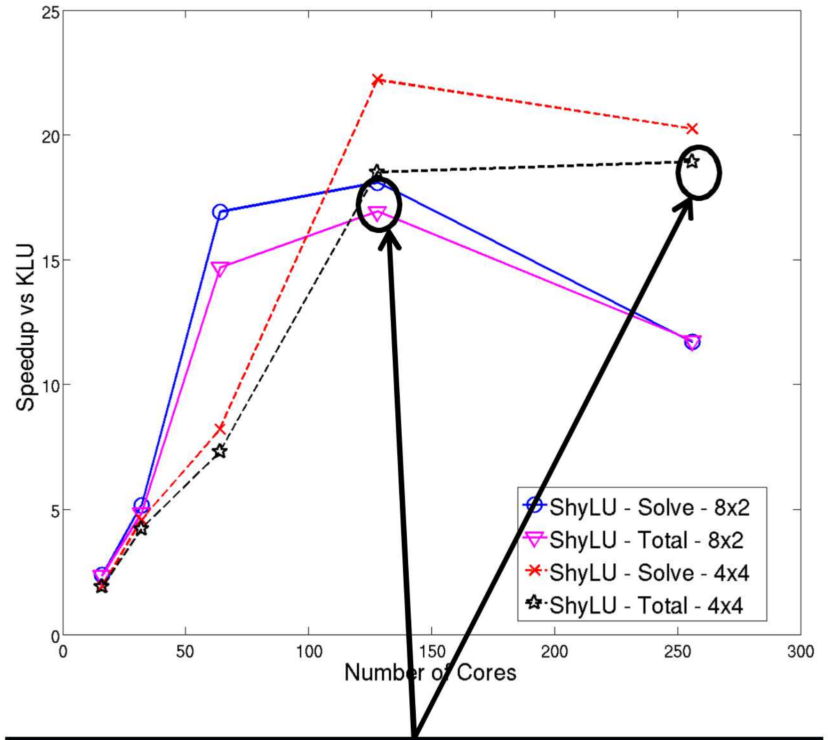
New Linear Solver Achieves 19x Speedup for Shasta 2x2 Simulation

ShyLU is a sparse linear solver framework, based on Schur complements (*S. Rajamanickam, E. Boman, M. Heroux*)

- Incorporates both direct and iterative methods
- Coarse-scale (multi-processor) and fine-scale (multi-threaded) parallelism
- Can be a subdomain solver / preconditioner or stand-alone linear solver

Shasta 2x2 ASIC: 1.6M total devices, ~ 2M unknowns:

- Xyce w/ KLU solver takes ~ **2 weeks**, w/ ShyLU solver takes ~ **1 day**
- ShyLU: Optimal # partitions = 64; number of rows in S = 1854 (4 MPI procs)



Strong scaling of Xyce's simulation time and ShyLU linear solve time for different configurations of MPI Tasks X Threads per node on TLCC

Lessons Learned from Shasta

- "Optimal" solver settings can be different for normal vs. abnormal environments.
- Shasta vs. Eiger discussion illuminated need for a linear solver that is efficient on Eiger matrices.
- Development of new algorithmic technology can take a significant amount of time.
- Conversations with designers about what they are trying to learn can help guide our research directions.

Simulation Advancements due to Shasta

Retaining hierarchical information about the circuit in the parsing and topology layers

- Enables detection of parasitic blocks (Shasta 2x2 w/pex has 104419 unique subckts)
- Allows tailored solution/simulation strategies

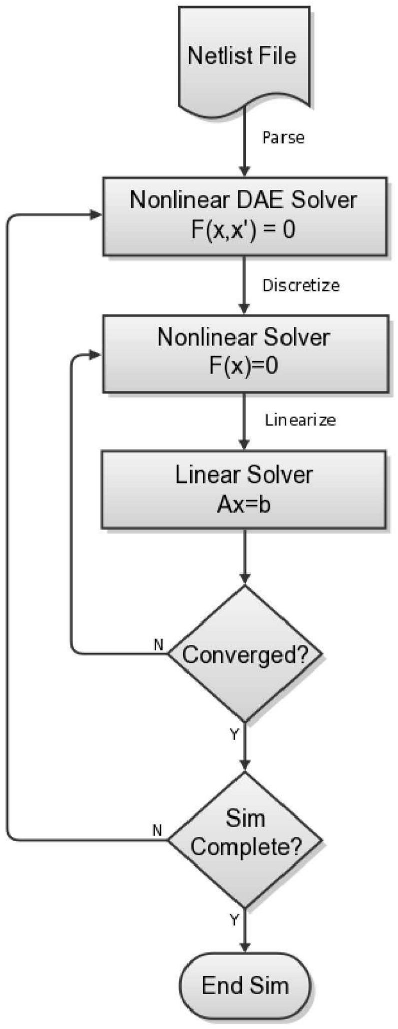
Addressing more inefficiencies in the parsing and topology layers

- A lot of excessive computation and memory usage has been eliminated
- Inefficient uses of common data containers have been eliminated

Improved time-integration methods, tailored for circuit simulation

In situ data measurement capabilities

- Locate extrema in voltage/current nodes, calculate integrals/derivatives, locate transient events, …



Next Generation Xyce Simulation

Requires a combination of programming paradigms / models

- Re-evaluate simulation structure for intra-node parallelism

Parsing

- Significant serial component
- Architecture-aware topological choices should be made for device partitioning and linear solver

Device Evaluation

- Devices can have a very different “costs” for evaluation
- Organize device evaluations for vectorization or threading
- Computational kernels to address architecture differences

Linear Solve

- Solvers that employ hybrid parallelism (ShyLU/Amesos2)
- Linear algebra that targets node-level parallelism