

Outlook for Si Detectors



PRESENTED BY

Quinn Looker

hCMOS Workshop

Sandia NM 1/17/19

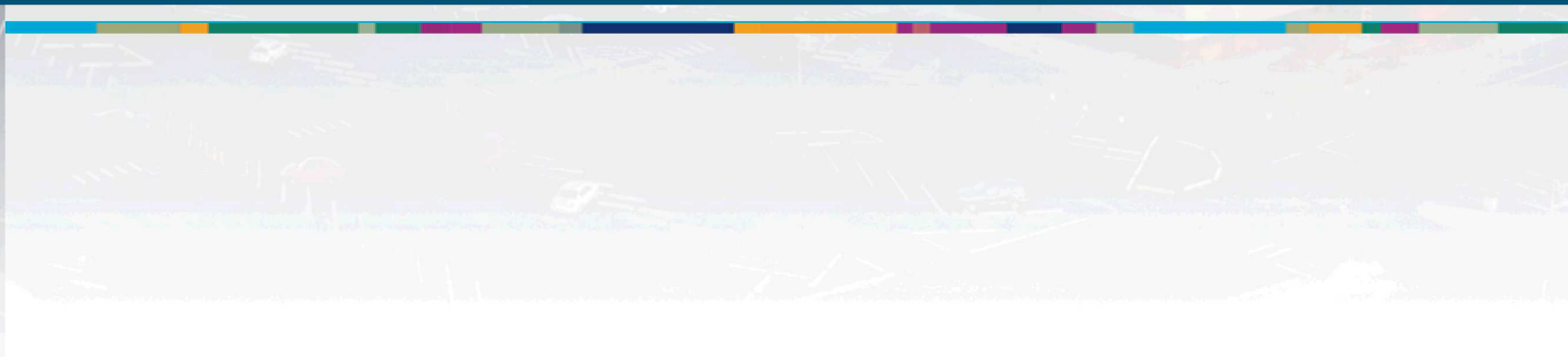
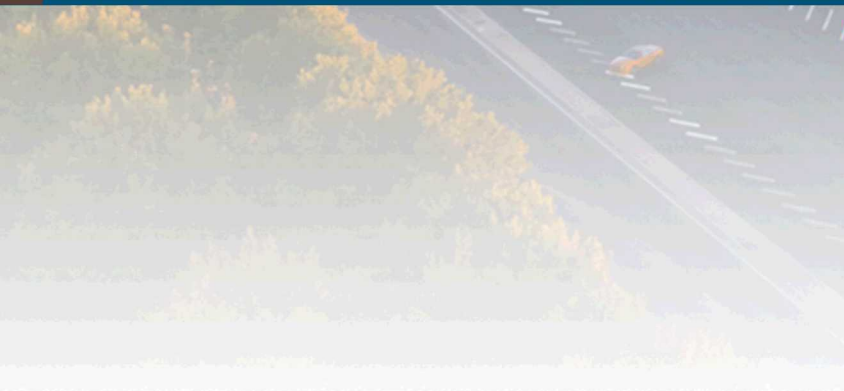


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SAND



Base Diode Design Complexity Reduction

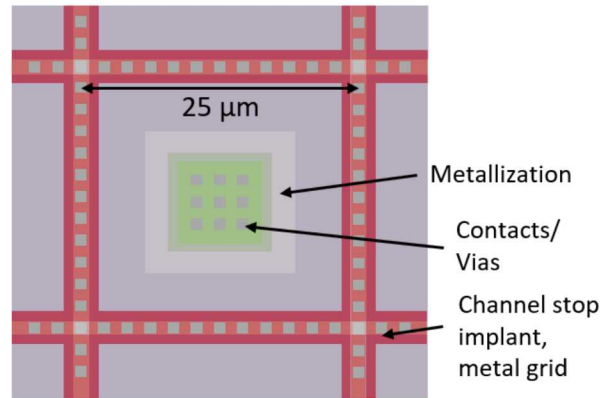


Diode Array Fabrication Changes

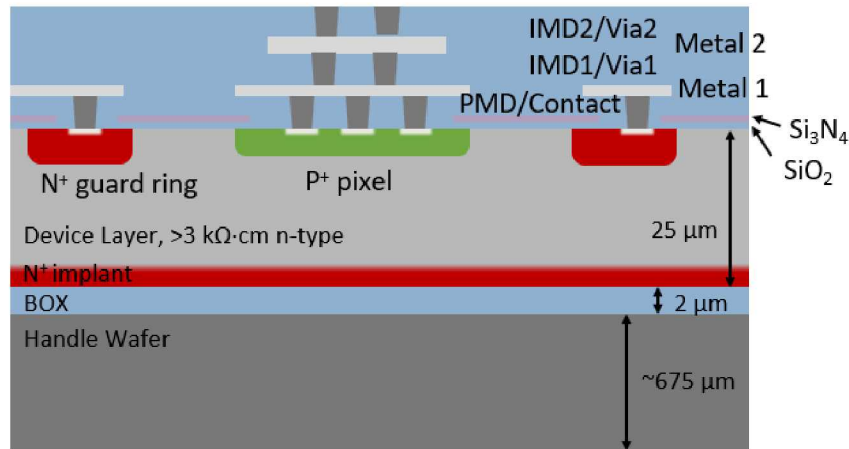
Detector Wafer, Single-pixel

Today's Pixel Design

Pixel
Plan
View

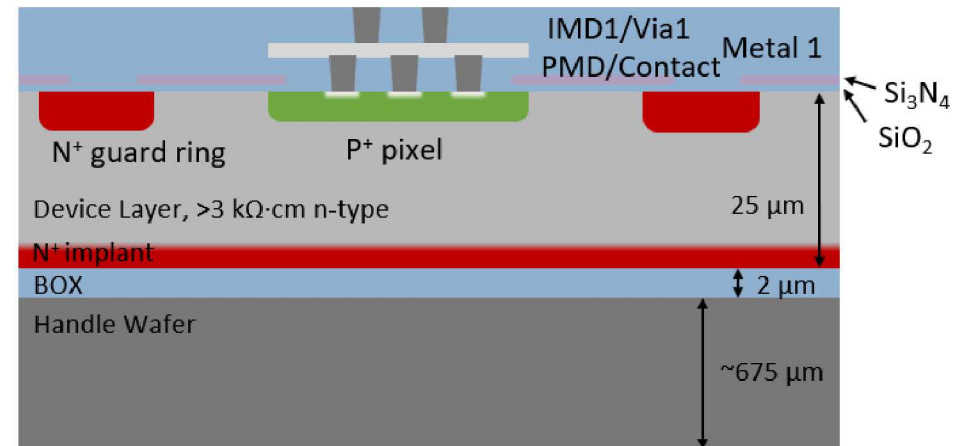
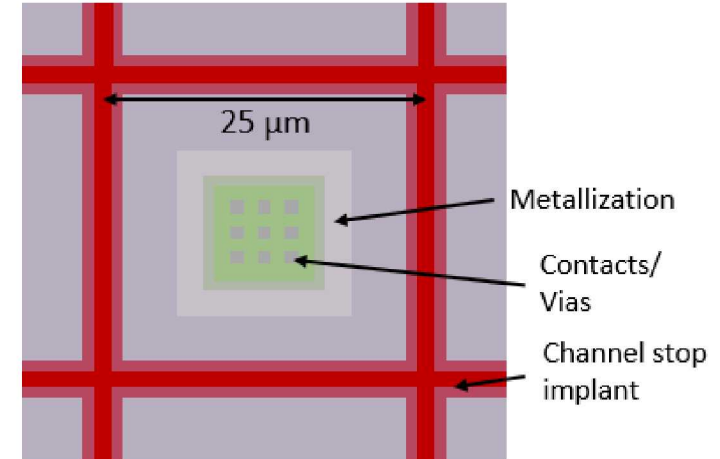


Cross
Section
View



Simplified Pixel Design

Pixel
Plan
View



Simpler Pixel Design

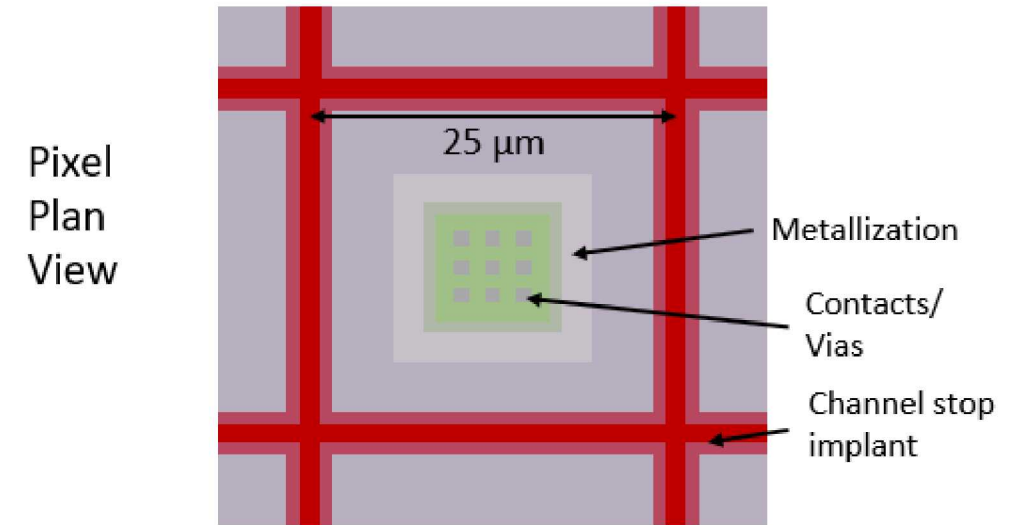
- Eliminate contacts and metal grid to channel stop
 - Lose ability to ROIC-side bias
 - Reduces mask complexity, potential short paths
- Eliminate M2/V2 stack
 - Fewer routing options available (not needed if ch stop metal not present)
 - Eliminates 45 steps, 2 mask layers

Base plan: 233 steps Modified plan: 188 steps
20% cost reduction?

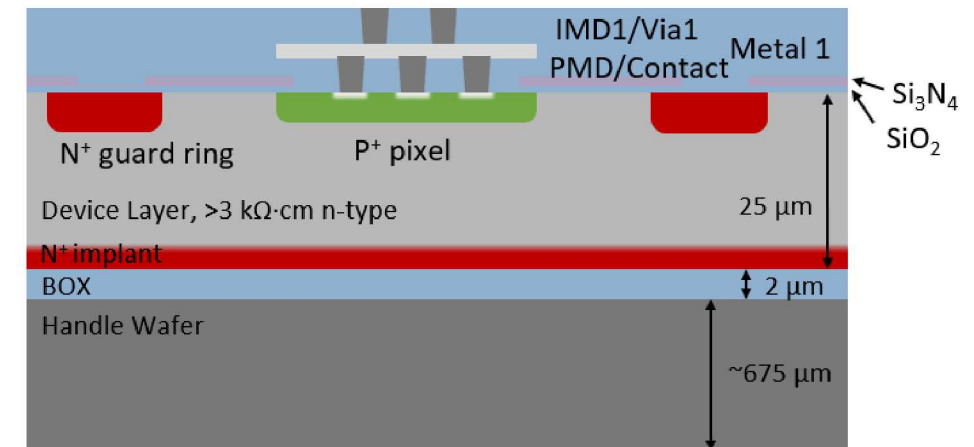
External Fab Option

- Processing capability requirements: cleans, implant, thermal oxide, CVD nitride, silicide, dry etch, via fill, CMP, metal dep

Single-pixel

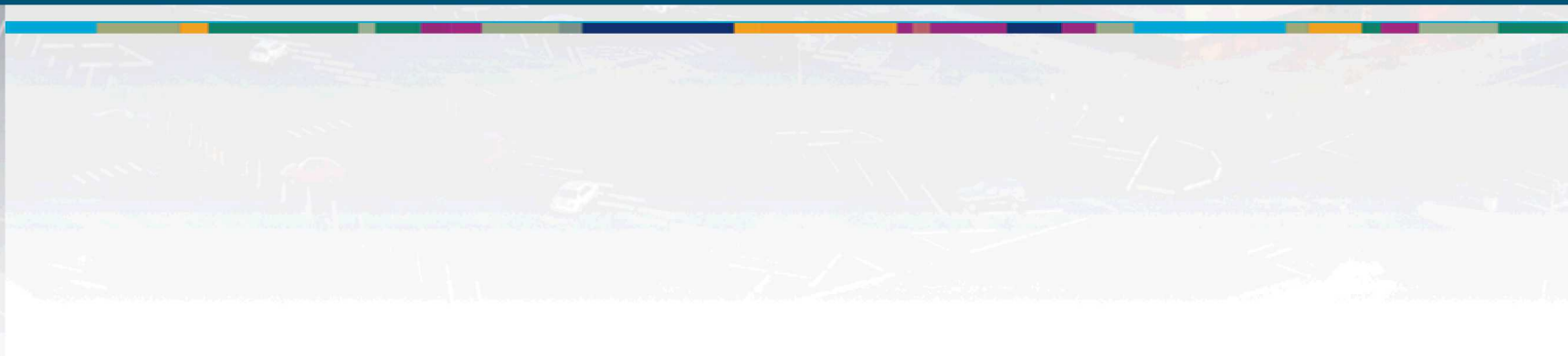


Cross Section View

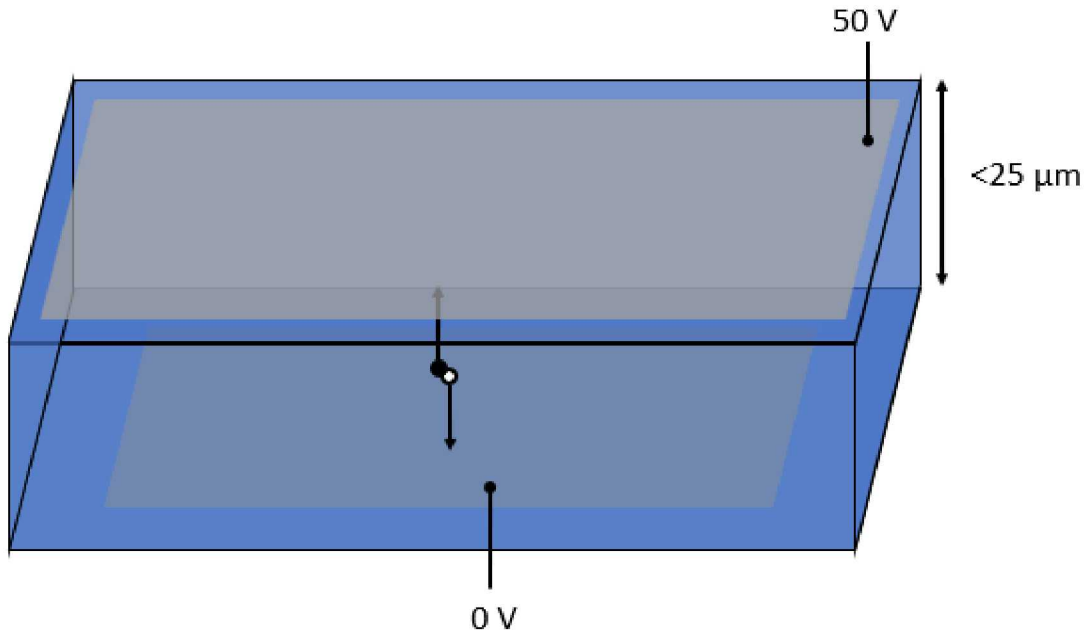




Potential Paths for Speed Improvements



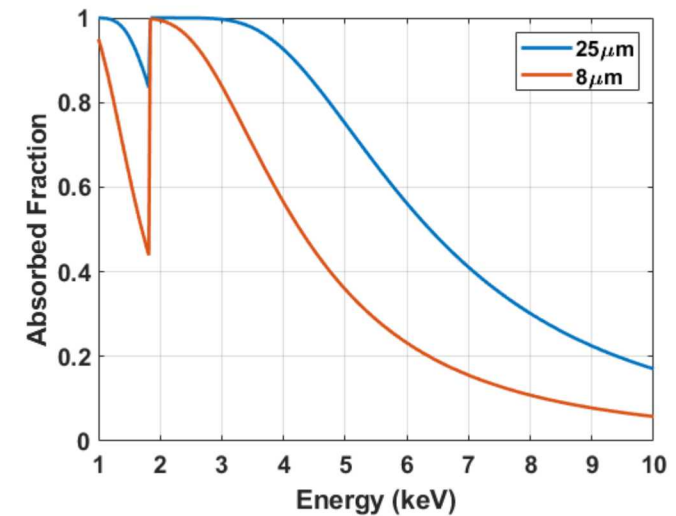
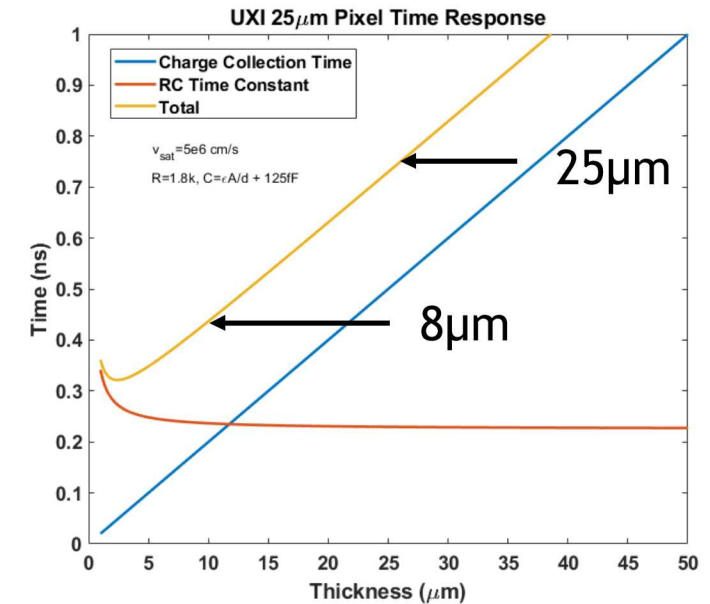
Thinner Absorber Layer



Key Features

- Proportional decrease in charge collection time with decreasing detector thickness
- Lower QE for all radiation types; may need thickness 10 μm or less
- Limit ~2 μm, where capacitance begins to take over

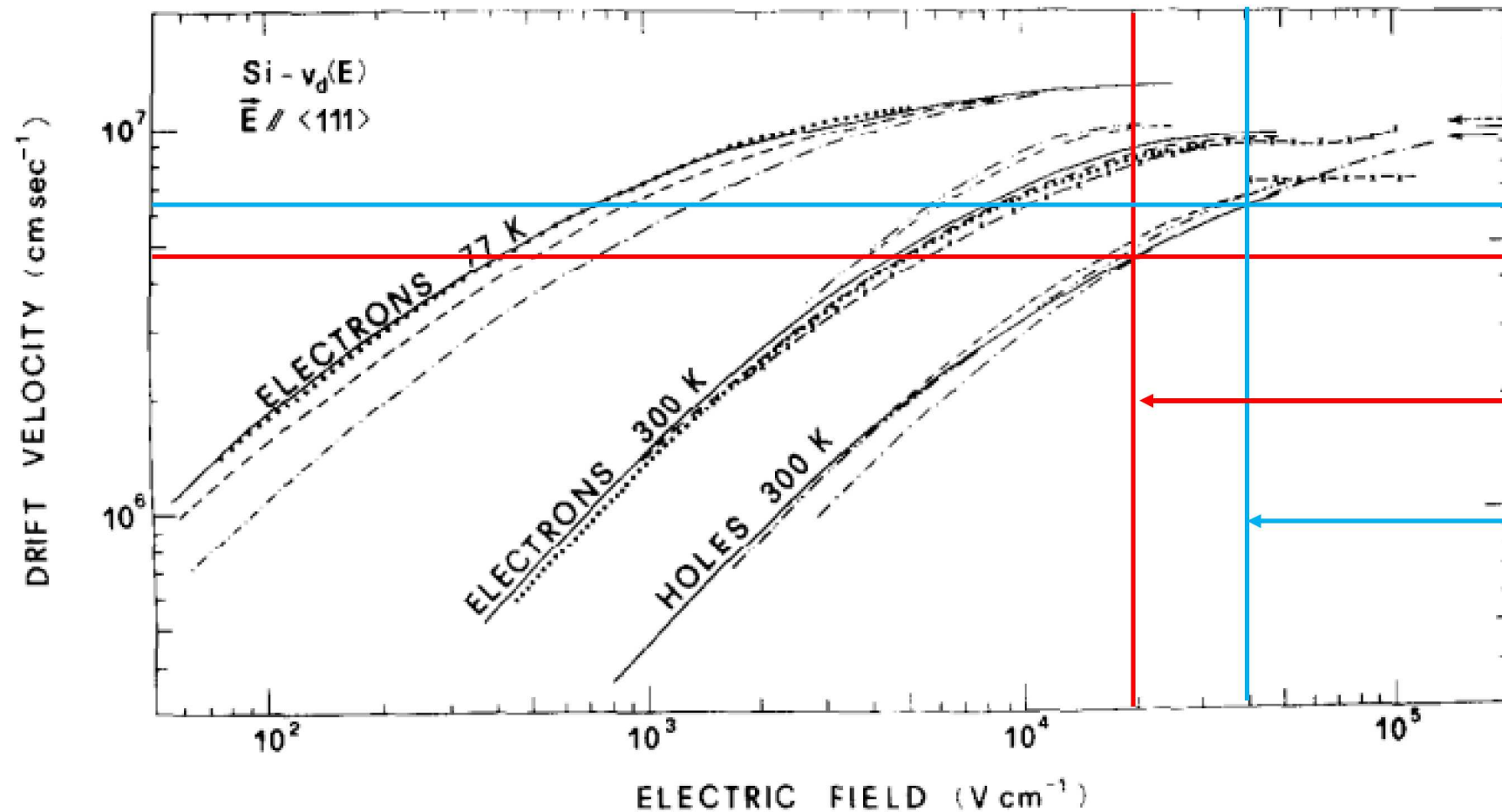
8μm thick diodes ~2x faster than standard 25μm



Feasibility: already done

Increasing Electric Field

Jacoboni et al., Solid-State Electronics Vol. 20, pp. 77-89 (1977)



We are probably here
~ $5 \times 10^6 \text{ cm/s}$

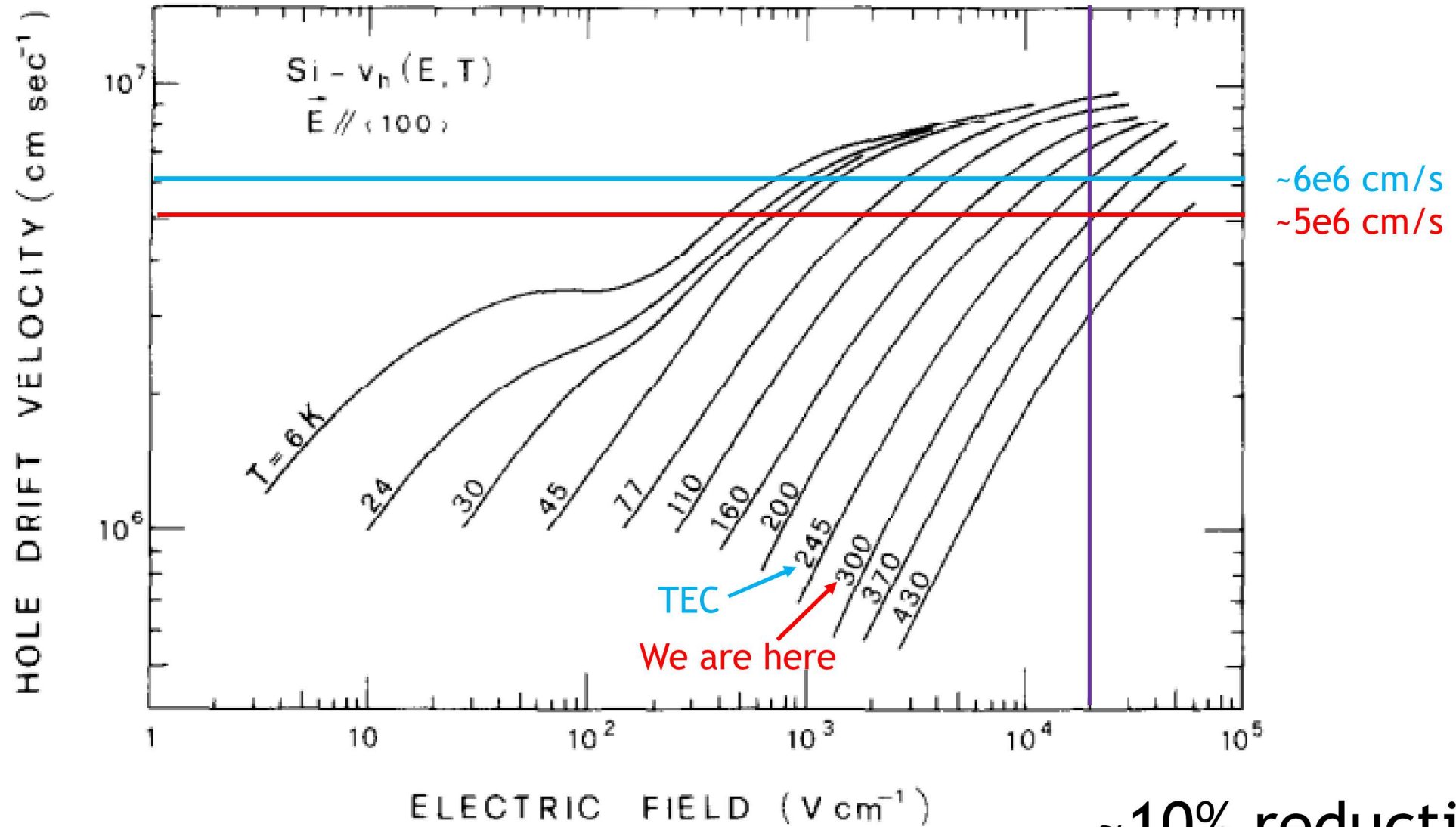
Maybe double E field?
~ $6 \times 10^6 \text{ cm/s}$

Key Features

- Likely minor design changes will allow the option of higher bias
- May reduce yield
- During operation, no inherent disadvantage

10-20% reduction

Feasibility: new diode lot



Key Features

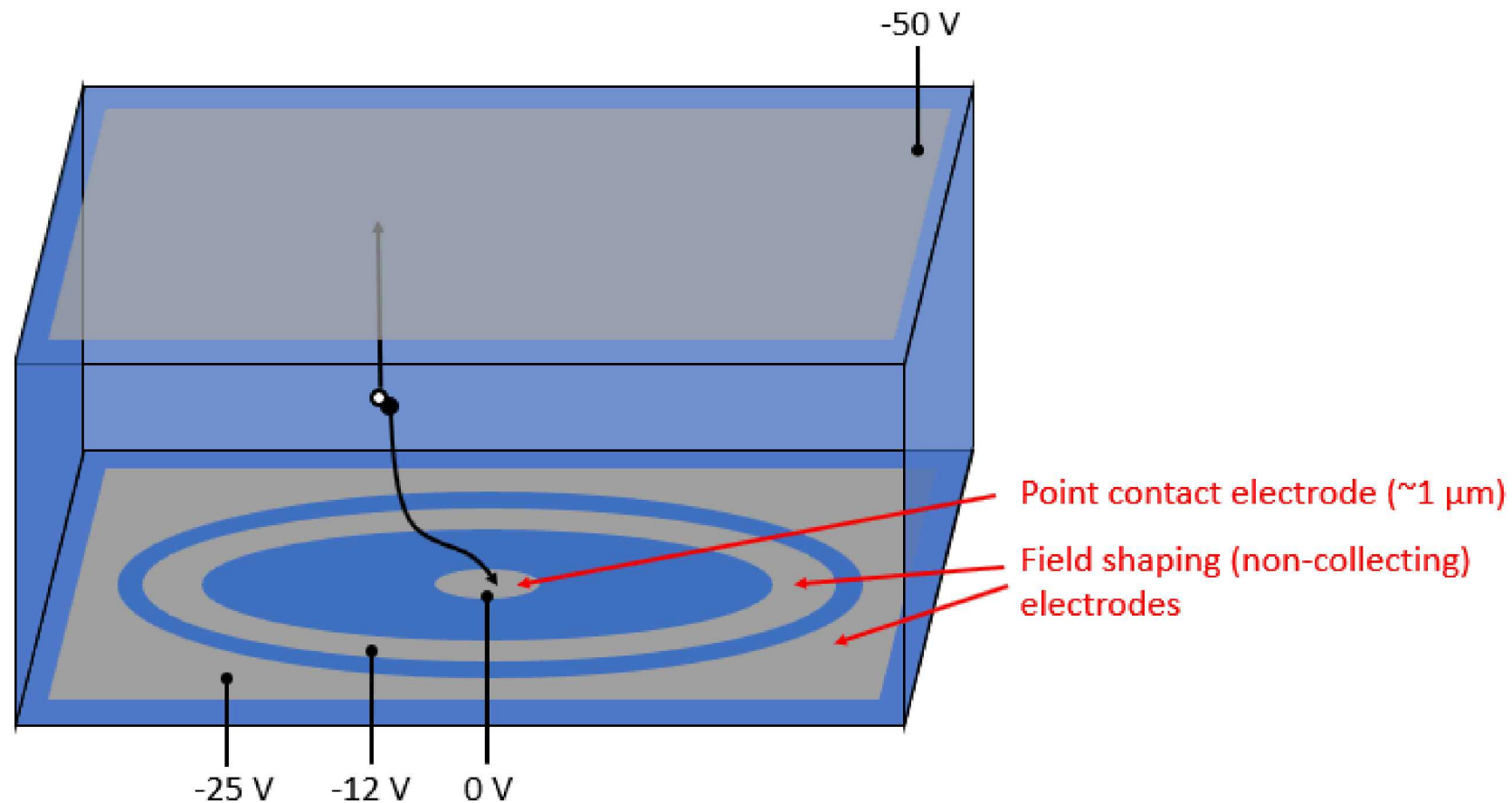
- Complementary to other efforts
- Use is optional; no risk to baseline use case
- More complex camera operation

~10% reduction

Feasibility: working on it now
Hippo only

Other Electrode Configurations:

9 Point Contact



Key Features

- Small collecting electrode senses moving charge only in small volume nearby
- Field shaping electrodes needed to funnel charge to collecting electrode
- Secondary benefit of lower junction capacitance

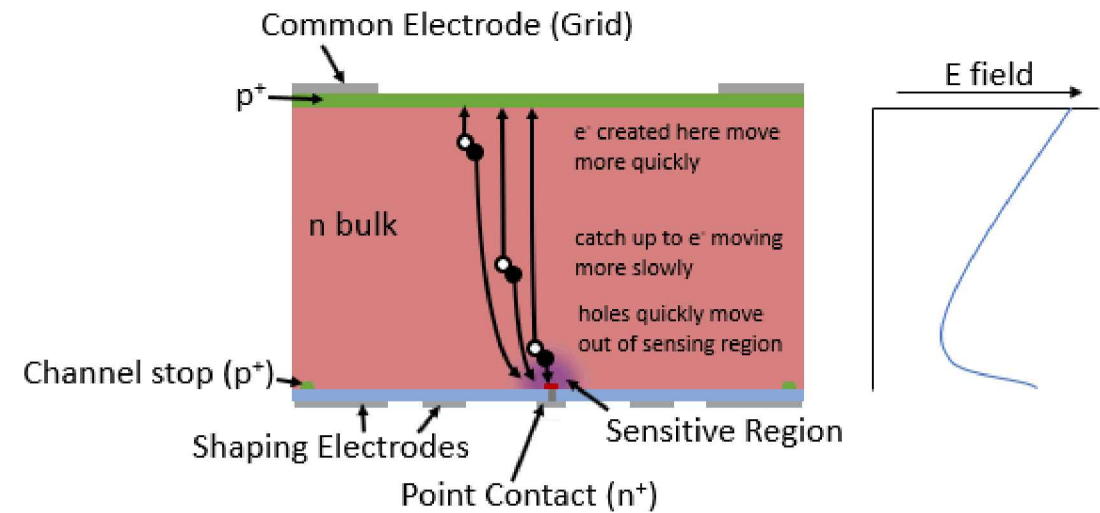
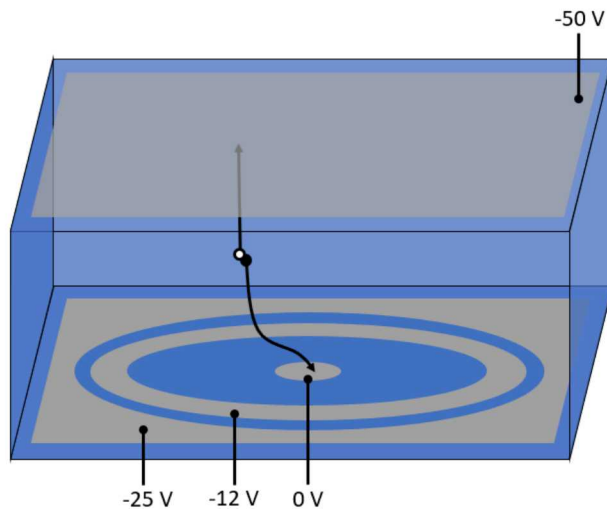
~40% reduction?

Feasibility: we can make it,
but high risk

Other Electrode Configurations:

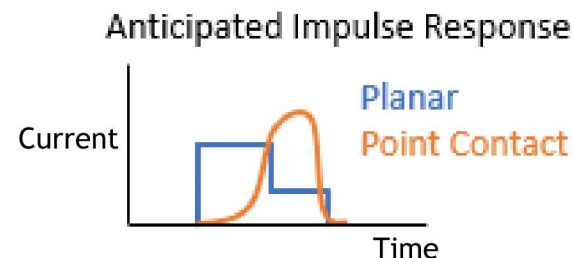
Point Contact Part 2

This on its own may not offer much improvement. To fully take advantage of this electrode structure, we would need to move the junction to the illuminated side and collect electrons.



Key Features

- Small collecting electrode senses moving charge only in small volume nearby
- Field shaping electrodes needed to funnel charge to collecting electrode
- Secondary benefit of lower capacitance

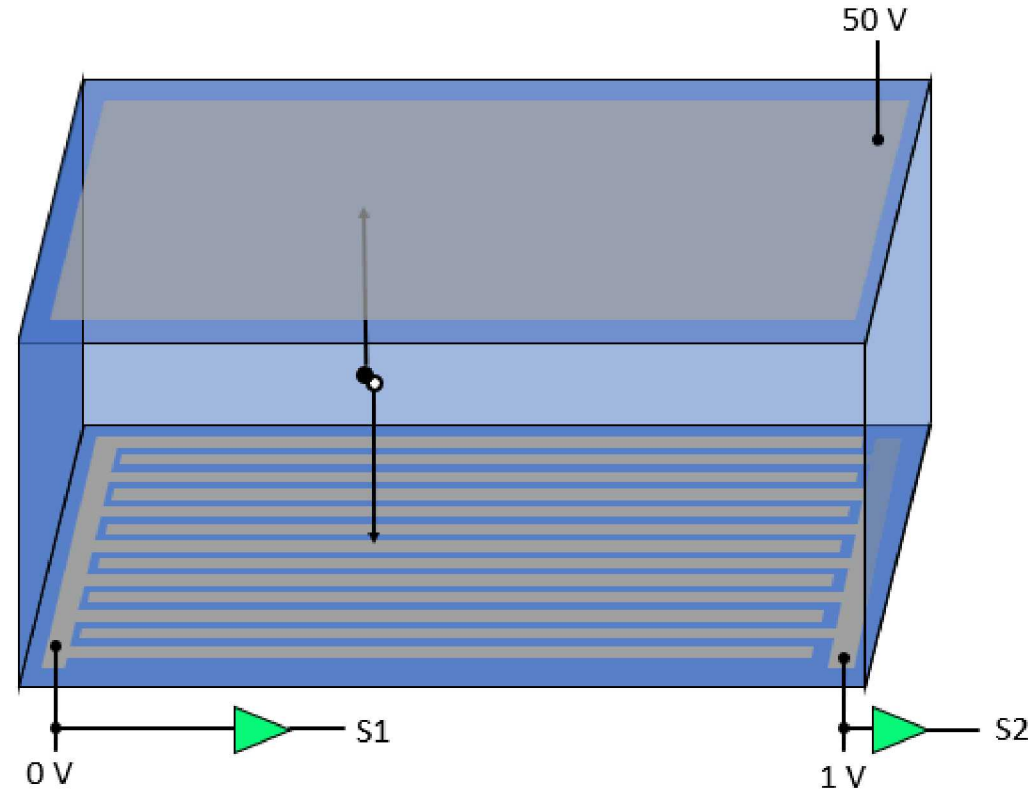
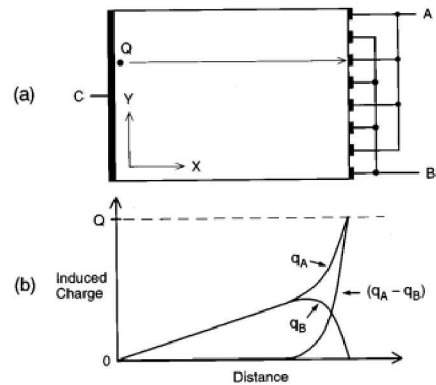


~40% reduction?

Feasibility: we can make it,
but high risk

Other Electrode Configurations: Coplanar Grid

P. Luke, APL 65, p.2884 (1994)



Key Features

- Requires more in-pixel structure
- Can operate as typical pixel when $PV = S1 + S2$
- Can increase dynamic range when $PV = S1$. $S2$ shunted to VRST.
- Can reduce sensitive volume when $PV = S1 - S2$, similar to point contact
- Unlike point contact, capacitance is higher

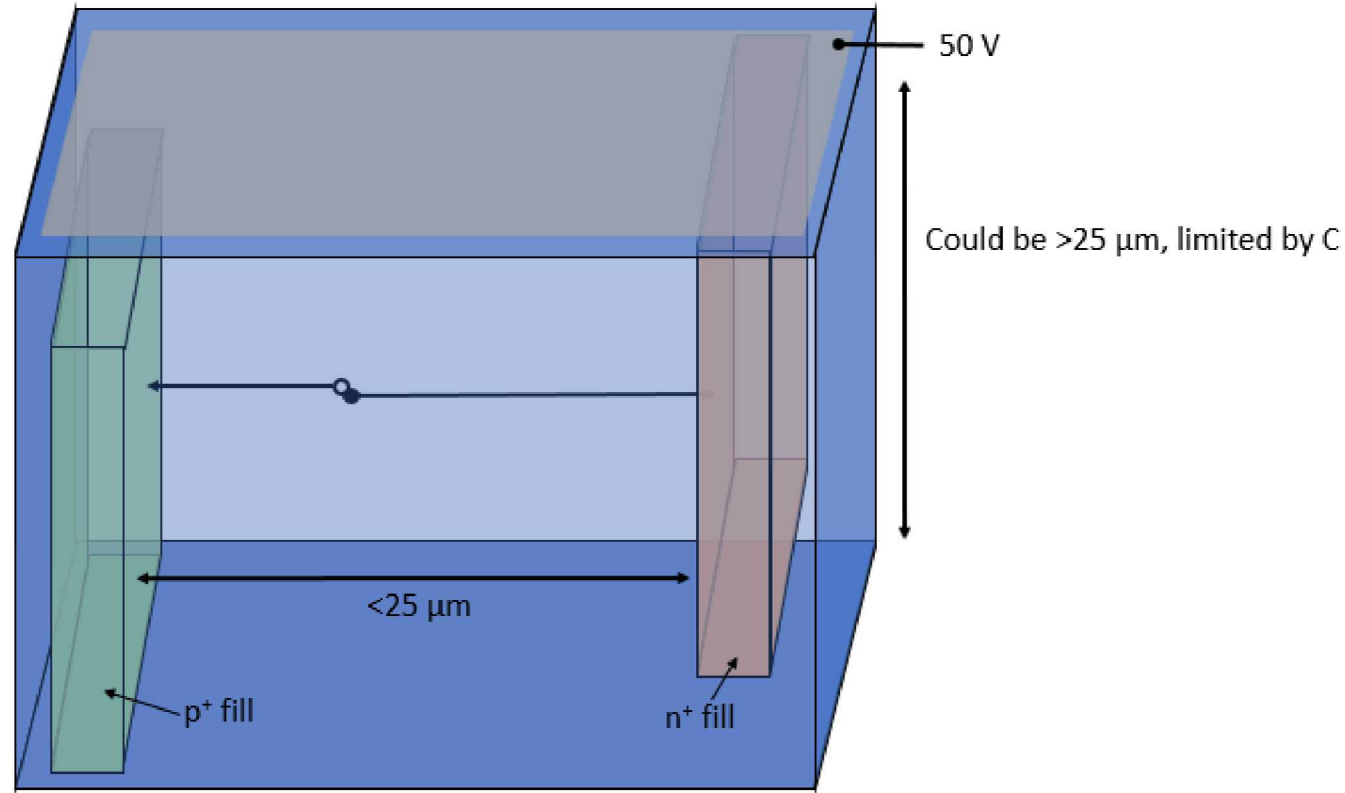
~40% reduction?

Feasibility: we can make it,
but high risk

Other Electrode Configurations:

3D Diode (Trench)

Doped polyfill column structures described in Parker 1997, Kenney 1999, Kok 2006, etc.



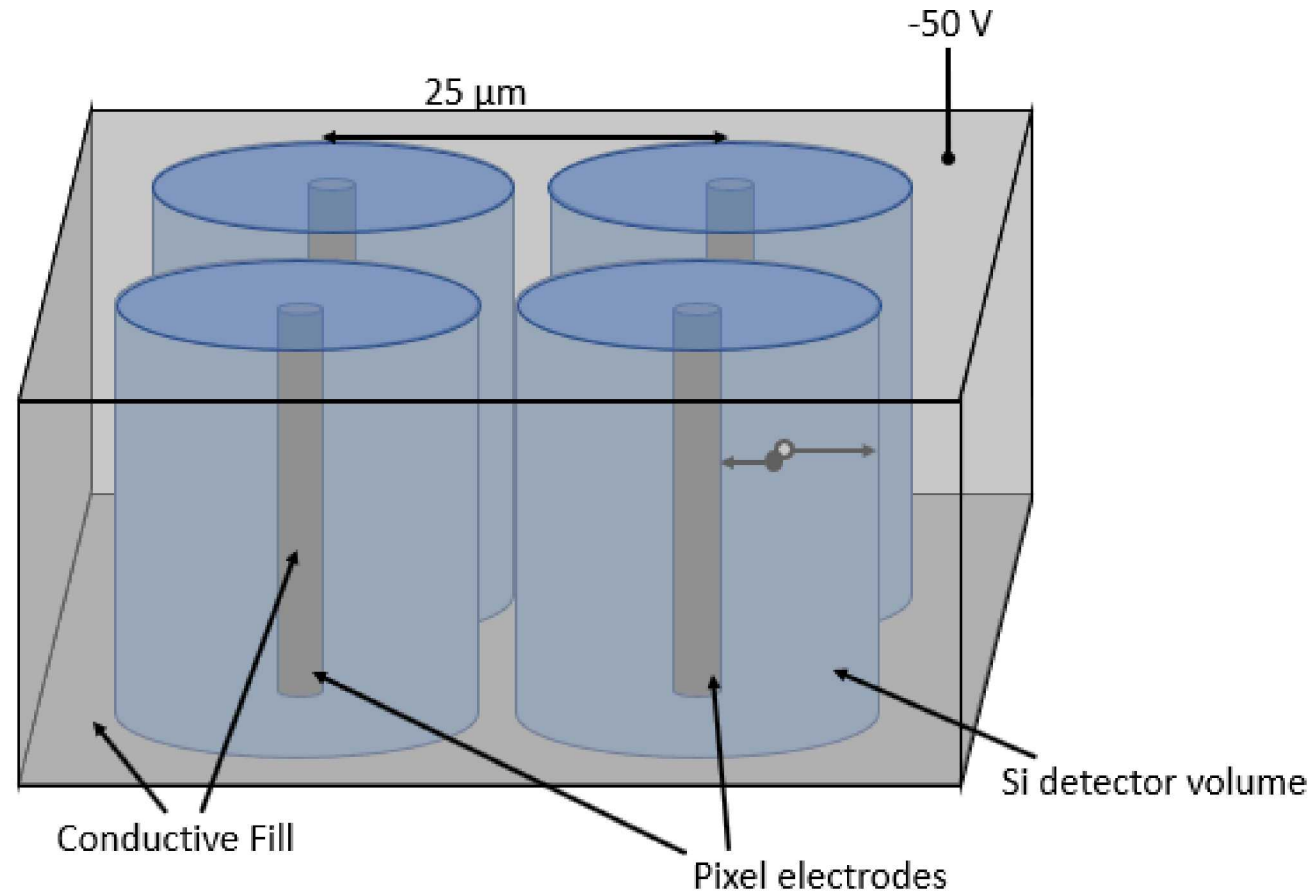
Key Features

- Can select width based on desired timing; may be connected to pixel size
- Thickness can be increased to keep high QE
- Need to develop dry etch and conductive fill process for thick device layers
- 2nd electrode would need to be created after hybridization (need low T process)

~50% reduction?

Feasibility: significant process development

Other Electrode Configurations: 3D Diode (Cylinder)



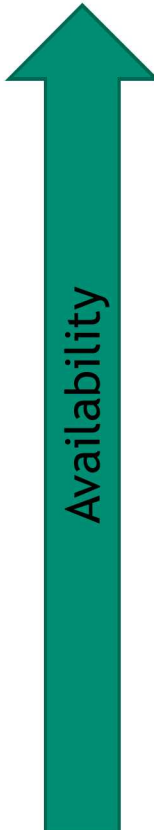
Key Features

- Need mature dry etch and conductive fill process
- Better takes advantage of geometry to reduce hole contribution to signal

~60% reduction?

Feasibility: significant
process development

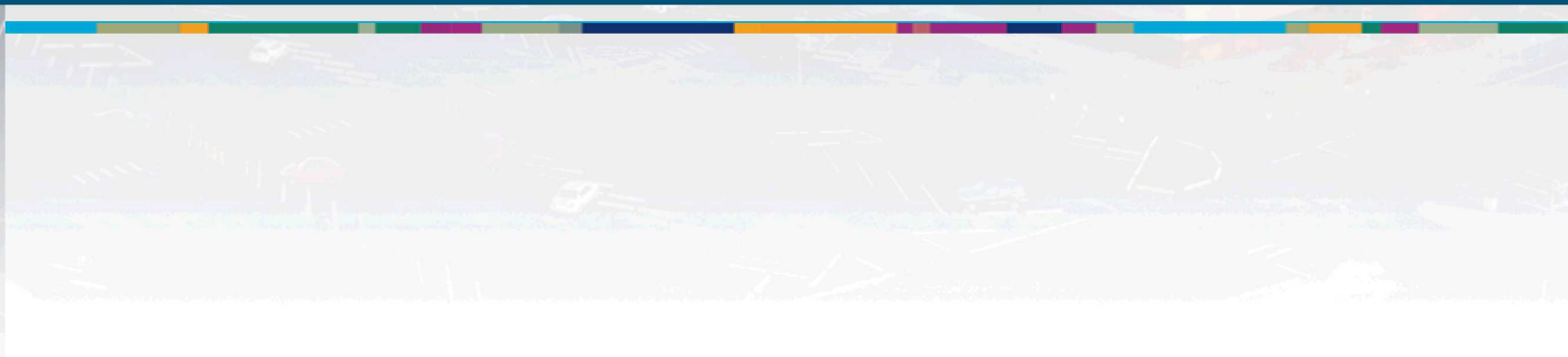
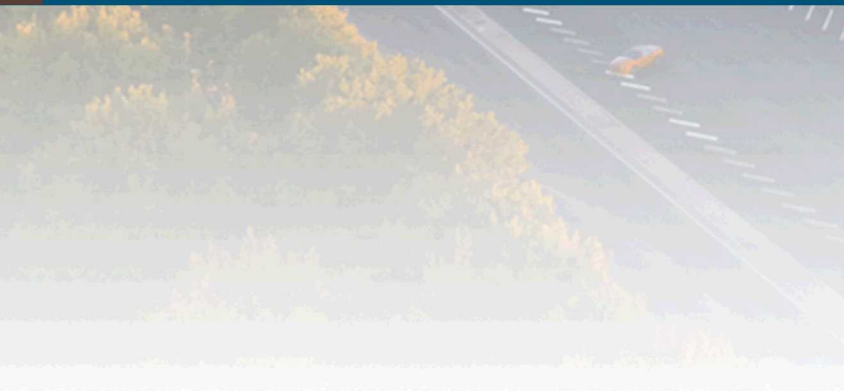
Potential Speed Improvements Summary



Method	Potential Reduction	Feasibility	
Thinner Absorber Layer	50%	Done	Undesirable QE reduction
Higher Electric Field	10-20%	New Diode Lot	Universal - stacks with other methods
Cooling	10%	No major technical hurdles	
Point Contact Electrode	40%?	Easy to fab, need to understand behavior	
Coplanar Grid Electrode	40%?	Can fabricate, need ASIC changes	Some uncertainty as to how these will behave
Trench 3D Diode	50%?	Some process development work done; more needed	Requires process development (\$\$\$)
Cylindrical 3D Diode	60%?	Major process development work needed	

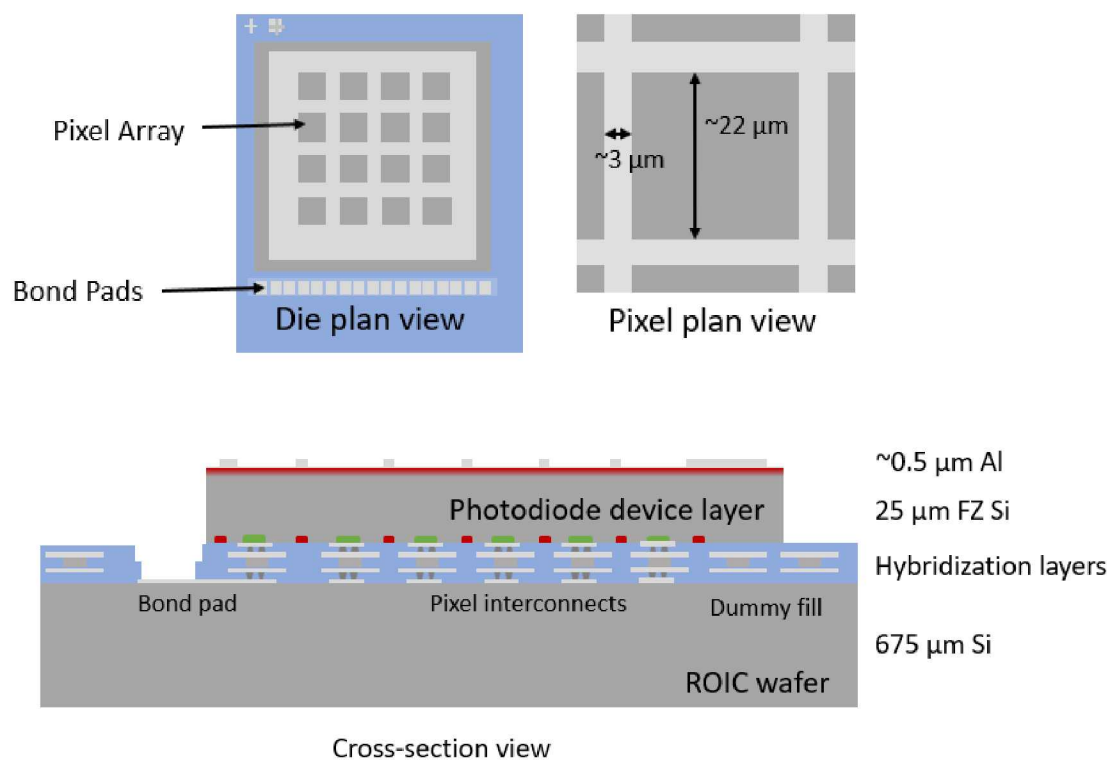


Extra Slides



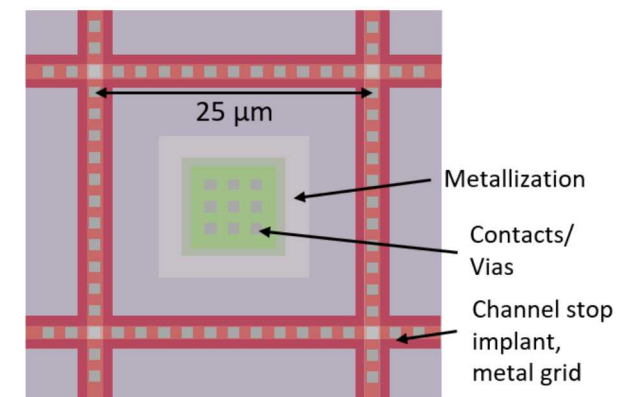
Today's Pixel Design

Hybrid Device, Die-level

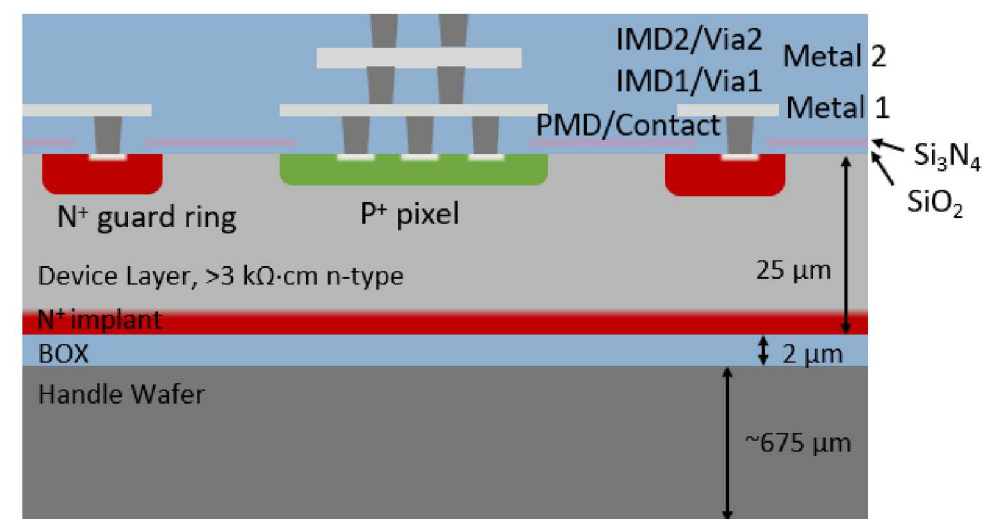


Detector Wafer, Single-pixel

Pixel Plan View



Cross Section View



Simpler Pixel Design v2

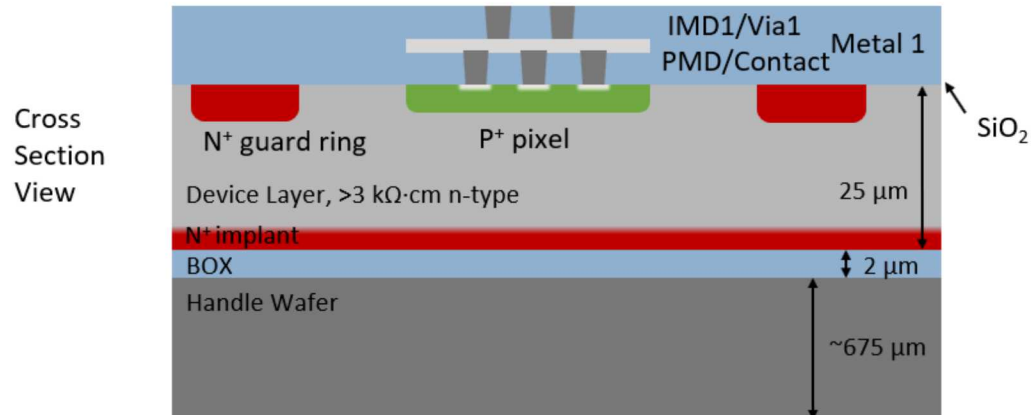
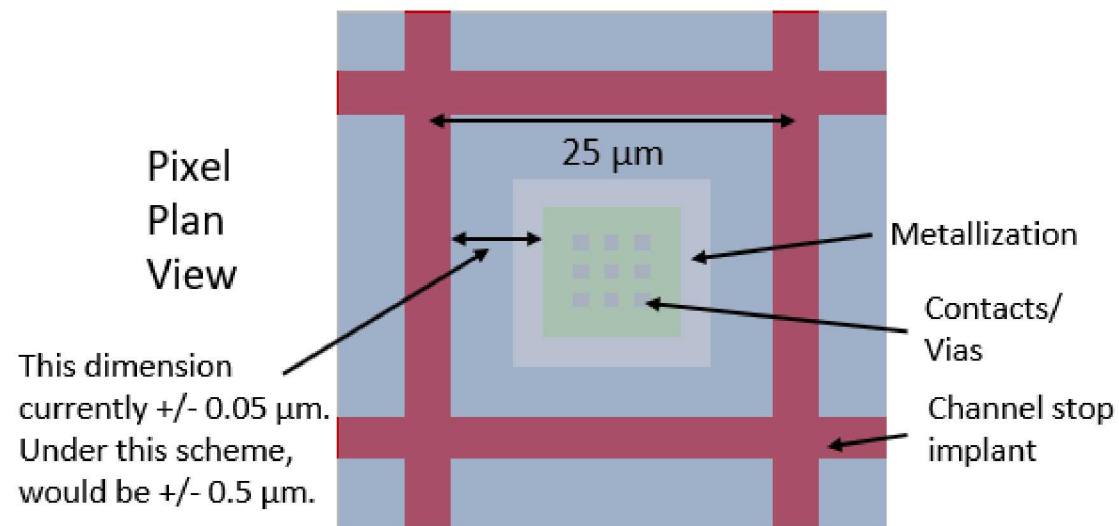
Base plan: 233 steps

- Eliminate nitride layer and etch
 - Eliminate 17 steps, 1 mask layer
 - Coarser implant-implant alignment
- Eliminate contacts and metal grid to channel stop
 - Lose ability to ROIC-side bias
 - Reduces mask complexity, potential short paths
- Eliminate M2/V2 stack
 - Fewer routing options available (not needed if ch stop metal not present)
 - Eliminates 45 steps, 2 mask layers

Modified plan: 171 steps
26% cost reduction?

I don't believe the additional cost savings of eliminating the nitride layer are warranted. If we want to pursue this, detailed simulations should be conducted to determine the effect of implant-to-implant spacing.

Single-pixel



Shockley-Ramo Theorem

Key Principle: charge induction efficiency of electrodes can be calculated as a function of volume, independent of real electrostatic conditions

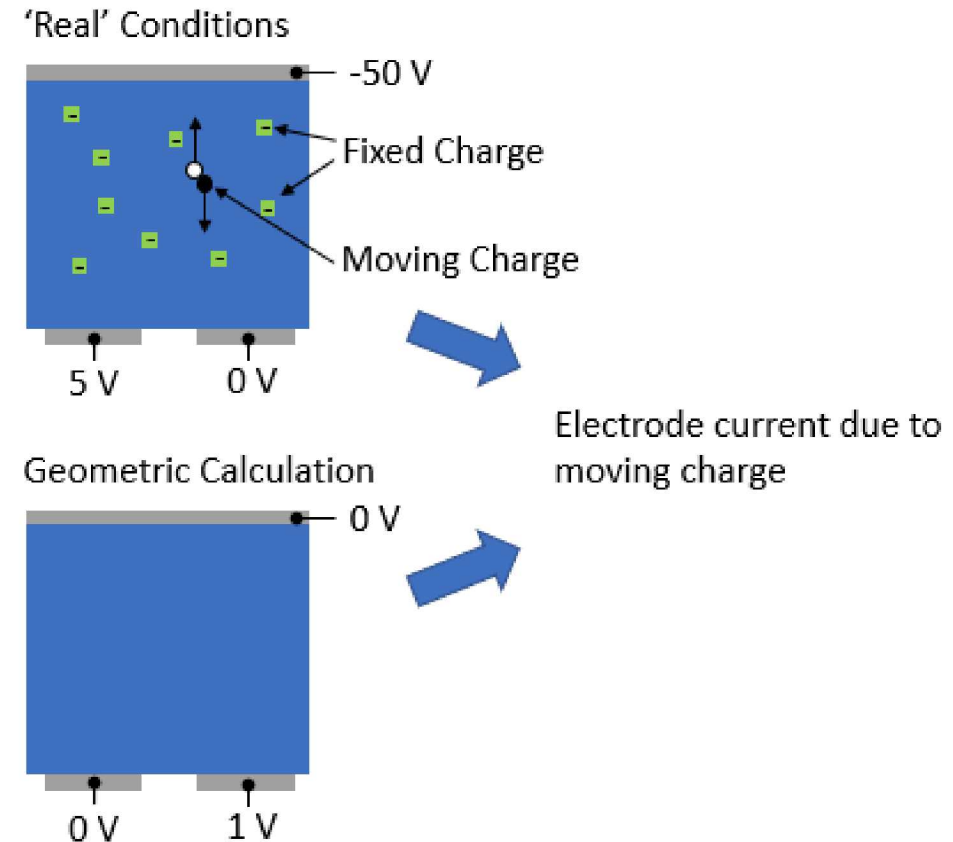
1. Remove all fixed charge
2. Set all electrodes to 0 V
3. Set electrode of interest to 1 V
4. Calculate potential => 'weighting potential' φ_0
5. Calculate E field => 'weighting field' \vec{E}_0
6. The following are true for given geometry:

Charge induced on an electrode $Q = -q\varphi_0$

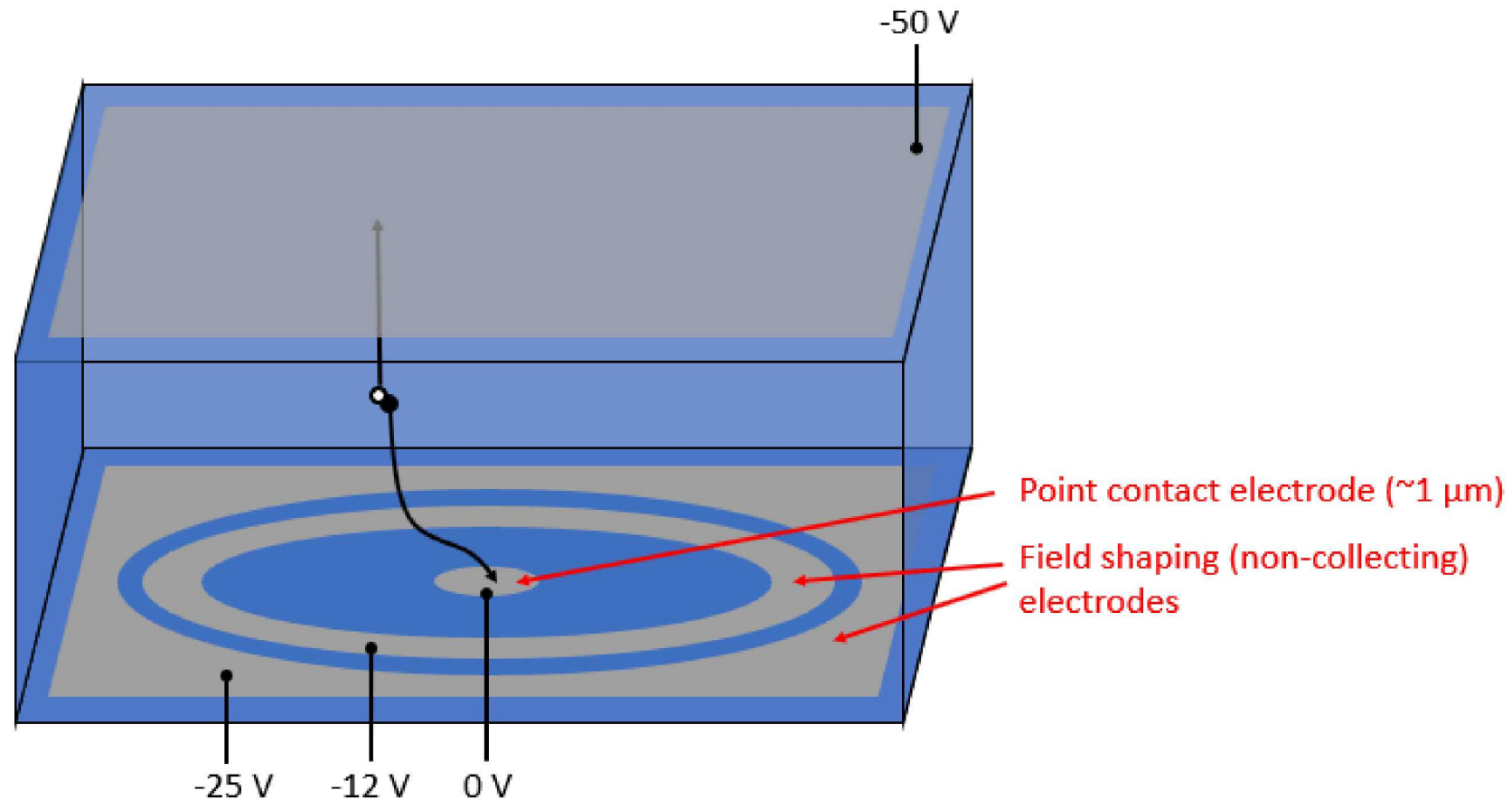
Current induced on an electrode $i = q\vec{v} \cdot \vec{E}_0$

From real electric field, we have $\vec{v} = v(|\vec{E}|)\vec{E}$

Combination gives $i = qv(|\vec{E}|)\vec{E} \cdot \vec{E}_0$



Point Contact



Key Features

- Small collecting electrode senses moving charge only in small volume nearby
- Field shaping electrodes needed to funnel charge to collecting electrode
- Secondary benefit of lower junction capacitance

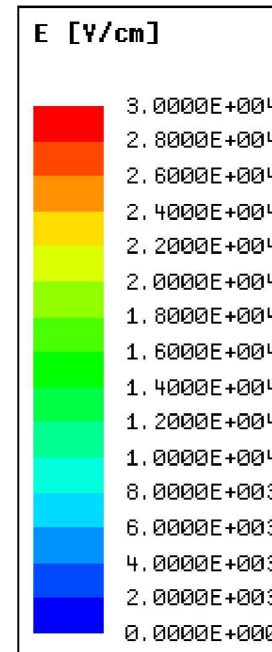
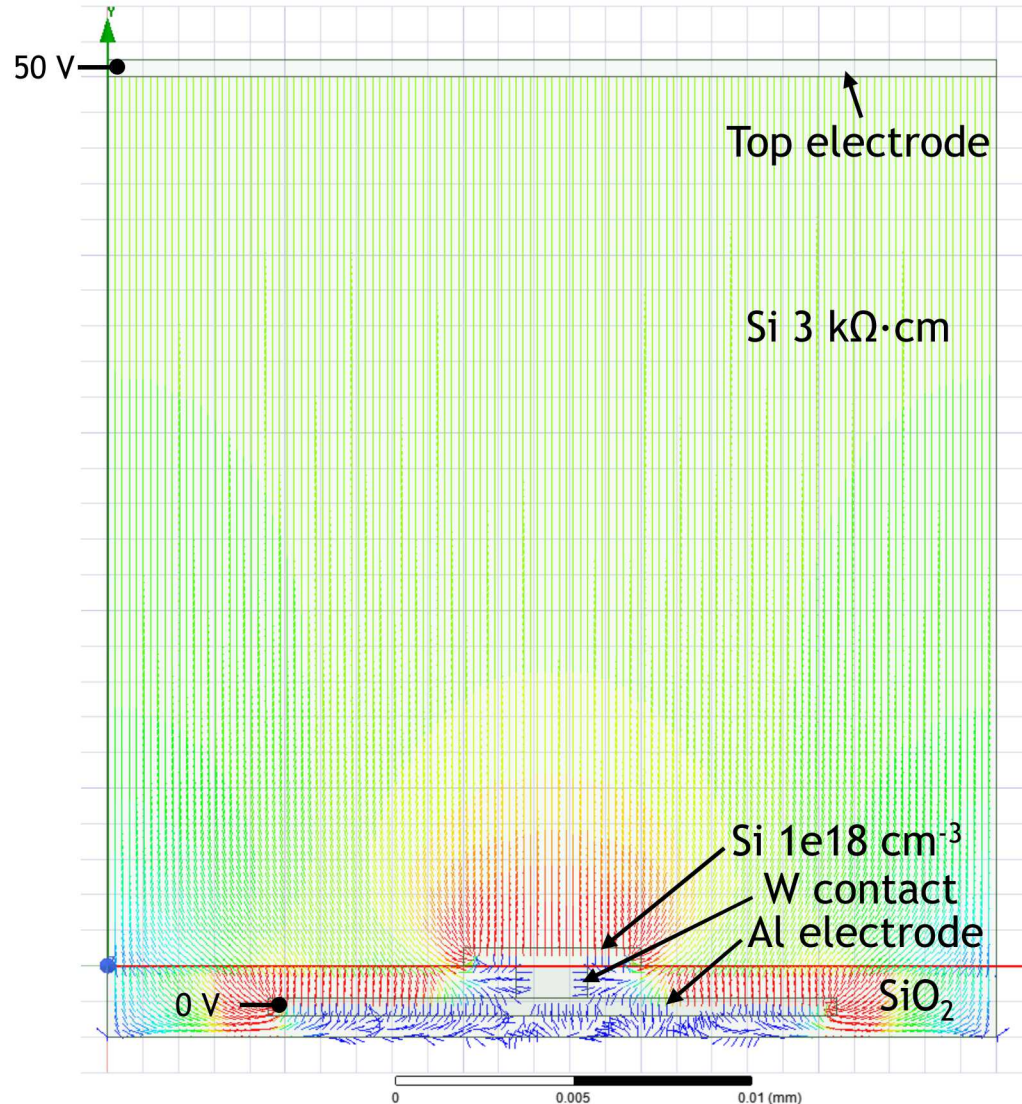
~40% reduction?

Feasibility: we can make it,
but high risk

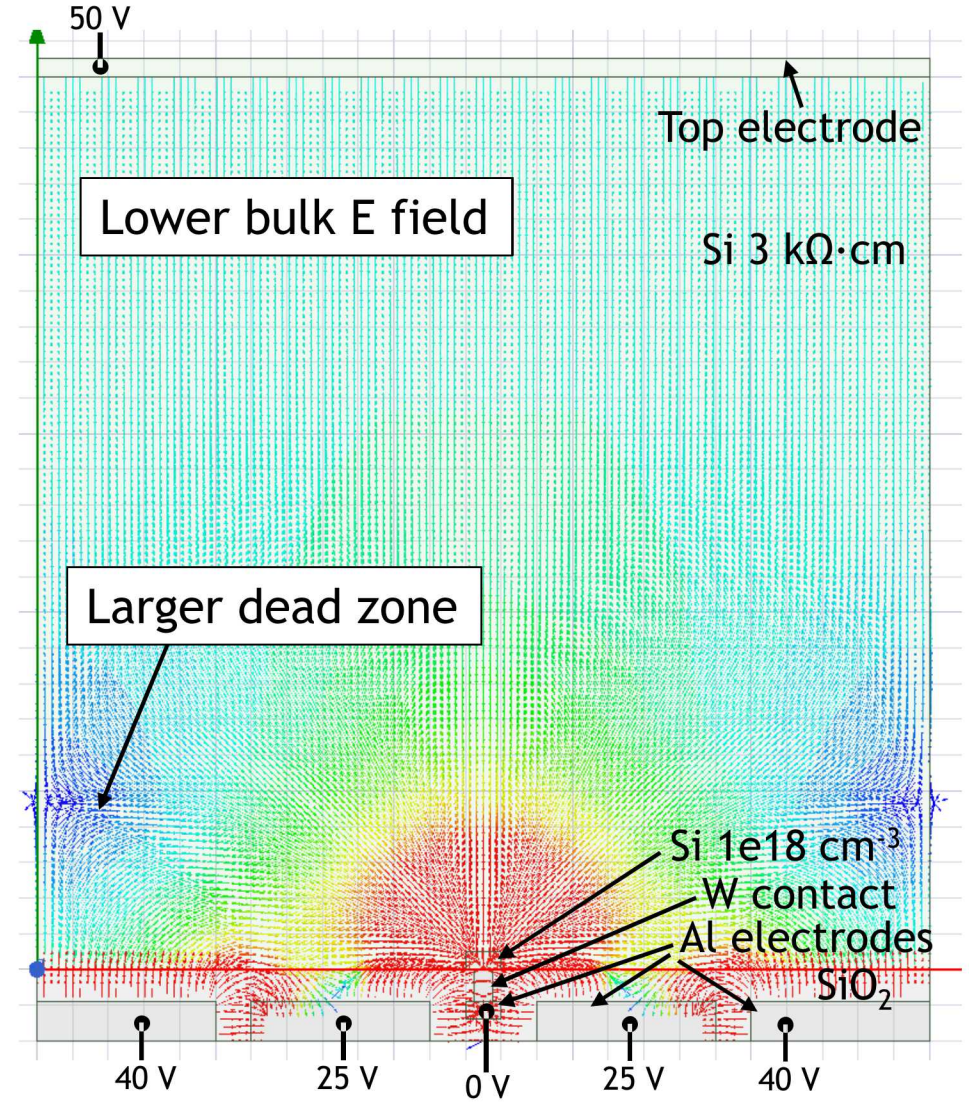
Point Contact

'Real' Electric Field

Pixel as it is now



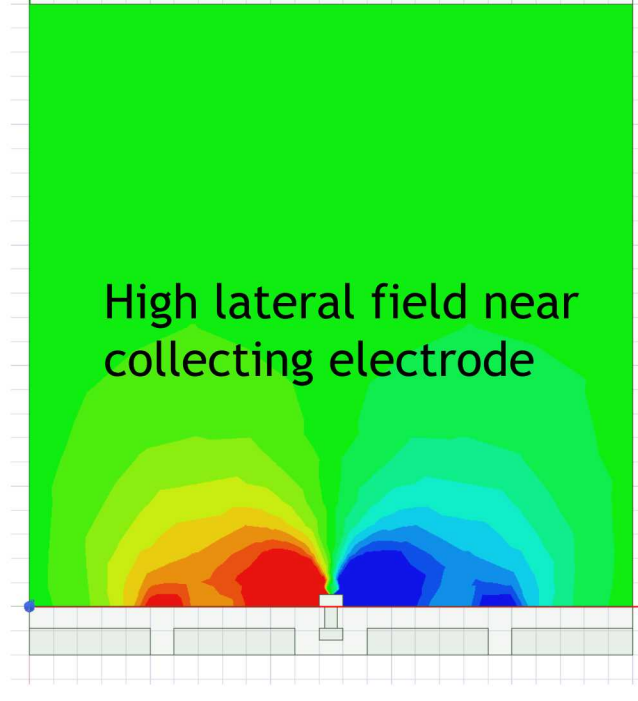
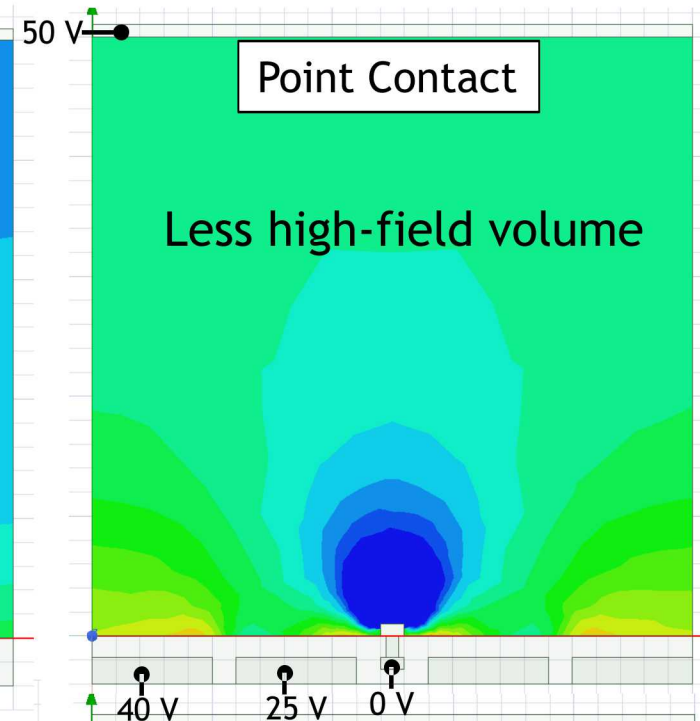
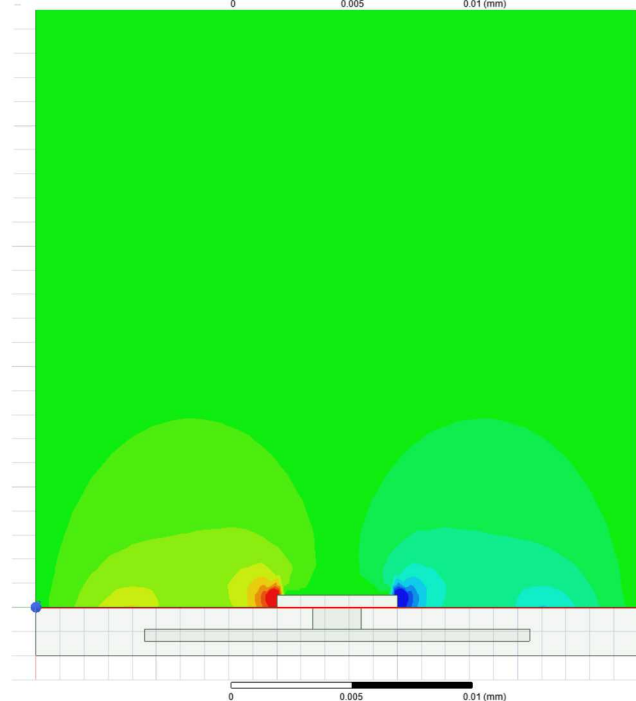
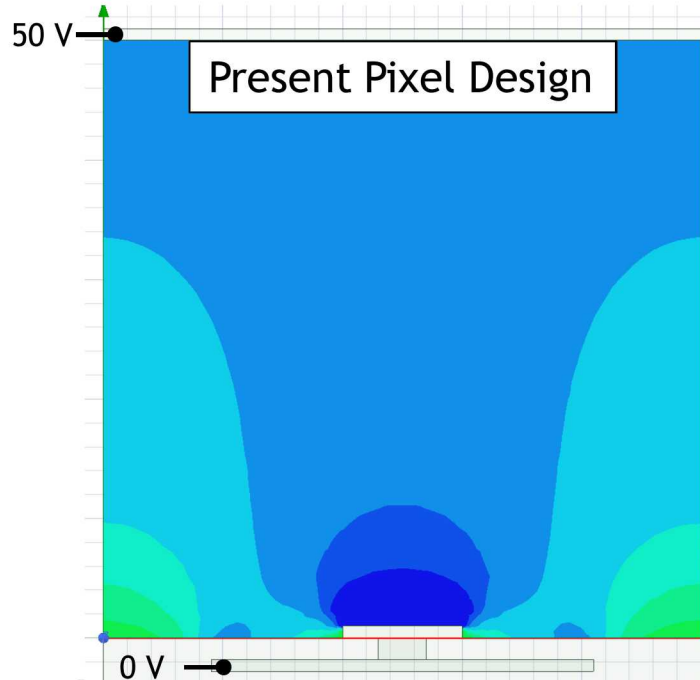
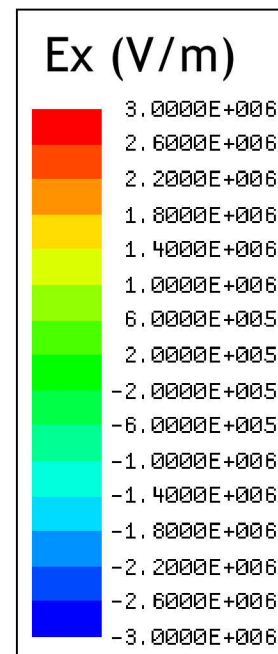
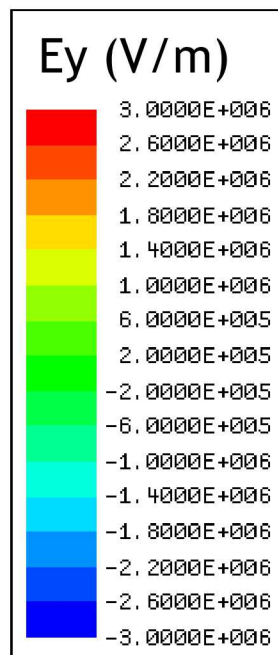
Point Contact



Point Contact

'Real' Electric Field

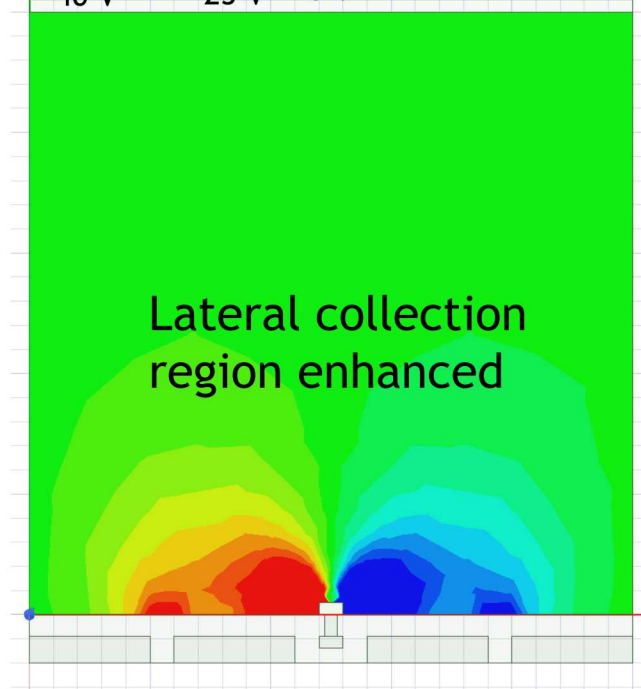
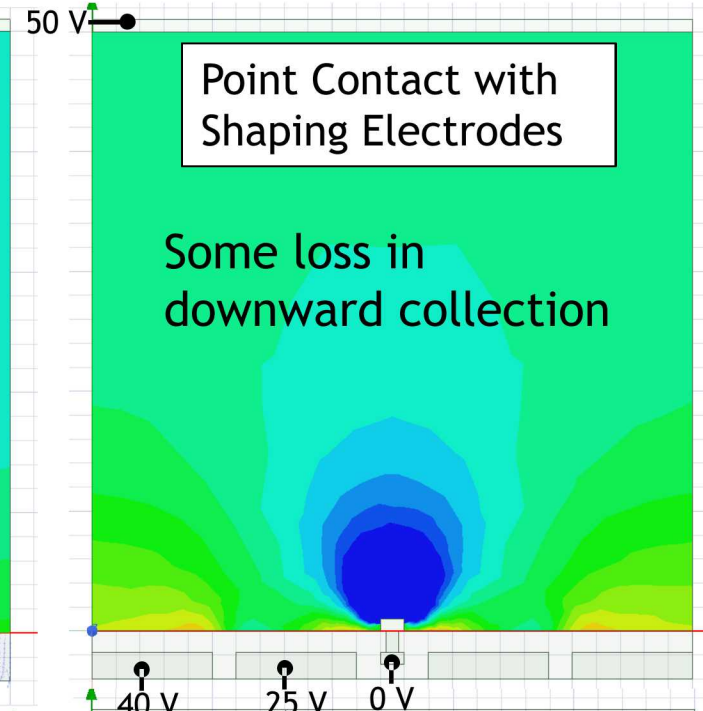
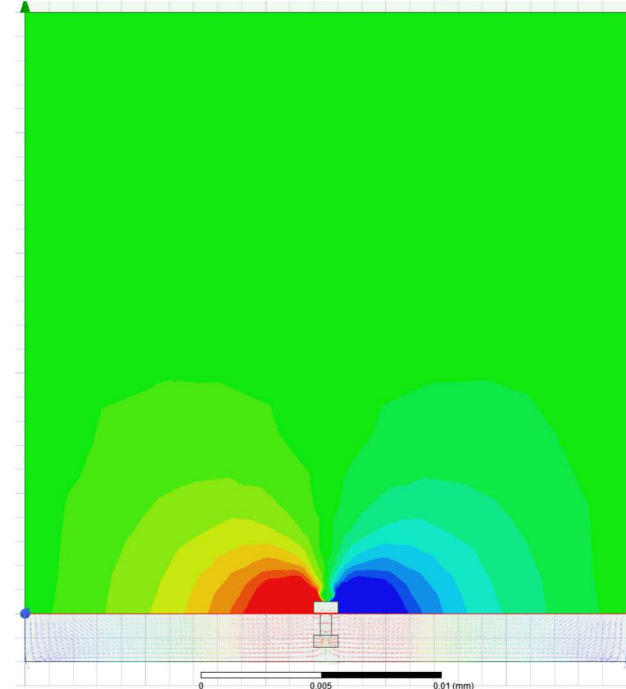
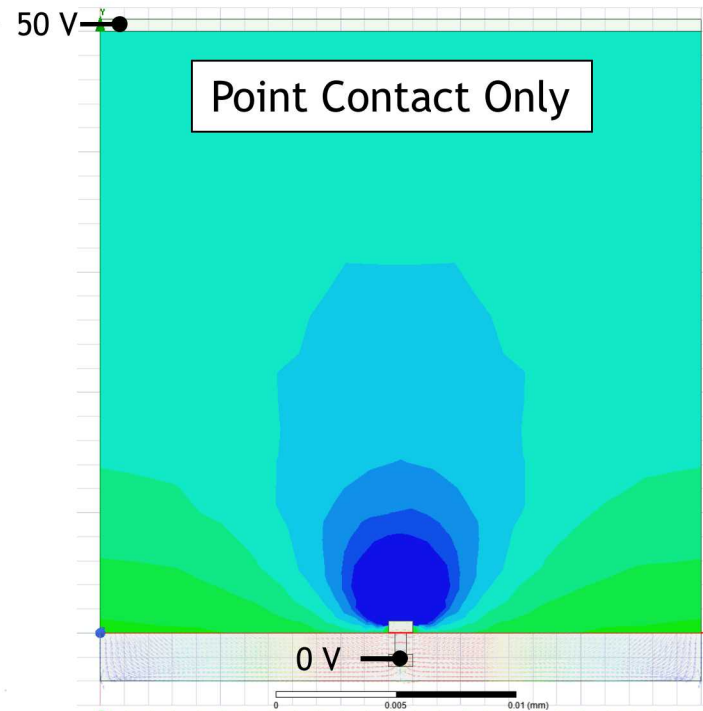
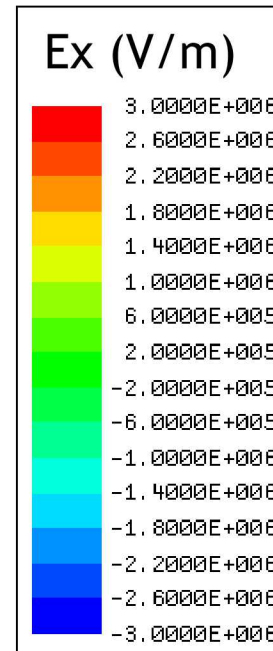
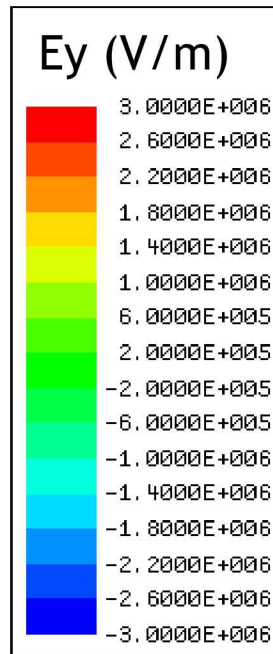
Point contact configuration likely less efficient in charge collection compared to standard design



Point Contact

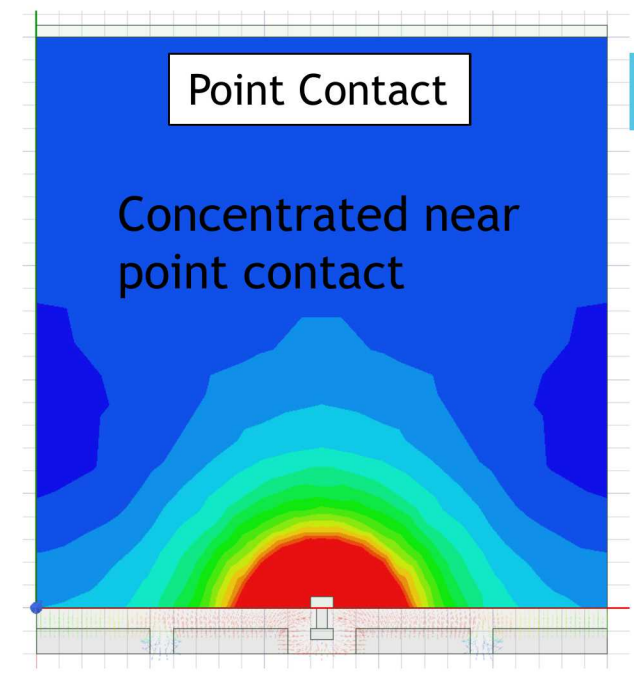
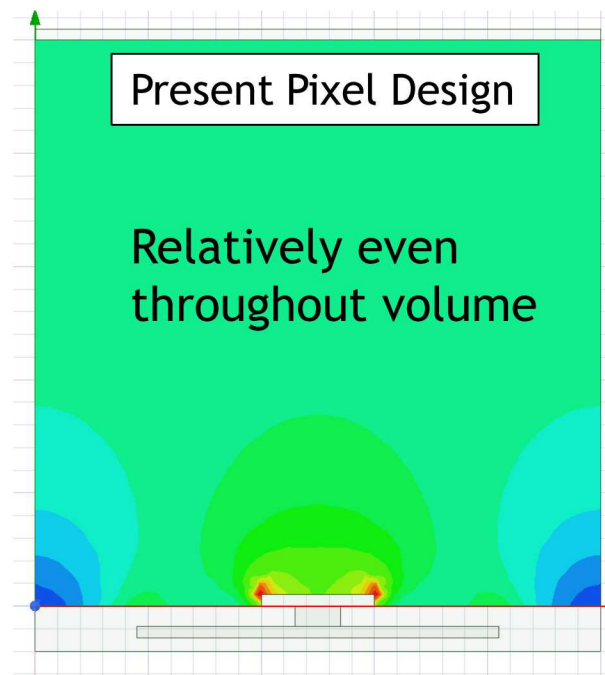
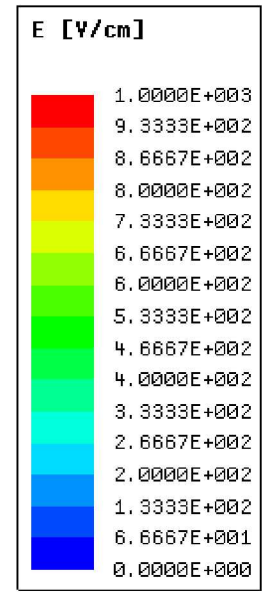
'Real' Electric Field

This is why shaping electrodes are necessary



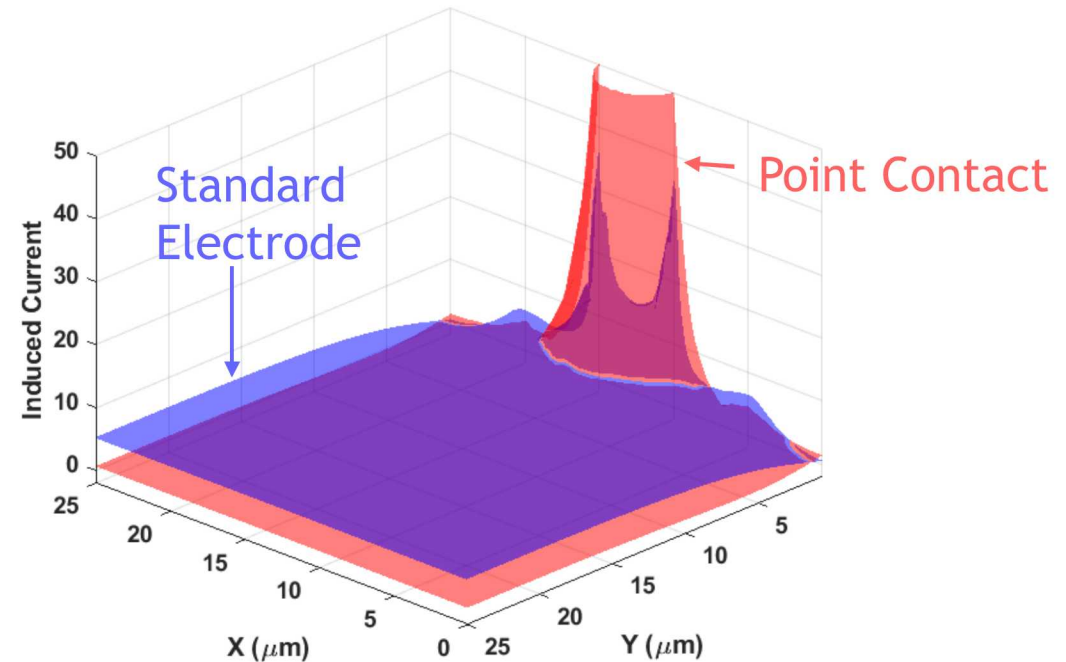
Point Contact

Weighting Field $|E_0|$
A measure of sensitivity
to moving charge

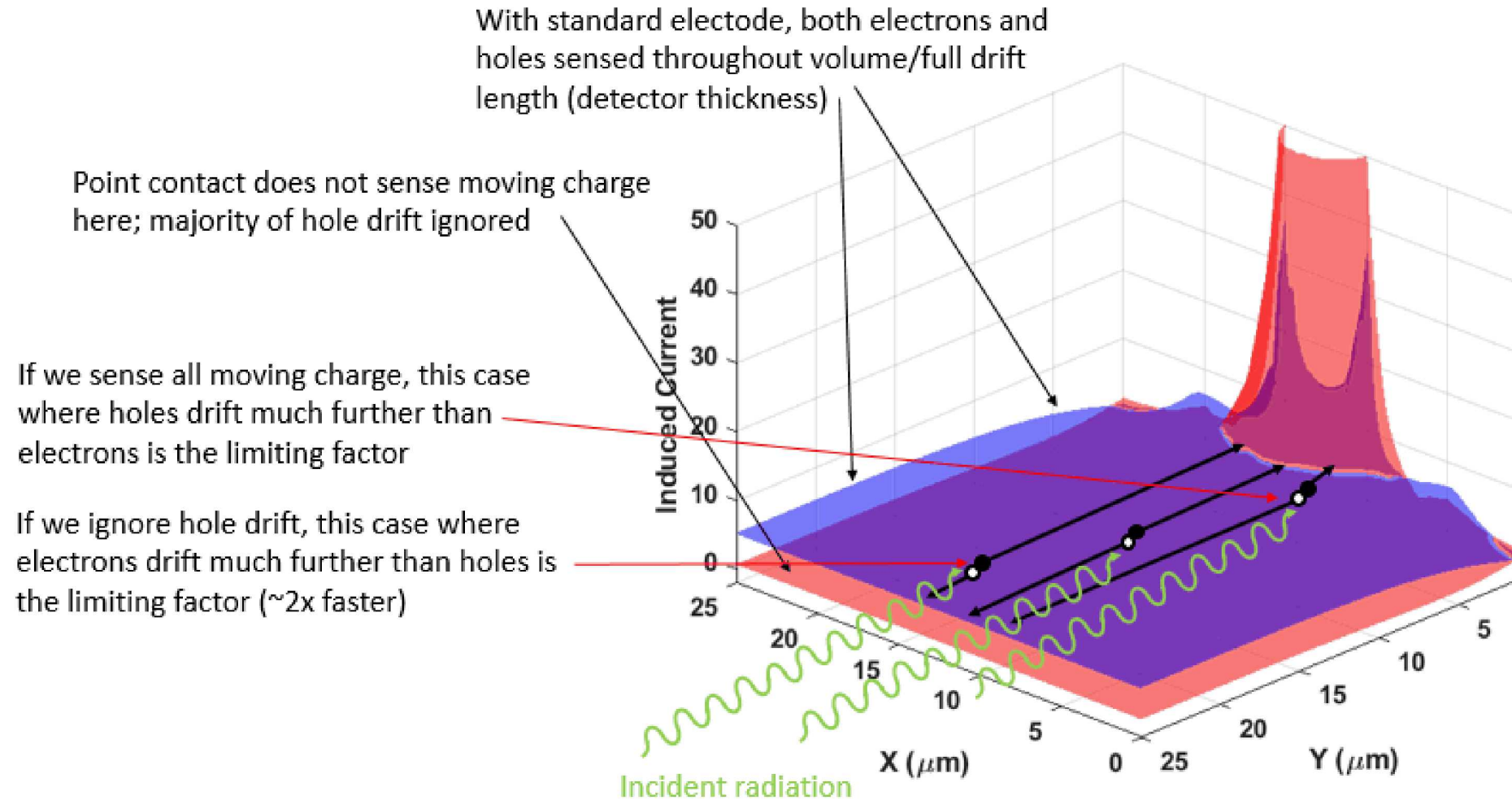


$$i = q \vec{v} \cdot \vec{E}_0$$

\vec{v} : Velocity due to real field
 \vec{E}_0 : Weighting field



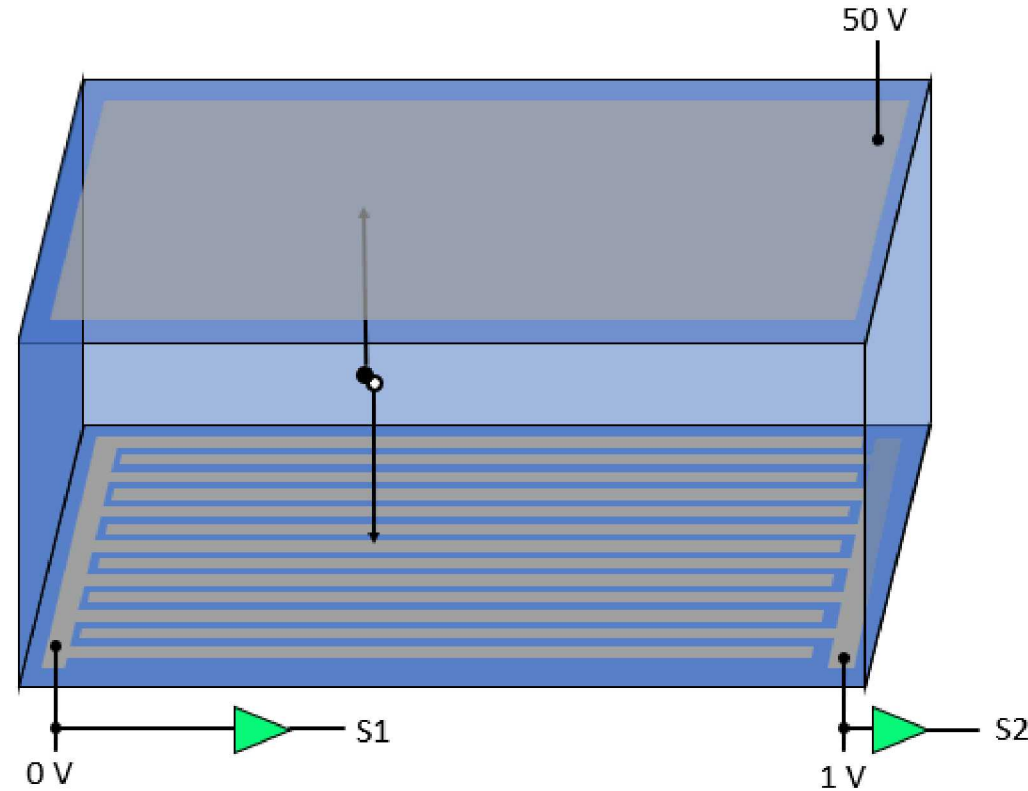
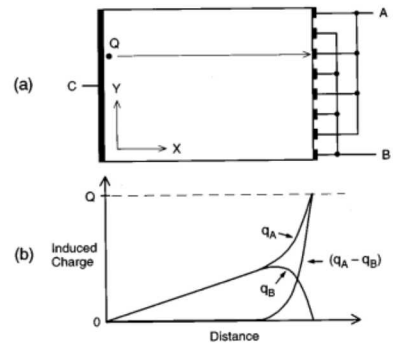
Point Contact



Other Electrode Configurations

Coplanar Grid

P. Luke, APL 65, p.2884 (1994)



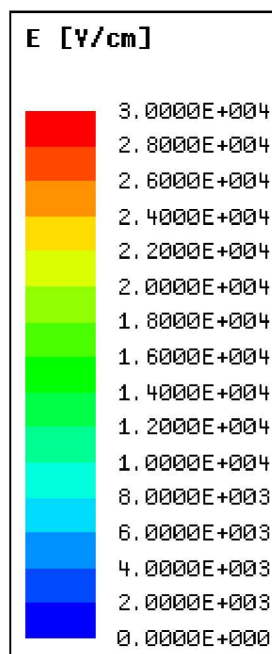
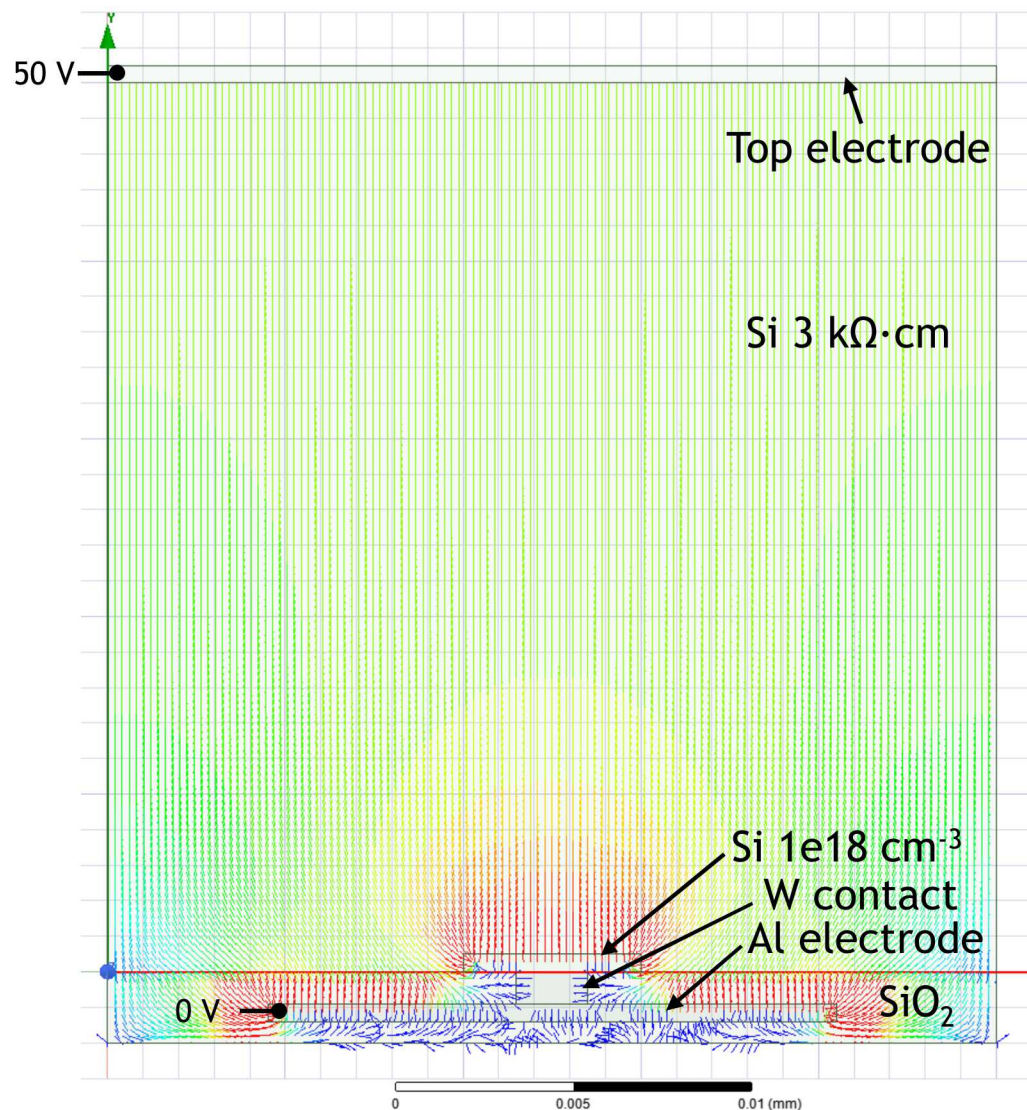
Key Features

- Requires more in-pixel structure
- Can operate as typical pixel when $PV=S1+S2$
- Can increase dynamic range when $PV=S1$. $S2$ shunted to VRST.
- Can reduce sensitive volume when $PV=S1-S2$, similar to point contact
- Unlike point contact, capacitance is higher

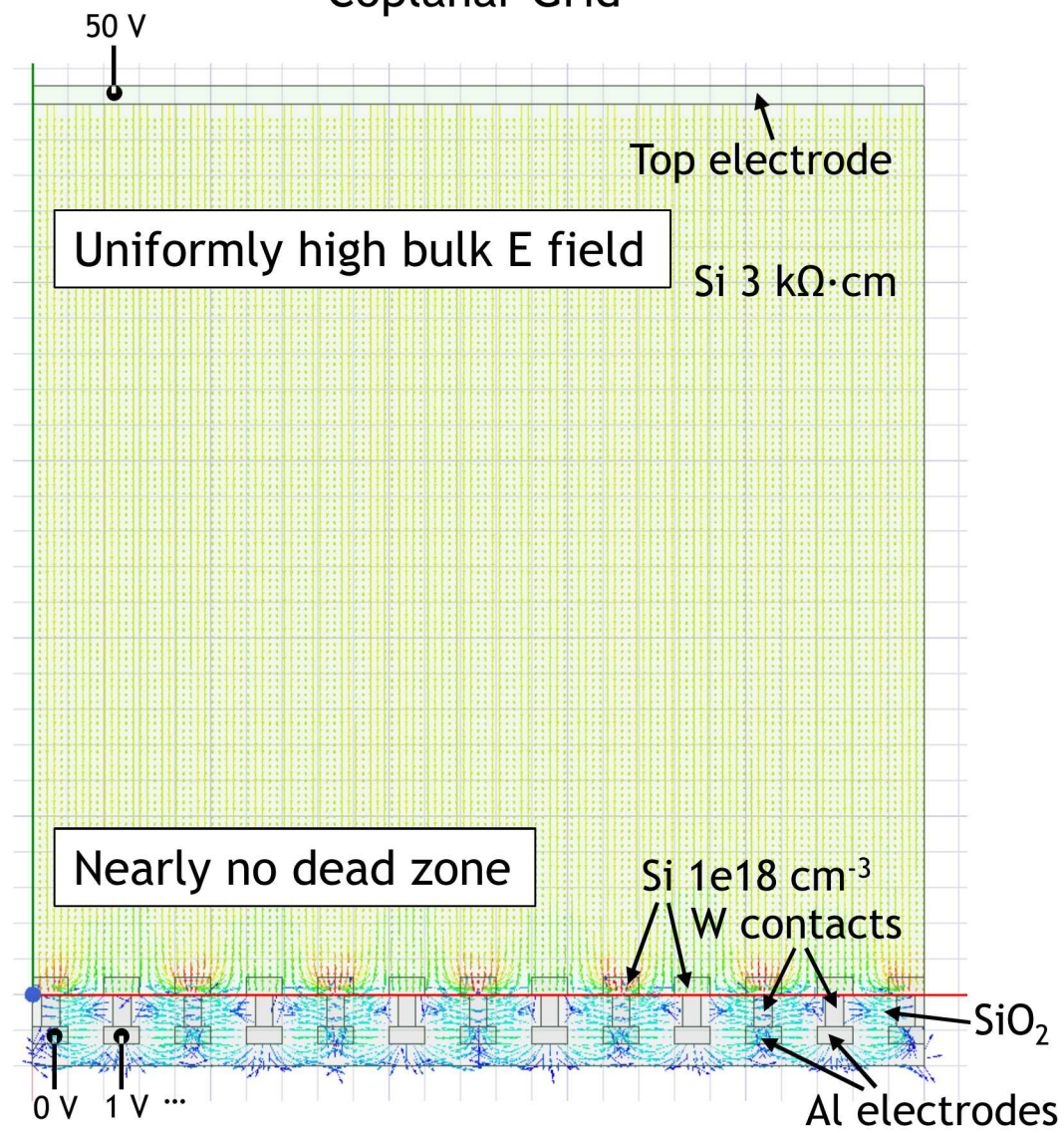
~40% reduction?

Feasibility: we can make it,
but high risk

Pixel as it is now

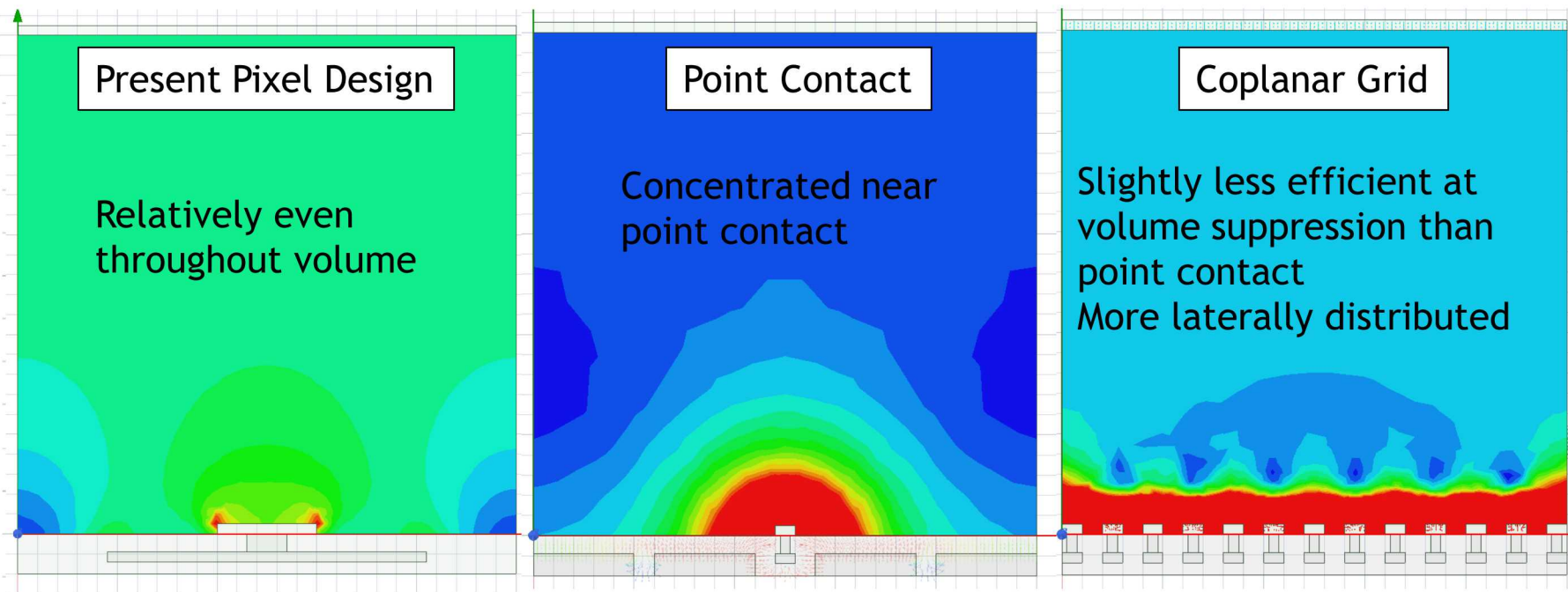
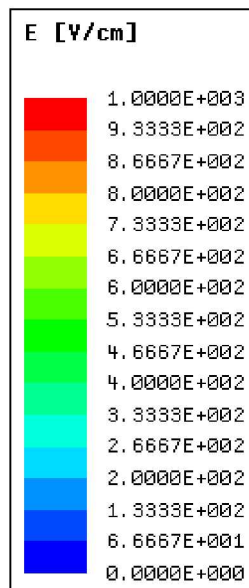


Coplanar Grid



Coplanar Grid

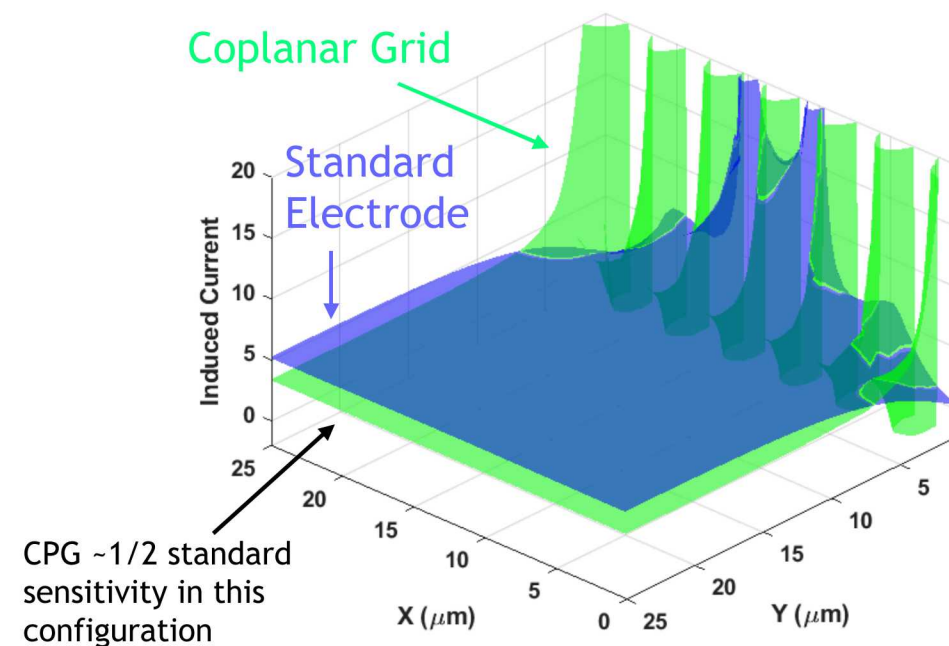
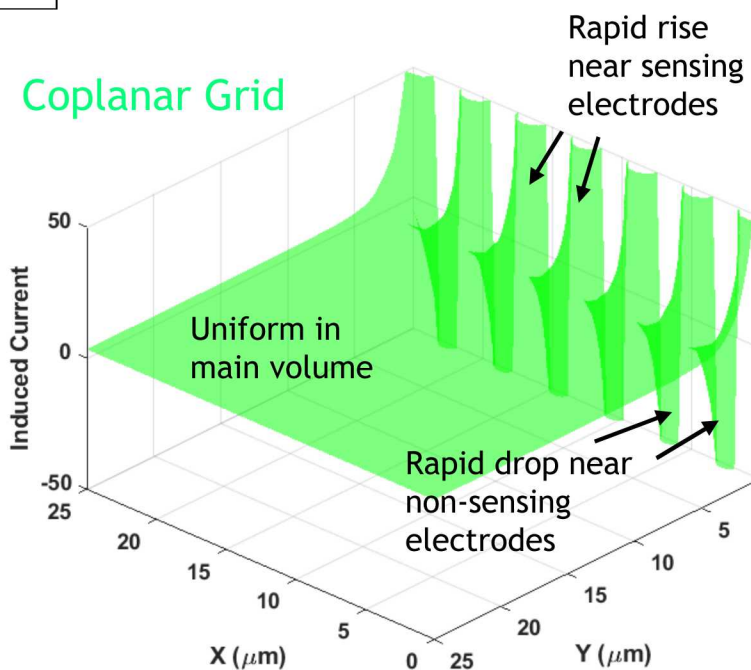
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A measure of sensitivity
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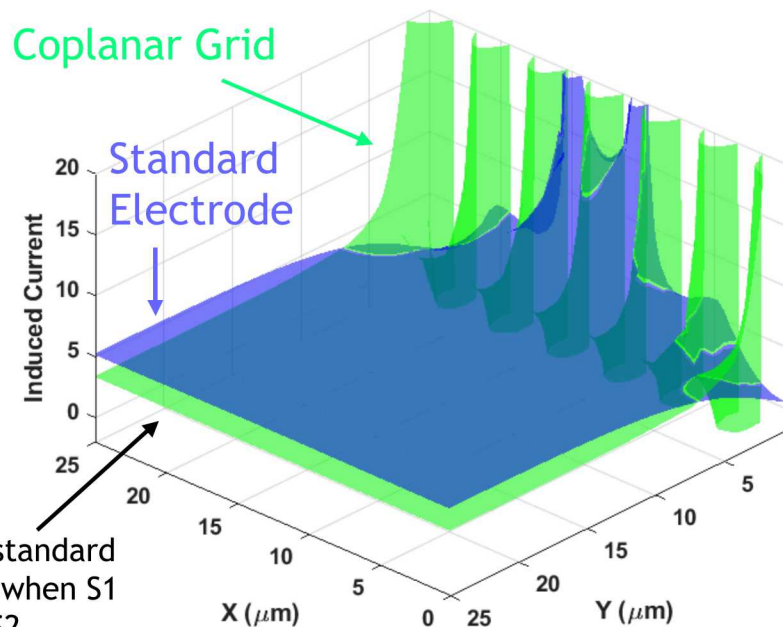
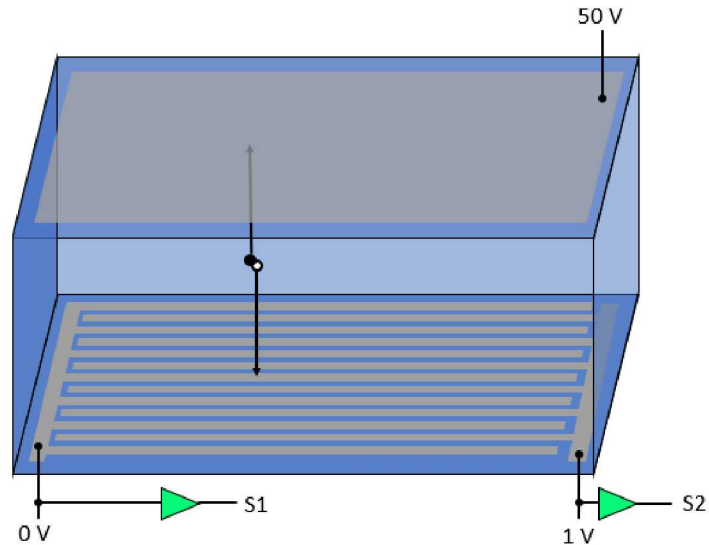
Velocity due to real field

Weighting field

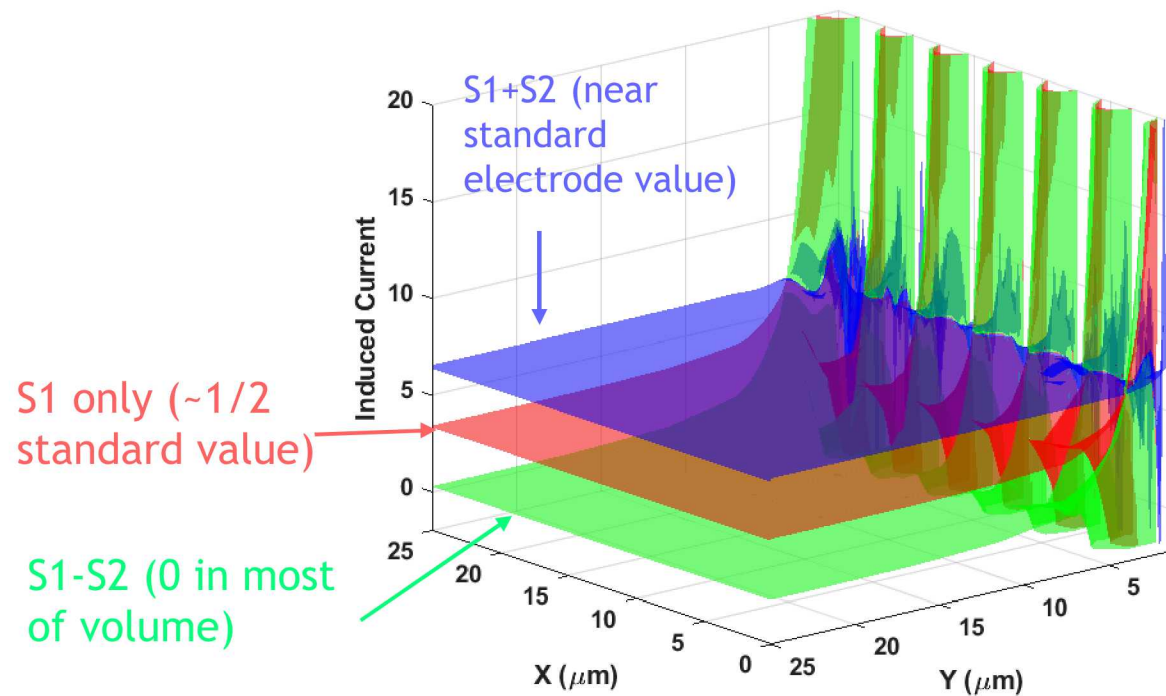


Coplanar Grid

Readout Options

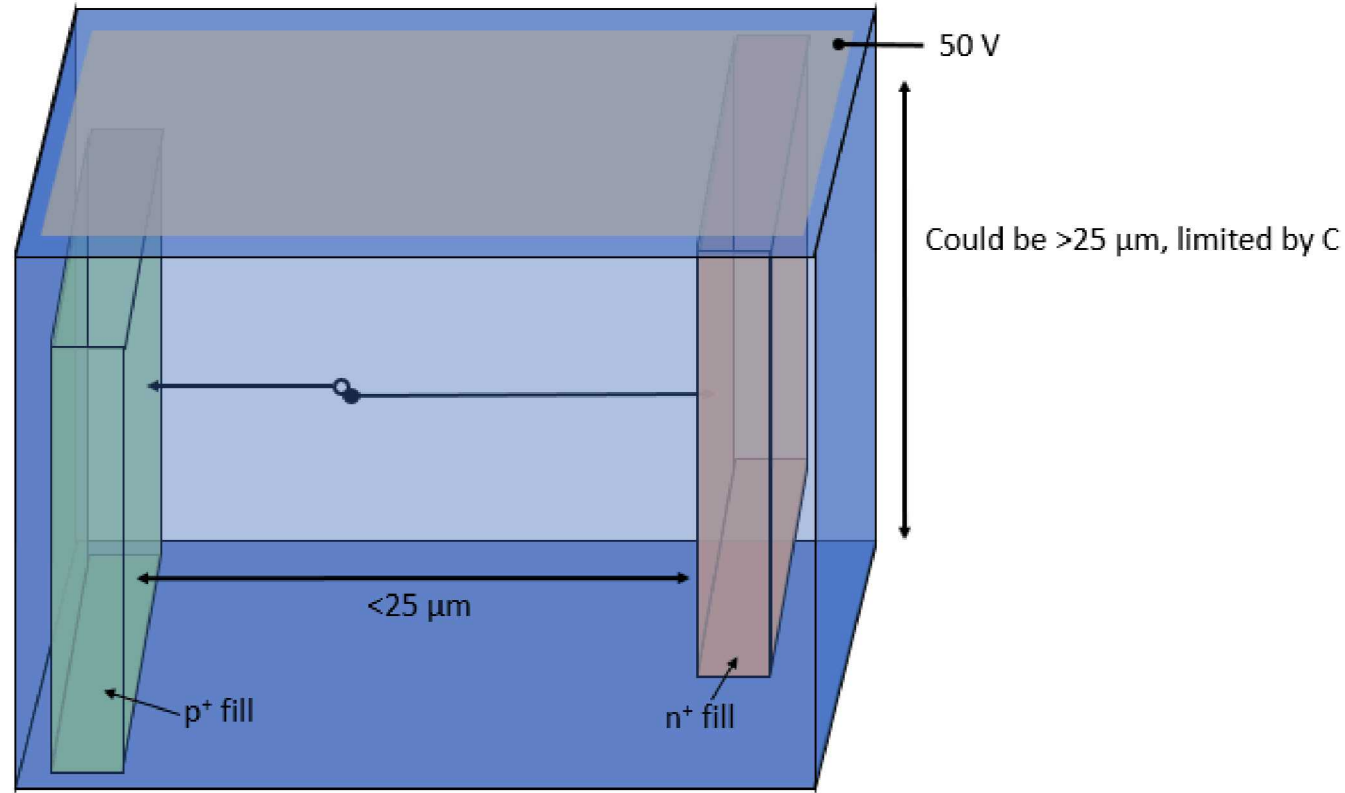


CPG $\sim 1/2$ standard sensitivity when S1 read out, S2 shunted to VRST



3D Diode (Trench)

Doped polyfill column structures described in Parker 1997, Kenney 1999, Kok 2006, etc.



Key Features

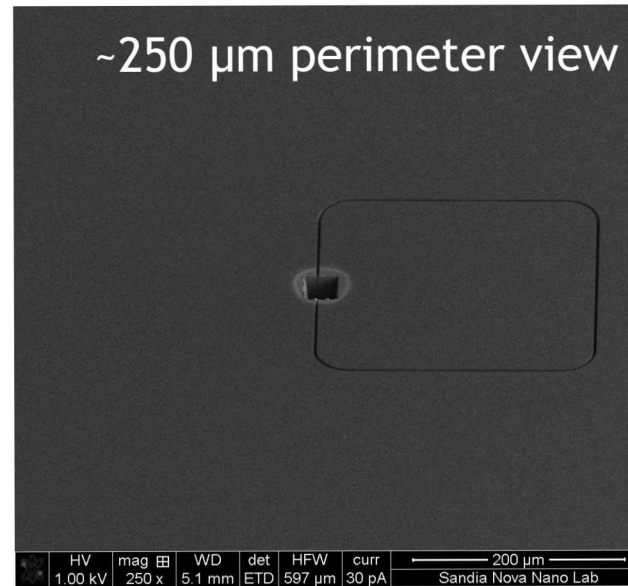
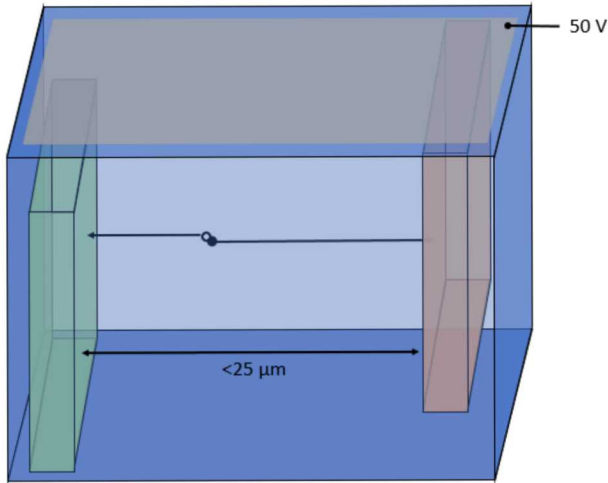
- Can select width based on desired timing; may be connected to pixel size
- Thickness can be increased to keep high QE
- Need to develop dry etch and conductive fill process for thick device layers
- 2nd electrode would need to be created after hybridization (need low T process)

~50% reduction?

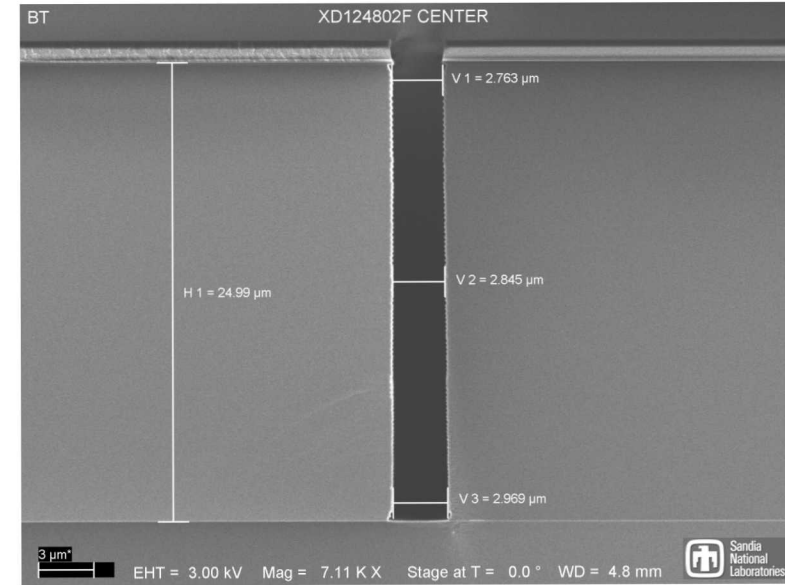
Feasibility: significant process development

3D Diode (Trench)

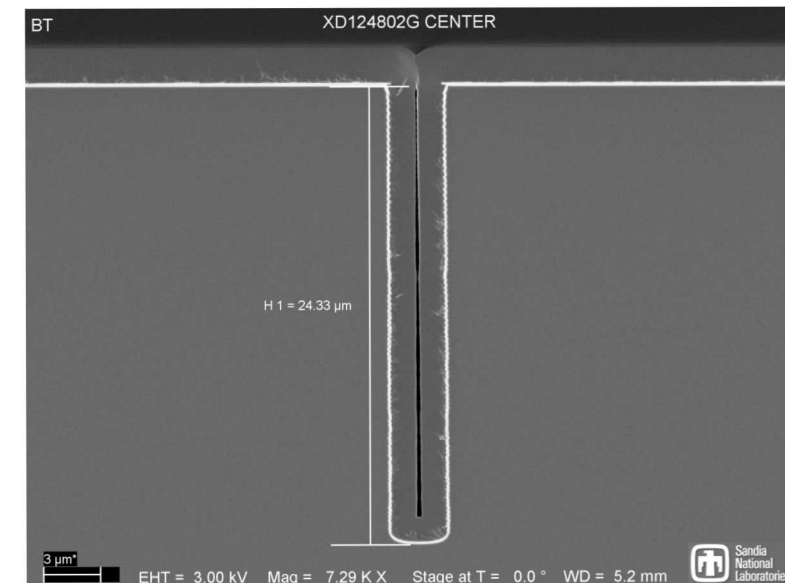
Polysilicon-filled trenches



Trench 25 μm deep with oxide stop

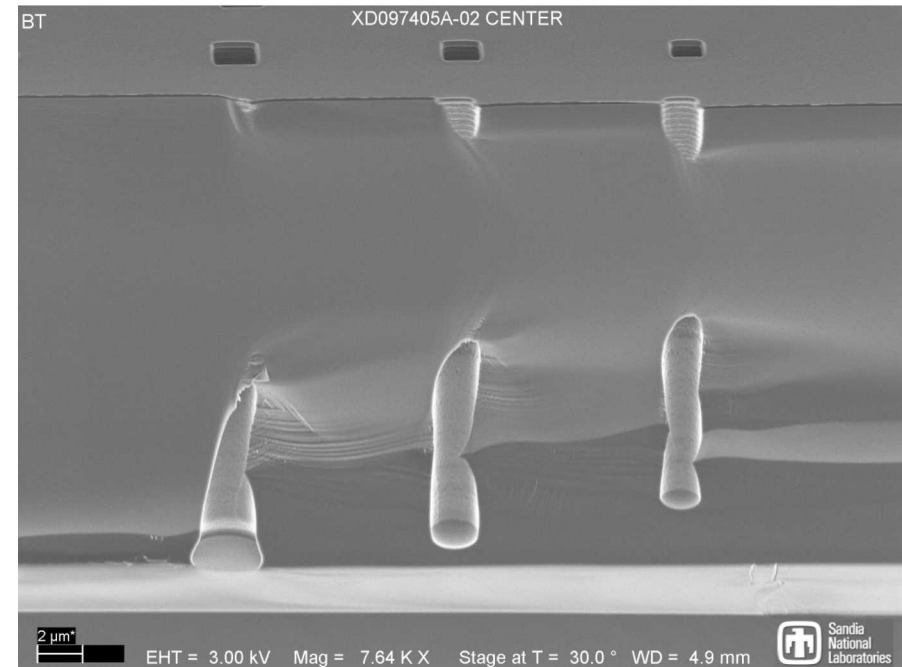
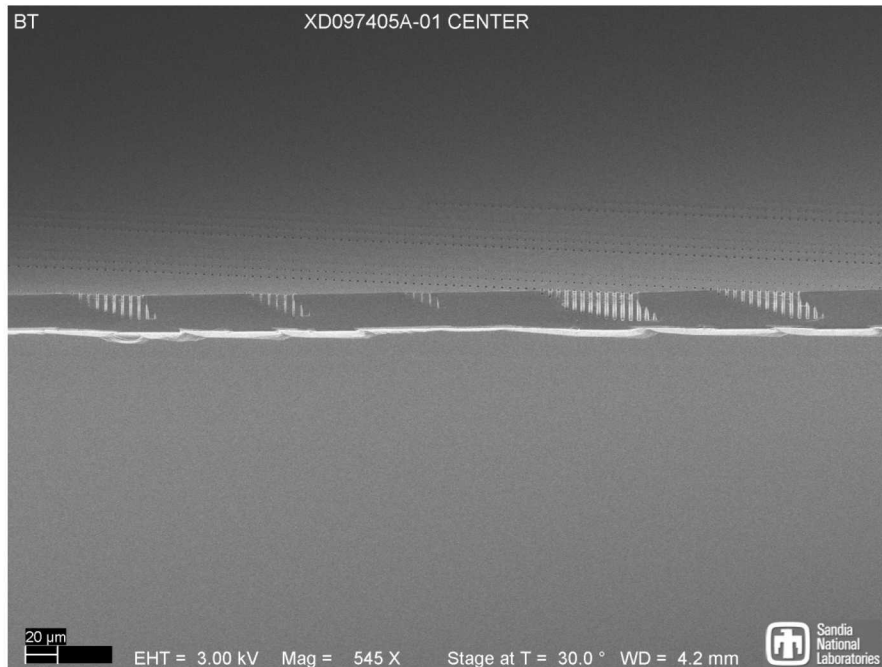
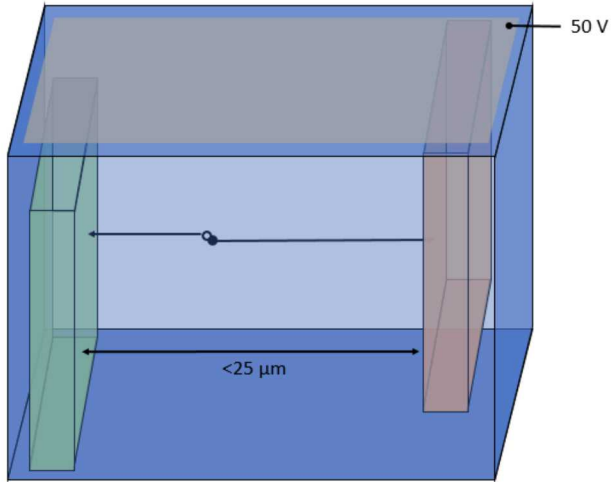


Poly-filled trench 25 μm deep

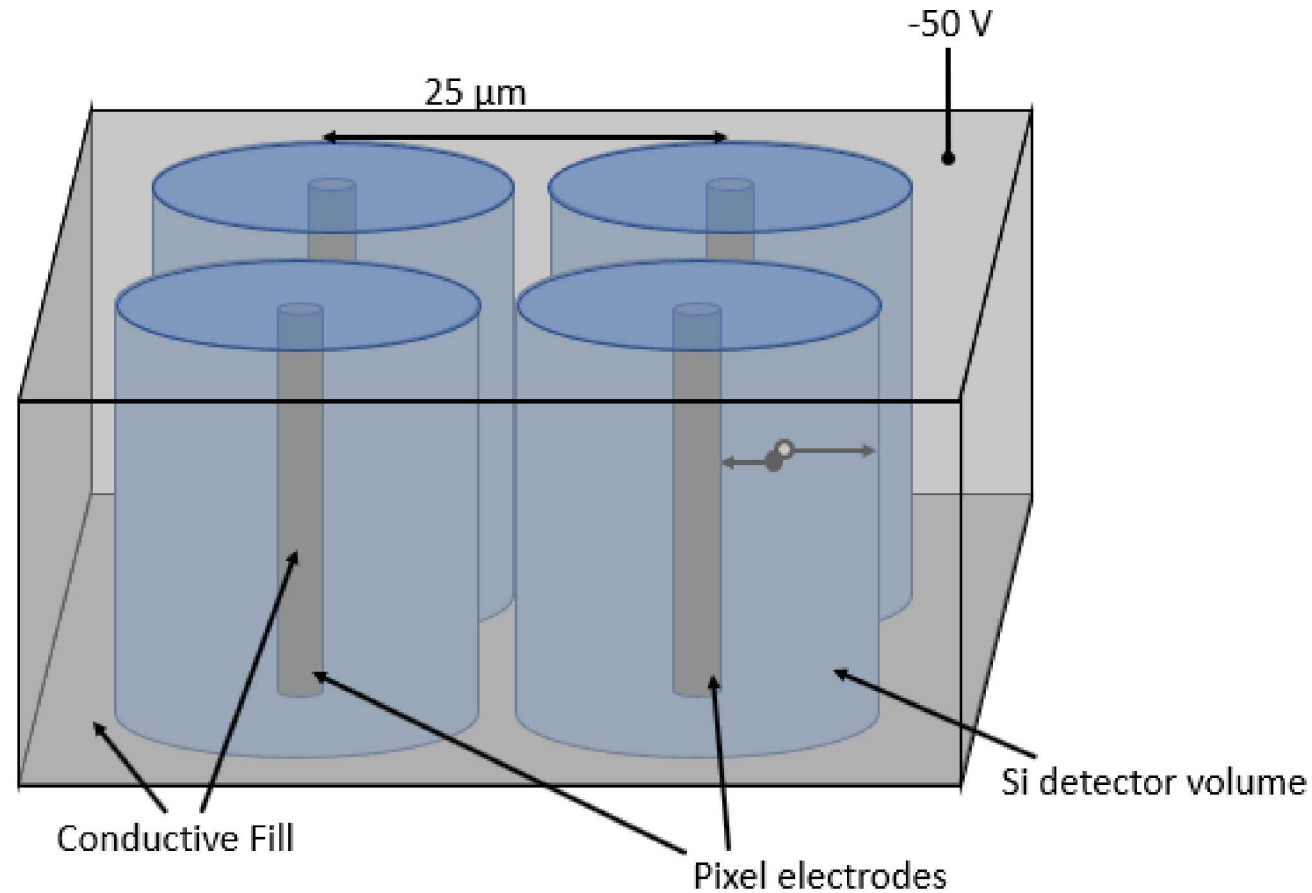


3D Diode (Trench)

2 μm holes/trenches for W fill



3D Diode (Cylinder)



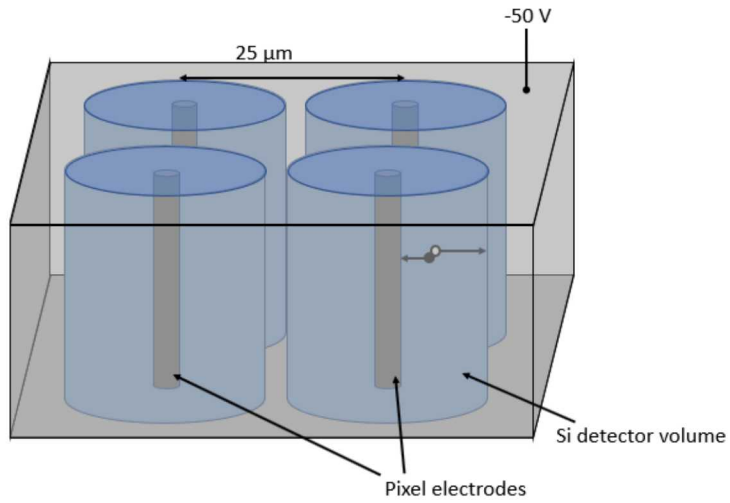
Key Features

- Need mature dry etch and conductive fill process
- Better takes advantage of geometry to reduce hole contribution to signal

~60% reduction?

Feasibility: significant
process development

3D Diode (Cylinder)



Very high field throughout

