Exceptional service in the national interest

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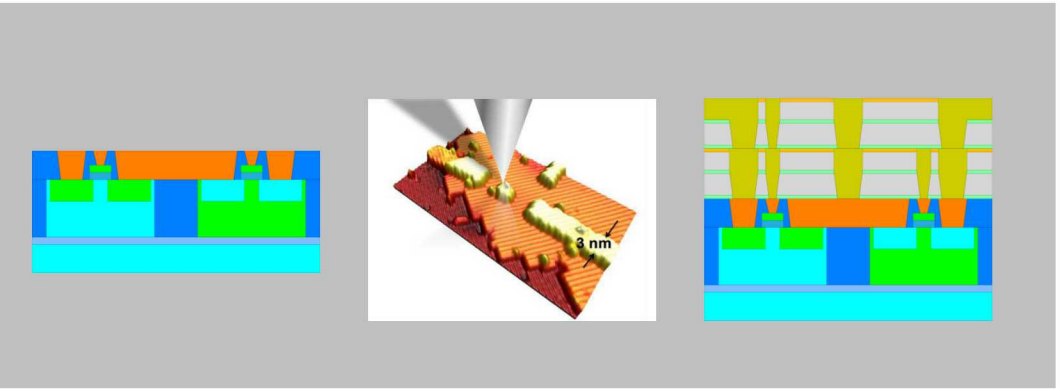

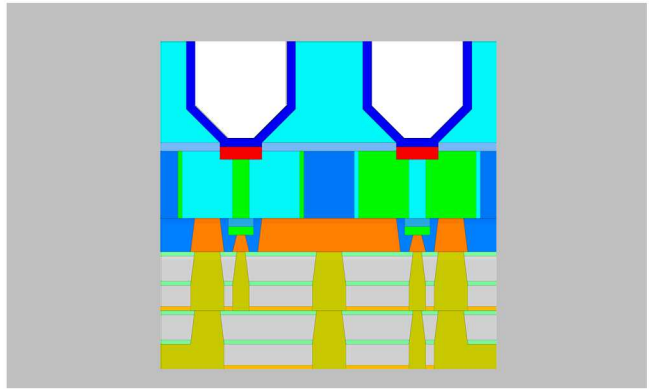

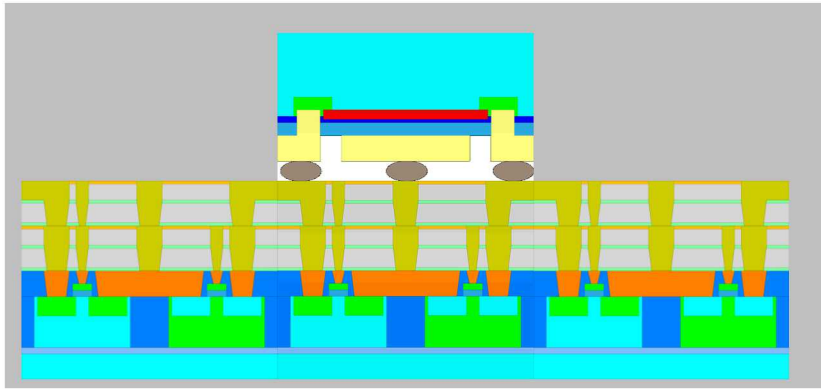

FAIR DEAL GC Thrust 3: APAM-CMOS Integration

Dan Ward, Steve Carr, Shashank Misra

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Digital electronics at the atomic limit (DEAL)

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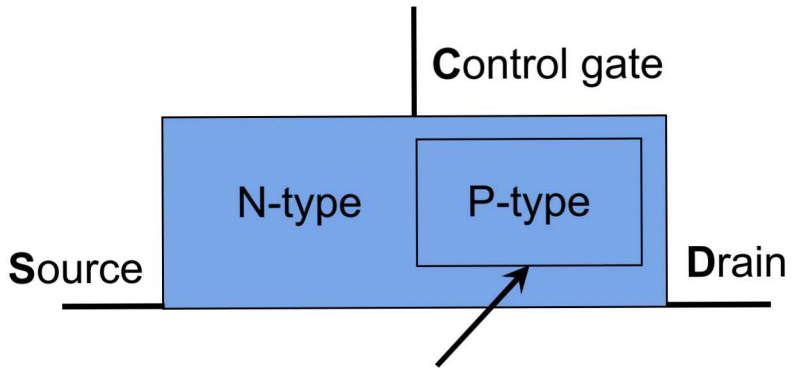
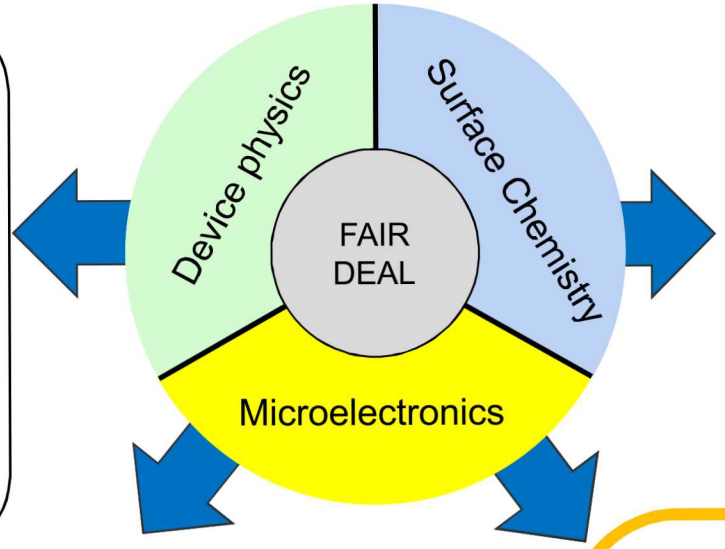
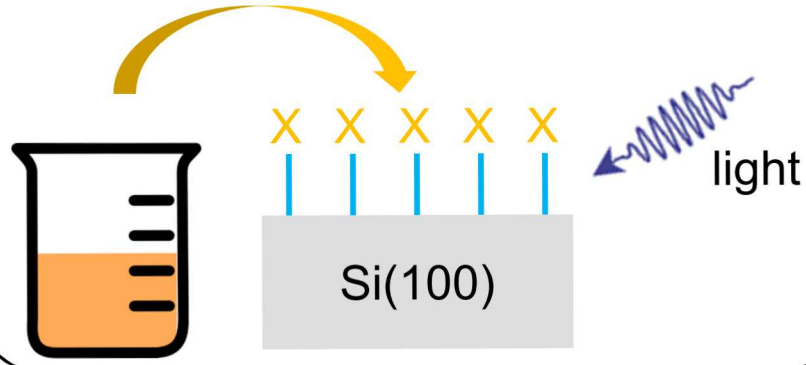
Thrust 1: APAM-enabled Devices

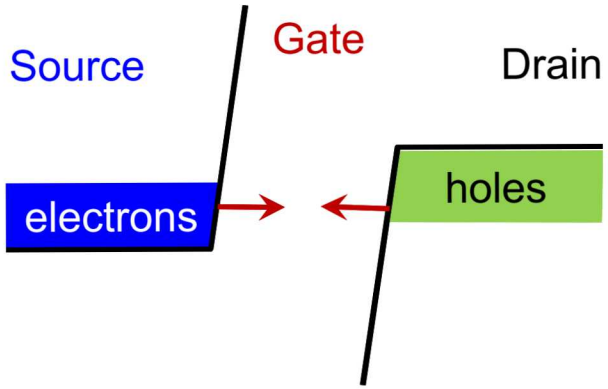




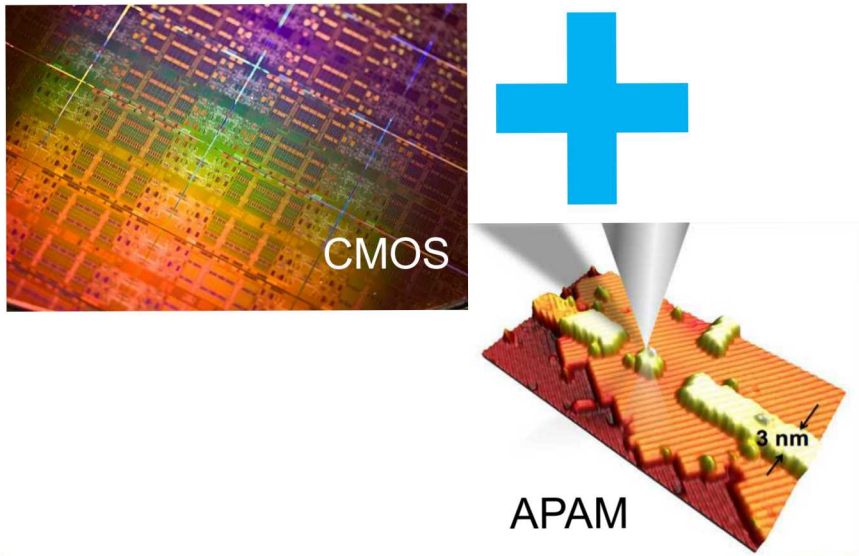
Thrust 4: Application Platform



Thrust 2: APAM Modeling



Thrust 3: CMOS Integration



CMOS Integration is critical to furthering APAM

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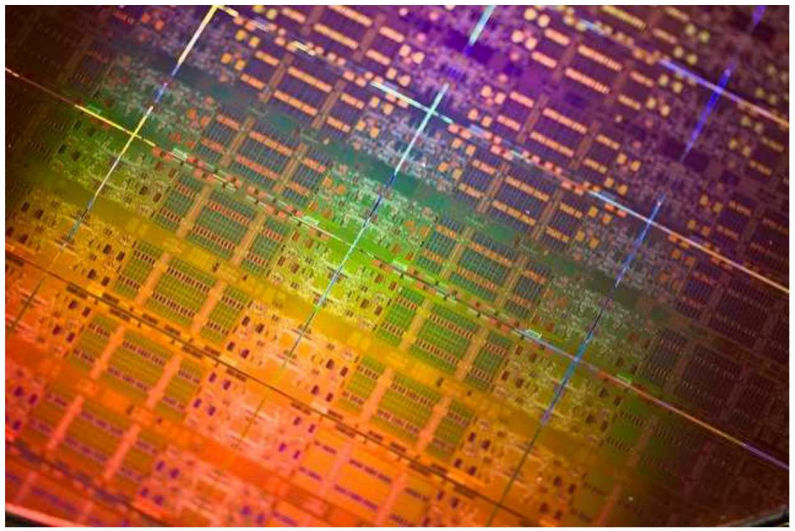
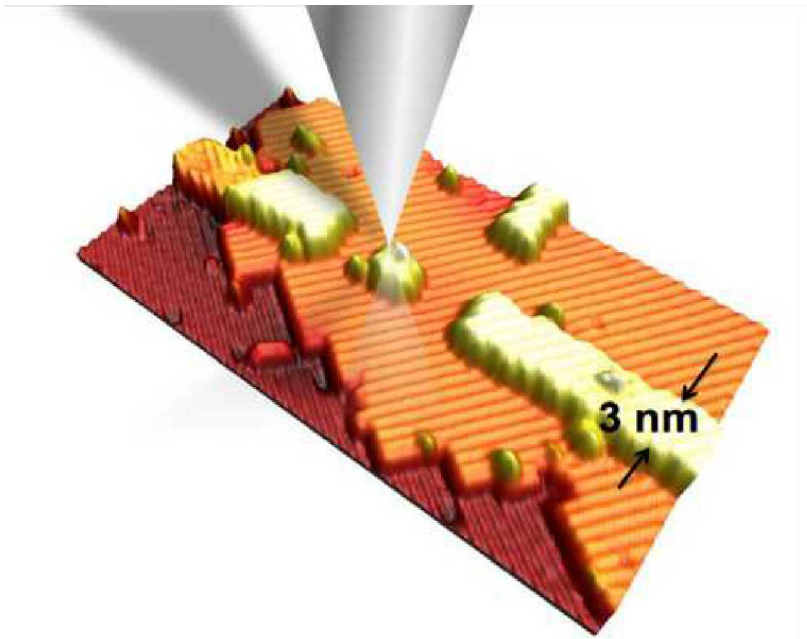
CMOS



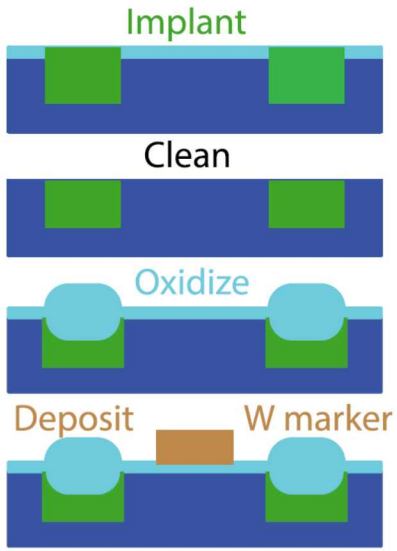
+

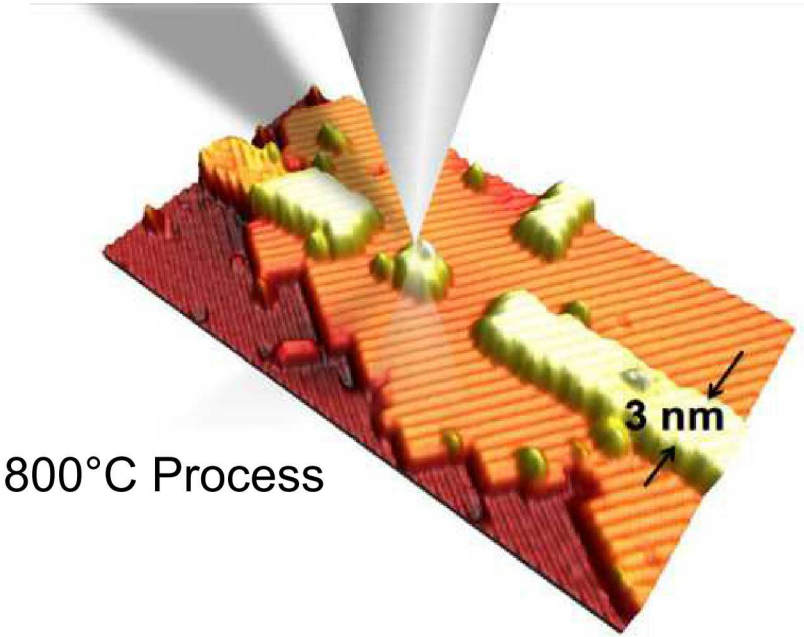
APAM



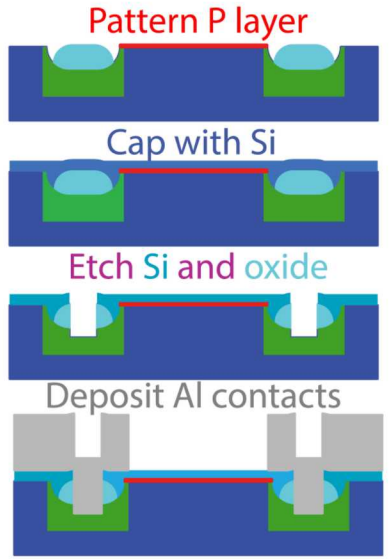
- CMOS is really good at many applications
- APAM will accelerate specific tasks
  - Not seen as a full replacement
  - Augments CMOS to provide task specific advantages
- Necessary to combine APAM and CMOS circuits to get maximum benefit

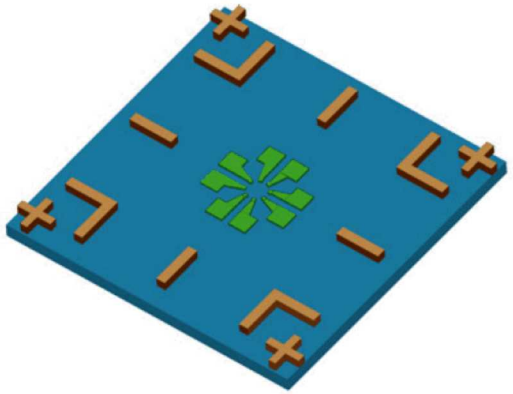
State of the Art for CMOS Integration



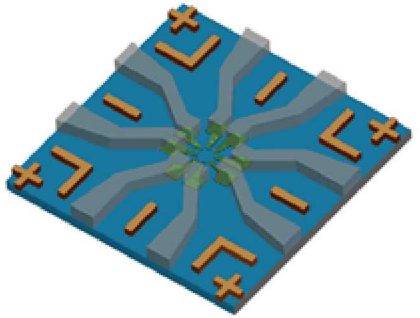


APAM 800°C Process





CMOS Integration is not impossible
Progress is being made



High T Processes (>800°C)

<300°C Processes

Thrust 3 Organizational Chart

Sandia National Laboratories

Program Leadership
PI: Shashank Misra
PM: Robert Koudelka
Deputy PM: Rick Muller

APAM-CMOS Integration
Lead: Dan Ward
CMOS Integration: Dan Ward
Reduced Temp. Processing: Shashank Misra
Heterogeneous Integration: Steve Carr

Support Team
Financial: Laurel Taylor
Logistics: Lori Mann
Web: Dorean Chaleunphonh
Administrative: Felicia Pena

Capabilities

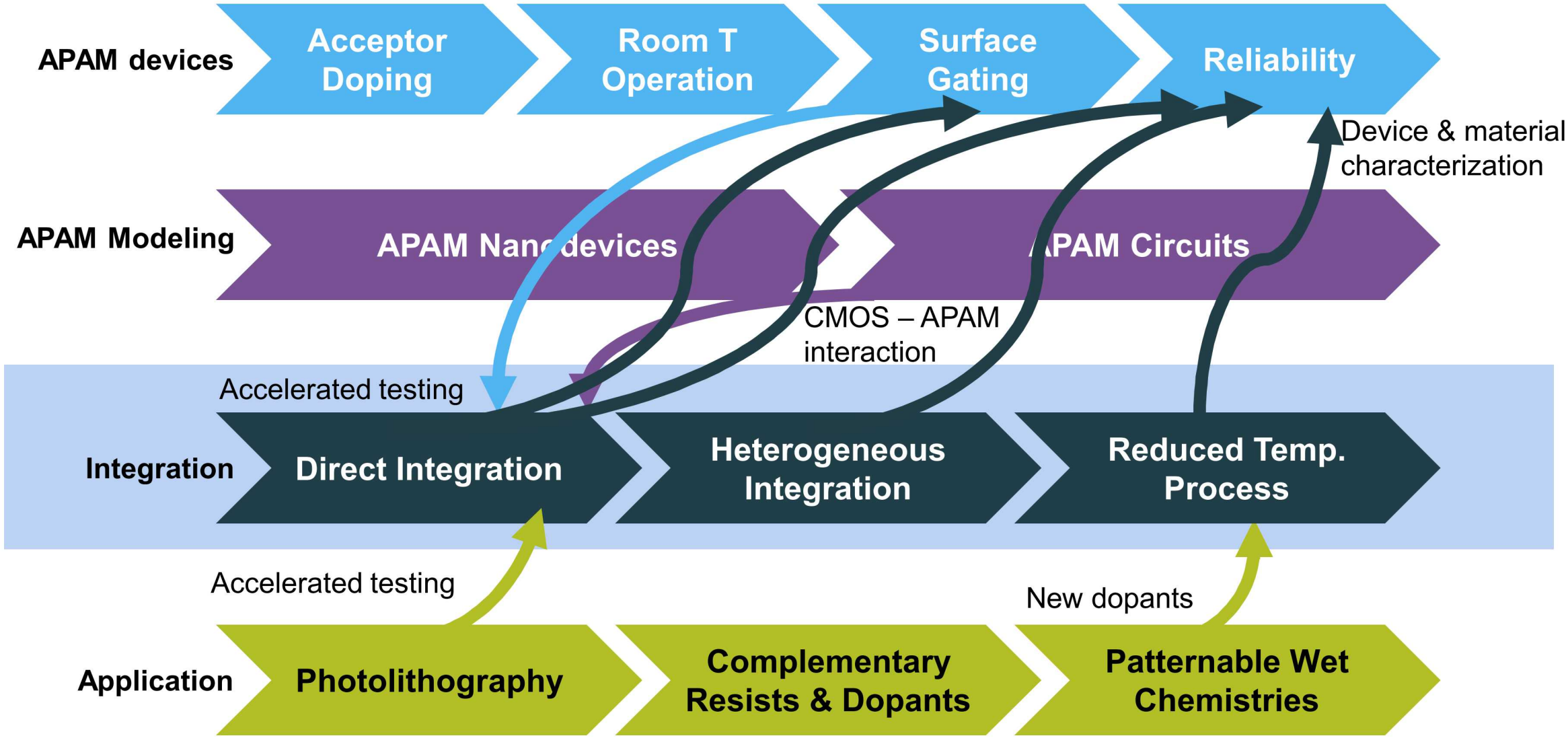
Measurement: Lisa Tracy, Tzu-Ming Lu**, David Scrymgeour**, **Ping Lu**, **Albert Grine**

Microfabrication: Dan Ward, DeAnna Campbell, Mark Gunter, Steve Carr, **Sean Smith**

Modeling: Denis Mamaluy, **Suzey Gao**, Leon Maurer, Andrew Baczewski, Peter Schultz, Quinn Campbell

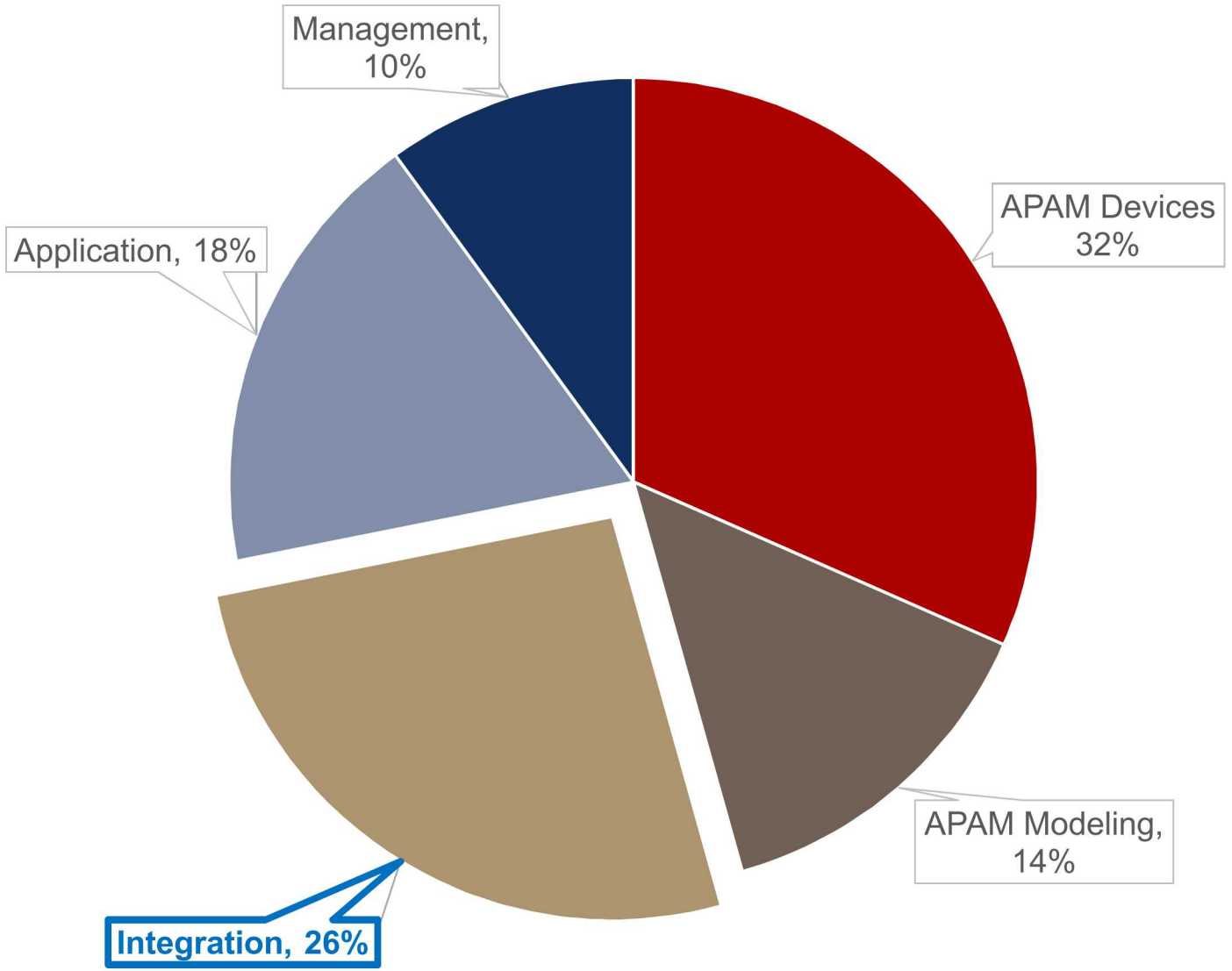
Surface Science: Shashank Misra, Ezra Bussmann**,** George Wang, **Aaron Katzenmeyer, Evan Anderson,** Bob Butera, Dave Wheeler

Thrust 3 Interactions

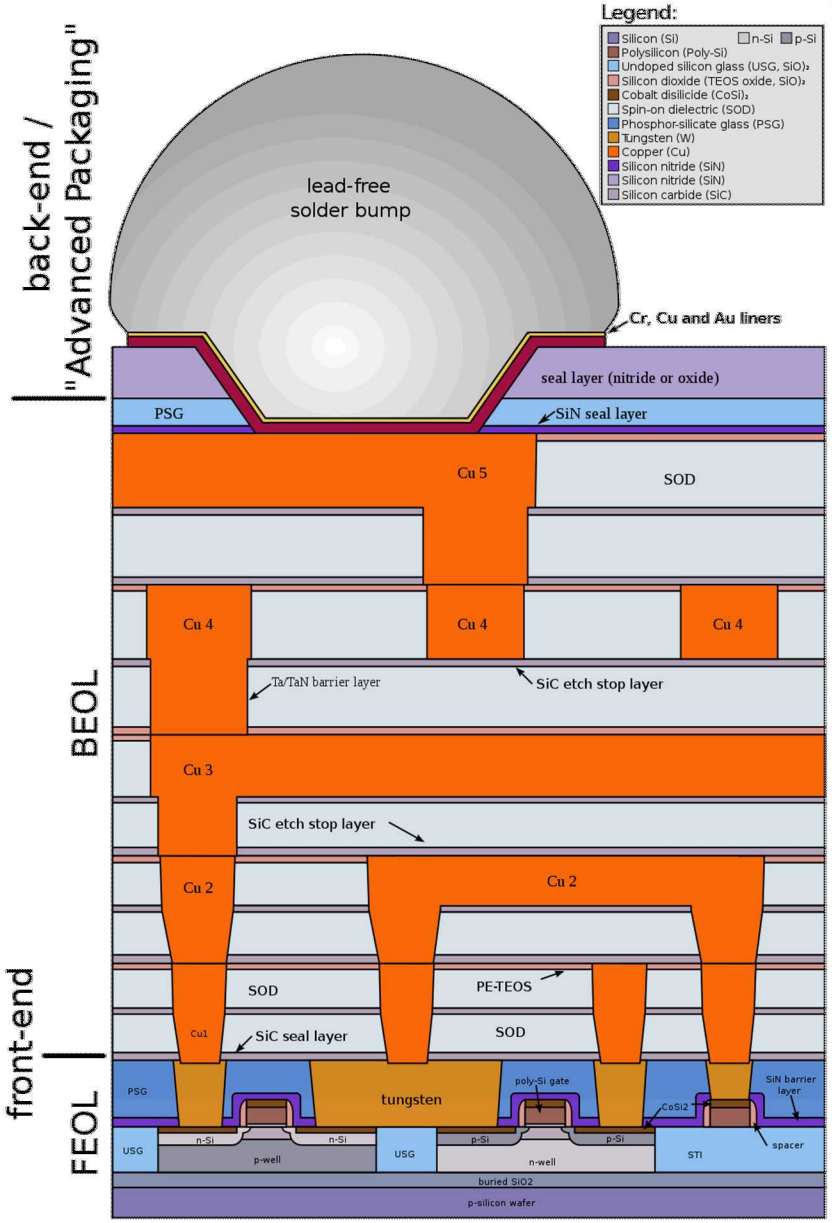


Thrust 3: Resources

Majority of funding split between fabrication and measurement



Quick Terminology Review



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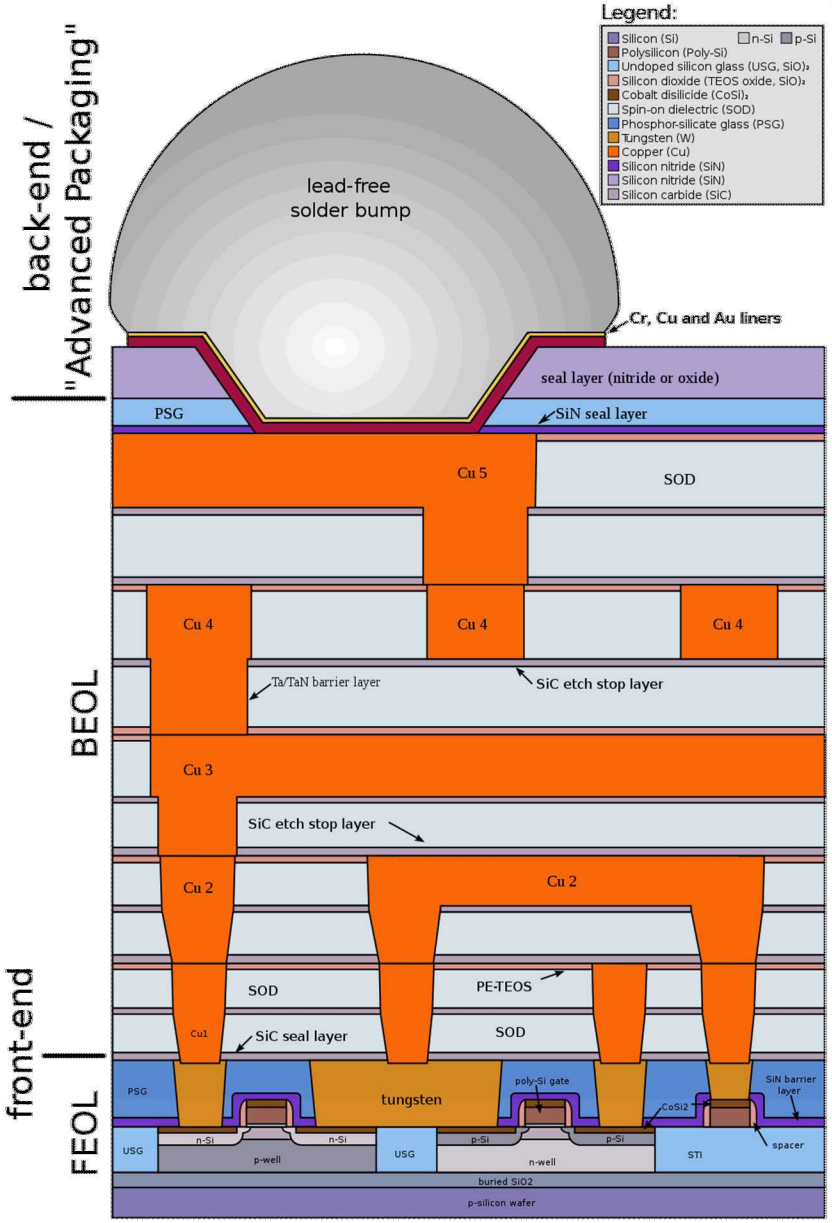
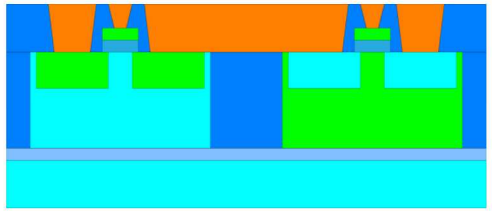
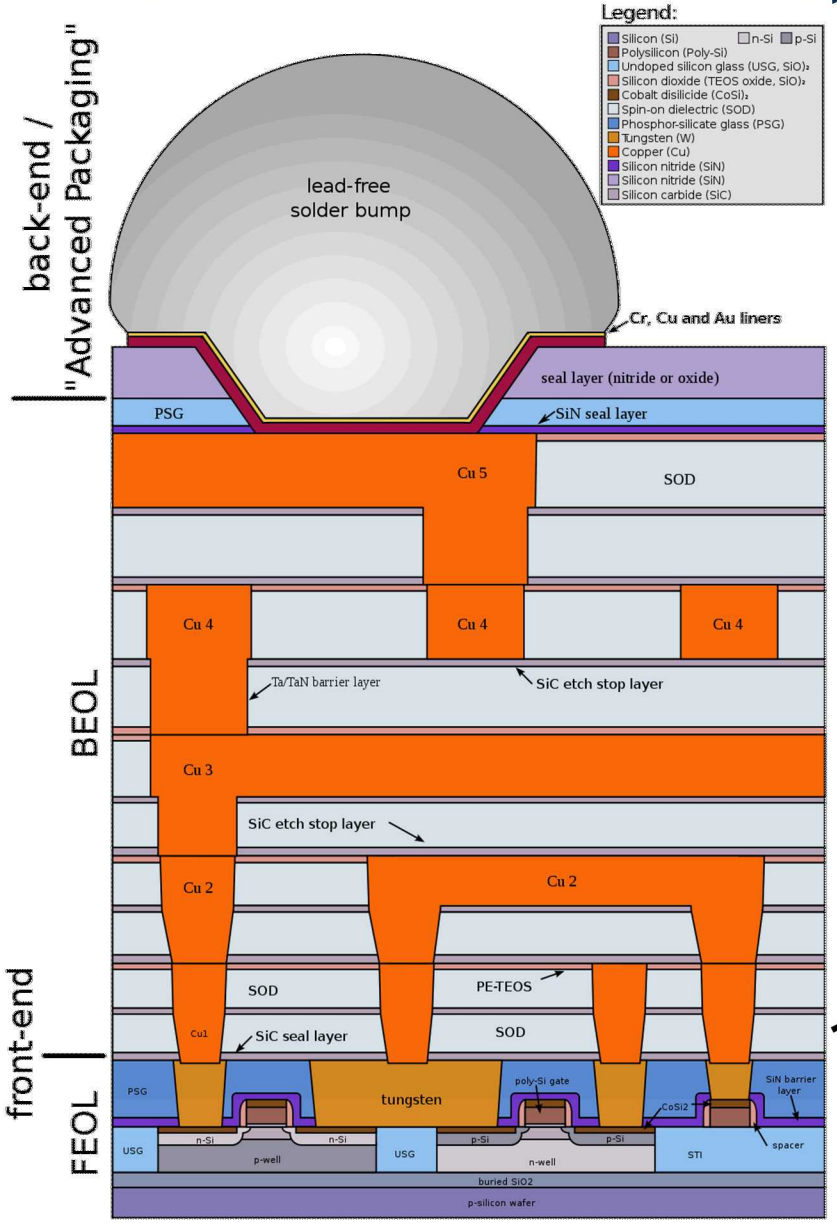


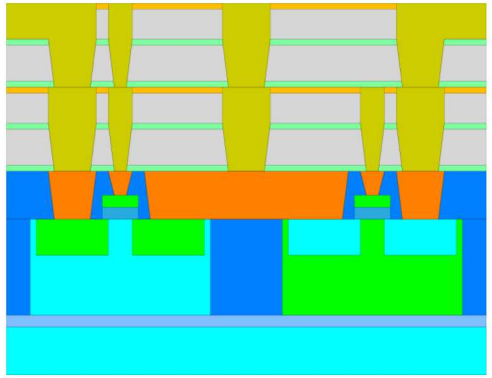


CMOS through FEOL

No metal present other than tungsten plugs
Thermal budget >800°C

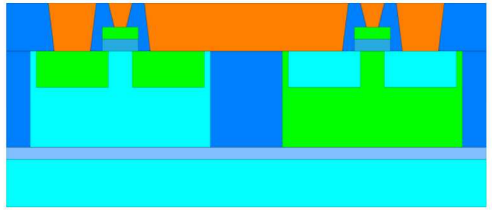
Quick Terminology Review





CMOS through BEOL

All metal layers completed
Thermal budget limited to <450°C



CMOS through FEOL

No metal present other than tungsten plugs
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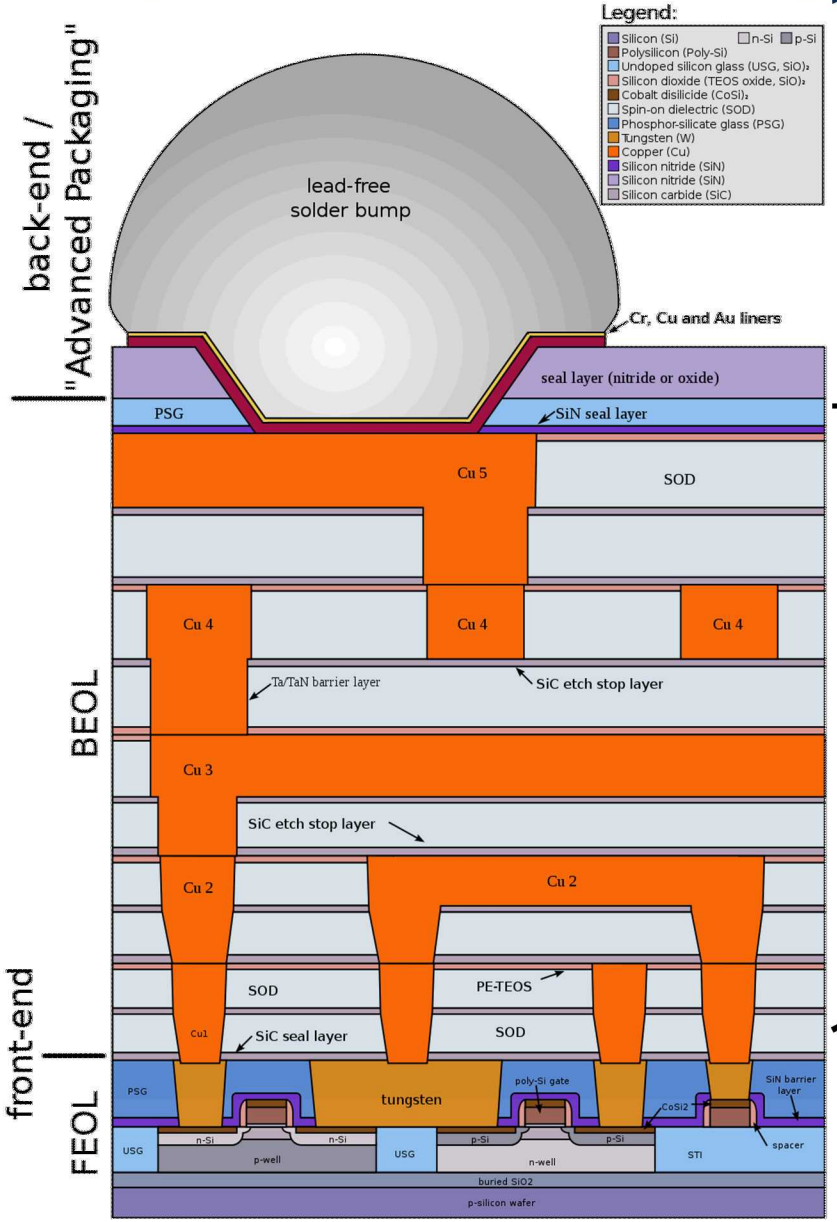
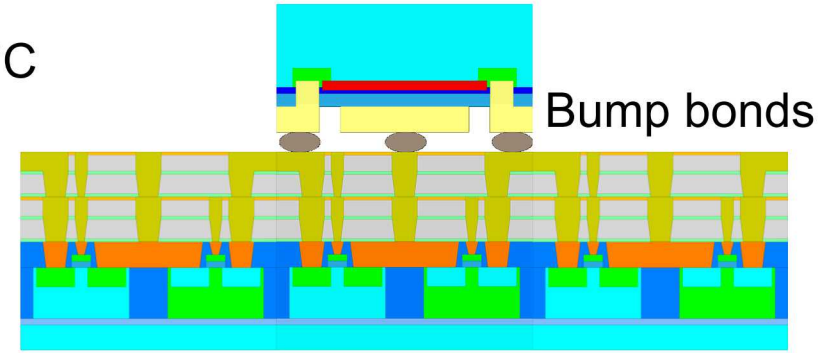
Quick Terminology Review



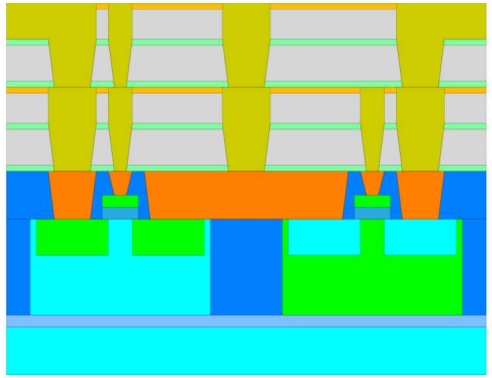
Device completed, die-to-die or wafer-to-wafer bonding allowed
Thermal budget limited to <450°C

APAM Die (Inverted)



Bump bonds

CMOS Die



CMOS through BEOL

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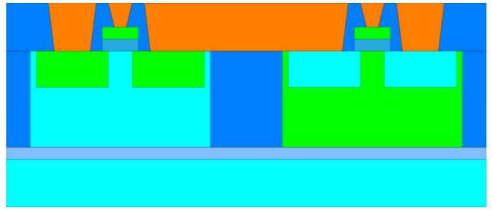

CMOS through FEOL

No metal present other than tungsten plugs
Thermal budget >800°C

How do we interface APAM devices with CMOS?

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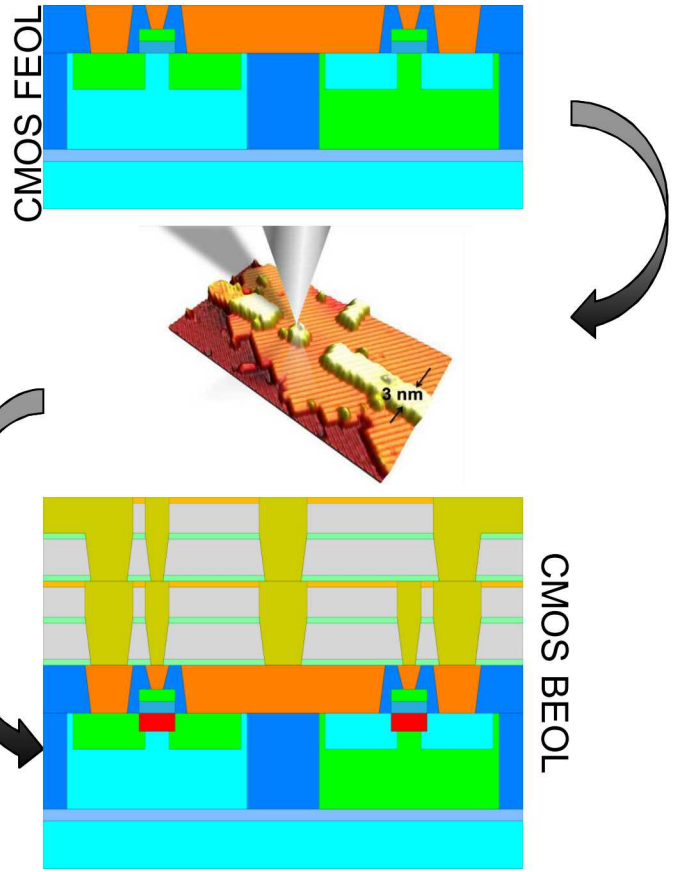
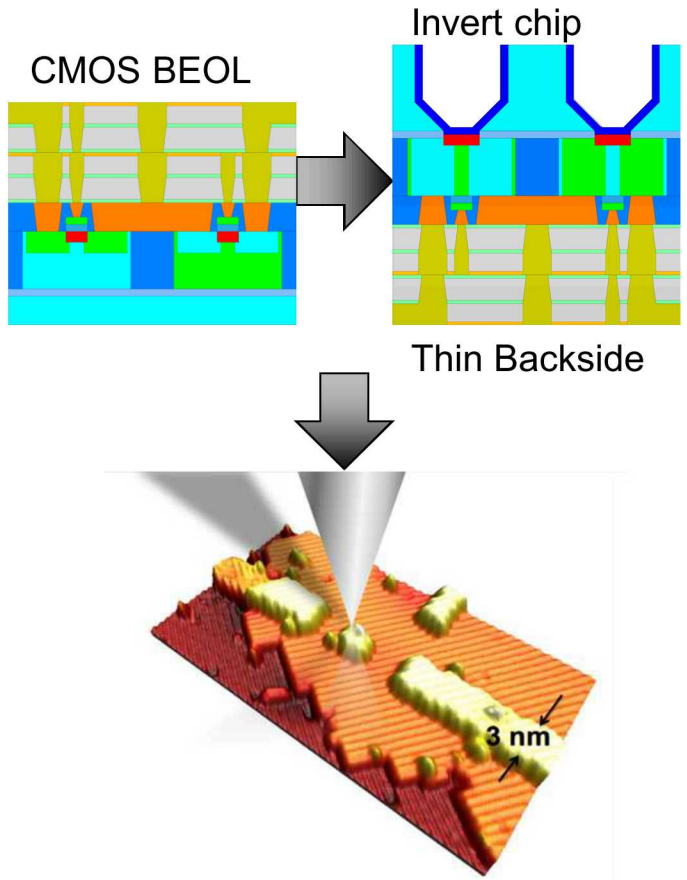
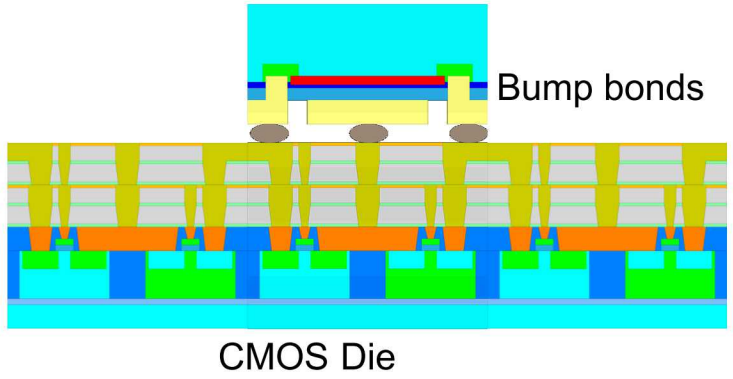
Direct CMOS-APAM integration



Reduced temperature processing



Heterogeneous integration



Increasing level of risk

Increasing level of development time

Parallel Integration Paths Tested With Common Approach

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Leverage SNL device libraries and design capabilities

CMOS / APAM Die Design

Common set of diagnostic devices used to assess all paths (Hall, CV, etc.)

Direct CMOS-APAM integration

APAM occurs between FEOL and BEOL

Reduced temperature processing

APAM occurs after BEOL

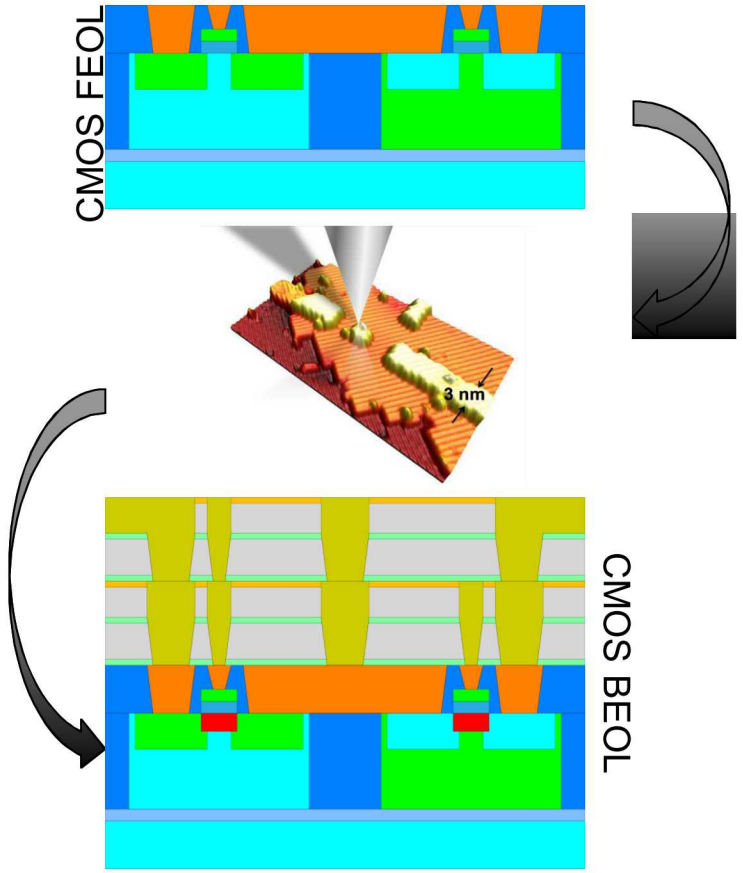
Heterogeneous integration

APAM occurs in custom flow

How do APAM devices perform?

How do CMOS devices perform?

Direct CMOS-APAM Integration Advantages



Advantages:
- Maximum integration with CMOS part
- APAM devices anywhere
- Best APAM quality/performance

Challenges:
- Potential fabrication process conflicts
- No single “CMOS” process flow
- Foundry accommodation of APAM process

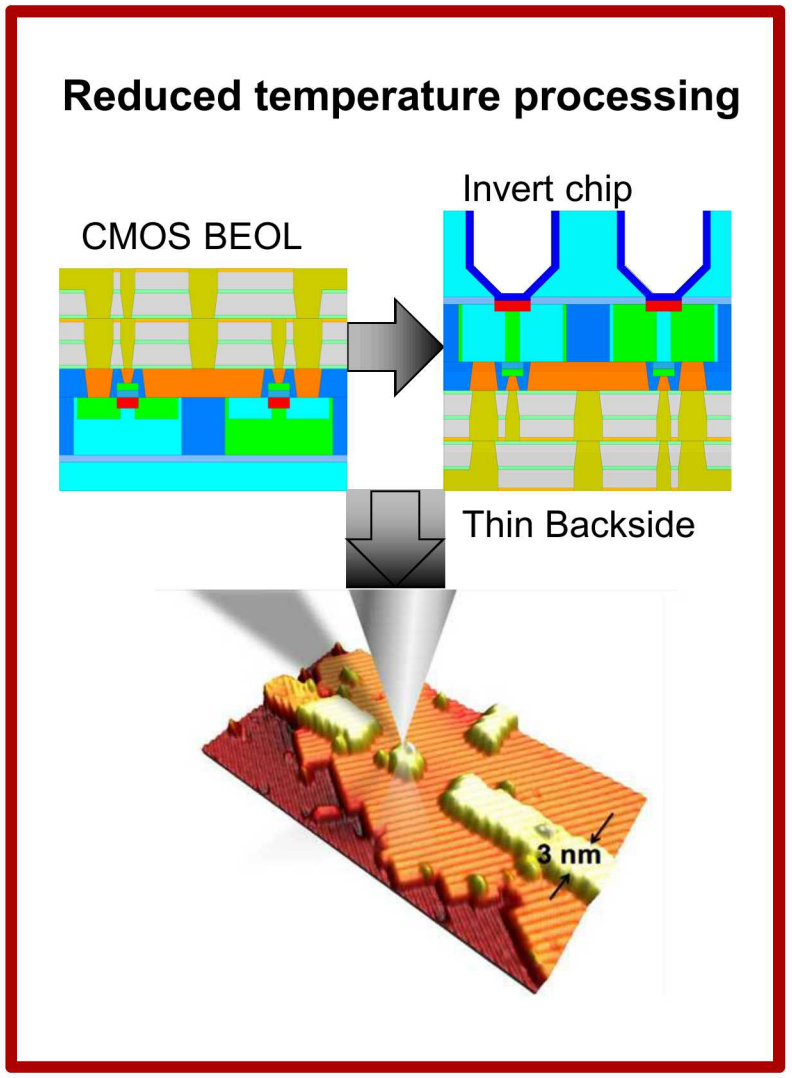
Impact:
- Highest impact of all paths → Best APAM quality
- Path to a CMOS module
- Platform for photolithography and wet chemistry integration (Thrust 4)
- Opens a potential application space → Supply chain assurance

Reduced Temperature Processing

Advantages:
- No CMOS foundry accommodation of APAM process/tools
- No need to modify CMOS processes

Challenges:
- Backside fabrication for APAM
- Lower temperature APAM
  - Lower resolution
  - Lower quality materials

Impact:
- Path to post CMOS-fabrication addition of APAM devices without foundry support
- Open a potential application space → Supply chain assurance



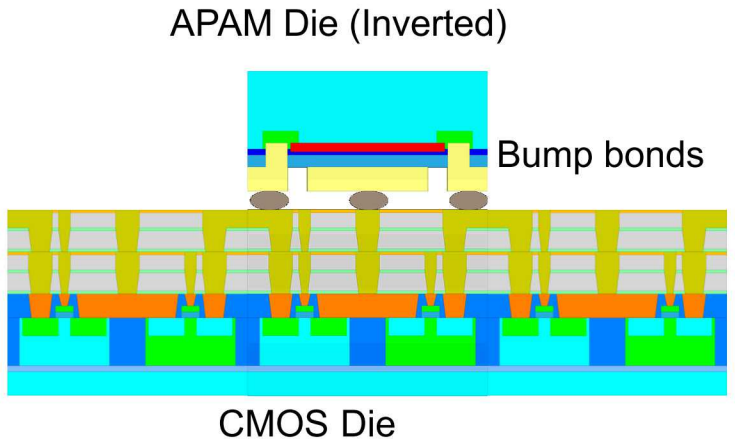
Heterogeneous Integration

Advantages:
- Quickest path to CMOS-APAM integration
- Does not alter CMOS process flow

Challenges:
- Chip-chip or wafer-wafer bonding required

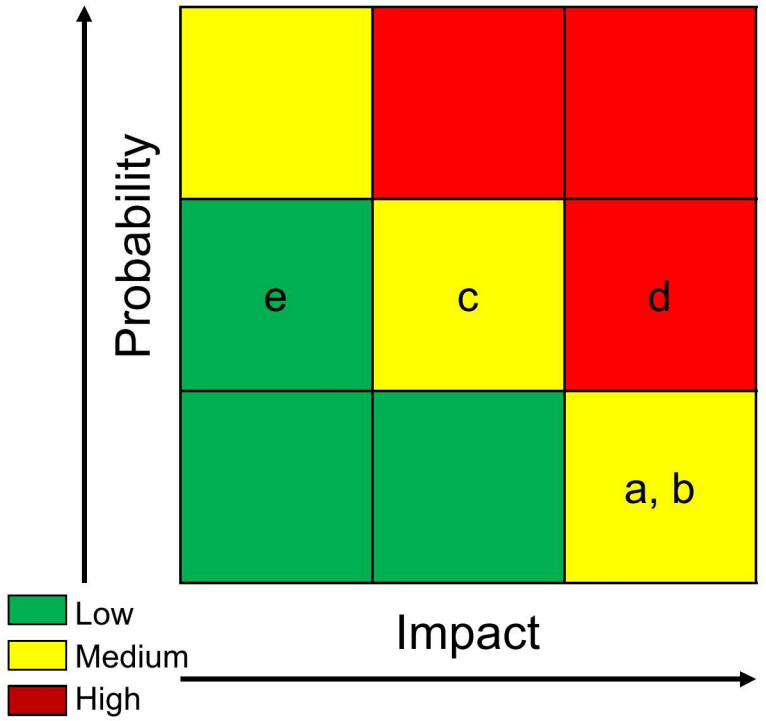
Impact:
- APAM accelerated chiplets to enhance CMOS performance

Heterogeneous integration



Multiple paths spread out risks

- Direct CMOS-APAM Integration
  - a) Incompatible thermal budgets for CMOS and APAM
  - b) Incompatible process flows
- Reduced Temperature Processing
  - c) Unable to sufficiently reduce APAM processing temperatures
  - d) Backside thinning results in APAM incompatible surfaces
- Heterogeneous Integration
  - e) Advanced heterogeneous integration techniques are incompatible with APAM processing



Year 1 Objectives

- Direct CMOS-APAM Integration
  - Design STM compatible CMOS diagnostic chip
  - Evaluate thermal budget of CMOS chip *ex-situ*
  - Evaluate thermal budget of CMOS chip *in-situ*

- Reduced temperature processing
  - Evaluate room temperature hydrogen termination
  - Develop lower temperature surface cleans
  - Demonstrate APAM recipes on thinned silicon

- Heterogenous integration
  - System-in-package demonstration
  - Plan bump bonding scheme

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Do process flows exist where APAM can directly integrated into CMOS flow?

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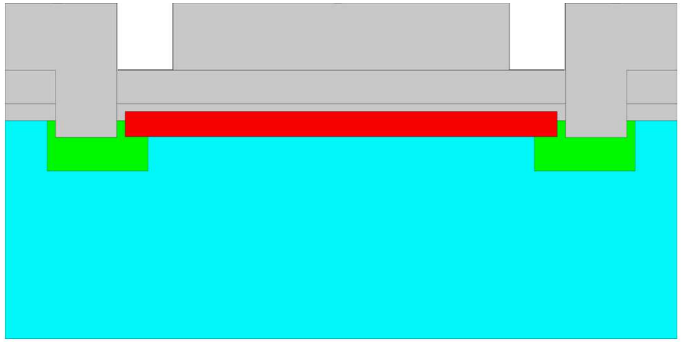
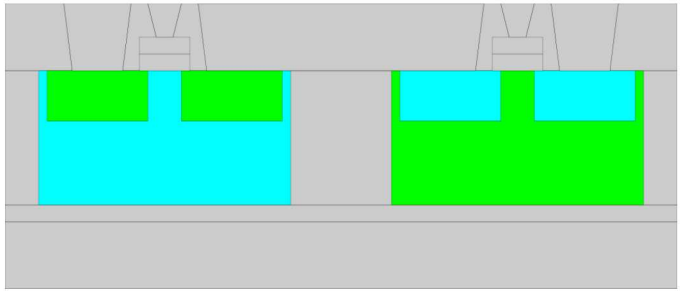
Current APAM Devices



CMOS FEOL Transistor



N-type Si P-type Si APAM

Do process flows exist where APAM can directly integrated into CMOS flow?

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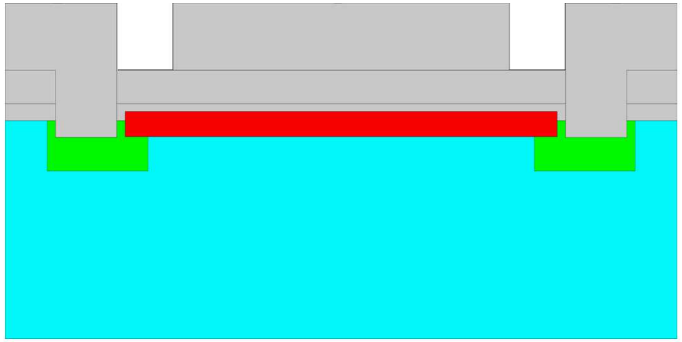
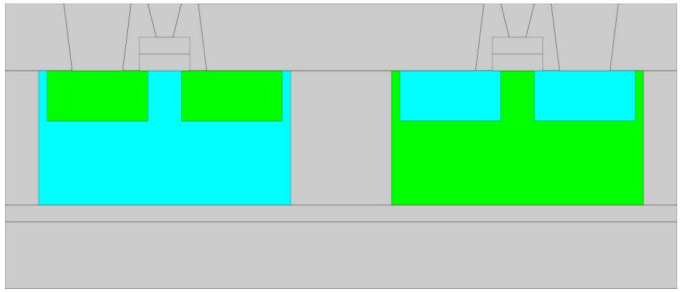
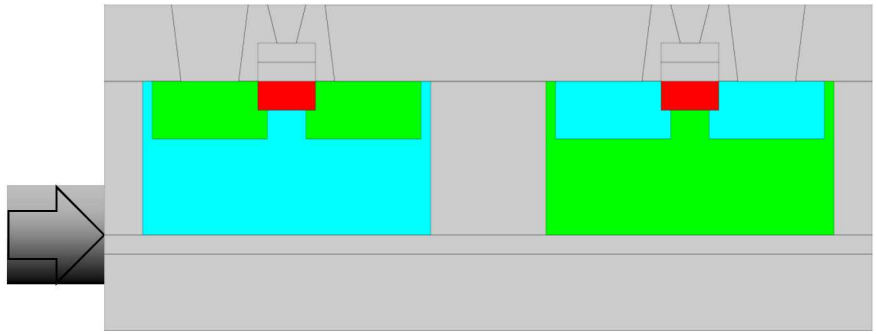
Current APAM Devices



CMOS FEOL Transistor



CMOS/APAM Device



Subject FEOL CMOS to APAM process flow

1. Cleans
2. H-termination
3. Donor doping
4. Donor incorporation
5. Si capping

N-type Si P-type Si APAM

Do process flows exist where APAM can directly integrated into CMOS flow?

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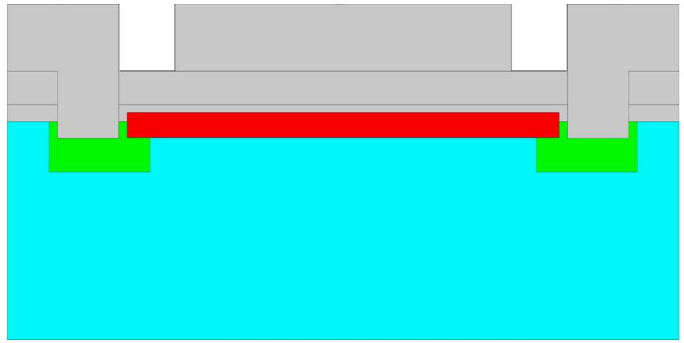
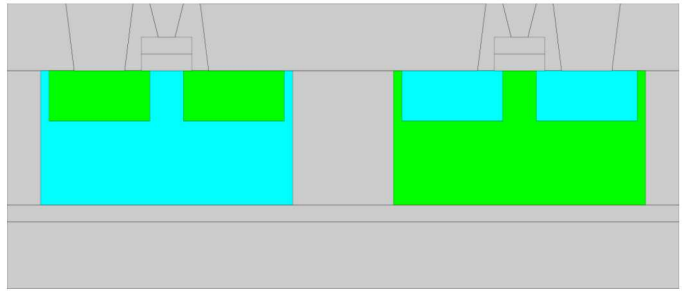
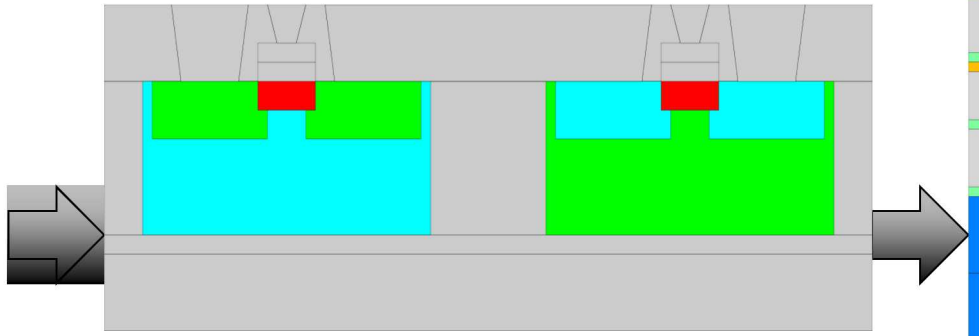
Current APAM Devices



CMOS FEOL Transistor



CMOS/APAM Device



Subject FEOL CMOS to APAM process flow

1. Cleans
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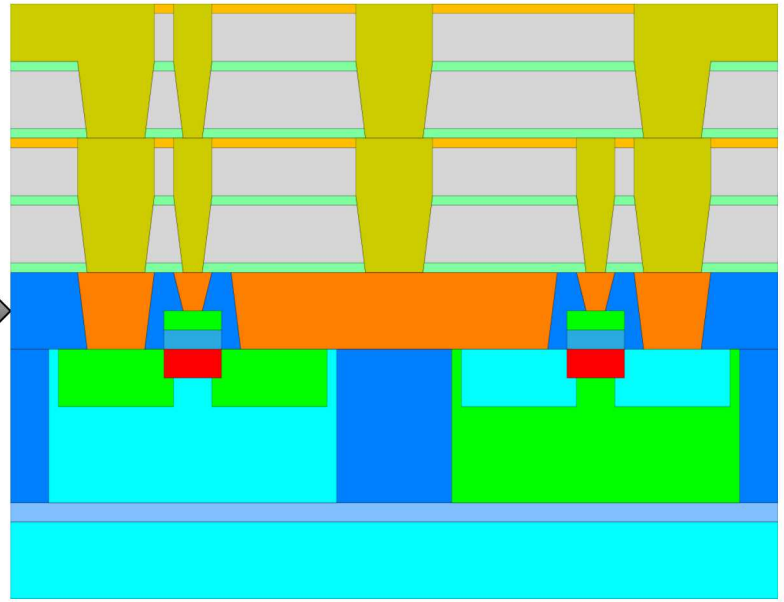
CMOS/APAM device after BEOL



Big Questions:

- **Are CMOS transistors still functional?**
- **Performance of APAM devices**

N-type Si P-type Si APAM

Integrated APAM/CMOS demonstration goals

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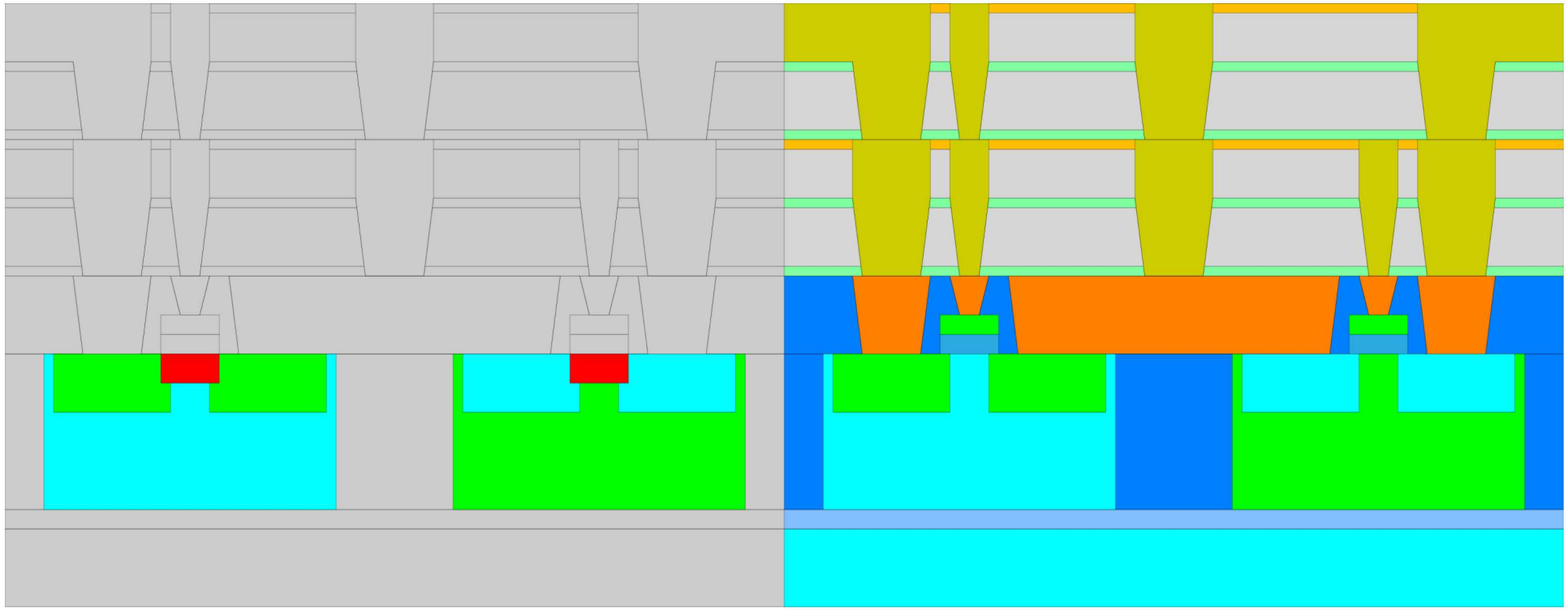
APAM control circuit

Standard CMOS transistors



Control CMOS transistor gate with APAM wire

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  - Design STM compatible CMOS diagnostic chip
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  - Evaluate thermal budget of CMOS chip *in-situ*

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- Heterogenous integration
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Are there processes that allow APAM device fabrication after CMOS processing?

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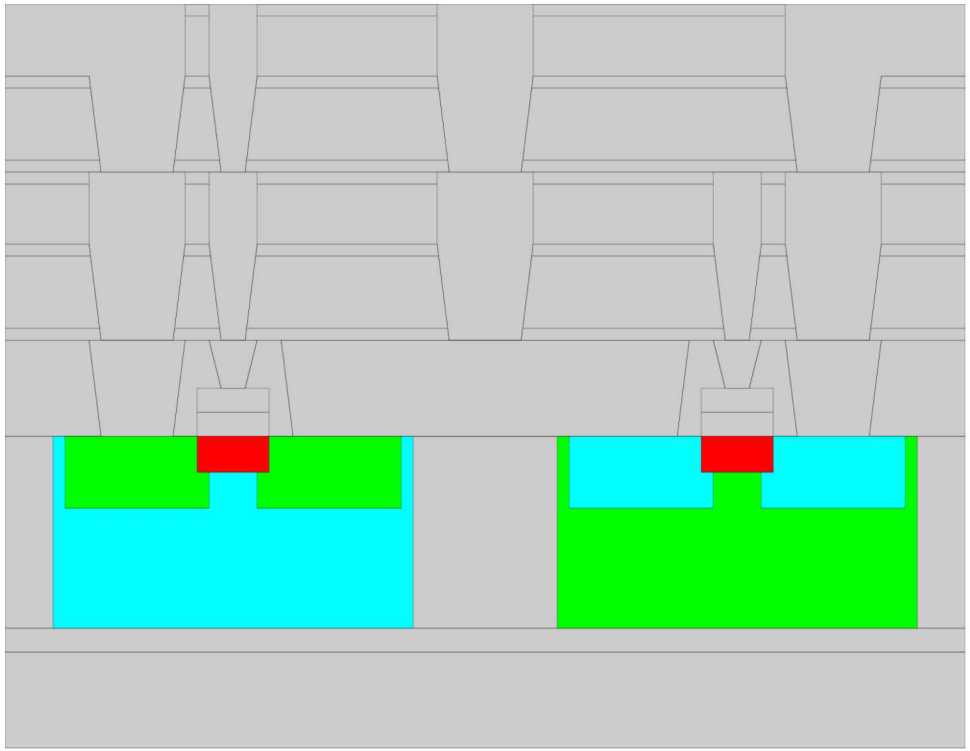
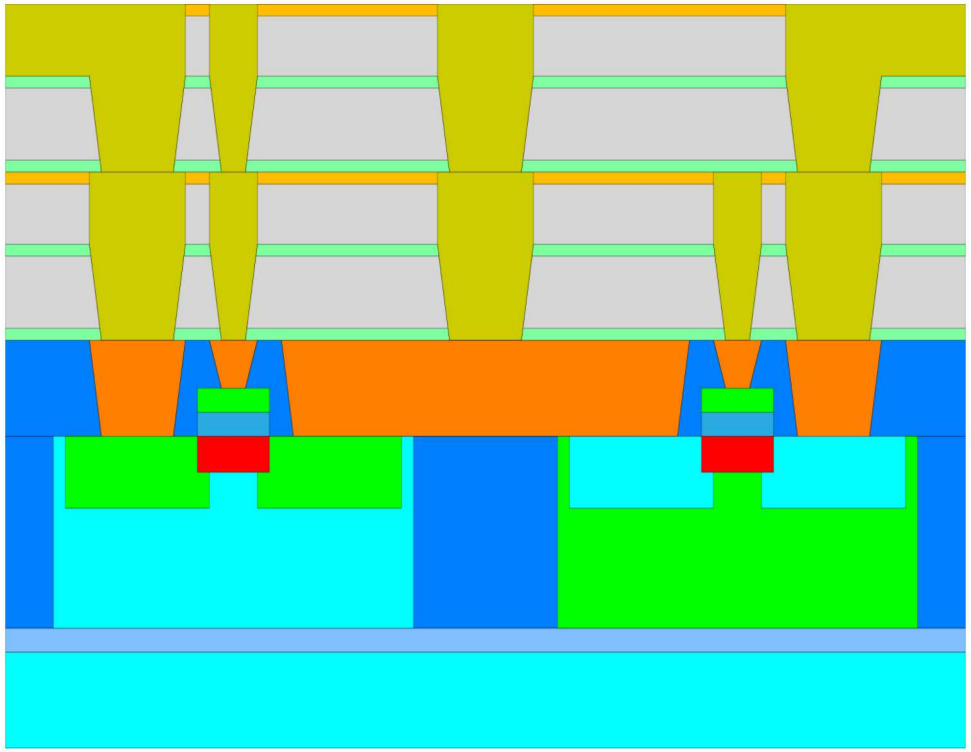
CMOS/APAM Device



CMOS/APAM Device



Two Critical Challenges:

Metal routing layers prevent access to doped silicon wells

Metal routing has limited thermal budget (<450°C)

Lower temperature processing required for post-CMOS APAM integration

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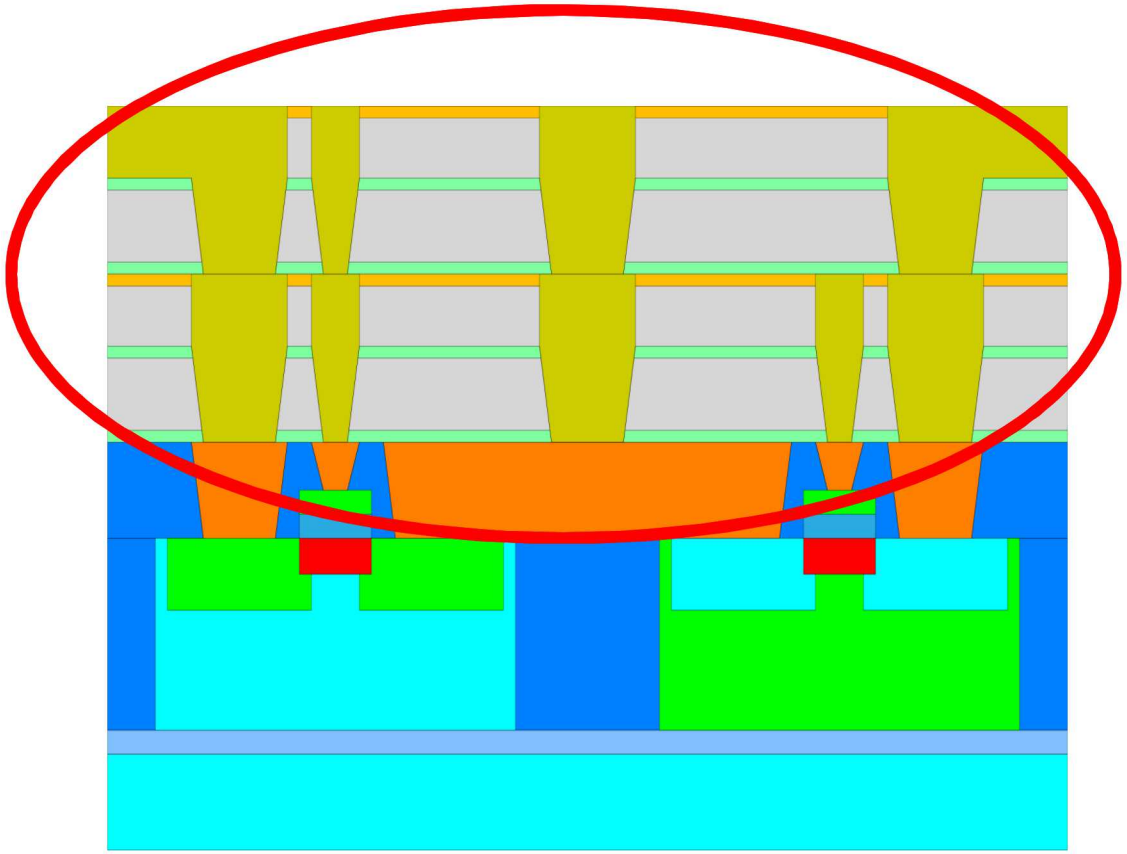
- APAM surface preparations require temperatures >800°C
- CMOS metal has max temperature of 450°C
- Completed CMOS devices have thermal budgets as low as 200°C
- Need to develop recipes for all APAM steps that run <200°C
  - Reduced temperatures affect chemistry of APAM
  - Loss of atomic resolution
  - Reduction in dopant density

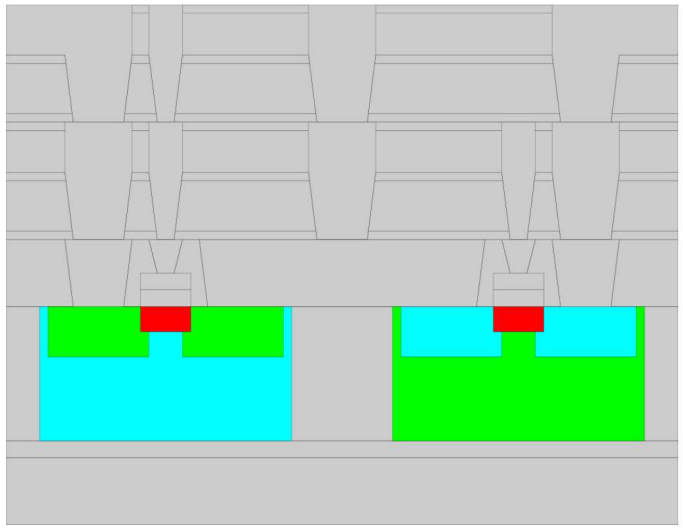


What is the performance cost of reduced temperature processing?

Backside processing required for post-CMOS integration

Sandia National Laboratories

Direct Integration CMOS/APAM



N-type Si

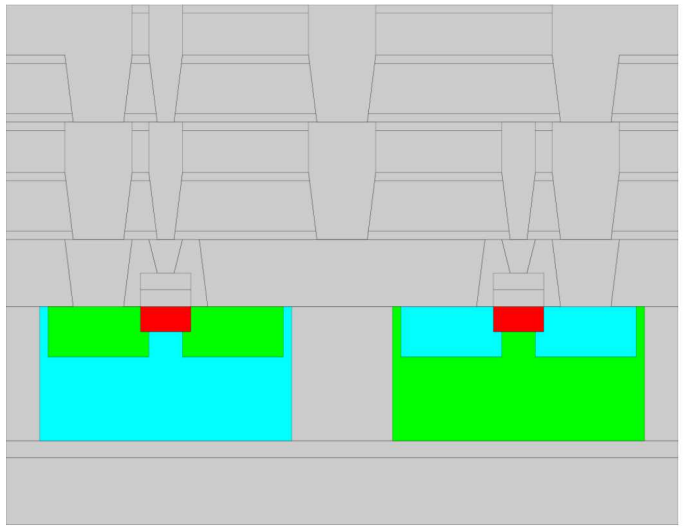
P-type Si

APAM

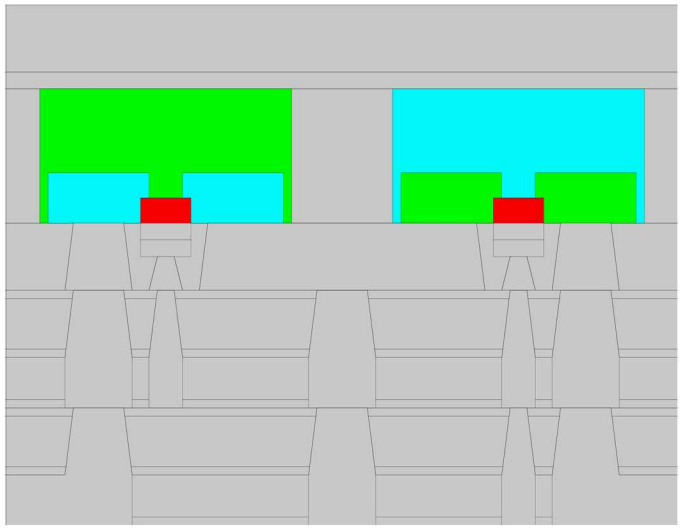
Backside processing required for post-CMOS integration

Sandia National Laboratories

Direct Integration CMOS/APAM



Inverted CMOS/APAM

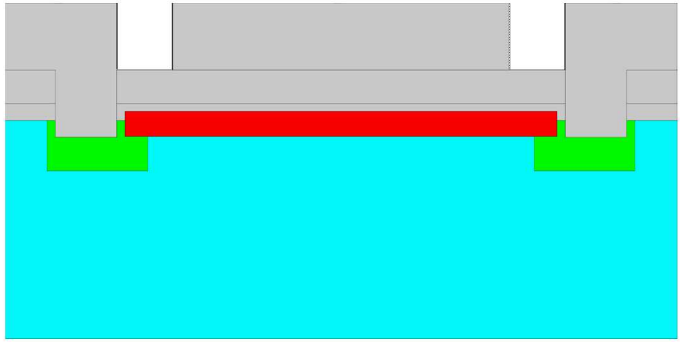


N-type Si

P-type Si

APAM

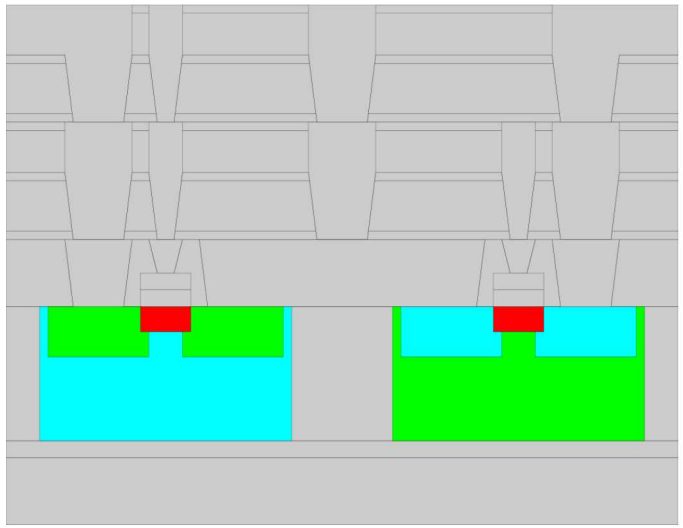
Current APAM Device



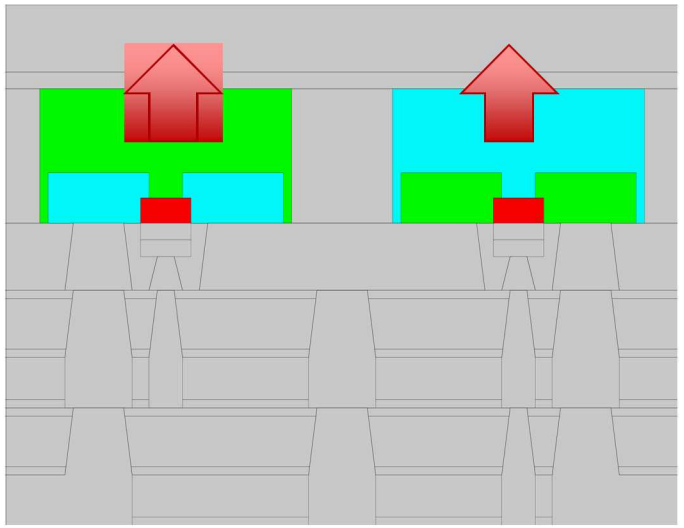
Backside processing required for post-CMOS integration

Sandia National Laboratories

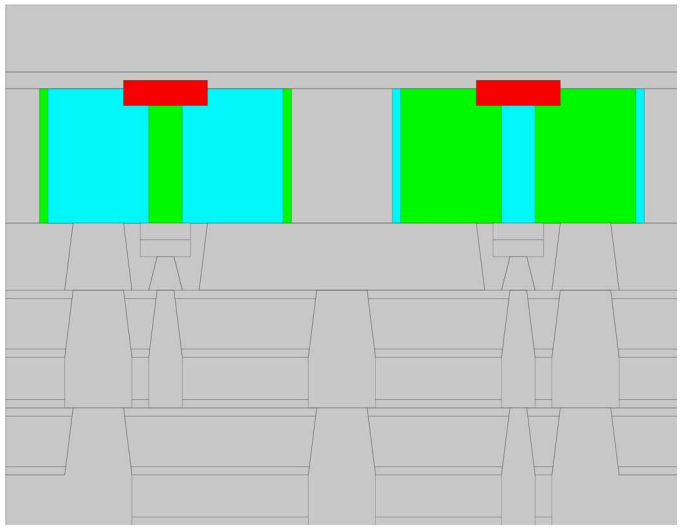
Direct Integration CMOS/APAM



Inverted CMOS/APAM



Altered wells

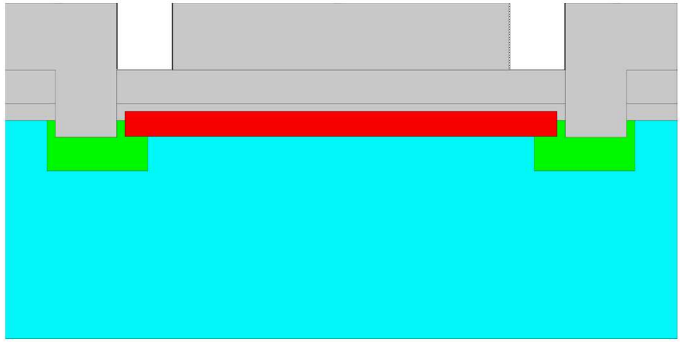


N-type Si

P-type Si

APAM

Current APAM Device



Backside processing required for post-CMOS integration

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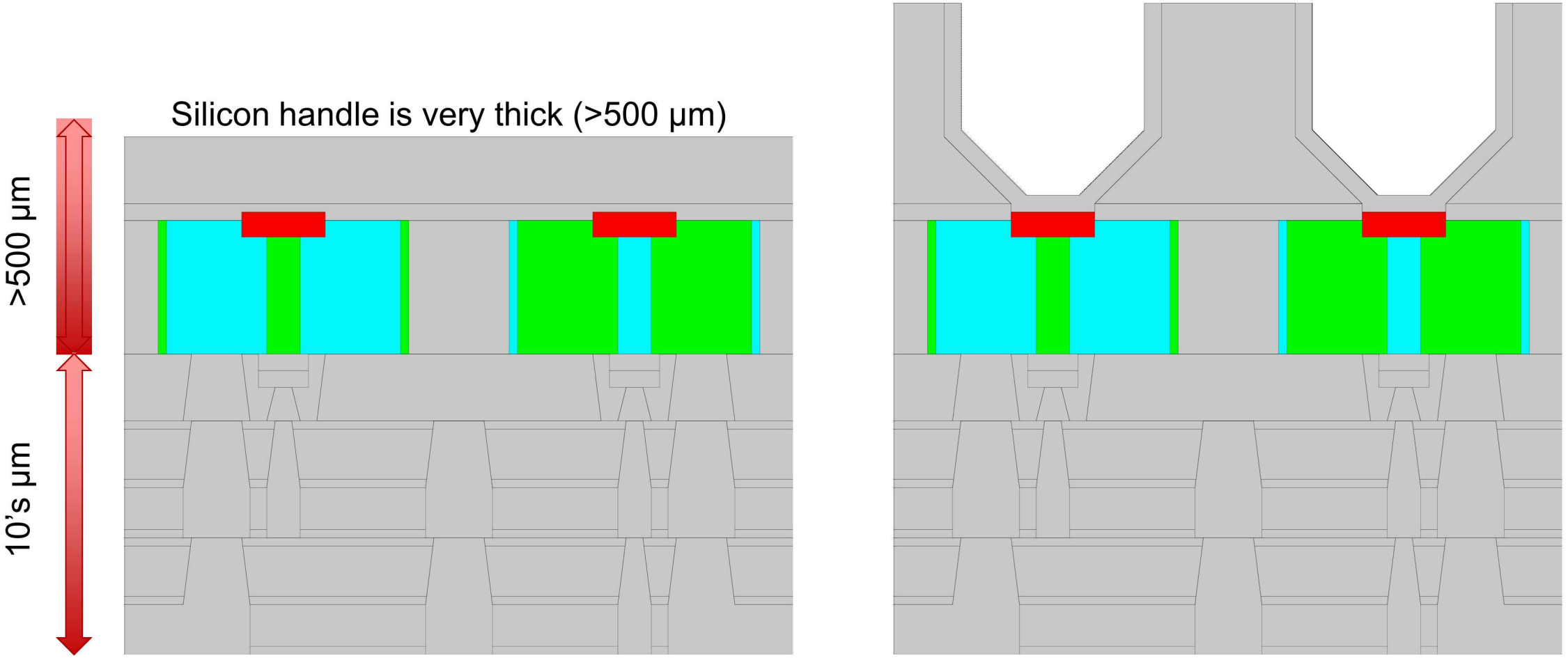
Need to thin backside to enable APAM fabrication



Can the backside be atomically cleaned after thinning?

Year 1 Objectives

- Direct CMOS-APAM Integration
  - Design STM compatible CMOS diagnostic chip
  - Evaluate thermal budget of CMOS chip *ex-situ*
  - Evaluate thermal budget of CMOS chip *in-situ*

- Reduced temperature processing
  - Evaluate room temperature hydrogen termination
  - Develop lower temperature surface cleans
  - Demonstrate APAM recipes on thinned silicon

- Heterogenous integration
  - System-in-package demonstration
  - Plan bump bonding scheme

Can APAM be integrated with heterogeneous integration schemes?

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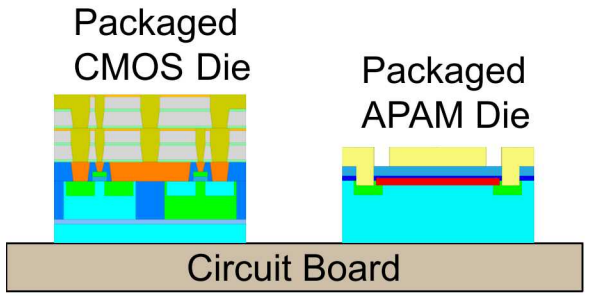
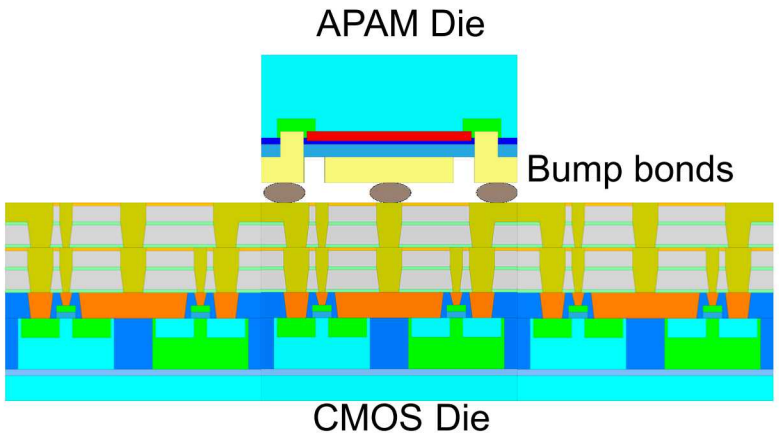
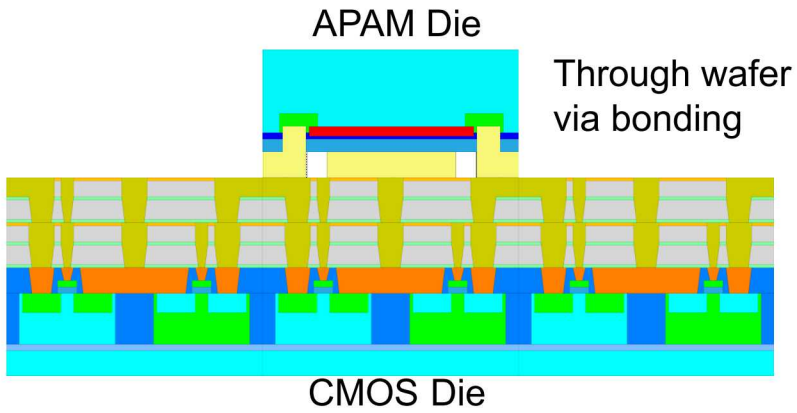
Separate ICs



Bump bonding



Chiplets

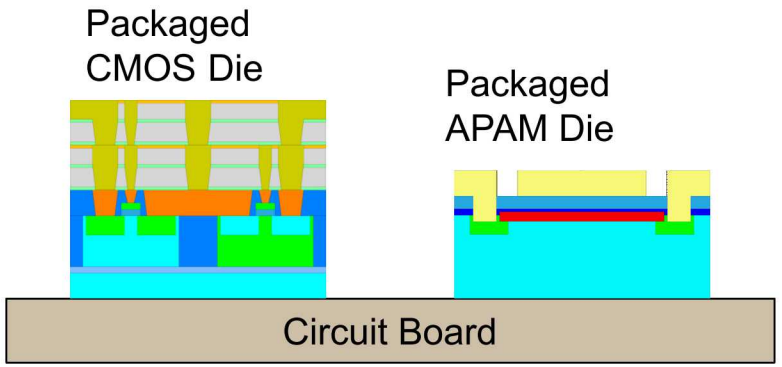


Increasing Difficulty

Heterogeneous Integration (HI) separates high end CMOS processing from APAM processing
Enables Non-CMOS custom fabrication process for APAM

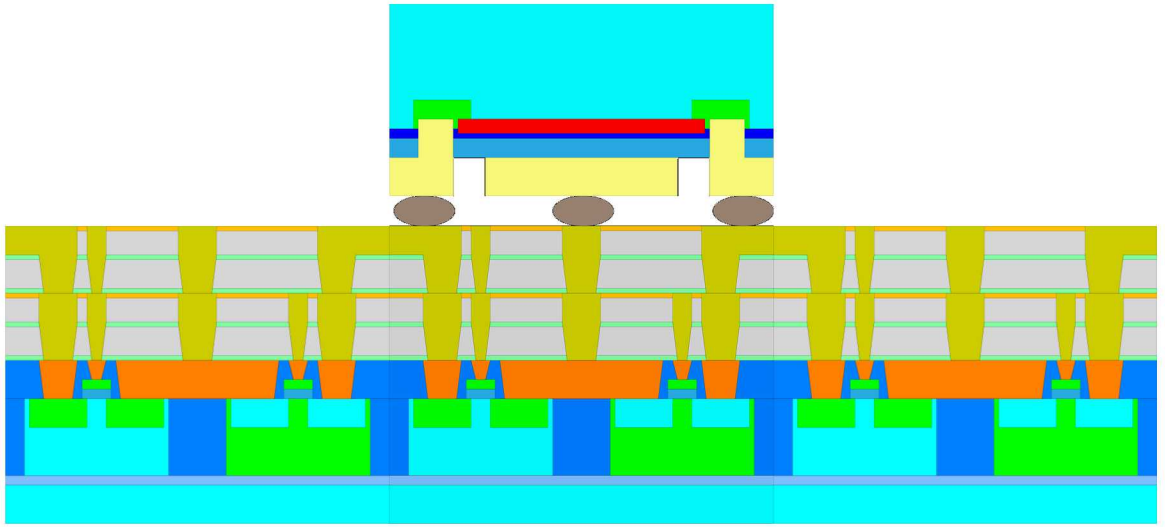
Paths to heterogenous integration

- Demonstrate IC integration
  - Drive CMOS transistor gate with APAM wire
  - Minesweeper for more advanced integration issues



- Develop path for bump bonding APAM chips to CMOS die
  - Understand process flow
  - Build CMOS base die
  - Drive CMOS transistor gate with APAM wire

APAM Die with custom fab flow



CMOS Die

Heterogenous integration buys down risk on CMOS integration

CMOS Integration Summary

- Big picture
  - Demonstrate APAM process integration with CMOS
  - Provide guidance for best paths for APAM integration in future
- Impact post GC
  - Deliver APAM enhanced functionality for CMOS devices through a variety of possible flows most compatible with target technology