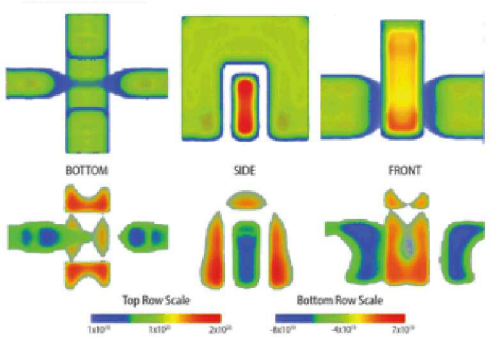
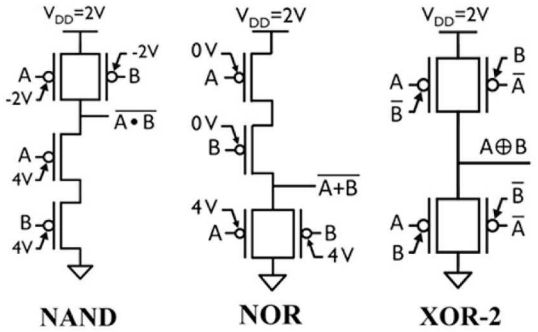
SAND2019-0240PE





FAIR DEAL GC Thrust #2: APAM Modeling

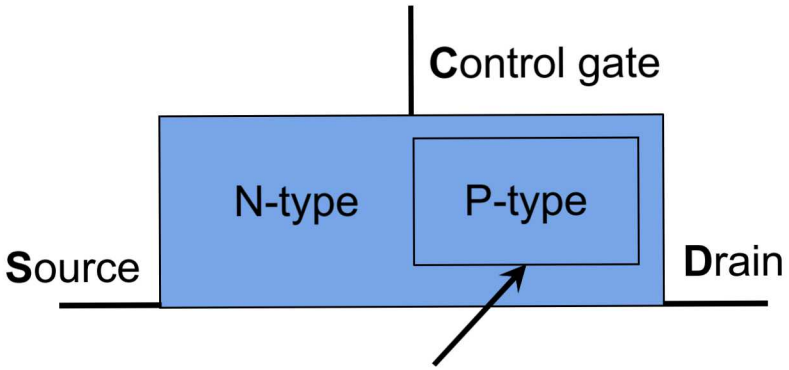
Denis Mamaluy, Suzey Gao, Leon Mauer

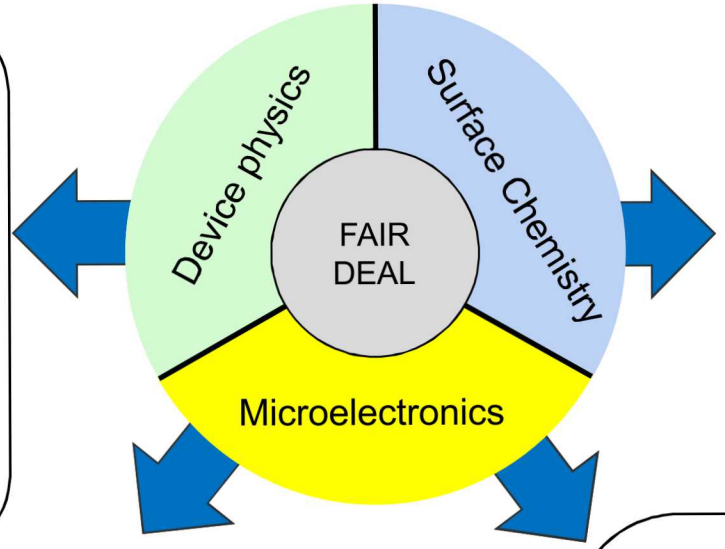
Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia, LLC, a wholly owned subsidiary of Honeywell International, Inc., for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

Digital electronics at the atomic limit (DEAL)

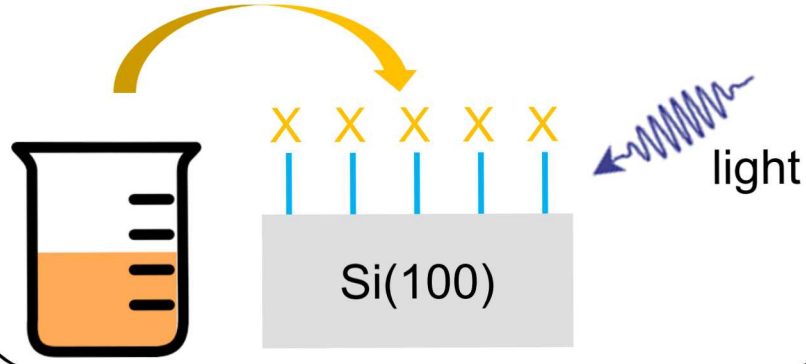
Sandia National Laboratories

Thrust 1: APAM-enabled Devices

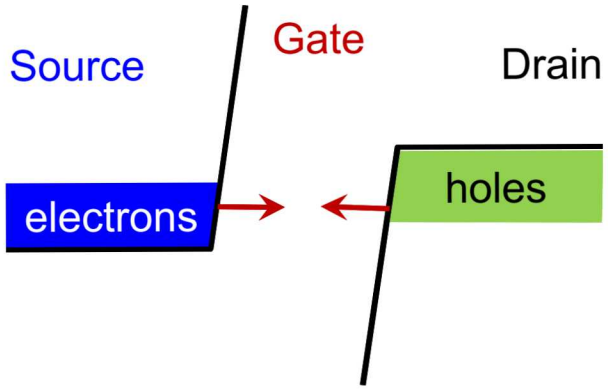




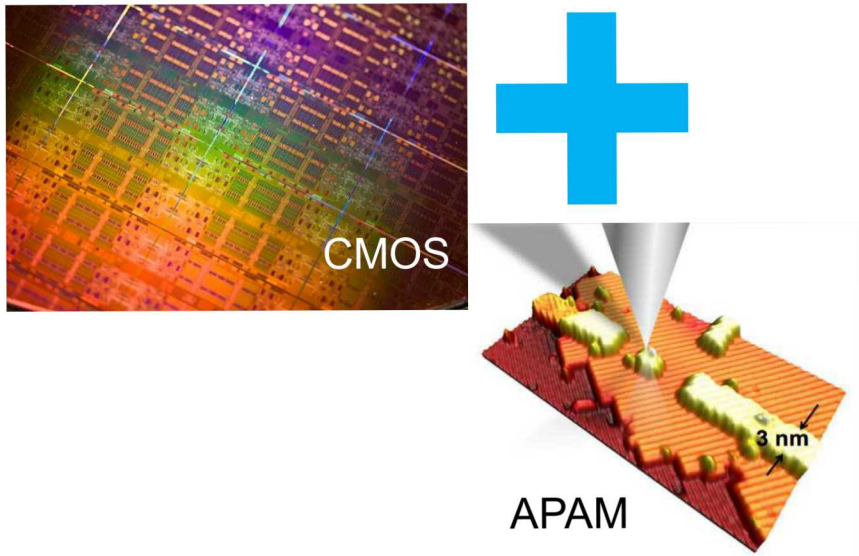
Thrust 4: Application Platform



Thrust 2: APAM Modeling



Thrust 3: CMOS Integration



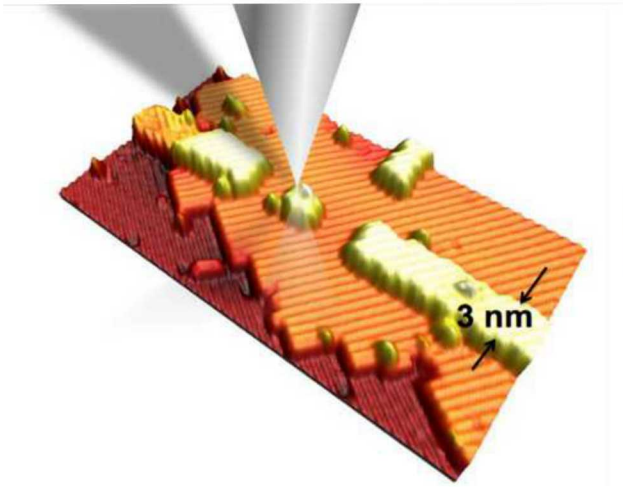
APAM Path to Beyond Moore Computing (BMC)

Sandia National Laboratories

Traditional BMC paths start **from large to small** by shrinking device sizes

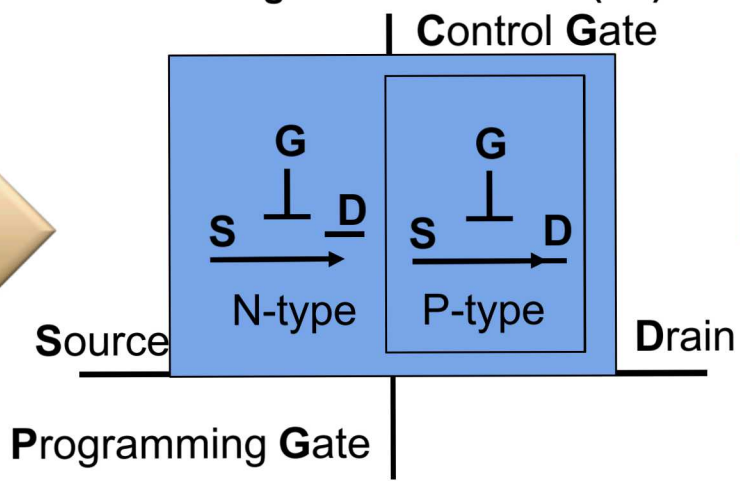
APAM path to BMC starts **from the atomic limit** to devices to circuits

APAM



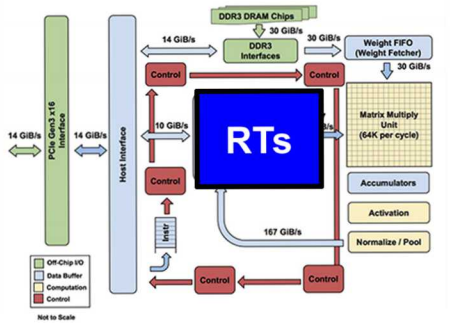
??

Reconfigurable transistor (RT)



??

ASIC

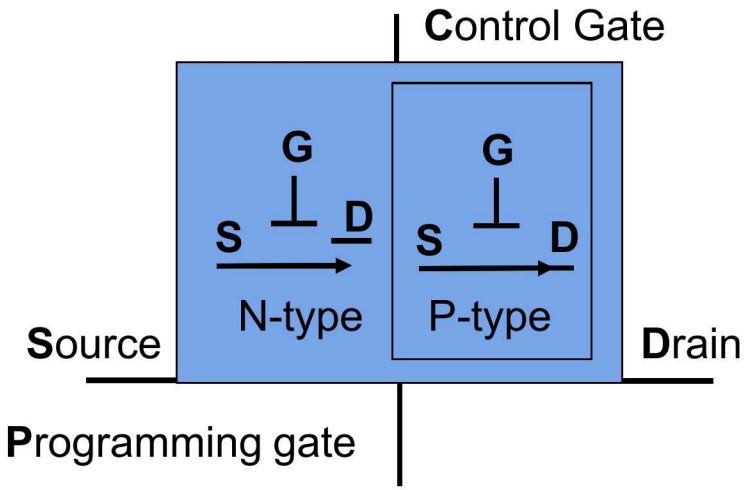


The APAM approach opens many new opportunities, but also comes with challenges:

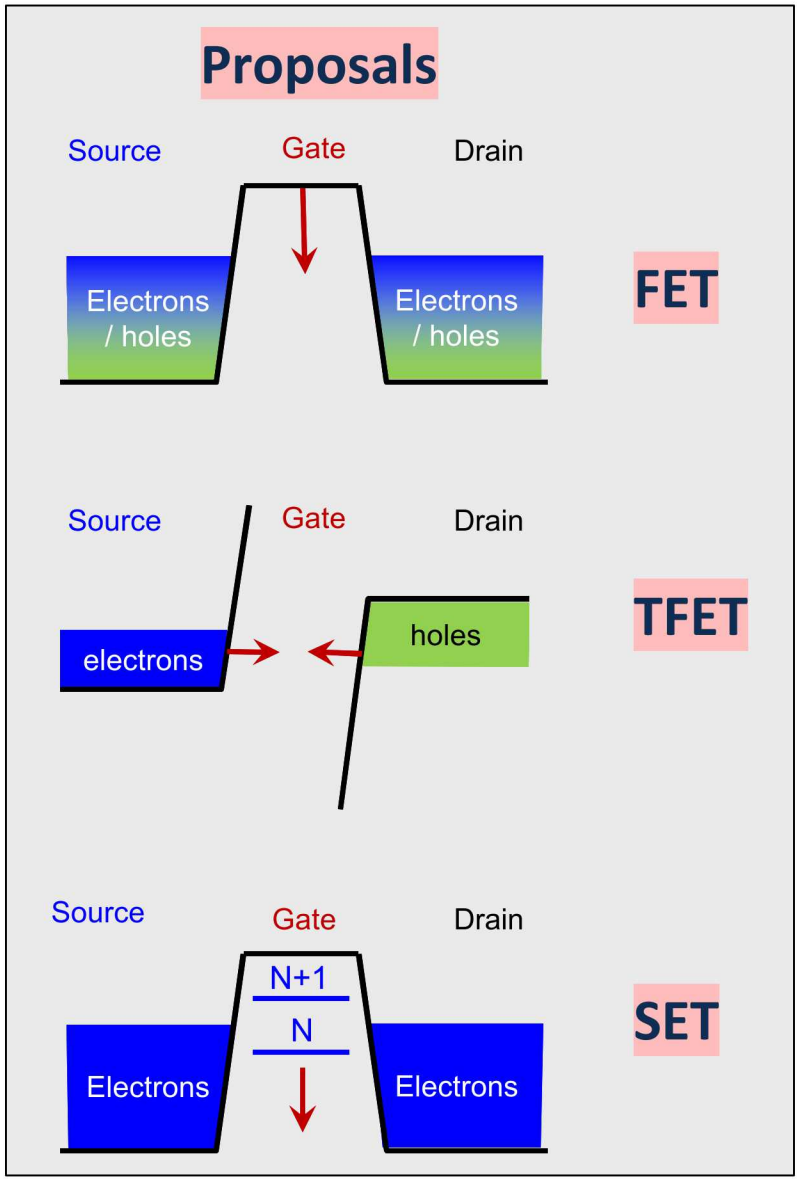
- What type of nanodevices to use for APAM-enabled reconfigurable logic?
- What are the rules of design for reconfigurable circuits?

Modeling and simulation (M&S) will help us answering these important questions !

What **type of nanodevices** to use for APAM-enabled reconfigurable logic?



This project is not proposing a specific device to optimize.



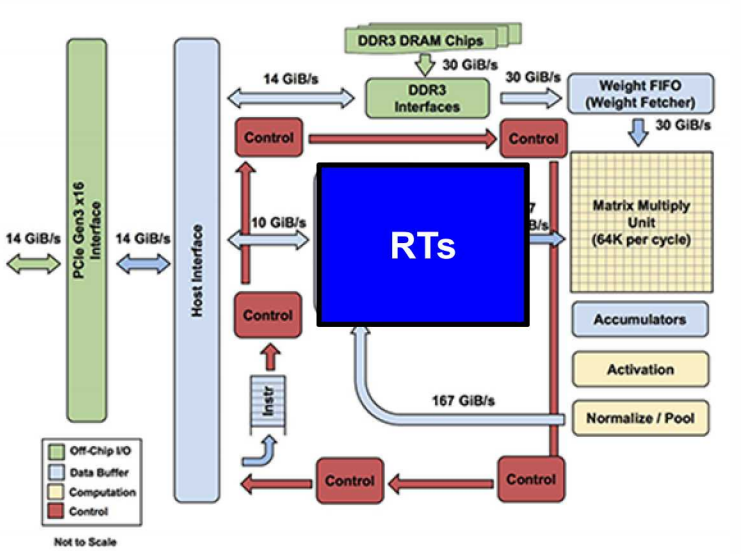
Pathfinding:

- **Design devices based on APAM toolbox**
- **Discover new device concepts**

What are the **rules of design** for reconfigurable circuits?

Sandia National Laboratories

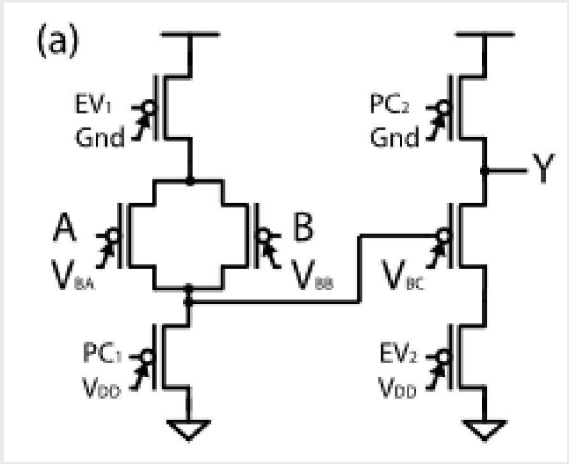
ASIC



This project is not proposing a specific circuit to make.

Proposal

Reconf. FET
Cost: 7 devices, 3 inputs
Benefit: 8 logic funcs.



Gaillardon, IEEE VLSI (2015)

Pathfinding:

- **Efficient way to implement logic**
- **Discover new circuit-level concepts**

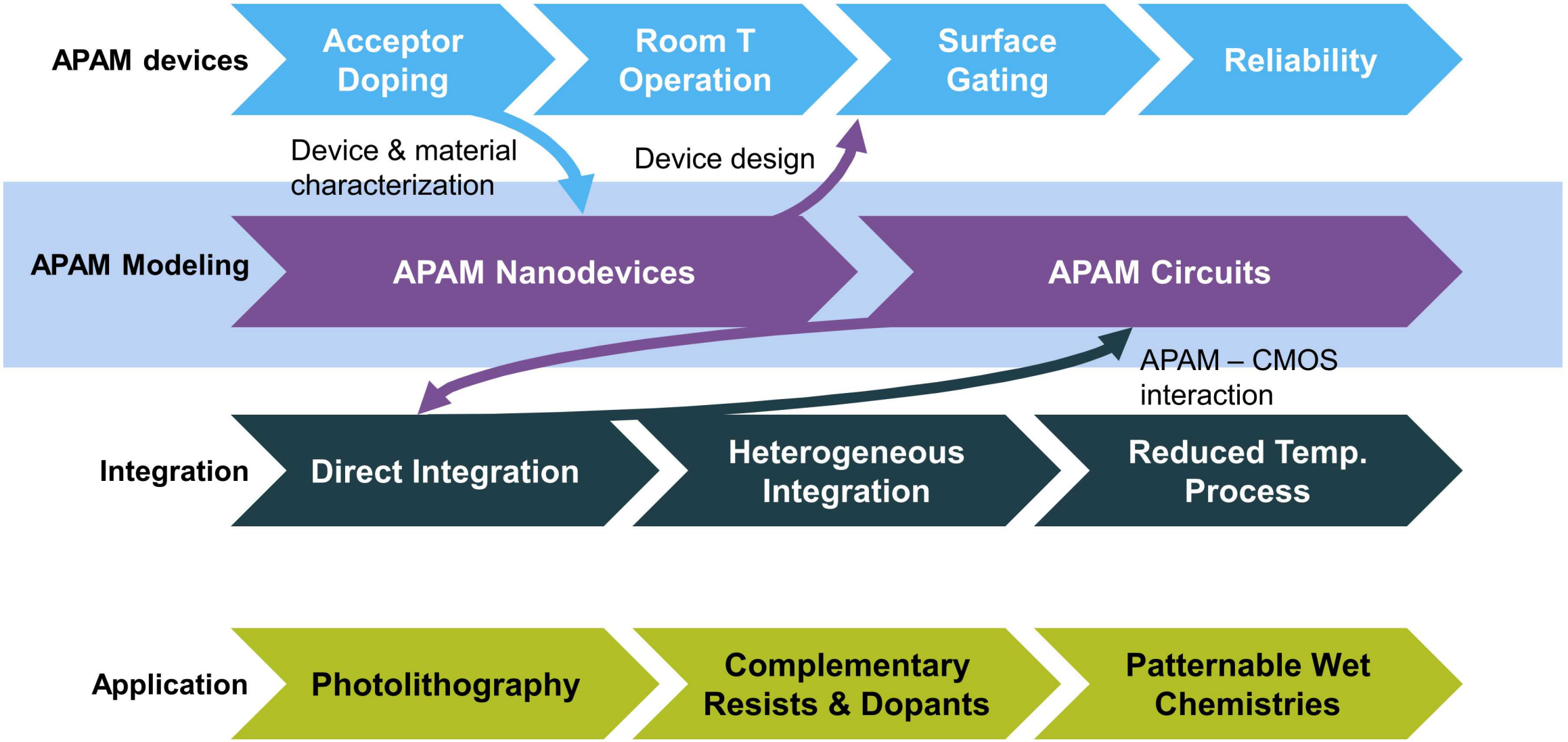
What Modeling and Simulation (M&S) Brings

Sandia National Laboratories

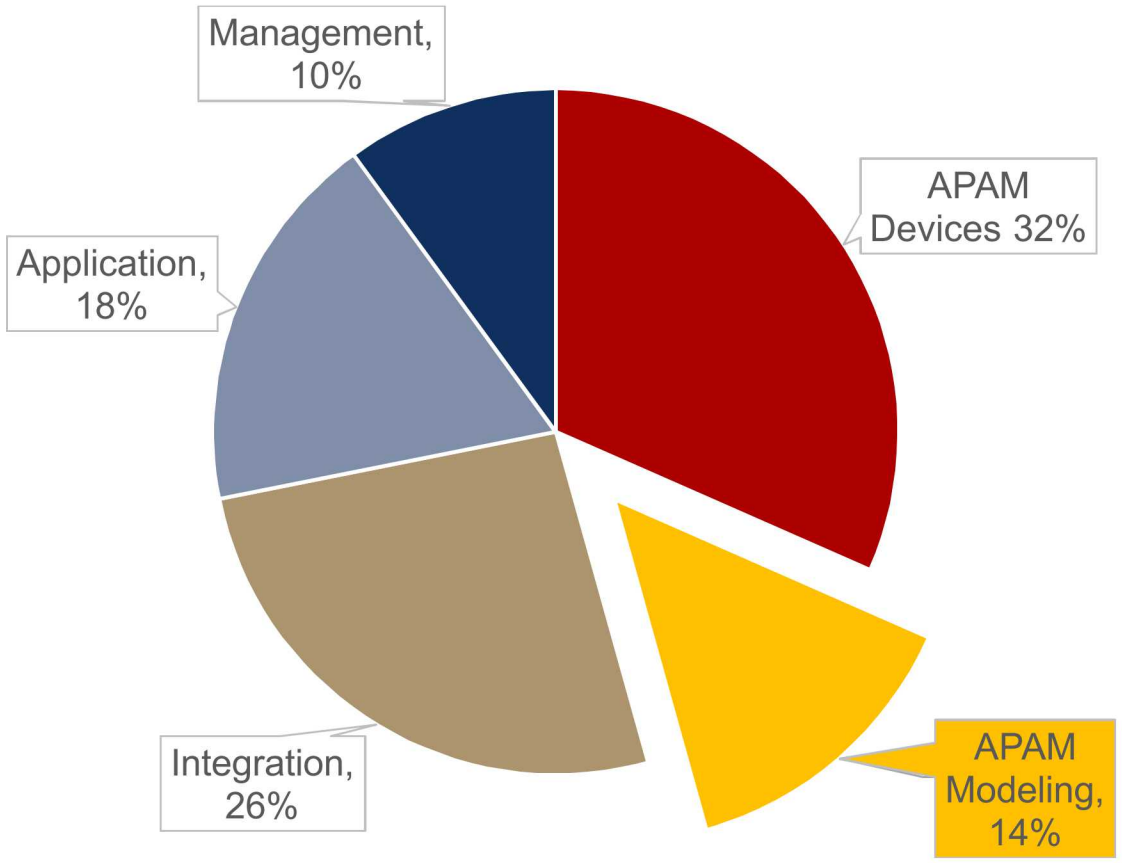
Not just help to interpret the data, but more importantly guide the experiments !

- M&S are vital to
  - understand new device physics
  - improve device designs
  - establish physical limits of different technologies
- Map the space of possibilities
- Study unmeasurable characteristics
- Assess system-level performance via multiscale M&S

Modeling thrust interactions



Modeling Thrust: Resources



Leverages:

- Investments into beyond-CMOS device simulation tools and TCADs
- SNL's excellent HPC resources

Modeling thrust organizational chart

Sandia National Laboratories

Thrusts

Program Leadership
PI: Shashank Misra
PM: Robert Koudelka
Deputy PM: Rick Muller

#2 APAM modeling
Lead: Denis Mamaluy
Nanodevices: Suzey Gao
Circuits: Leon Maurer

Support Team
Financial: Laurel Taylor
Logistics: Lori Mann
Web: Dorean Chaleunphonh
Administrative: Felicia Pena

Cross-cutting capabilities

Measurement: Lisa Tracy, Tzu-Ming Lu, David Scrymgeour, Ping Lu, Albert Grine

Microfabrication: Dan Ward, DeAnna Campbell, Mark Gunter, Steve Carr, Sean Smith

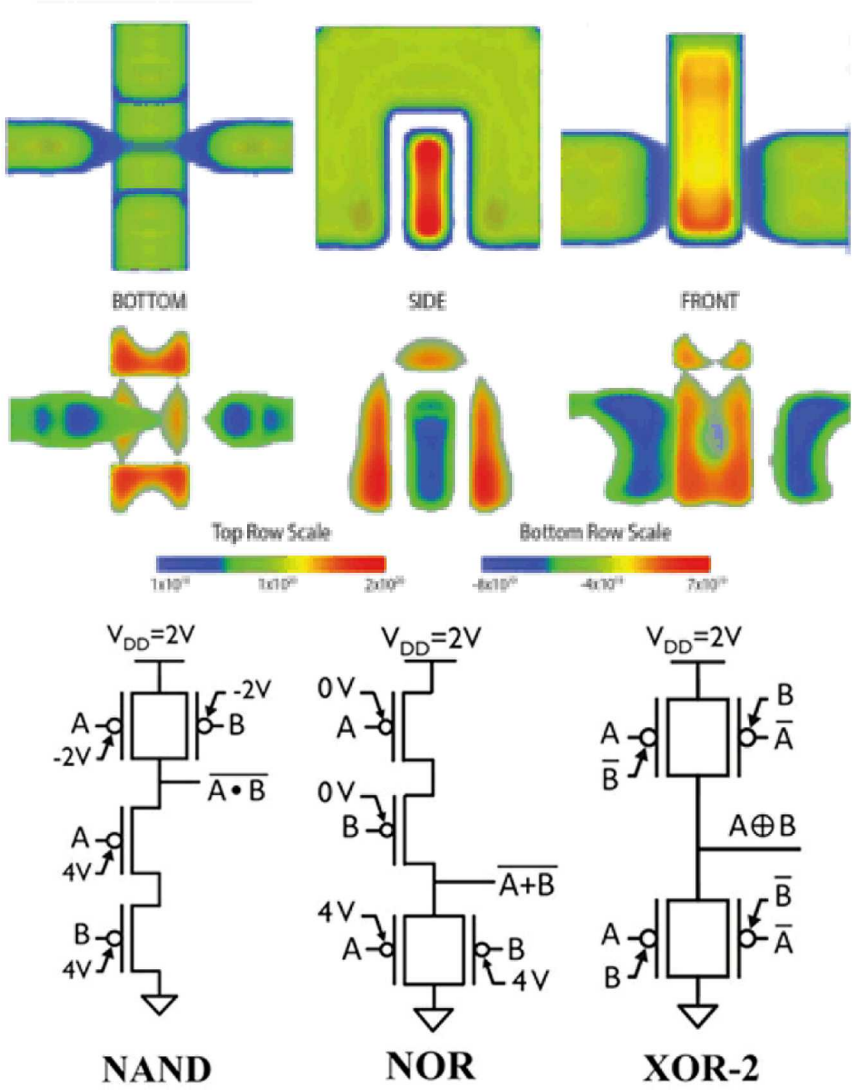
Modeling: Denis Mamaluy, Suzey Gao, Leon Maurer, Andrew Baczewski, Peter Schultz, Quinn Campbell

Surface science: Shashank Misra, Ezra Bussmann, George Wang, Aaron Katzenmeyer, Evan Anderson, Fabian Pena, Esther Frederick, Bob Butera, Dave Wheeler

Integral parts of APAM Modeling Thrust

1. **APAM device simulation**
   - **Necessary to understand device physics**
   - **Propose and improve device designs**

2. APAM circuit modeling
   - Necessary for logic design
   - Can assess system-level performance



What do we need in an APAM Device Simulator?

Sandia National Laboratories

- The APAM Device Simulator should
  - be based on a Quantum Transport formalism
  - be sufficiently fast to be able to treat realistic APAM-enabled structures and devices
  - accurately describe APAM-materials system
  - include relevant physics: scattering effects, impurities, interface roughness, discrete dopants
  - correctly describe bipolar transport (both carriers make significant contributions to the current)

No existing quantum transport simulator is capable of all of the above.

Device Simulator: Quantum Transport

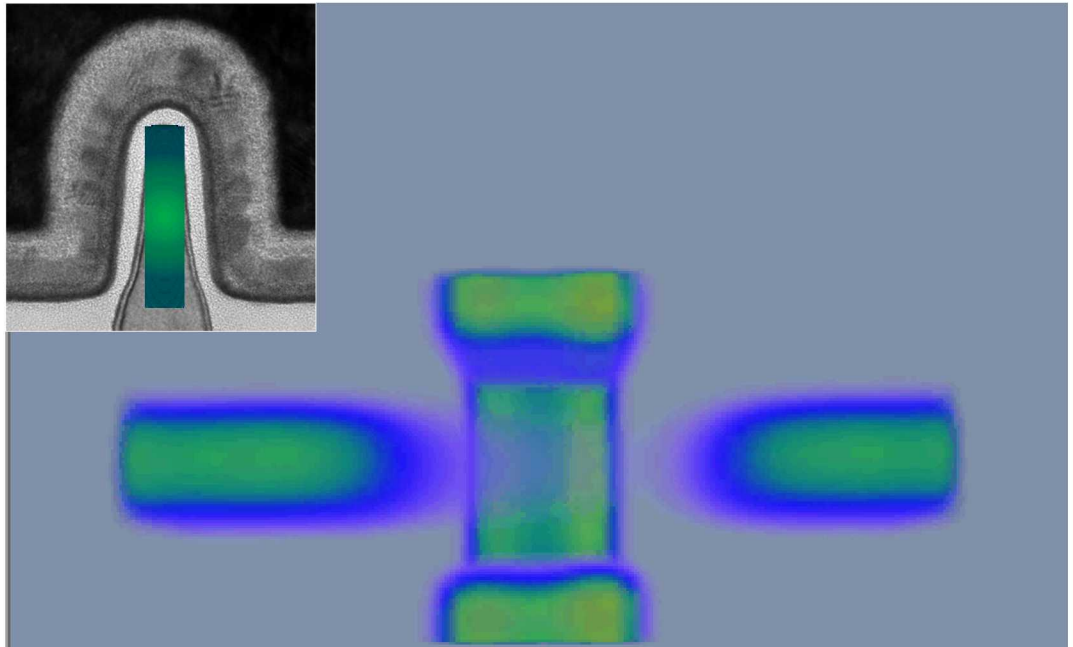
Sandia National Laboratories

- Transistors have become so small that charge transport can no longer be described by the laws of classical physics:

- Principally new physical effects arise (tunneling, quantum confinement, quantum capacitance)

- Semi-classical (drift-diffusion or particle-MC based) methods do not provide the adequate description at atomic scale

We have created an electron quantum transport simulator for multi-terminal nanodevices in a prior project at Sandia



D. Mamaluy, X. Gao, APL **106**, 193503 (2015).

Challenges for creating APAM Device Simulator

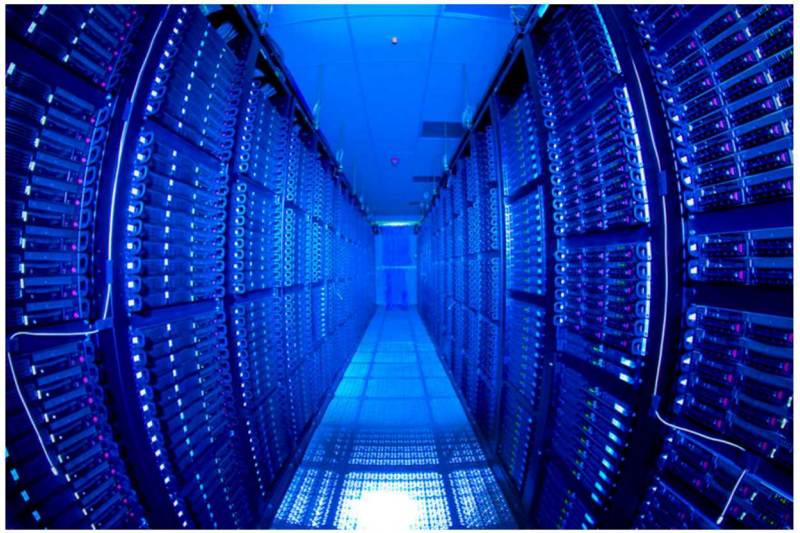
Sandia National Laboratories

The Big Numerical Challenge of quantum transport

A large dense matrix inversion is $O(N^3)$, $N \sim 10^5$-10^6 atomic sites

Quantum transport simulation is at the edge of the (im)possible.

⇒ We have developed a method that scales **linearly**
⇒ Numerics is still very challenging…
but now we can use *regular workstations*



Gives more flexibility for device design and speeds up optimization

Risk assessment: milestones for creating APAM Device Simulator

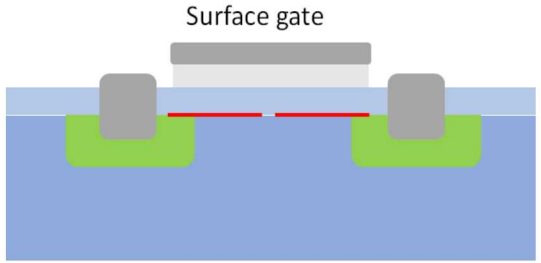
Goal: create a predictive Simulator for designing APAM-enabled reconfigurable devices

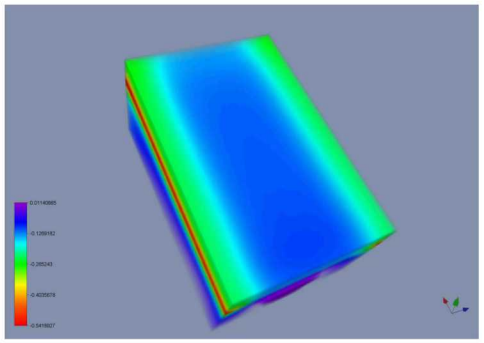
A. Quantum Transport for electrons → **B.** Quantum Transport for holes (Y2) → **C.** Bipolar Quantum Transport (Y3)

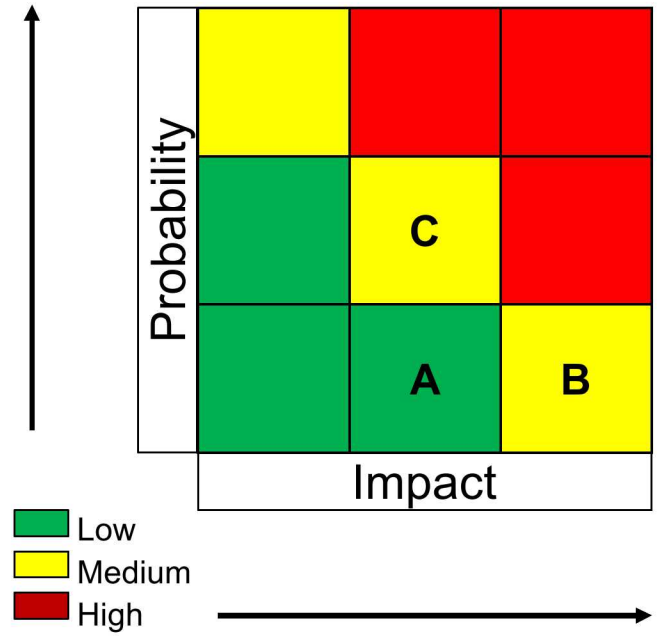
Year 1:
creation (done)
calibration
validation

Year 2:
creation
calibration

Year 3:
creation
calibration







Bipolar Quantum Transport for APAM Devices

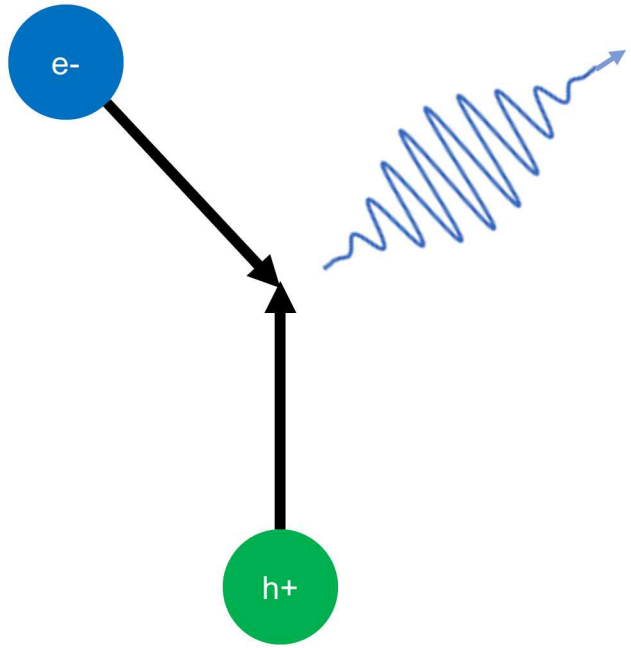
Sandia National Laboratories

Simulation of APAM bipolar devices requires **bipolar quantum transport**

The biggest challenge for **bipolar quantum transport** is

❑ Electron-hole (e-h) recombination in the quantum regime

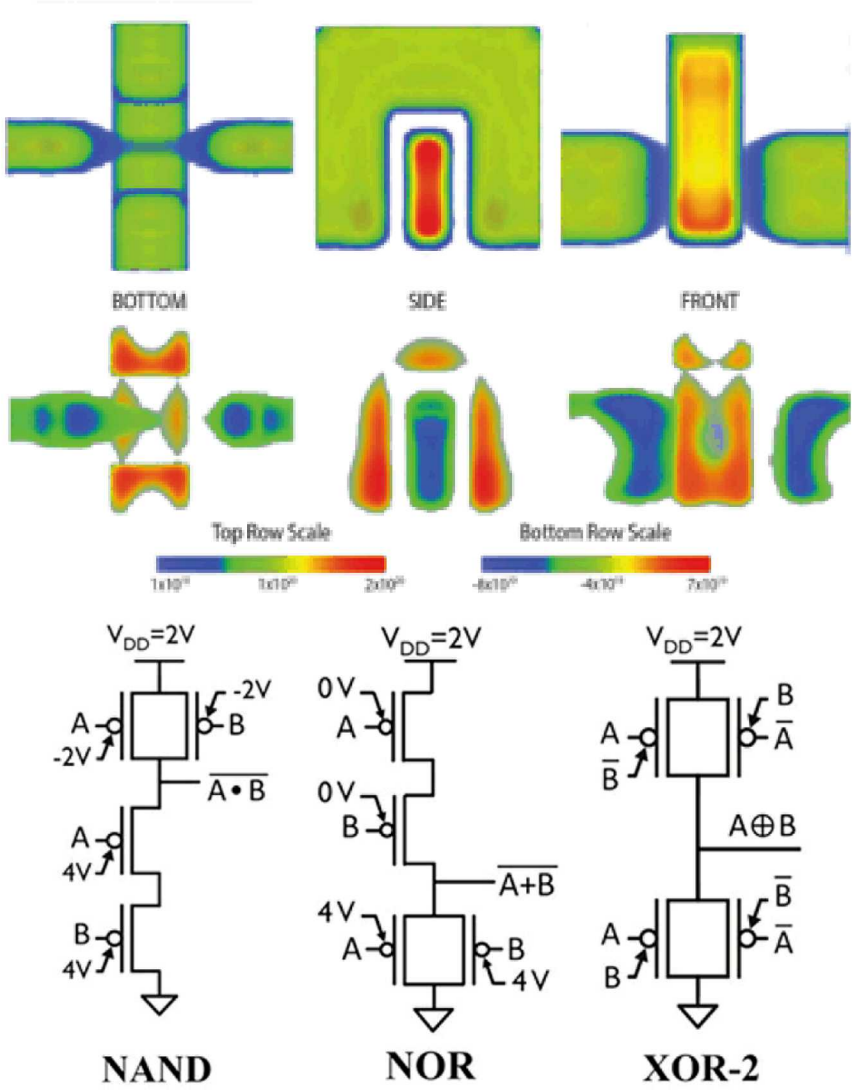
- E-h recombination can significantly alter device characteristics, well modeled in classical transport
- Little work exists to properly treat e-h recombination in the quantum transport regime
- Need to develop a new and efficient approach based on either the master equation or the Büttiker probe method



Integral parts of APAM Modeling Thrust

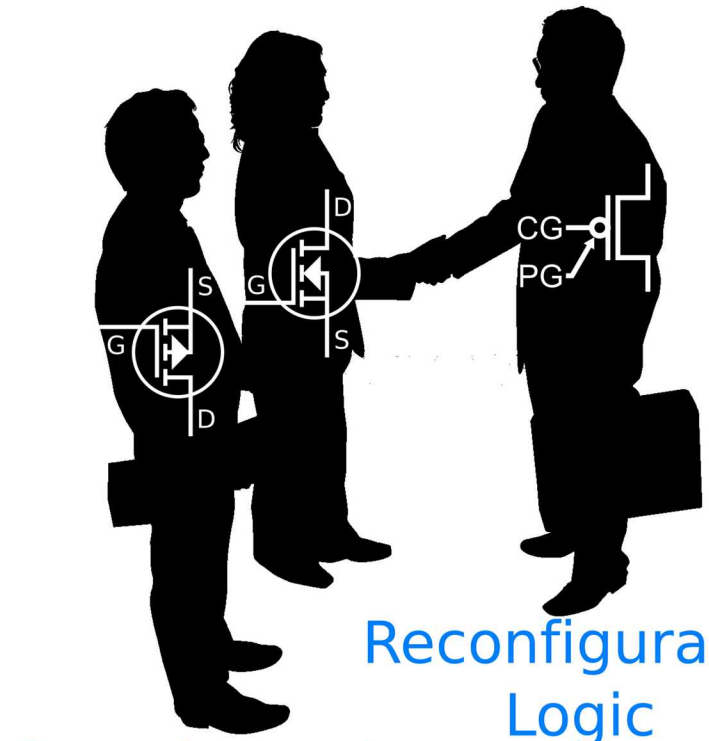
1. APAM device simulation
- Necessary to understand device physics
- Propose and improve device designs

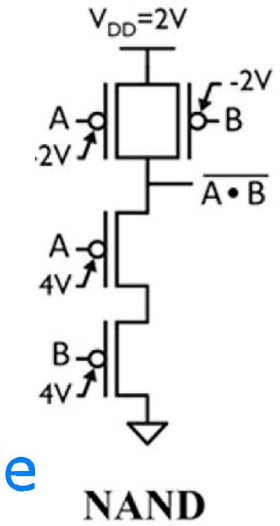
2. APAM circuit modeling
- **Necessary for logic design**
- **Can assess system-level performance**



Modeling reconfigurable circuits

- Reconfigurable transistors are relatively *new circuit elements*
- Usable in both reconfigurable-only and reconfigurable+complimentary circuits
- Requires new circuit *designs* and *design rules*
- Need a freely available modeling tool for others to explore both kinds of circuits
- Will use Xyce, a Sandia-developed, open-source, SPICE-compatible, high-performance analog circuit simulator

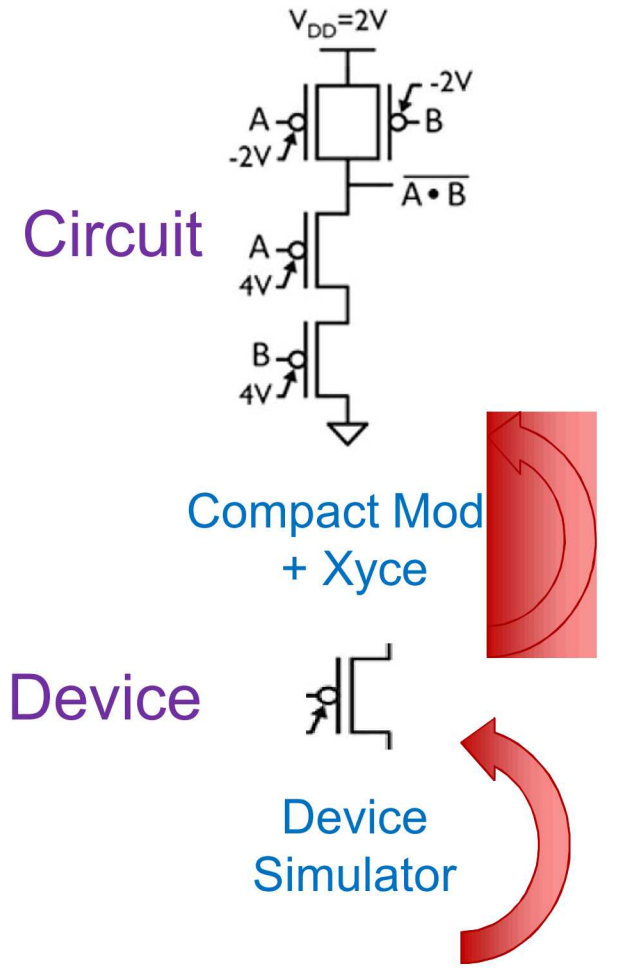




G. V. Resta, Y. Balaji, D. Lin, I. P. Radu, F. Catthoor, P.-E Gaillardon, and G. De Micheli, ACS Nano **12**, 7039 (2018).

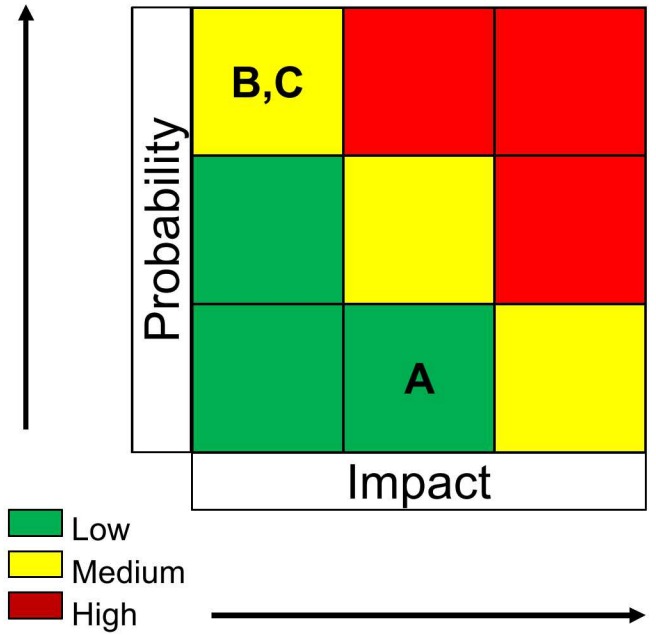
Circuit simulation with APAM devices

- Circuit simulation requires a *compact model*
  - Replicates external behavior of device (current-voltage relations)
  - Simpler and faster than full APAM device simulator
- Two approaches, both informed by results from APAM device simulator and experiment
  - Simplified physics with phenomenological adjustments
  - Lookup table of results from device simulator or experiment
- Can work backwards from a desired circuit characteristic to a device design



Risk Assessment: circuit modeling

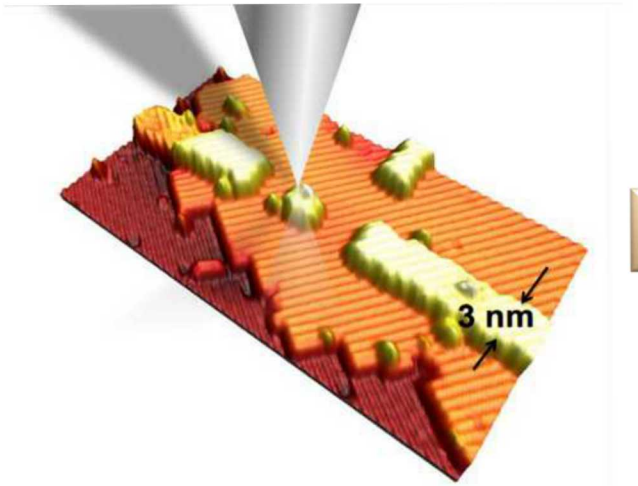
- **A:** Implement *existing, non-APAM* reconfigurable transistor compact model in Xyce
  - Allows *immediate* exploration of reconfigurable circuits
- Implement *APAM* reconfigurable transistor compact model in Xyce. Two options:
  - **B:** Simple lookup table is not flexible enough
  - **C:** Flexible physics-based compact model is too complex



APAM Path to Beyond Moore Computing (BMC)

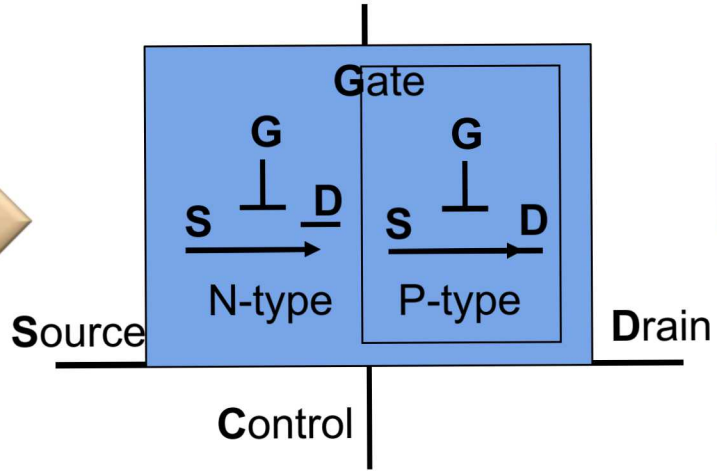
Sandia National Laboratories

APAM



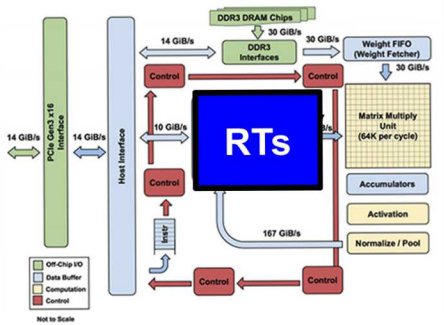
??

Reconfigurable transistor (RT)



??

ASIC



The APAM approach opens many new opportunities, but also comes with challenges:

- What type of nanodevices to use for APAM-enabled reconfigurable logic?
- What are the rules of design for reconfigurable circuits?

Backup slides

Sandia National Laboratories

End of CMOS scaling and paths to Beyond Moore Computing

Sandia National Laboratories

YEAR 2025:
THE END OF CMOS SCALING
Predicted by ITRS at L_g=10nm, inevitable due to fundamental physics* around 5nm

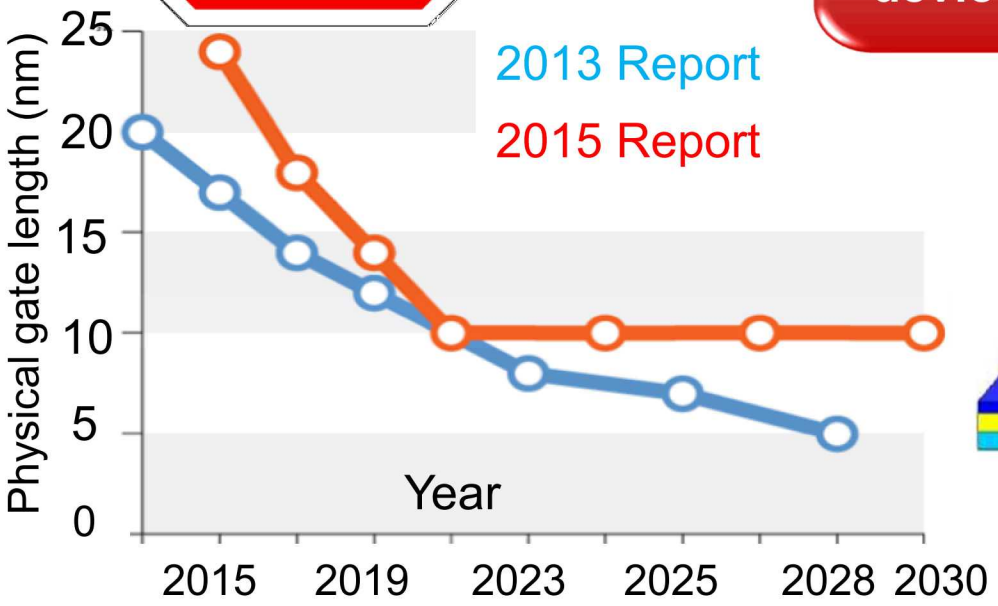
BMC

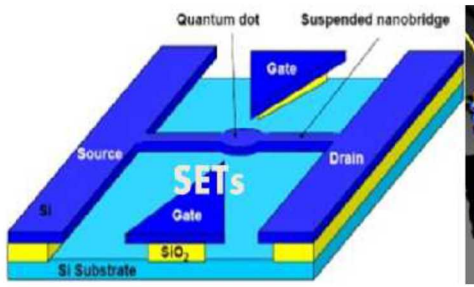
Continue increasing device density with a new "Moore's law"

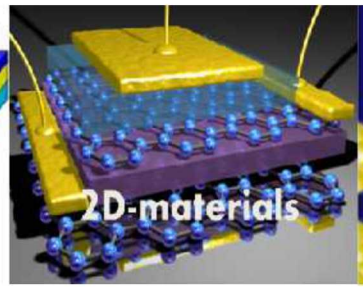
- Single electronics
- Spintronics
- Non-FET two-terminal devices (memristors)

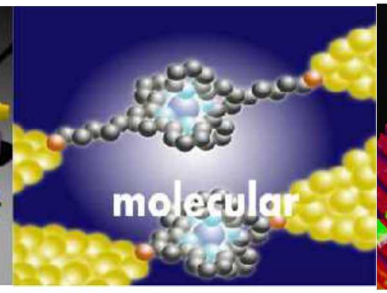
Gain exponential decreases in power with fixed device density

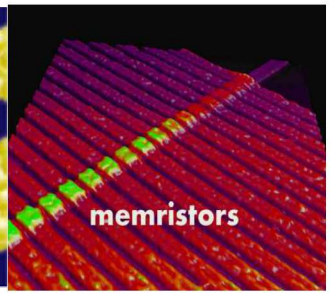
- Adiabatic computing
- TFETs, optoelectronics
- Superconducting electronics









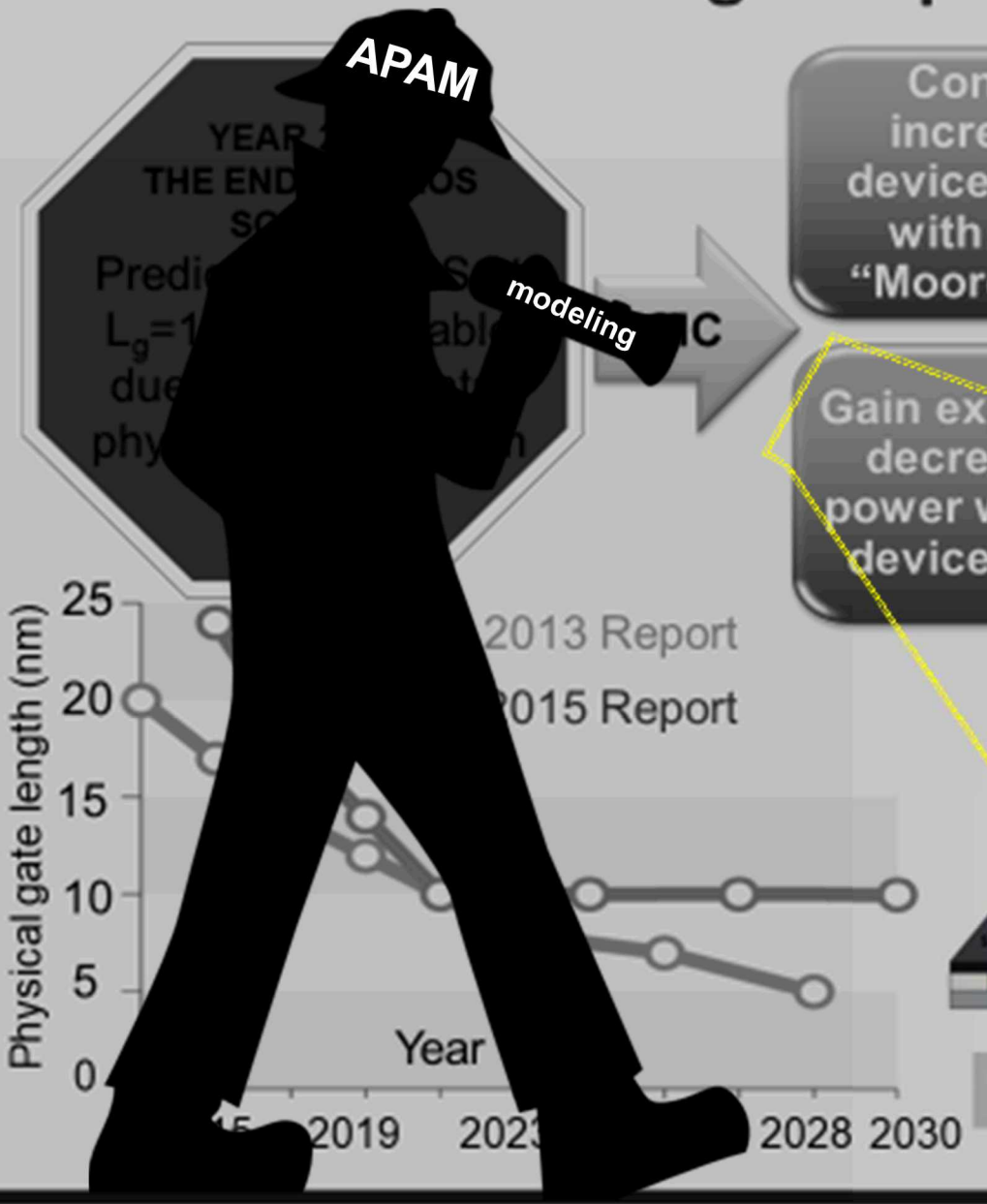


The industry's dilemma: which technology will replace CMOS?

*"The fundamental downscaling limit of field effect transistors", D. Mamaluy, X. Gao, APL **106**, 193503 (2015).

End of CMOS scaling and paths to Beyond Moore Computing

Sandia National Laboratories

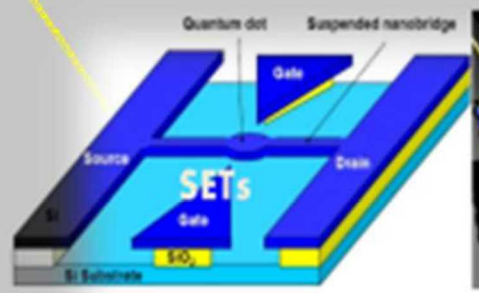


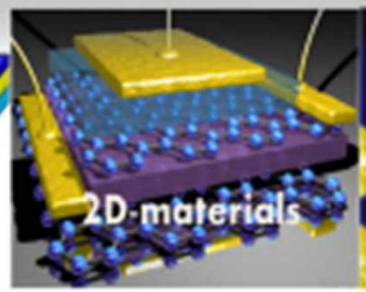
Continue increasing device density with a new "Moore's law"

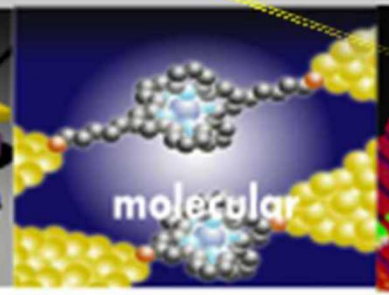
- Single electronics
- Spintronics
- Non-FET two-terminal devices (memristors)

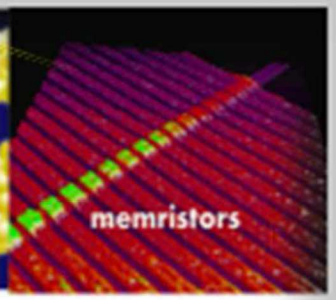
Gain exponential decreases in power with fixed device density

- Adiabatic computing
- TFETs, optoelectronics
- Superconducting electronics









The industry's dilemma: which technology will replace CMOS?

*"The fundamental downscaling limit of field effect transistors", D. Mamaluy, X. Gao, APL **106**, 193503 (2015).