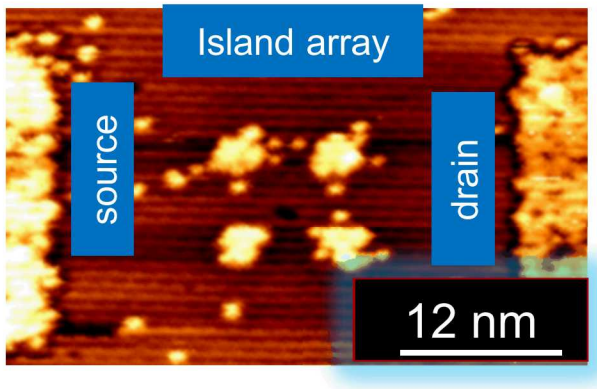
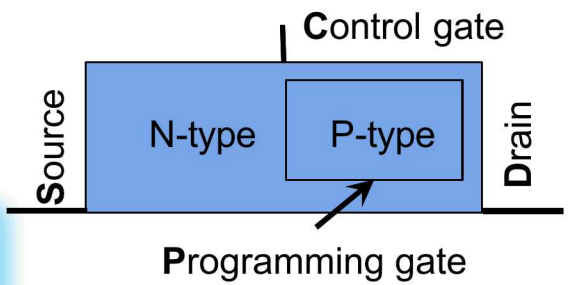
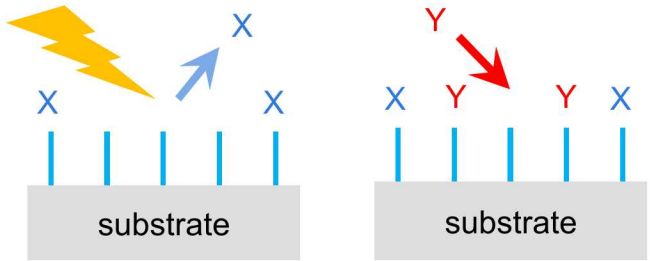
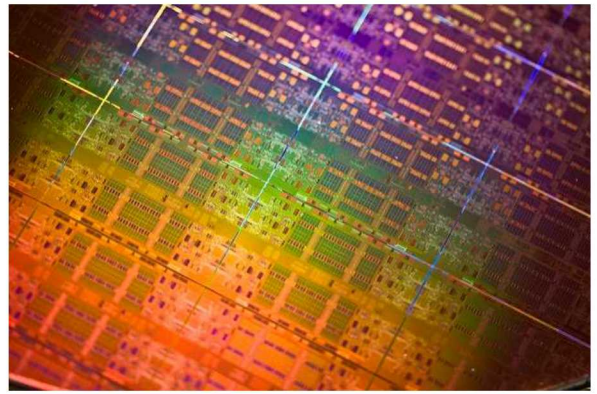
SAND2019-0237PE







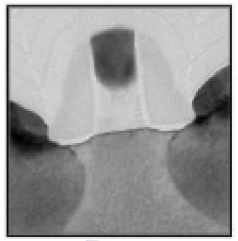


FAIR DEAL GC Technical Overview

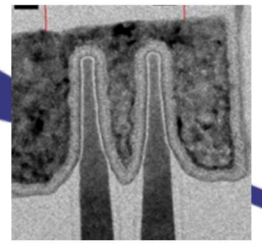
Shashank Misra

What if you could make devices atom-by-atom?

Sandia National Laboratories



65 nm



10 nm

Top-down fabrication

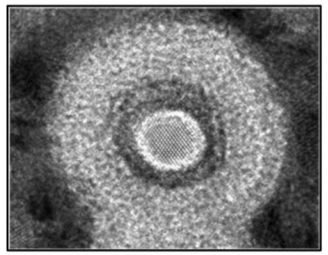
?

5-7 nm

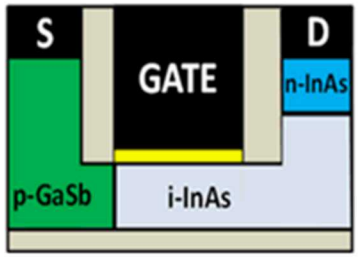
Atomic Limit

Evaluate new device opportunities starting from the physical limit of atoms

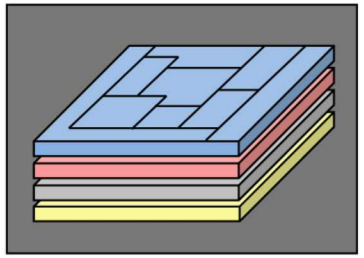
New path to scaling functionality / area without shrinking transistor size



Nanowire Transistors

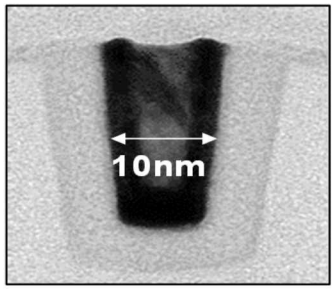


III-V Transistors

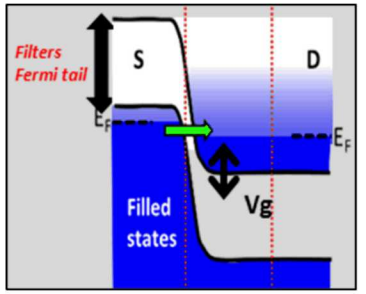


3D Stacking

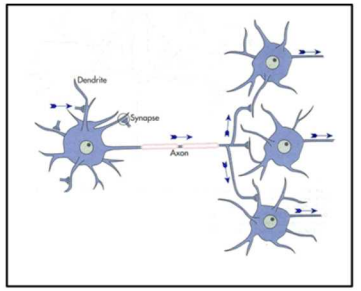
Mark Bohr, Intel 2018



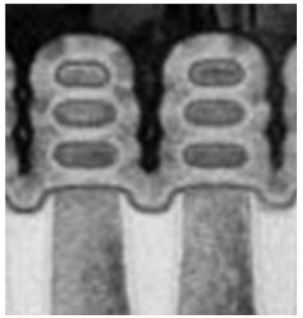
Dense Interconnects



Tunnel FETs

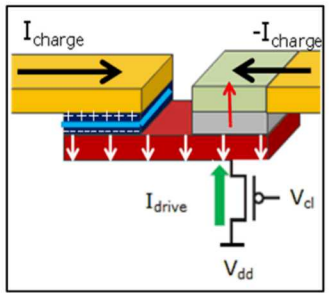


Neuromorphic Computing

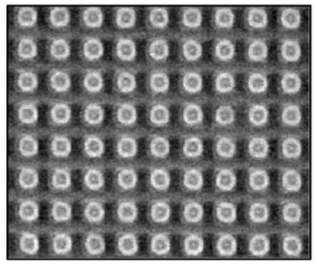


Nanosheets

Huiming Bu, IBM 2017

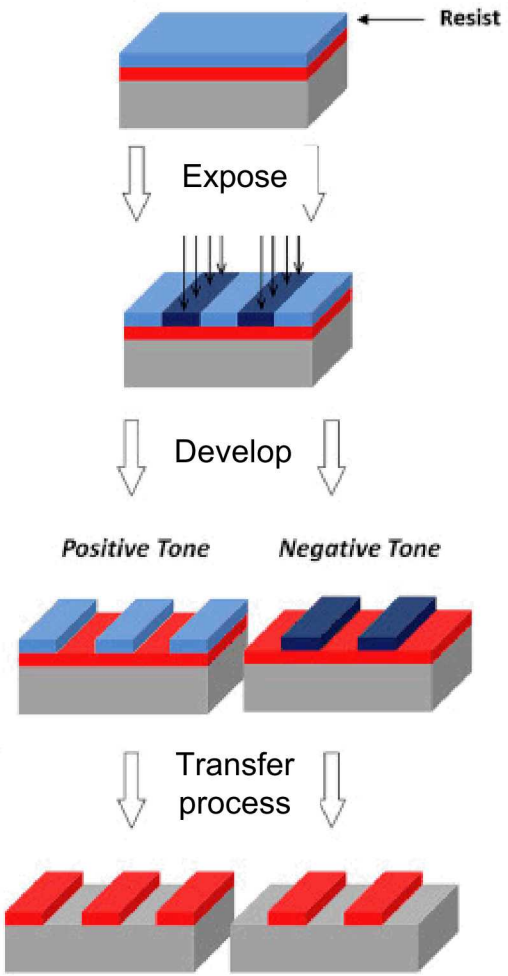


Spintronics



Dense Memory

What if you could do atomic-scale processing?

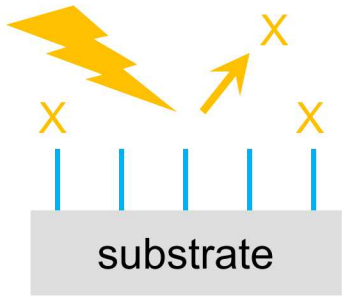


Traditional etch process

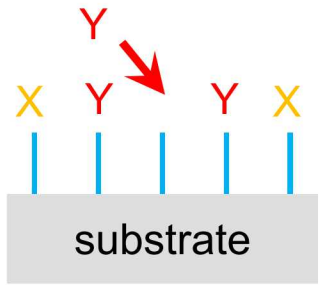
Obviate-

- Over-exposure of resist
- Resist stability after development
- Resist process stability

New approach to processing having different limitations



Expose & develop



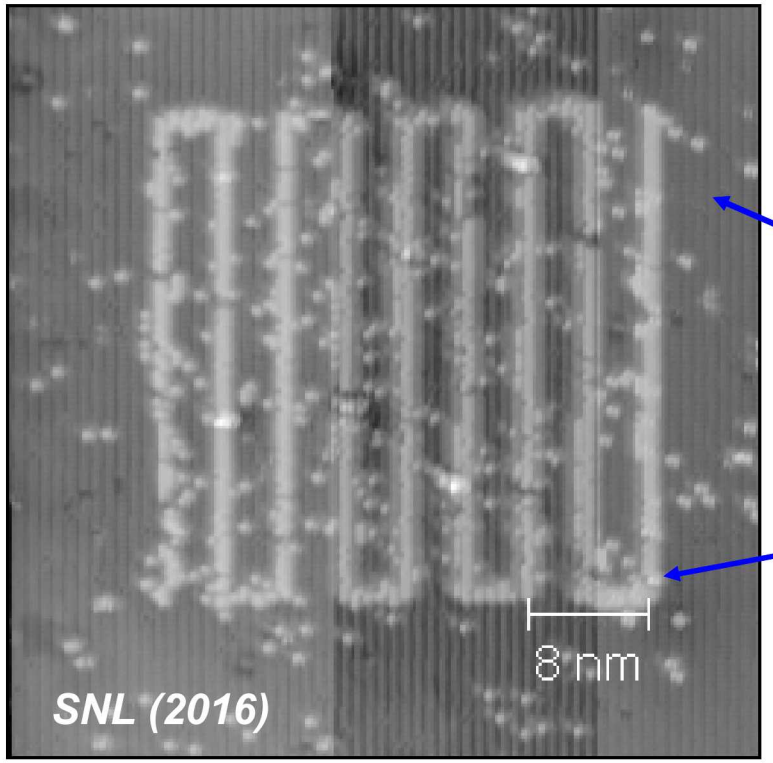
Transfer process

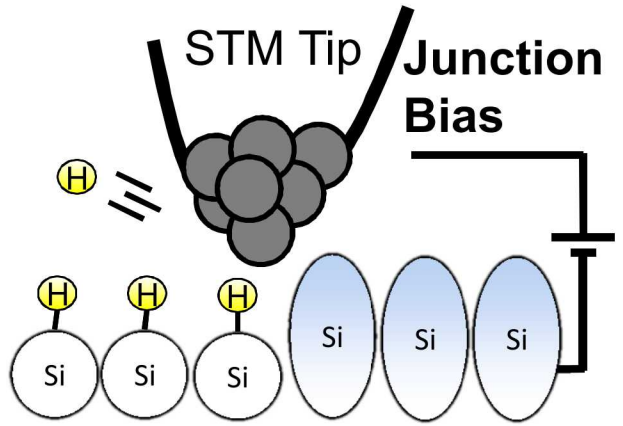
Area selective chemistry

Atomically precise advanced manufacturing (APAM)

"Chemical contrast" at Si surface

- Unterminated Si: 1 reactive bond/ atom
- H-terminated Si: unreactive

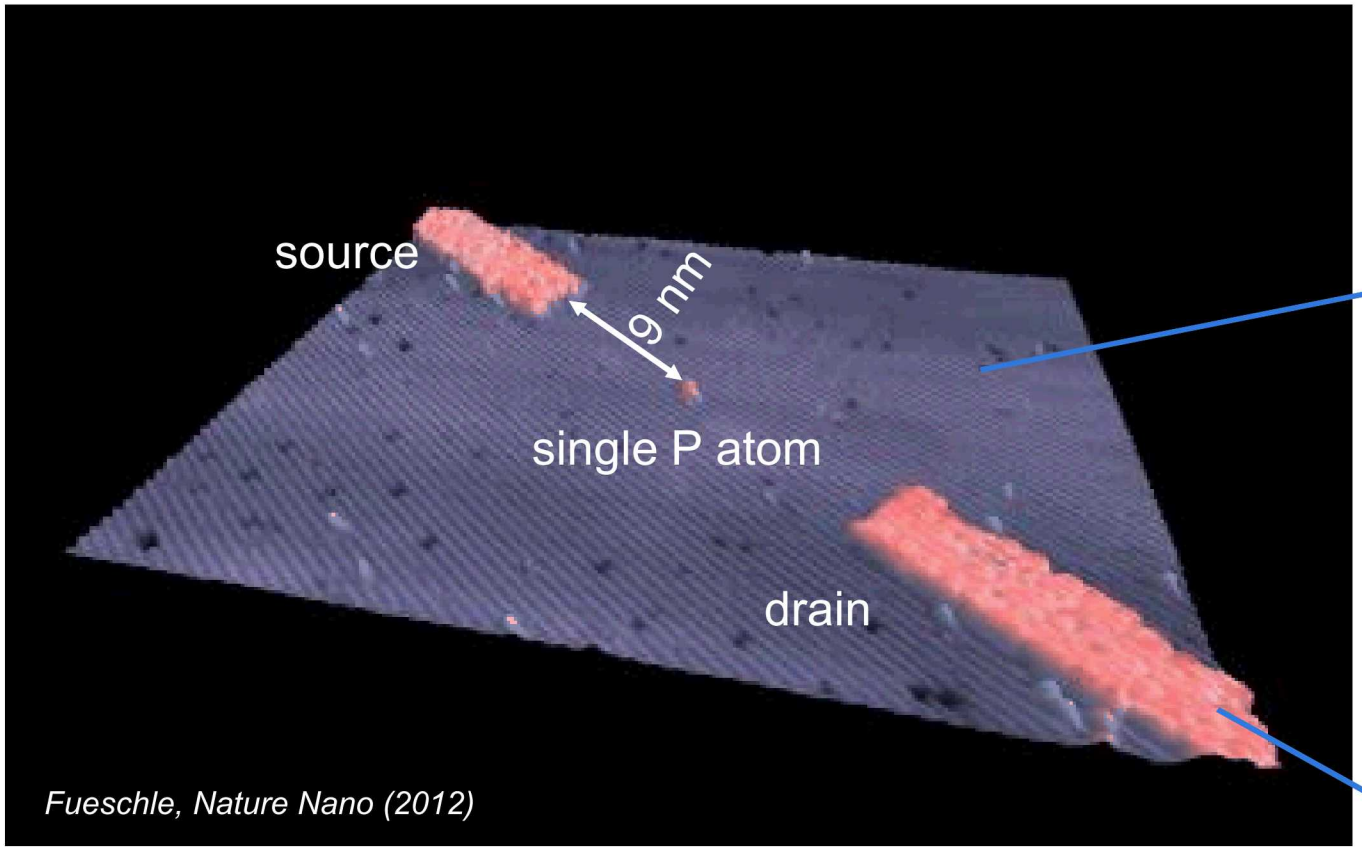


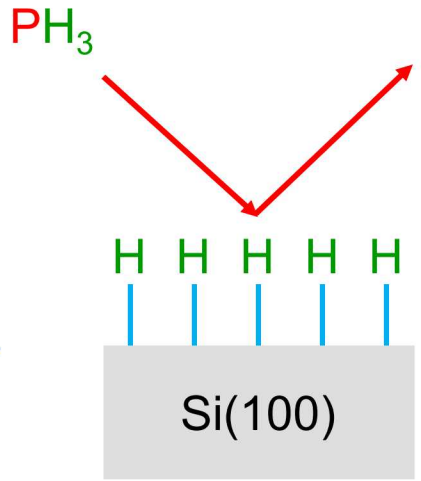


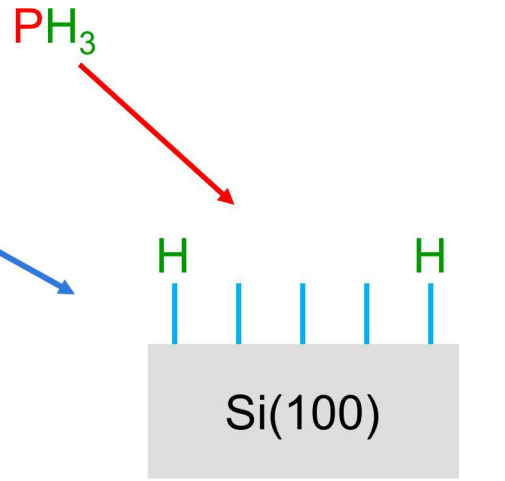
Scanning tunneling microscope (STM) can image and pattern the H-terminated surface

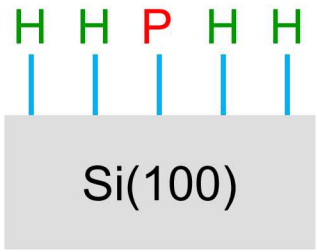
Originally: Swartzentruber, Hamers, Lyding, Shen, Avouris

Electronic devices at the limit of single atoms









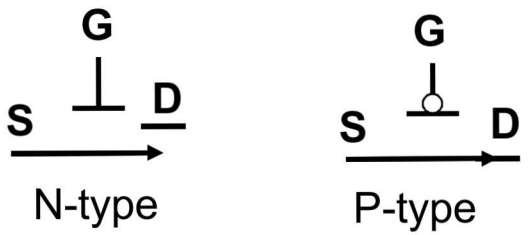
2D areas of highly P doped Si to +/- 1 lattice site precision

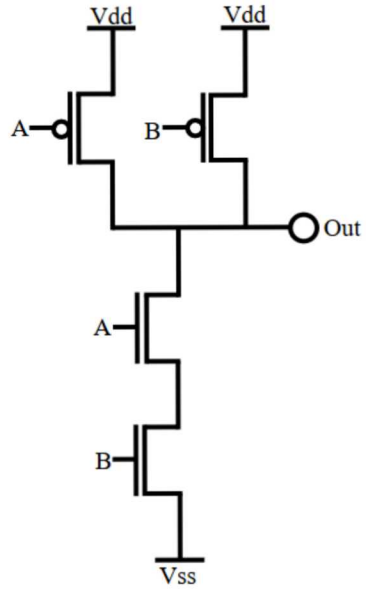
Originally: Simmons

Reconfigurable transistors – reconfigure logic at run time

Sandia National Laboratories

Conventional CMOS

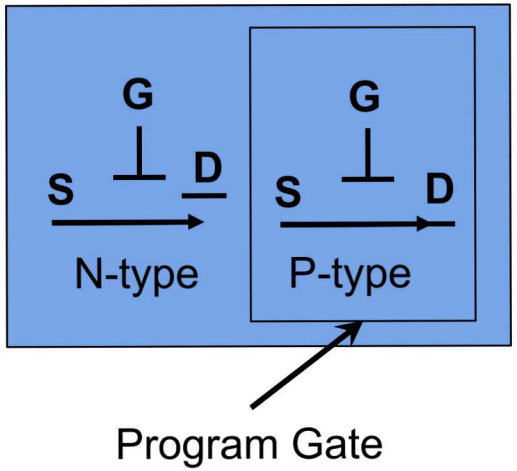


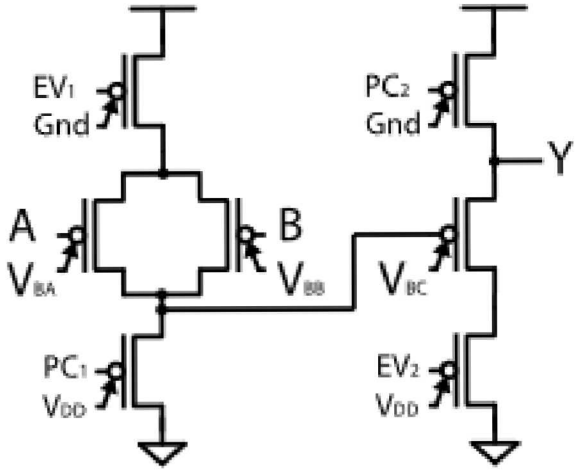


4 transistors

1 logic gate

Reconfigurable transistors





4 reg. transistors

3 reconf. transistors

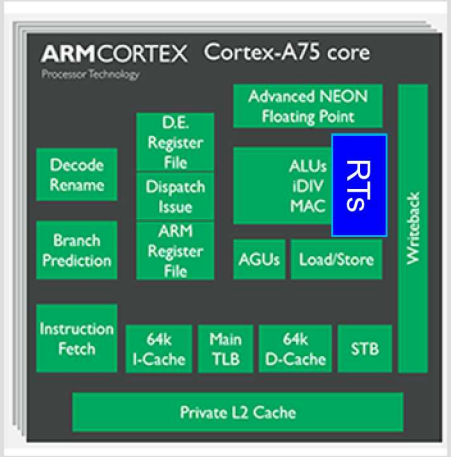
8 poss. logic gates

Gaillardon, IEEE VLSI (2015)

Reconfigurable transistors (RTs) - impact

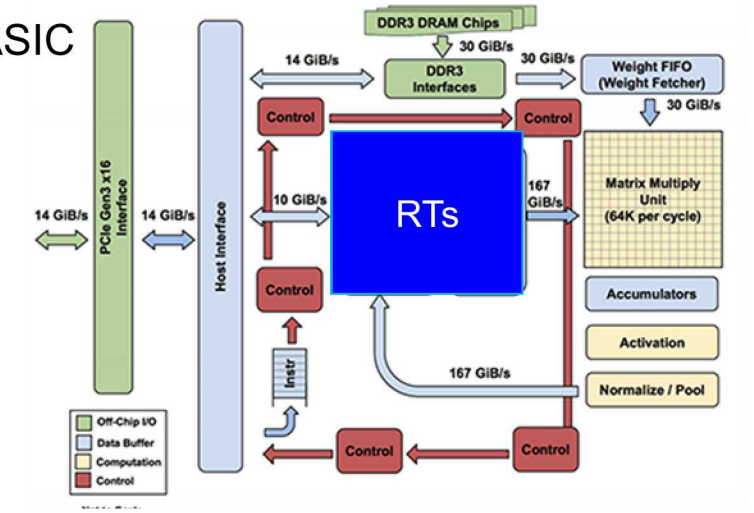
Commercial perspective

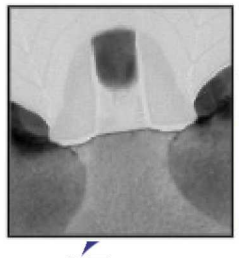
Increase functionality per unit area, power



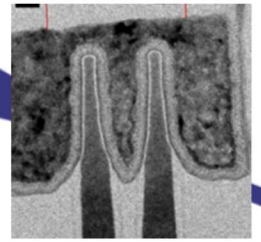
Government perspective

Mission flexibility vs. performance





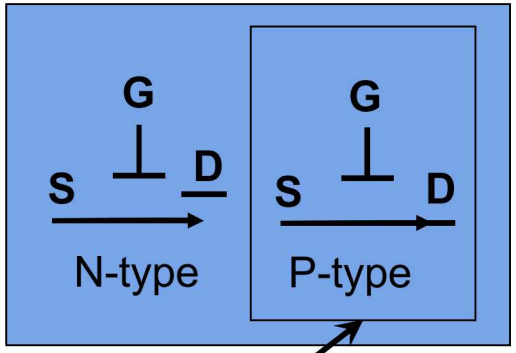
65 nm



10 nm

?

5-7 nm



Program Gate

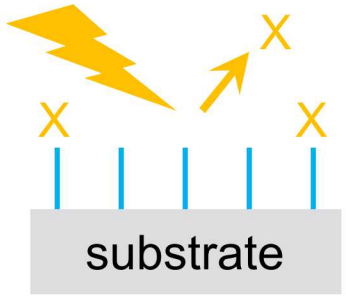
Atomic Limit

Opportunity to evaluate future impact of reconfigurable transistor technologies

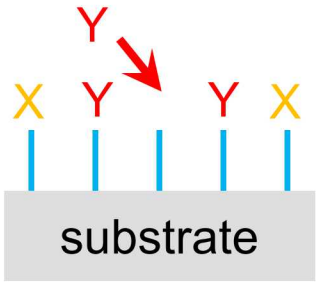
Atomic processing - impact

Sandia National Laboratories

Area selective chemistry

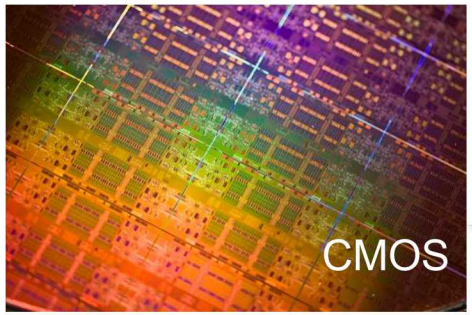


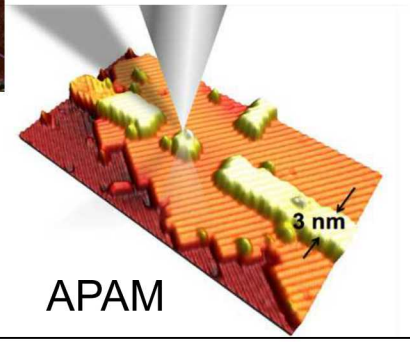
Expose & develop



Transfer process

Government perspective

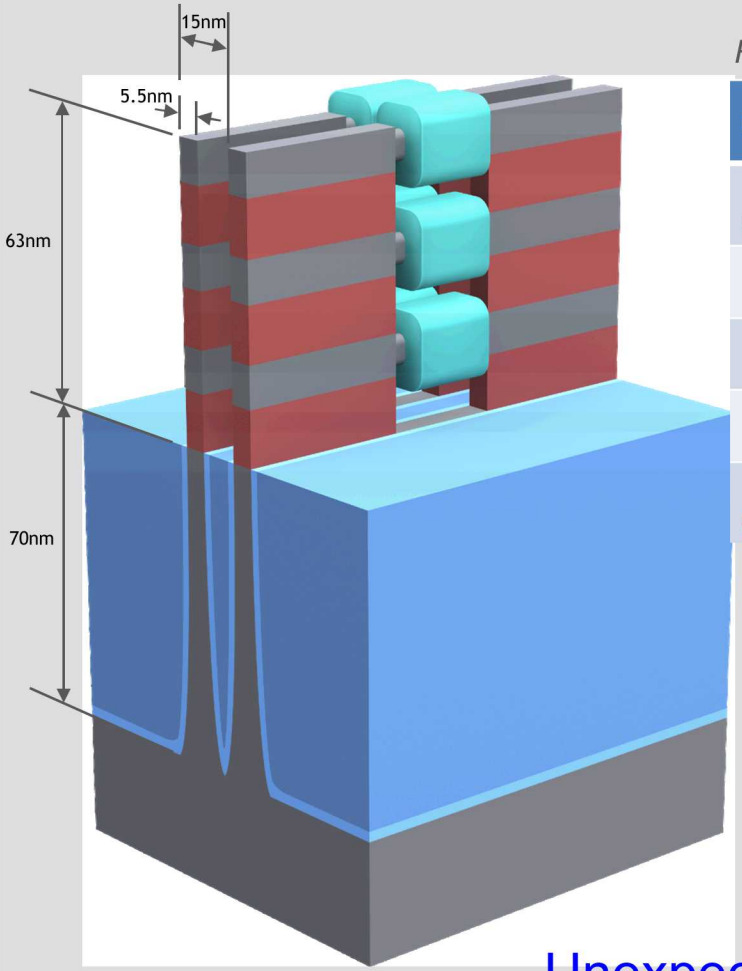




APAM

Supply chain assurance

Commercial perspective



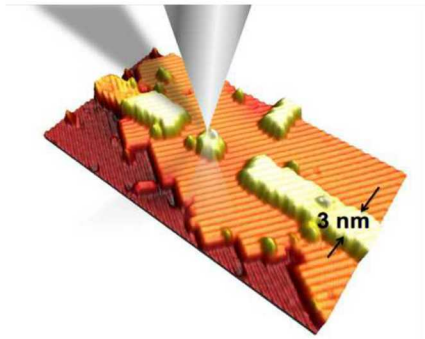
R. Arghavani estimates

Parameters	I_{ON} (mA/μm) @ $V_{GS}=V_{DS}=0.7V$	$\Delta I_{ON}/I_{ON\_FF}$
Si FinFET (H_{FIN}=37nm)	0.630	0
1 NW GAA	0.286	-0.55
2 NW GAA	0.525	-0.17
3 NW GAA	0.576	-0.09
Si FinFET (H_{FIN}=54nm)	0.690	+0.095

Compare to APAM: over 2 mA/ μm (cryogenic)

Unexpected material properties

Limitations of APAM state of the art



1

Oxide

Silicon

2

Sample clean

× Clean sample: T > 800°C

3

Hydrogen termination

4

Hydrogen patterning

5

Phosphorus incorporation

× Patterning in UHV, with STM
× Only one proven resist & dopant

6

Silicon capping

7

source

drain

Al

Al

Post processing

× Limit diffusion: T < 450°C
× Cryogenic operation only

Problems span surface chemistry, device physics, microelectronics

Foundational capabilities

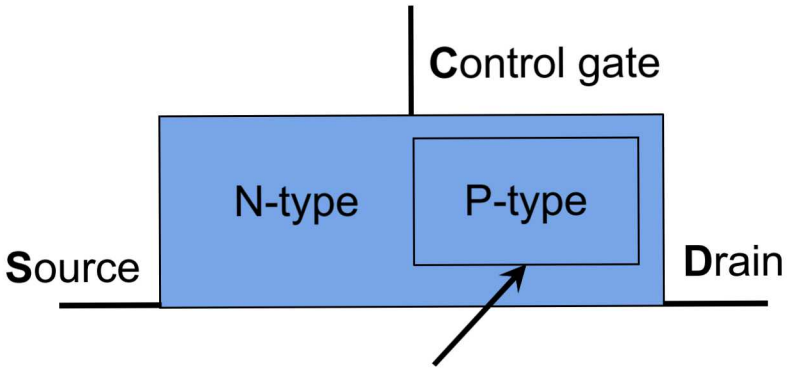
Sandia National Laboratories

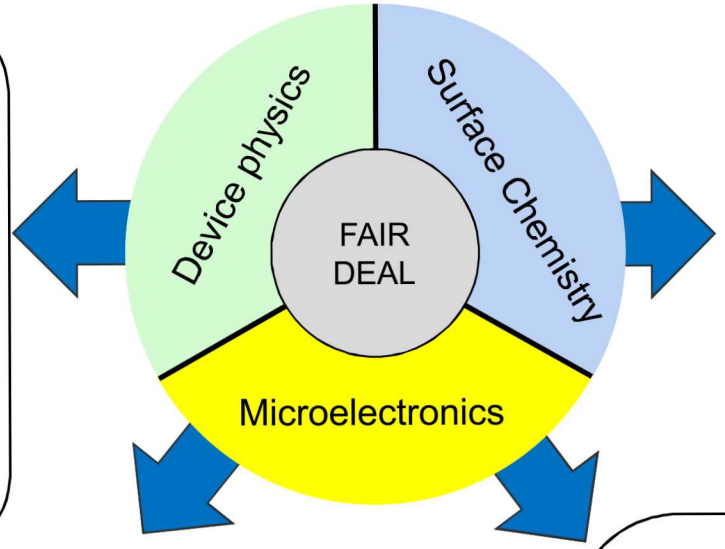
APAM SOA	FAIR DEAL	Future Impact
Purely donor-based devices	Include common transistor elements	Understand beyond CMOS device concepts at limit of atoms
Operate at cryogenic temperatures	Room temperature operation	
Rudimentary quantum transport	Reconfigurable logic	Enhance CMOS with APAM-enabled devices and processes
	Quantum transport	
No clear way to integrate with CMOS	Combine APAM & CMOS	
No clear path to manufacturability	Broaden range of resist and dopant chemistry	New manufacturing pathways – flexibility, scalability

Digital electronics at the atomic limit (DEAL)

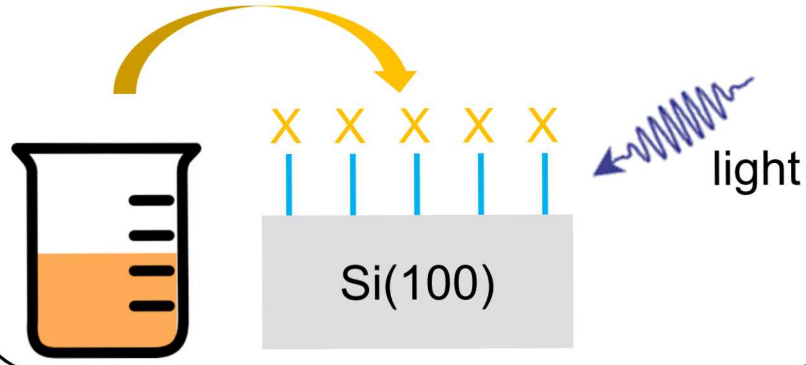
Sandia National Laboratories

Thrust 1: APAM-enabled Devices

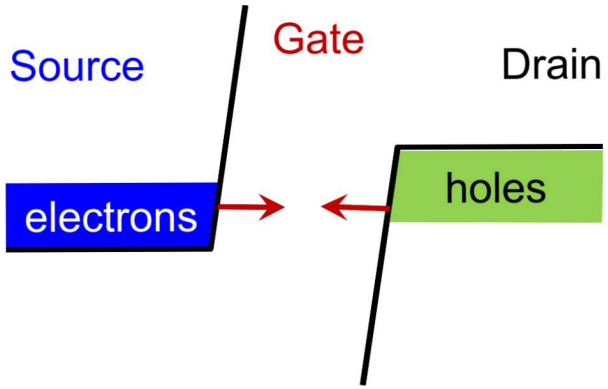




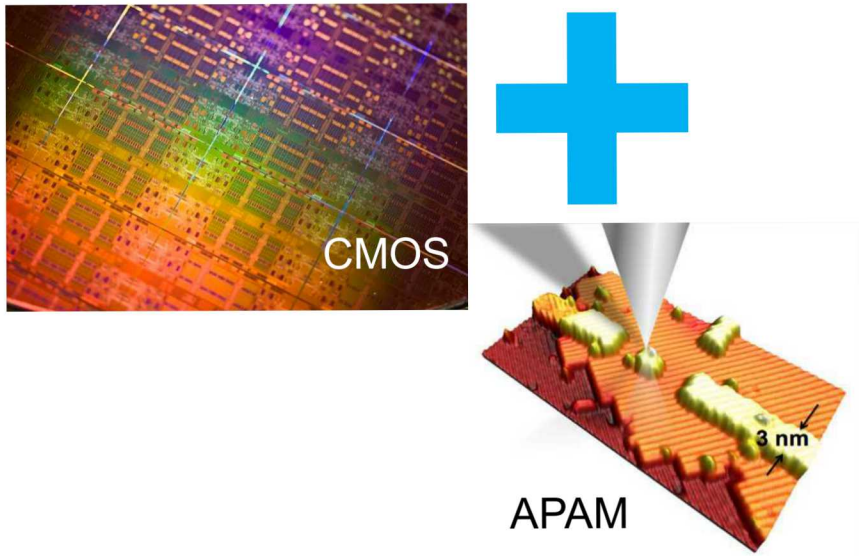
Thrust 4: Application Platform



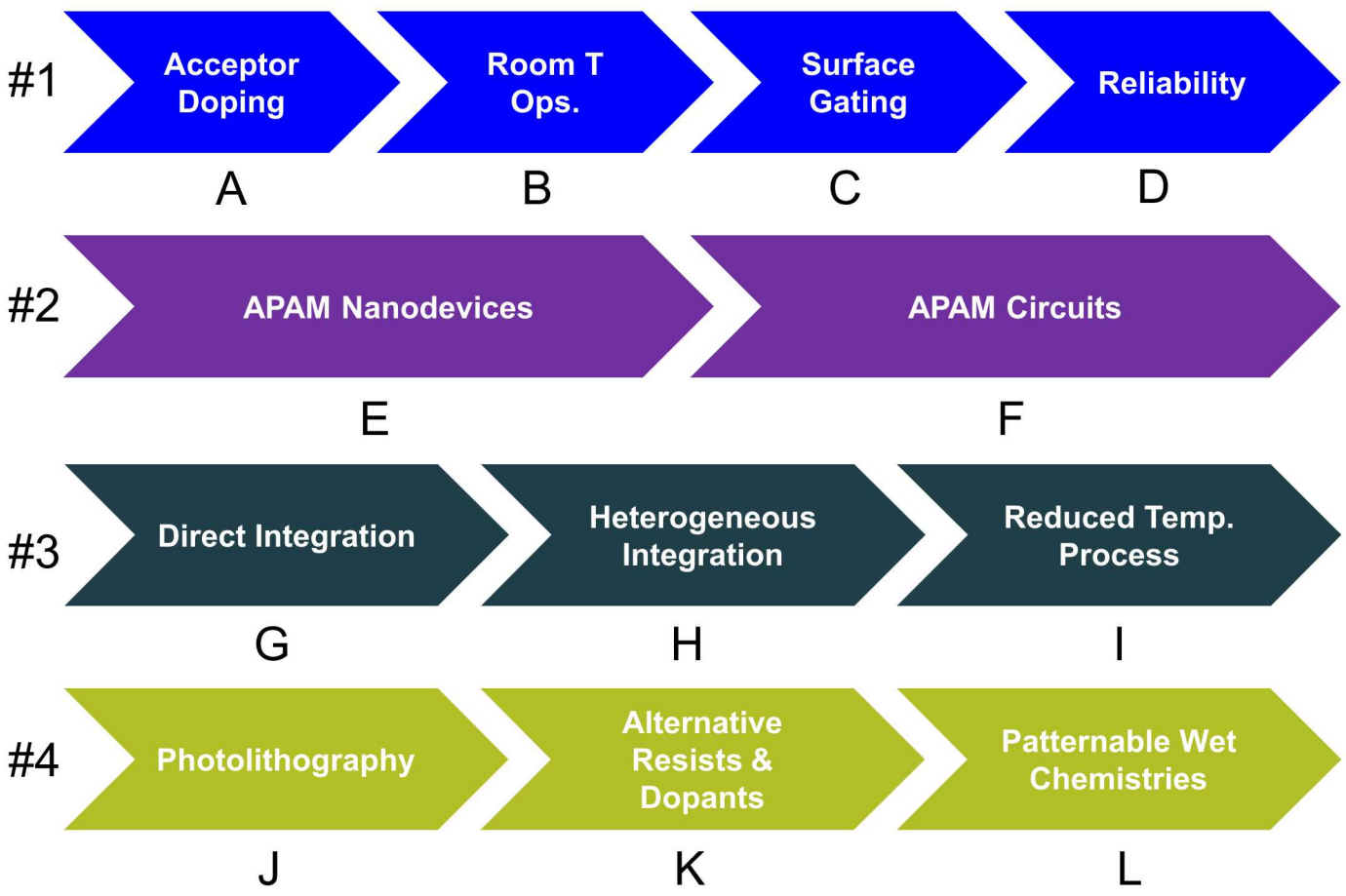
Thrust 2: APAM Modeling

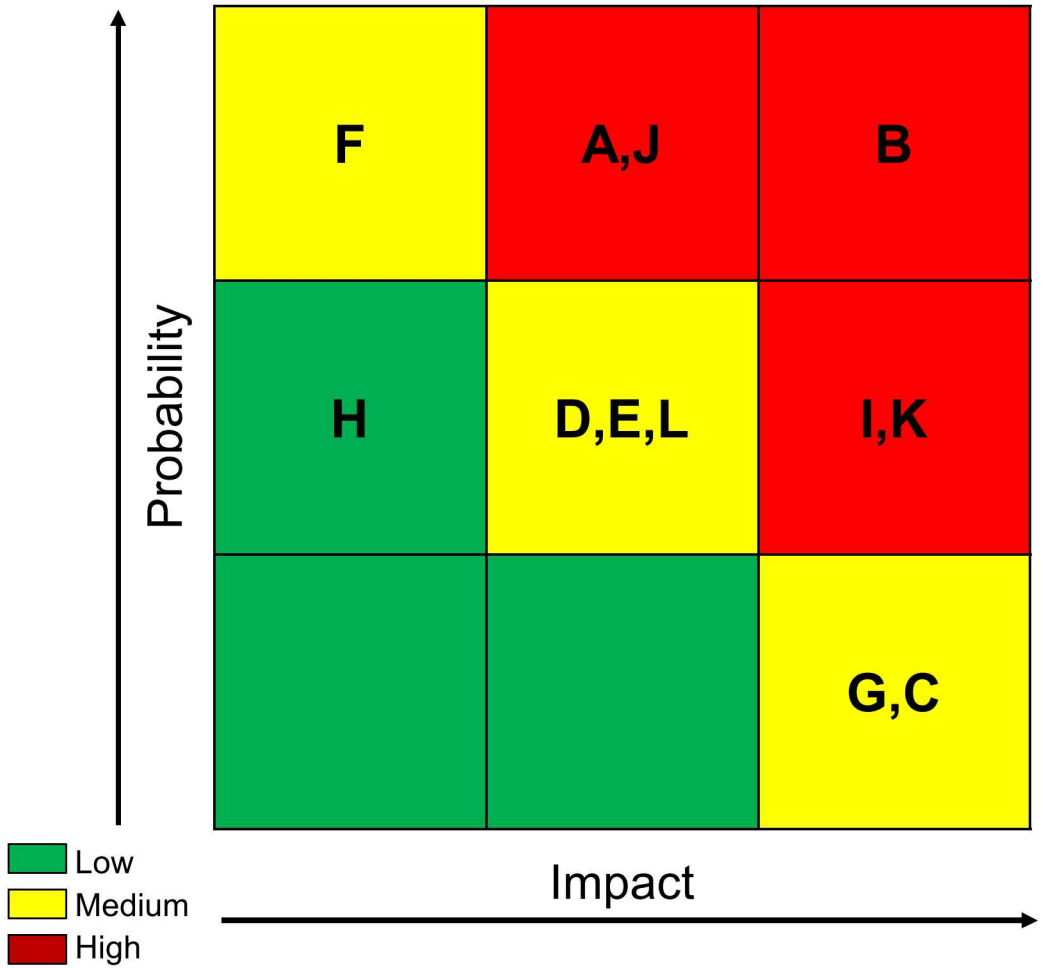


Thrust 3: CMOS Integration



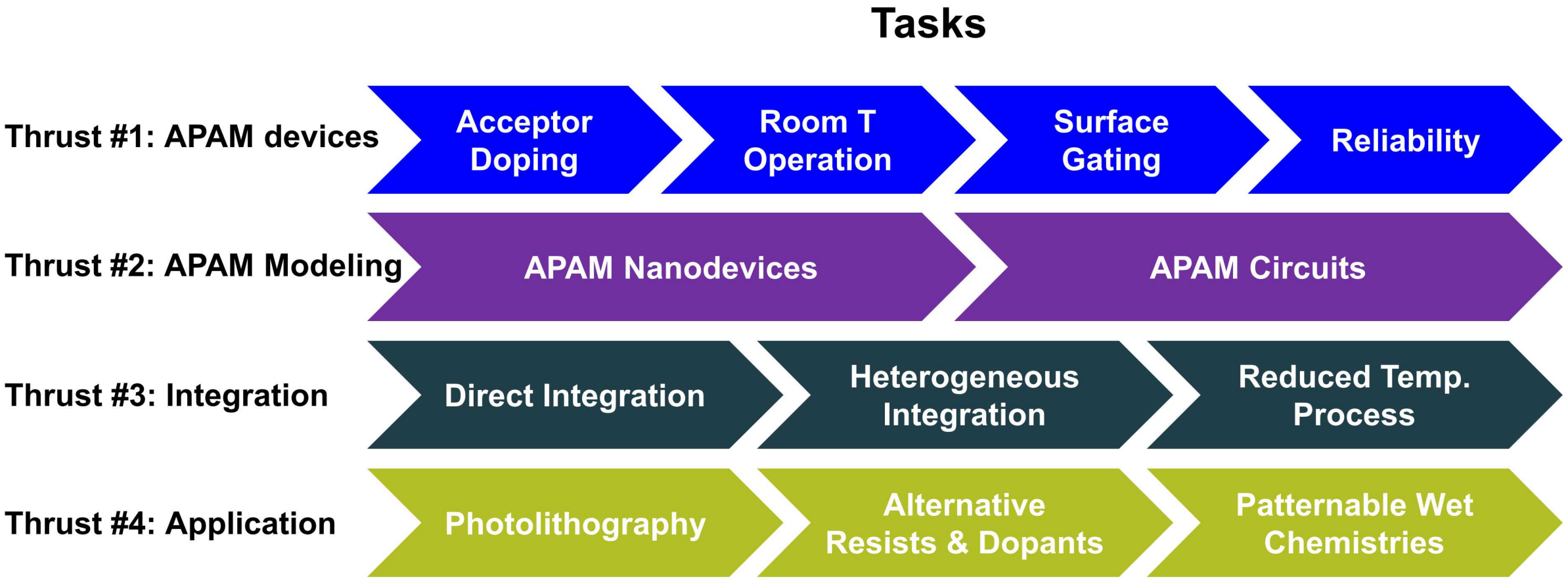
Answer high risk science questions





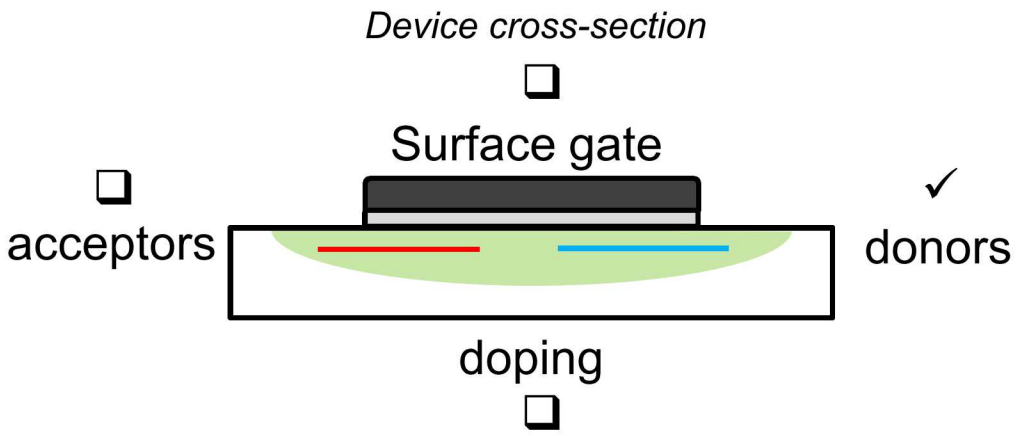
High risk derives from open science questions.
Goal: Reduce risk → move to engineering questions.

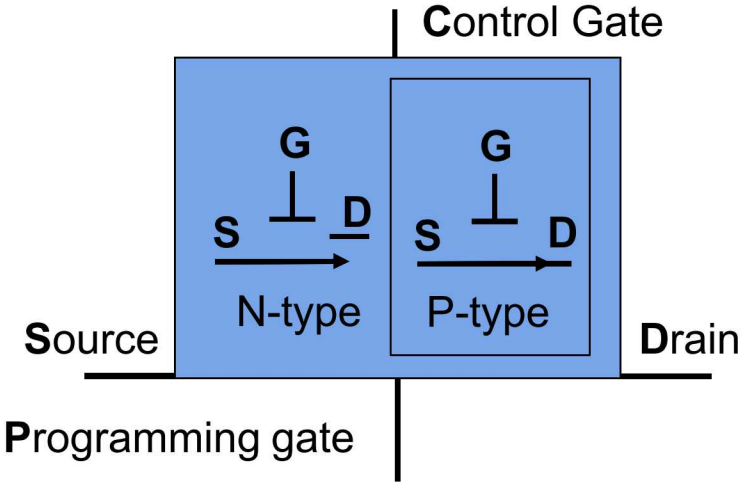
Pathfinding approach



Year 1: Try the obvious approach, evaluate alternative paths.
Year 2: Try alternative paths that remain in scope. Integrate things that work together.
Year 3: Consolidate to crosscutting goals that remain in scope.

Thrust #1: APAM devices





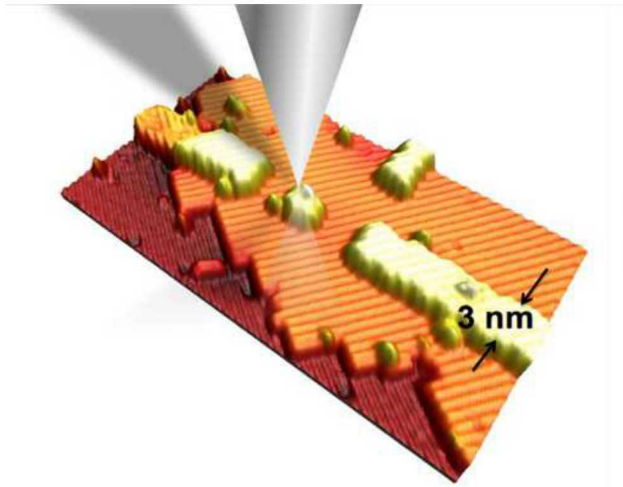
Technology	Result
Acceptor chemistry	Complementary transistors
Doping	Room temperature operation
Surface gate	Control, program device

DEAL expands the APAM toolbox to discover new transistor technologies with atomic control

Thrust #2: APAM modeling

Sandia National Laboratories

APAM



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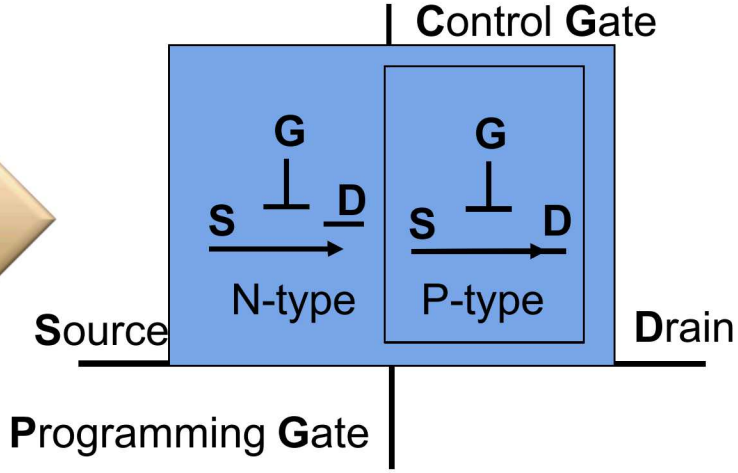
Reconfigurable transistor (RT)



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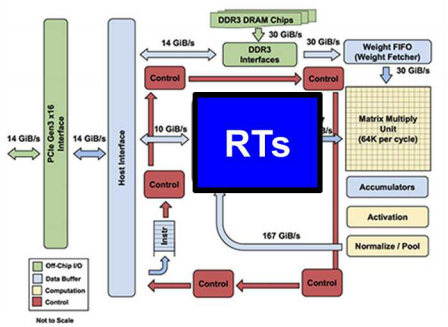
ASIC

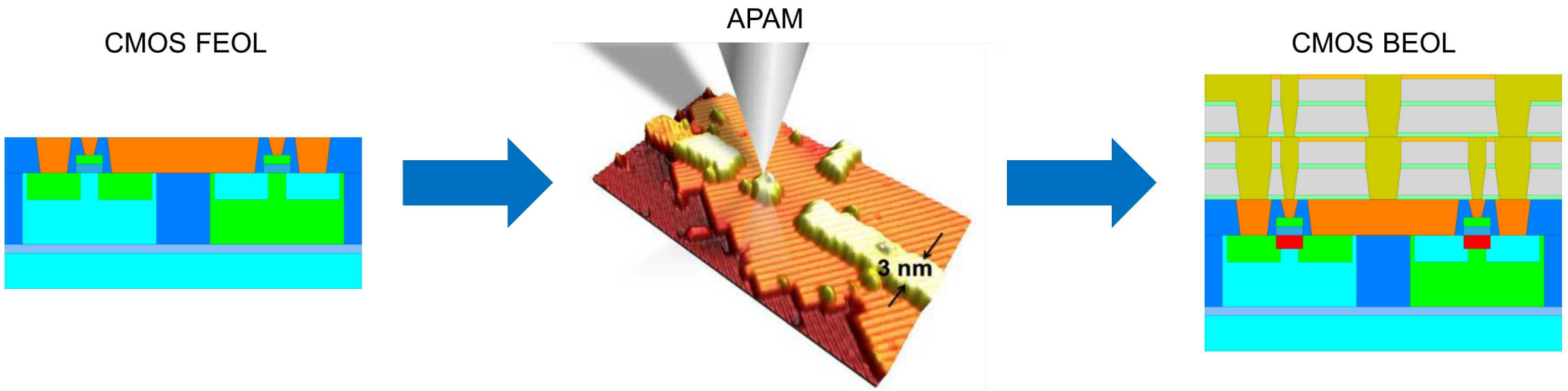


What type of nanodevices to use for APAM-enabled reconfigurable logic?

What are the rules of design for reconfigurable circuits?

DEAL establishes modeling tools to design devices and circuits for reconfigurability

Thrust #3: CMOS integration



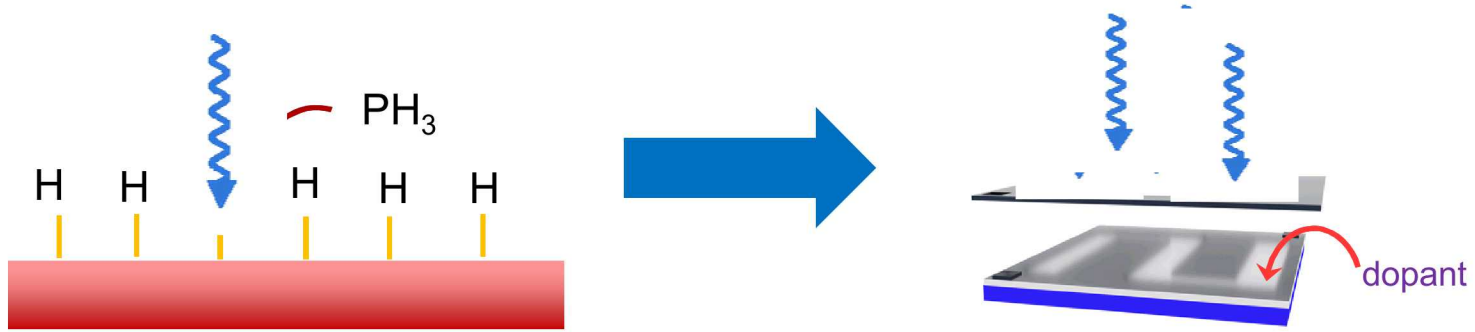
DEAL establishes proof-of-principle integration with CMOS:

- Enhance CMOS circuit with small number of APAM devices
- Add APAM processing into regular CMOS manufacturing

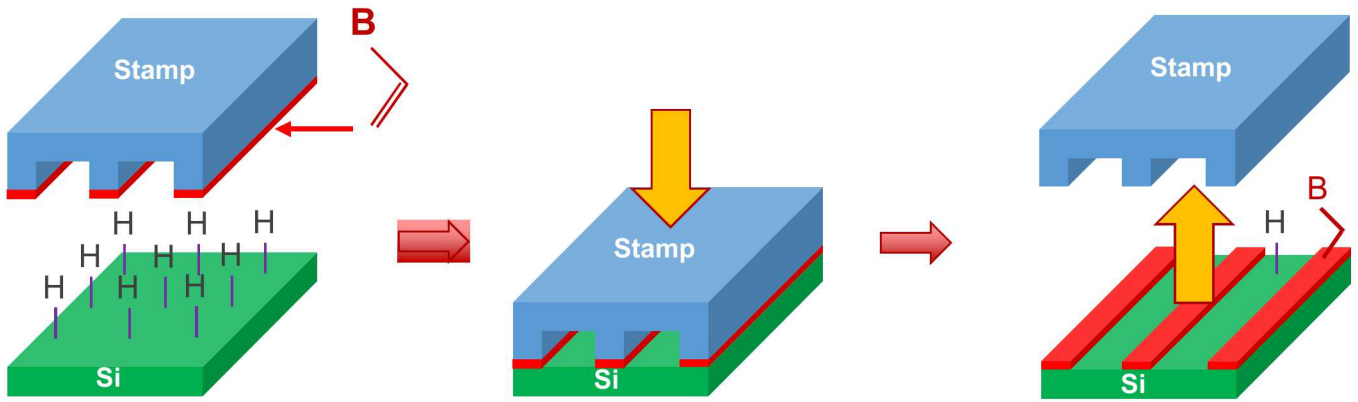
Thrust #4: Application platform

Sandia National Laboratories

Scalable photolithography



Wet stamp with molecular precursor



DEAL develops proof-of-principle *scalable workflows* built on atomic / molecular resists and dopants

Organizational chart

Sandia National Laboratories

Thrusts

Program Leadership
PI: Shashank Misra
PM: Robert Koudelka
Deputy PM: Rick Muller

#1 APAM-enabled devices
Lead: Shashank Misra

#2 APAM modeling
Lead: Denis Mamaluy

#3 Integration
Lead: Dan Ward

#4 Application platform
Lead: George Wang

Support Team
Financial: Laurel Taylor
Logistics: Lori Mann
Web: Dorean Chaleunphonh
Administrative: Felicia Pena

Cross-cutting capabilities

Measurement: Lisa Tracy, Tzu-Ming Lu, David Scrymgeour, Ping Lu, Albert Grine

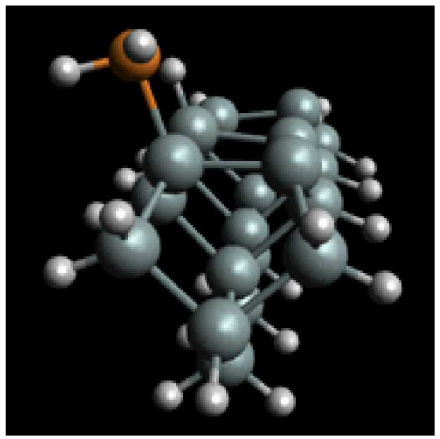
Microfabrication: Dan Ward, DeAnna Campbell, Mark Gunter, Steve Carr, Sean Smith

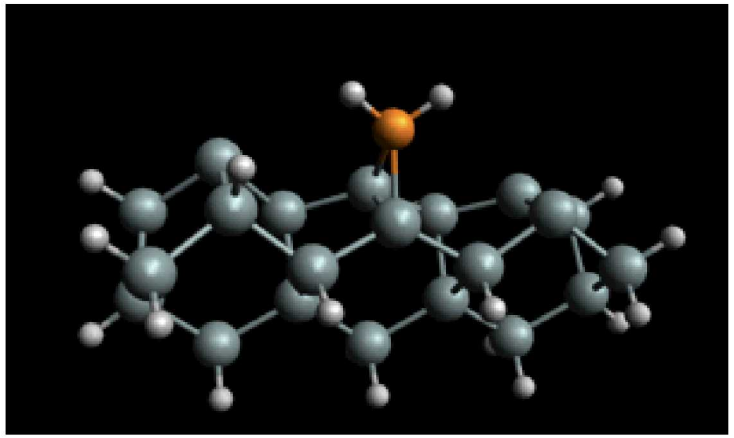
Modeling: Denis Mamaluy, Suzey Gao, Leon Maurer, Andrew Baczewski, Peter Schultz, Quinn Campbell

Surface Science: Shashank Misra, Ezra Bussmann, George Wang, Aaron Katzenmeyer, Evan Anderson, Bob Butera, Dave Wheeler

Atomistic modeling toolkit

Need to pioneer a lot of ‘new chemistry’





Some of the steps involved in phosphorus incorporation from a phosphine precursor

Accelerate pathfinding in thrusts 1 & 4

- Screening dopant chemistries
- Understanding atomic resists
- Exploring, rationalizing wet chemistry

Tools: density functional theory, quantum Monte Carlo, and kinetic Monte Carlo

Accelerate workflows

Sandia National Laboratories

Need to make many devices to answer science questions

Need faster cycles of learning for thrusts 1, 2, 3

Task	**Existing Throughput**	**Existing shortcut**	**Future accelerators**
STM	2 days	μfab proxy	Photolithography (4), sample prep (3,4)
μfab	***6 per day***	Simulators	CMOS integration (3)
Measurement	1 day	Simulators	New systems, packaging, RT operation (1)

Focus on removing rate-limiting steps & 'device-i-fying' every advance.

- '17-18: Interdisciplinary advances speed up μfab
- '18-19: Communication: sample tracking database

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