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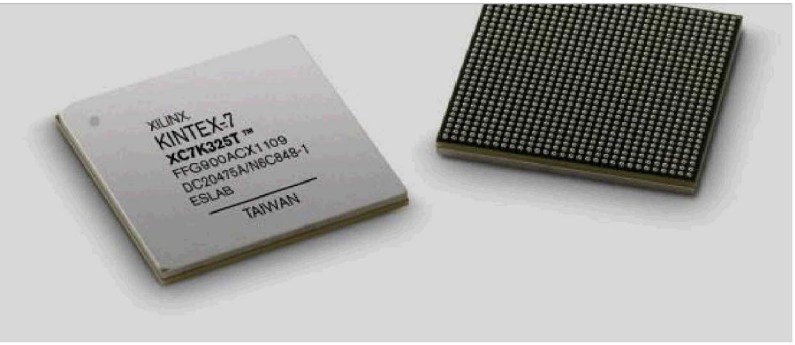

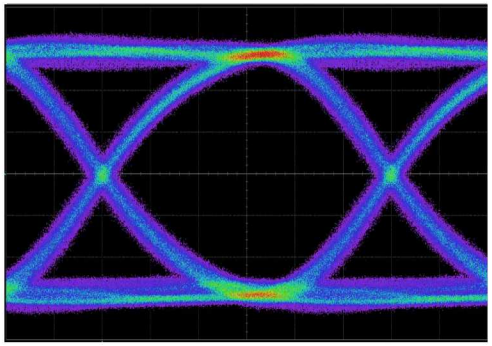

A First Peek at the KU060 UltraScale DUT Card

David Lee

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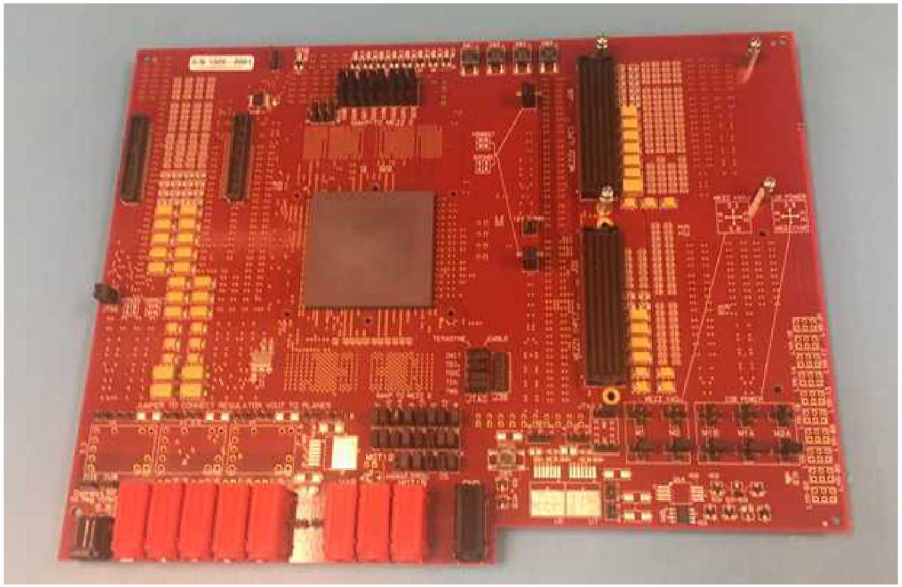
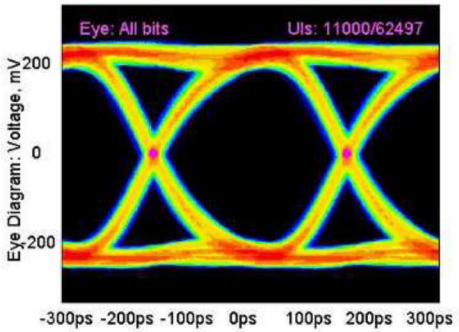
Background

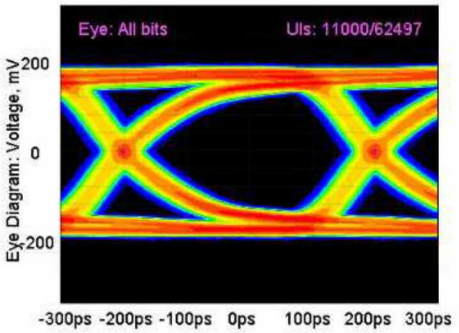
- Xilinx has announced their next space part will be based on the 20nm Kintex UltraScale KU060 device
- Sandia began development on a test platform for the KU060 device to support radiation testing and general in-house IP development in mid-2018
- Leverage lessons learned from previous Virtex-5 DUT card development (see lower right)

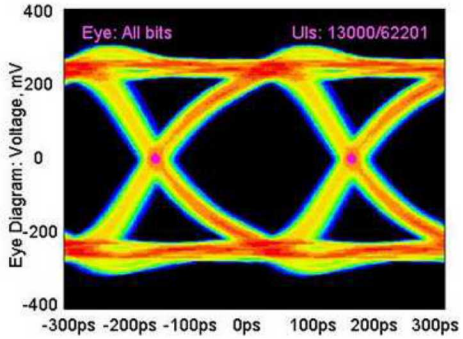


Thoughts from Virtex-5 DUT

- Expansion capabilities are extremely useful and allow your card to adapt to service a wide range of needs – within reason!
  - Too much flexibility can be dangerous
  - Diminishing returns from over-design: designing 200% extra capability will result in only 20% of it being used anyway
- Independent power rails are great for rad testers but horrible for developers
- Follow good, quantifiable engineering practices, which sometimes contradict manufacturer or “rule-of-thumb” design recommendations





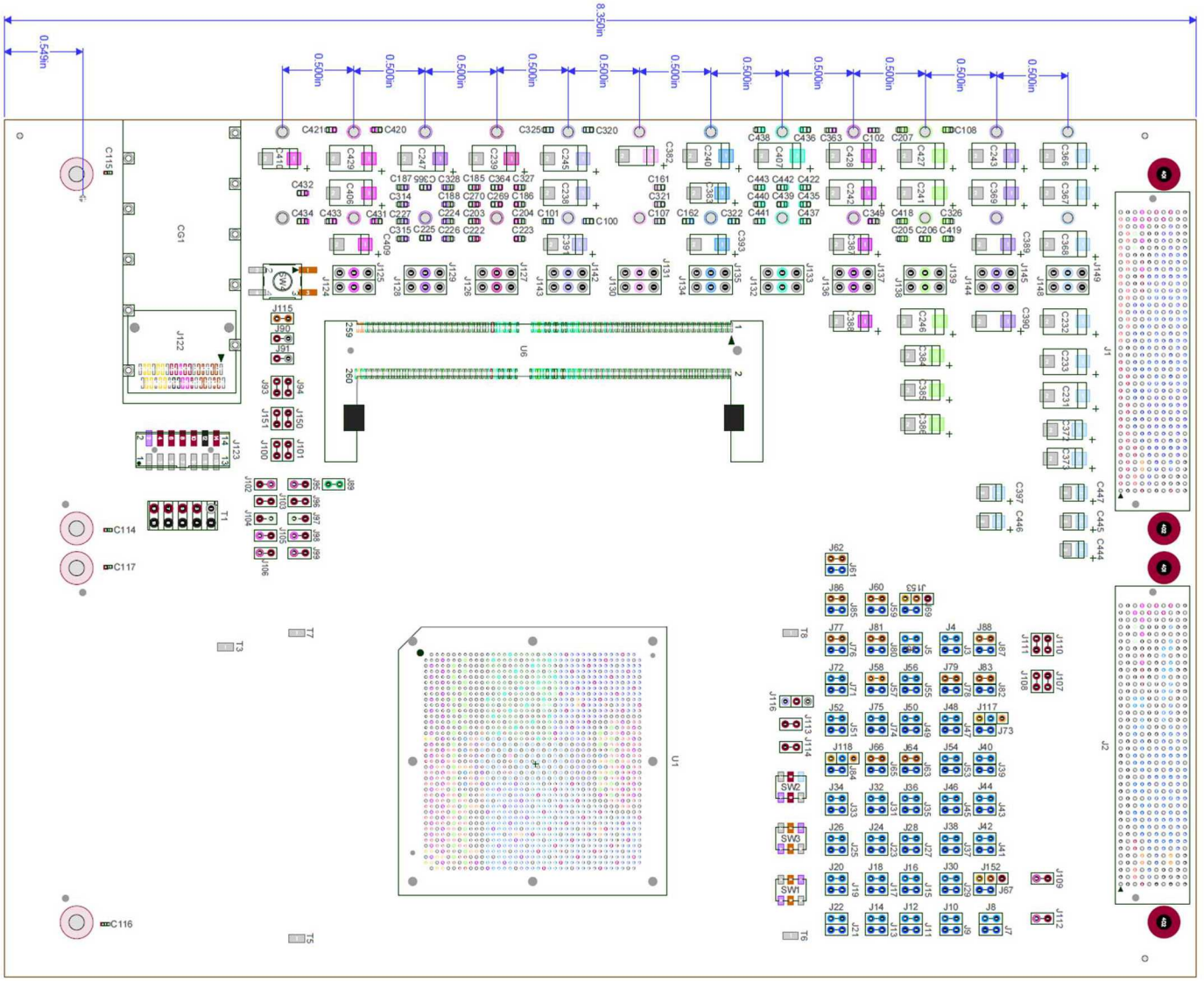


KU060 DUT Philosophies

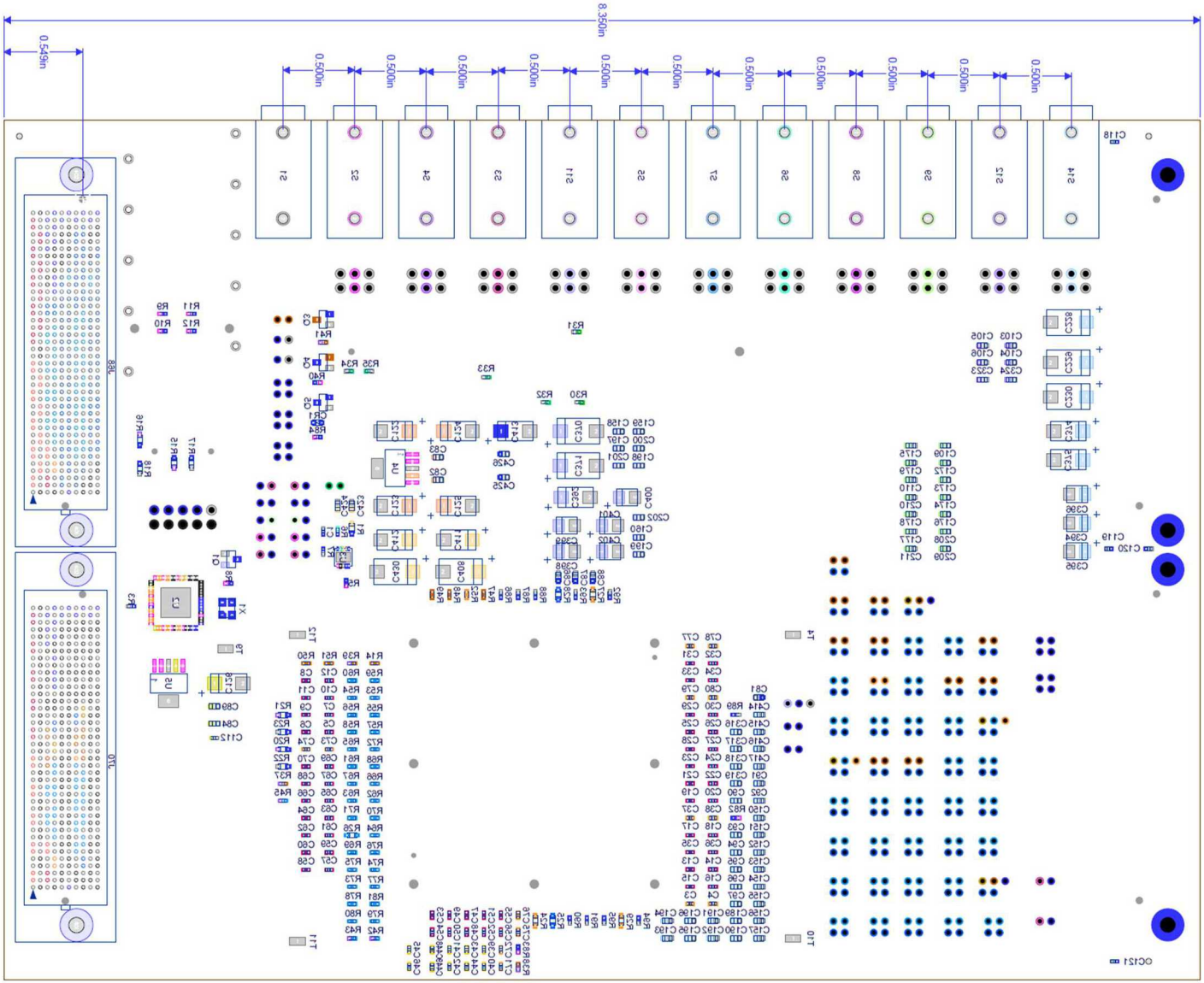
Sandia National Laboratories

- Creatively support multiple use-case scenarios while minimizing complexity
- Provide a small amount of on-board capability for the “common” things that designers use (clocks, memory, I/O) and rely on expansion cards for the rest
- Design well, but don’t over-design

KU060 DUT Card, Top

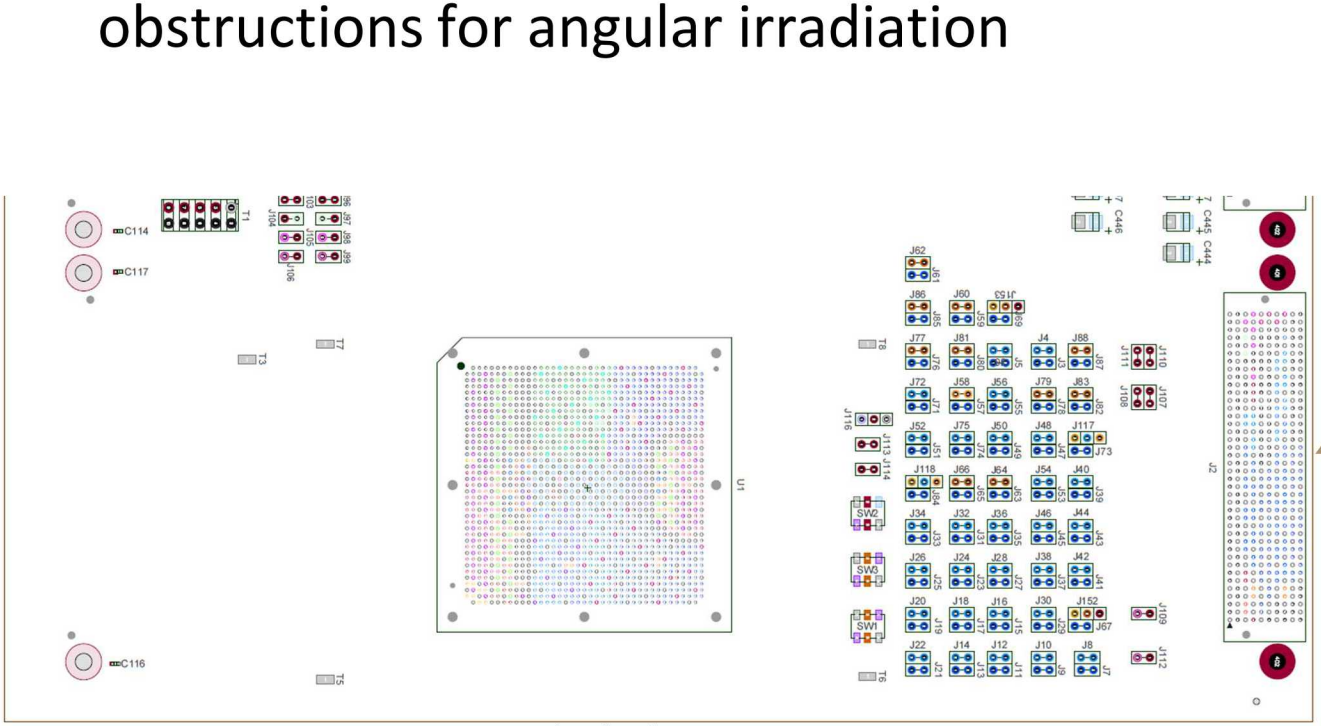


KU060 DUT Card, Bottom

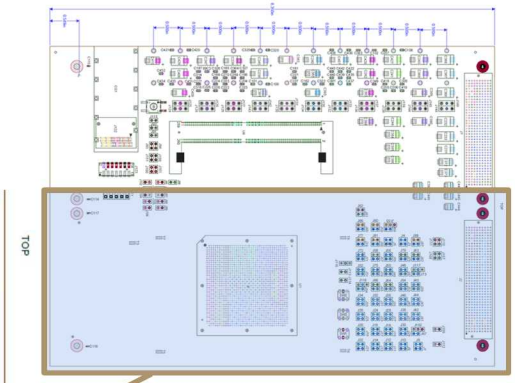


KU060 DUT Card: DUT

- DUT footprint is pin-compatible with either commercial or future rad-tolerant part
- DUT has holes around it for an optional socket
- Area to the west and south of the part are left clear to reduce obstructions for angular irradiation



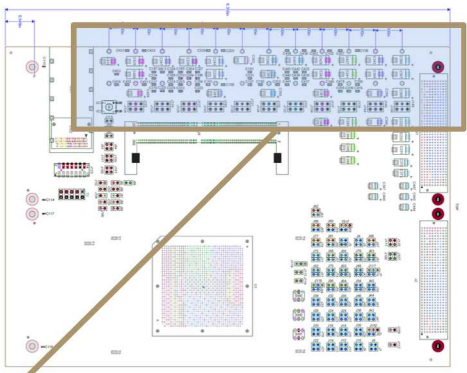
top of card



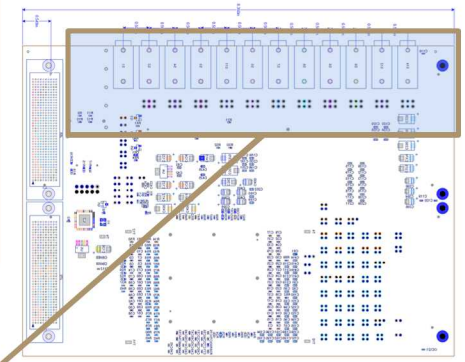
top of card

KU060 DUT Card: Power

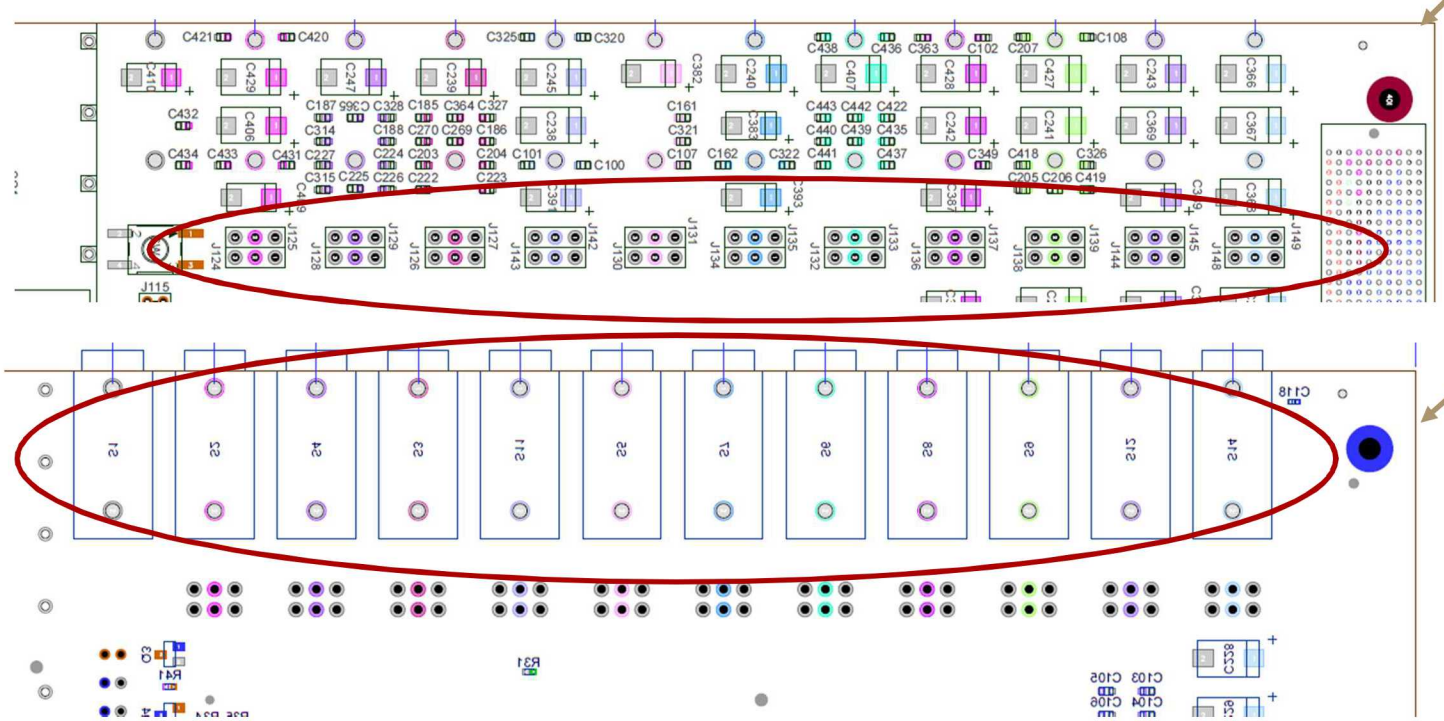
- Card is powered either through banana jacks on bottom of card, or by attaching daisy-chained Sandia power-board modules to the 6-pin connectors on the top of board



top of card

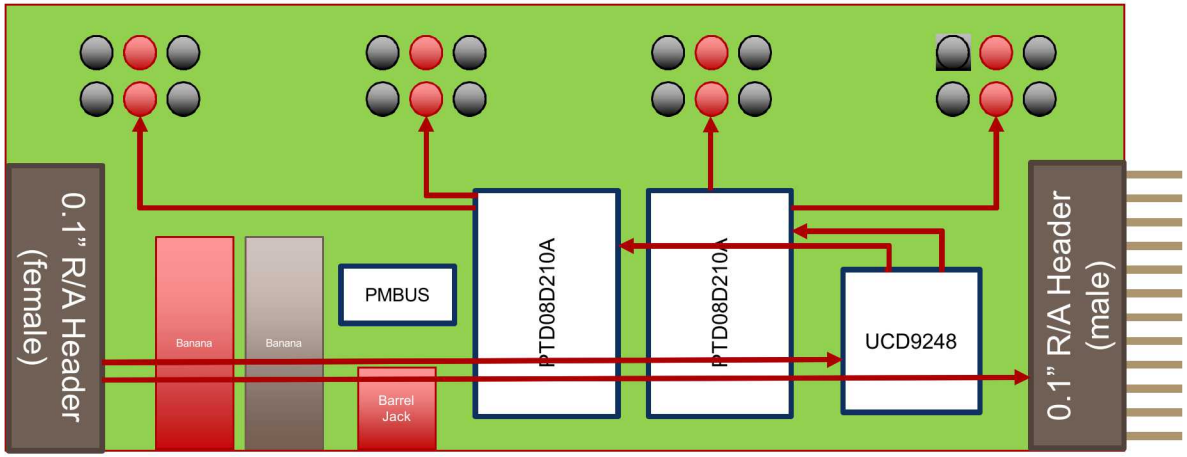


bottom of card



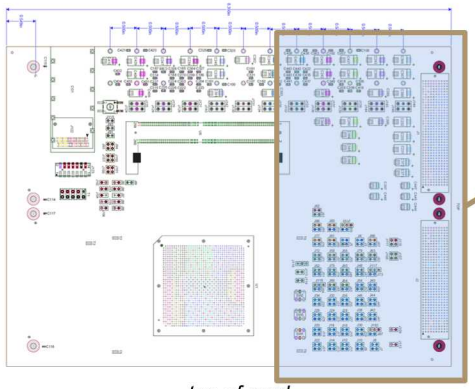
Power-board modules (PBM)

- The power-board module is based on the powering scheme used on Xilinx Virtex-7 Evaluation Boards
  - Utilizes Texas Instruments UCD9248 programmable 4-rail digital PWM controller with ECC-protected NVRAM for configuration
  - Two PTD08D210W power modules (dual-output modules at 10A output per channel) enabling four 10A outputs per PBM
  - Discrete GPIOs and “daisy-chainable” architecture allow sequencing and power-on dependencies to be set

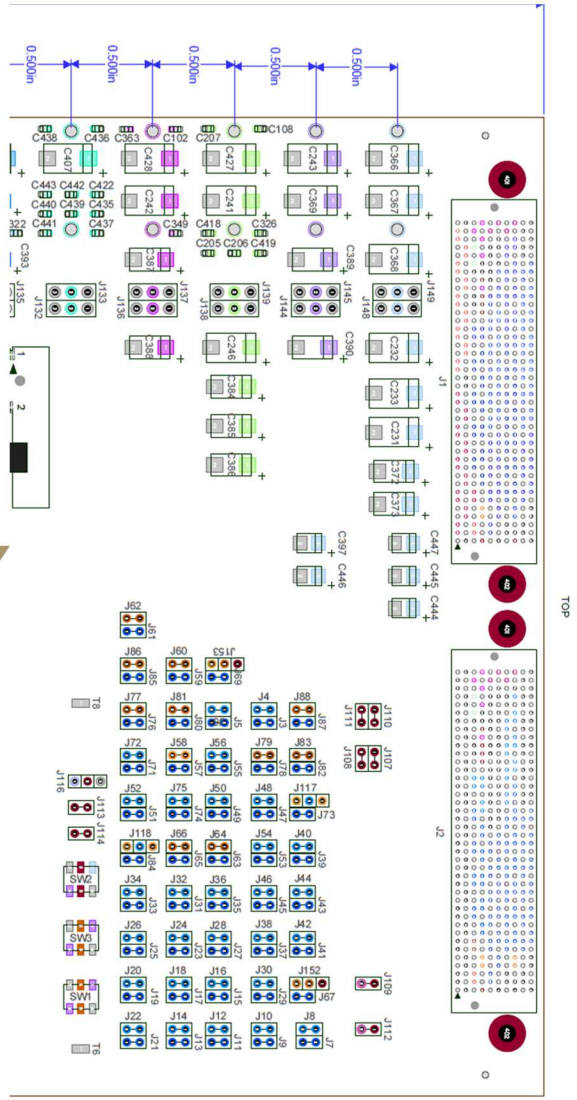


KU060 DUT Card: Top FMCs

- FMCs on the top side are **receptacles** (female) to accept expansion FMC mezzanines
- One FMC implemented as HPC and one as LPC
- VADJ is fixed at 1.8V



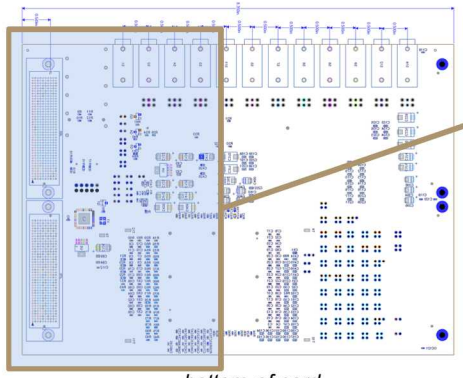
top of card



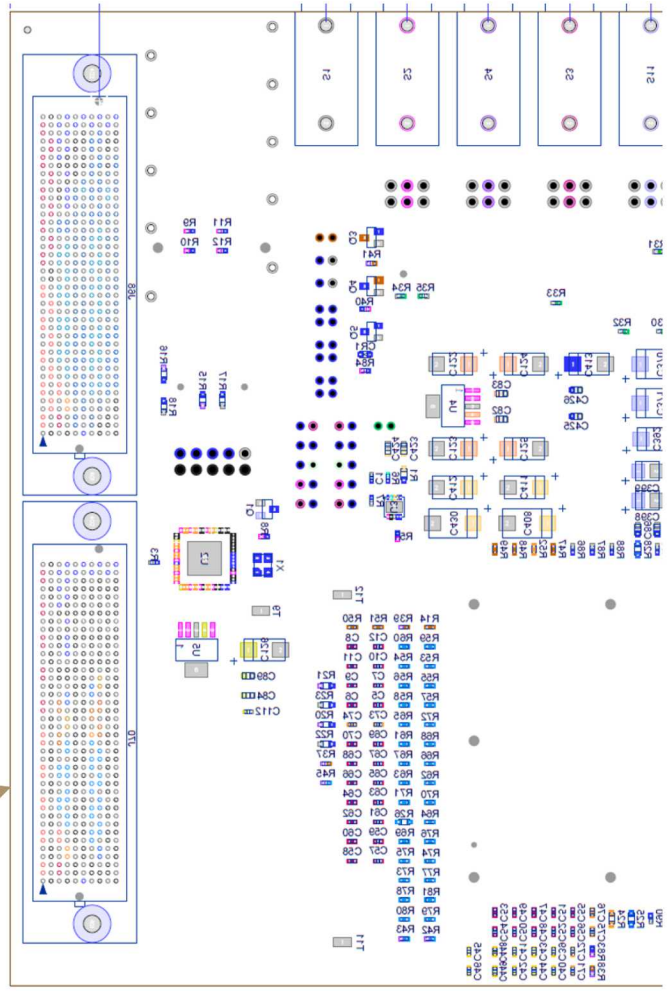
top of card

KU060 DUT Card: Bottom FMCs

- FMCs on the bottom side are **plugs** (male) allowing the DUT card to act as a FMC mezzanine
- One FMC implemented as HPC and one as LPC, VADJ is fixed at 1.8V
- Allows this card to be plugged in to many Xilinx eval boards, or even into another DUT board



bottom of card

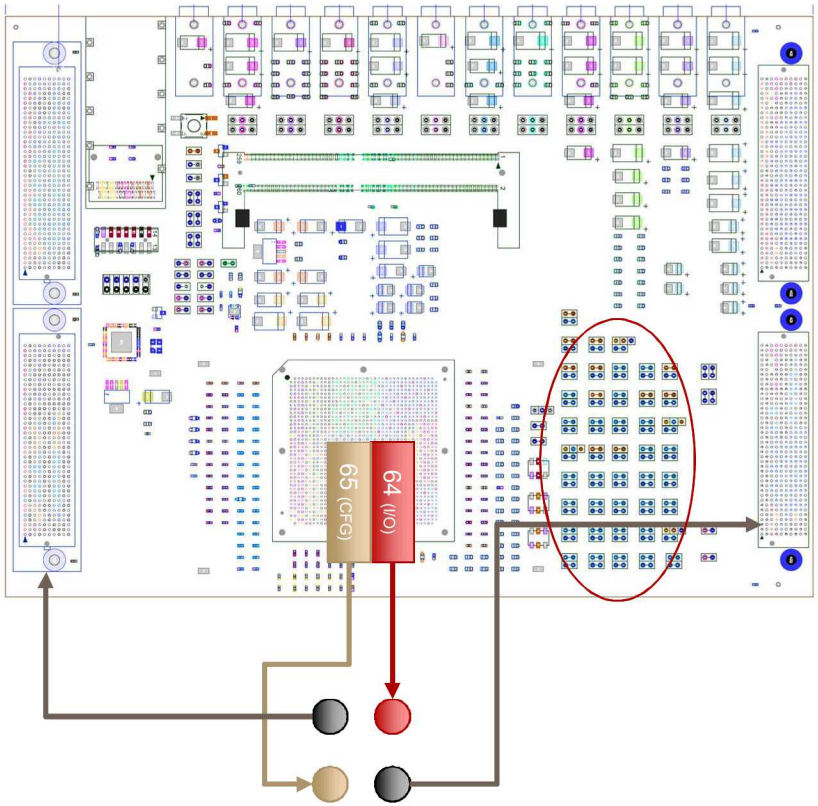


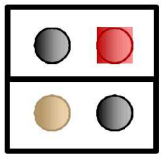
bottom of card (looking through the card)

KU060 DUT Card: JTAG/SelectMAP

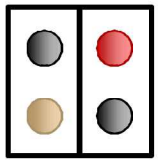
- A number of 2mm jumper blocks are placed to route JTAG/ SelectMAP/BPI signals to either the top (mezzanine) or bottom (carrier) FMC connector
- Installing shunts horizontally route bank 65 (SMAP/BPI) up and bank 64 (HRIO) down; installing shunts vertically routes bank 65 down and 64 up
- Allows different configuration schemes:
  - Attach BPI flash to FMC expansion connector on top of board
  - Drive SelectMAP from ZC706 carrier from bottom FMC
  - Install 0.1” shunt diagonally to connect bank 64 to bank 65

Top and bottom of card, overlaid together





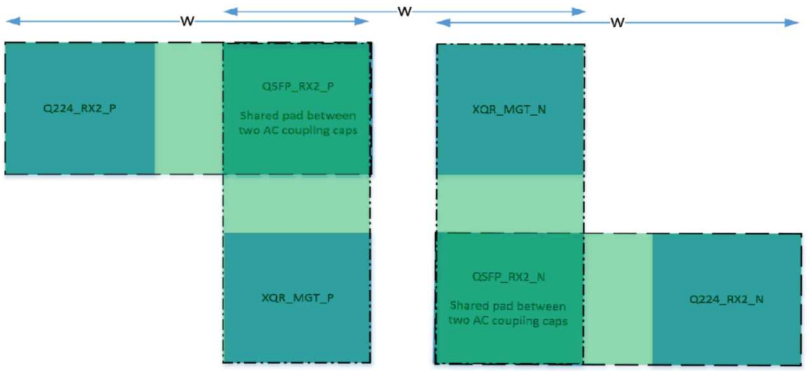
Shunts in this orientation: Bank 64 HRIO connected to carrier, SMAP/BPI pin on Bank 65 connected to mezzanine expansion connector



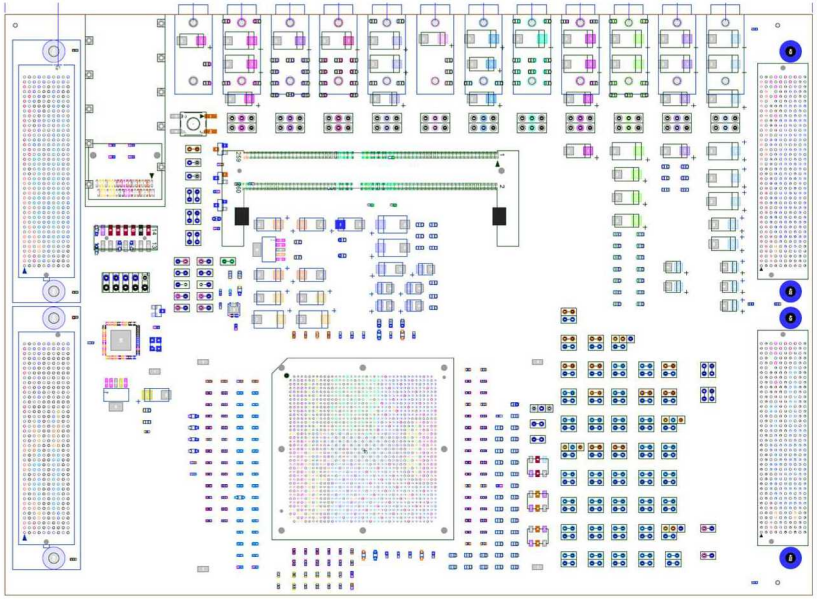
Shunts in opposite orientation: Bank 64 HRIO connected to mezzanine expansion connector, SMAP/BPI pin on Bank 65 connected to carrier

Other stuff

- QSFP connector for MGTs
  - Quick way to get MGTs off-board without the real estate of SMAs
  - One MGT RX lane is on different pins for the new part
  - A small AC-coupling capacitor “mux” allows both commercial part and new part package to use this lane
- Clock synthesizer
- SODIMM socket for DRAM
- Pushbutton for PROG



Top and bottom of card, overlaid together



Conclusion

- Board should be built in early September 2018
- Testing priorities are:
  - Re-verify SEL under a variety of operating parameters
  - Collect better fidelity static characterization data for configuration SRAM, flip-flops, and BlockRAM™
  - I/O, MGTs, DSPs, and/or MMCMs are next priority, but will coordinate with XRTC to avoid duplication of efforts