SAND2018-8749C

Design and characterization of a novel, 1 ns, multi-frame imager for the Ultra-Fast X-ray Imager (UXI) program at Sandia National Laboratories

L. Claus[1]*, A. Boone[1], T. England[1], L. Fang[1], Q. Looker[1], B. B. Mitchell[1], A. Montoya[1], J. L. Porter[1], M. Sanchez[1], A. Vigil[1], E. R. Hurd[2], A. Carpenter[2], M. Dayton[2], C. E. Durand[2], G. Rochau[1]

[1]Sandia National Laboratories, 1515 Eubank SE, Albuquerque, NM 87123, USA

[2]Lawrence Livermore National Laboratory, Livermore, California 94550, USA

ABSTRACT

The Daedalus camera is a second-generation imager for the Ultra-Fast X-ray Imager (UXI) program, achieving 1 ns, time-gated, multi-frame image sets for High Energy Density (HED) physics experiments. Daedalus includes a 1024 x 512 pixel array with 25 μm spatial resolution with three frames of storage per pixel with three times larger full well (1.5 million e^-) than the last generation camera, Icarus. Daedalus incorporates an improved timing generation and distribution concept to facilitate broader user configurability and application space while improving timing resolution to 1 ns. Electrical timing measurements demonstrated 1 nanosecond shutters. Analog dynamic range is sufficient to provide the expected full well. Read noise of 210 e^- has been measured, exceeding design goals.

Sandia National Laboratories is a multimission laboratory managed and operated by National Technology and Engineering Solutions of Sandia LLC, a wholly owned subsidiary of Honeywell International Inc. for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-NA0003525.

Keywords: ASIC, multi-frame, pixel, ROIC, hybrid-CMOS, high-speed

1. INTRODUCTION

The Ultra-Fast X-ray Imager (UXI) program has produced a series of nanosecond-time-scale, time-gated, multi-frame hybrid-CMOS sensors for the High Energy Density Physics (HEDP) community. The experiments conducted in this field of research evolve on the picosecond to nanosecond timescale while lasting a few nanoseconds in total duration. There is a robust need in the community for 2D sensors to document the temporal evolution of experiments to yield deeper insight to the phenomena under investigation.

Past UXI sensors are being fielded across the national HEDP experimental facilities with new applications and diagnostics being proposed frequently. Previous UXI sensors [1,2] have demonstrated shutters as fast as 1.5 nanoseconds for two to four image frames. These past sensors have targeted two different full wells of 500 ke^- to 1.5M e^-, trading total full well for number of frames. The Icarus sensor has lower full well (500ke^-) with four frames per pixel and has demonstrated significantly improved timing uniformity compared to the earlier Furi [3,4] and Hippogriff [5] sensors. All three sensors have been fielded in a variety of HEDP diagnostics; a Furi sensor provides time gated imagery of the Laser Entrance Hole on the NIF (GLEH) [4], while Icarus sensors have been deployed to the Single Line-Of-Sight (SLOS) based diagnostics at the OMEGA facility and the NIF [6]. These novel diagnostics have yielded multi-frame image sequences with integration times down to 30 ps.

2. DAEDALUS ARCHITECTURE

The Daedalus sensor set out to improve on Icarus performance and aimed to achieve 1 nanosecond integration time with a larger full well of 1.5 million e^-. Daedalus maintains the same 25 µm spatial resolution as past sensors but is reduced to three frames-per-pixel to achieve the 1.5 million e^- full well requirement. Significant improvements to timing distribution and flexibility are also implemented. Daedalus is one-side abutable without bond pads on the top of the die. This enables two die to be abutted together to create a 51.2 mm x 12.8 mm array with a small dead space between the two active arrays.

Daedalus functions like past sensors. The sensor is programed with the desired shutter timing sequence and operational mode, the pixel array is initialized to a known state and waits for an asynchronous trigger from the experimental facility.

This trigger initiates an internal oscillator that clocks the pre-programmed digital shutter timing generator. Three unique, nanosecond scale shutter pulses are then propagated to the pixel array on a row-wise level and driven from each side of the array to the middle of the sensor, triggering the individual pixel rows. Image readout occurs after images have been captured on a much slower timescale of approximately 200 ms.

Table 1 is a list of Daedalus specifications, and Figure 1 is a block diagram of the sensor.

Table 1. Daedalus specifications

Design Goal	Daedalus
Spatial Resolution	25 µm
Array Size	1024 x 512
Detector Architecture	Common Cathode
Dynamic Range	66 dB (2000:1)
Full Well	1.5 million electrons
Noise Floor	750 electrons
Min Integration Time	1.0 ns
Min dead time between frames	1.0 ns
Number of frames	3 frames
Tiling option	1 side abutable
Max row timing skew	150 ps
Min row-to-row timing mismatch	150 ps
Min frame-to-frame gain and coupling	< 10%
Interlacing capability	Yes
Zero-Dead-Time mode	Yes
Independent Hemisphere Timing	Yes

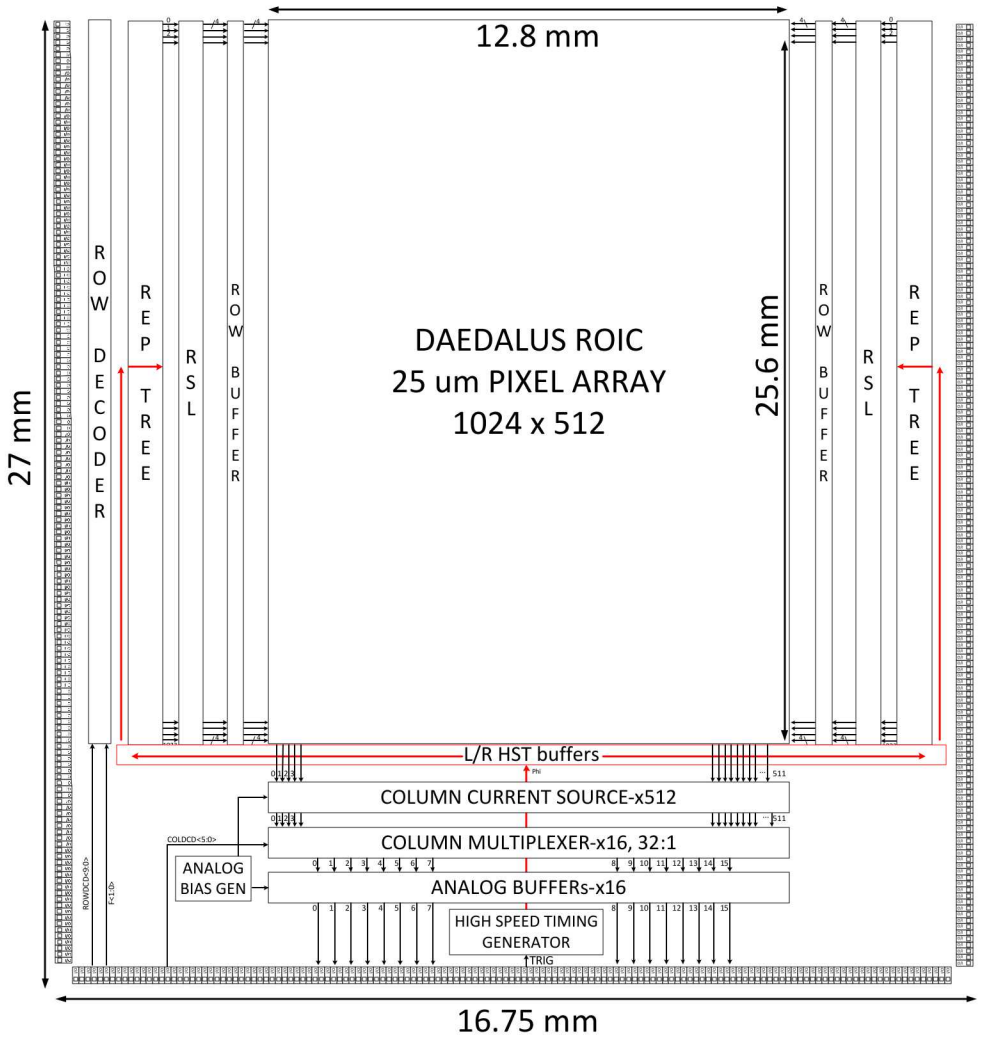

Figure 1. Daedalus block diagram.

Significant modifications were made to the high-speed timing generation architecture, the circuitry responsible for generating pre-shot initialization as well as configurable and fully independent shutters. Timing generation and propagation was constructed to distribute shutters serially to a row-wise block called the row shutter logic (RSL) where this serial shutter information is deserialized and buffered to drive pixel row shutter lines. Incorporating the RSL concept allows for multiple new timing modes. Effort was also applied to improve the performance of existing timing circuitry. Additional features include digitally programmable trigger delay, "infinite" row-wise interlacing, digital hemisphere tuning, high full well (HFW) mode and zero dead time (ZDT). Each of these functions will be described in the subsequent sections. Figure 2 is a linear flow comparing the past Icarus timing distribution to the current Daedalus timing distribution while Figure 3 demonstrates global timing distribution signal flow.

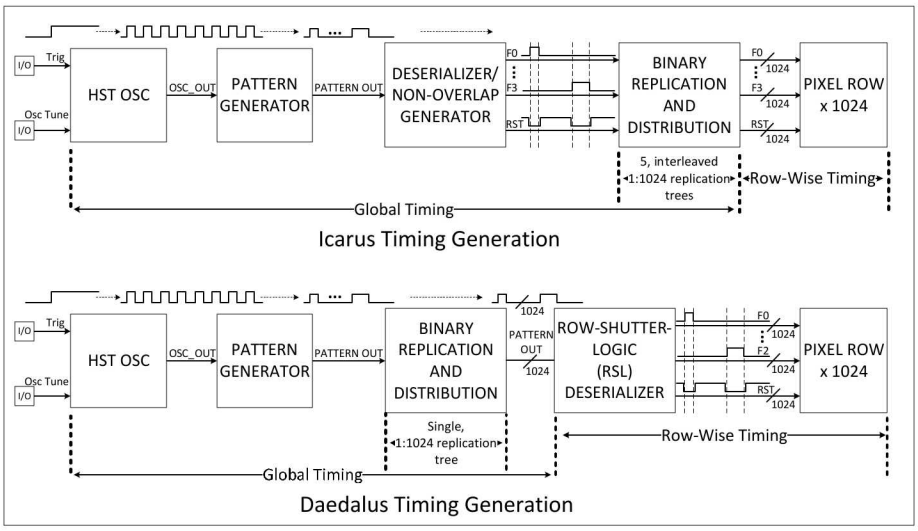

Figure 2. Linear signal flow comparing Icarus to Daedalus timing distribution.

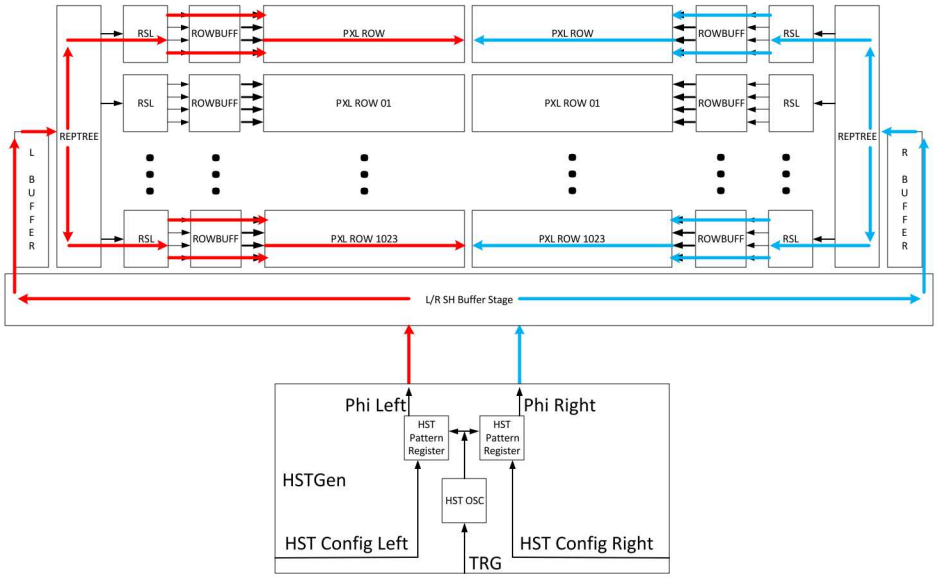

Figure 3. Block diagram showing global timing distribution architecture.

2.1 High Speed Timing Generator (HSTGen) Modifications

Past testing results have indicated that relaxation oscillators designed for previous sensors demonstrate better jitter performance and operate more closely to 50% duty cycle than equivalent performing ring oscillators [2]. Dual edge flip flops used in the digital pattern generator are an effective method to double clock speed, but 50% duty cycle operation is critical [3]. A 100 MHz relaxation oscillator was added to increase operational frequency range. In addition, startup characteristics of the relaxation oscillators were also improved. Digitally programmable delay cells were introduced to the external trigger path to allow easier synchronization with other ROICs. Left/Right hemisphere tuning [1] has been modified from an analog based current starved inverter tuning circuit to a digitally programmable delay.

2.1.1 Oscillator

Daedalus has three digitally selectable on-chip oscillators and an external clock input to clock the high-speed timing generator circuitry. There are two relaxation oscillators tuned to 500 MHz and 100 MHz operation and a seven-stage ring oscillator tuned to 500 MHz. One of the three oscillators are selected via a two-bit digital multiplexer with the external test clock input available as the fourth option. Figure 4 identifies frequency ranges available with the various oscillator options.

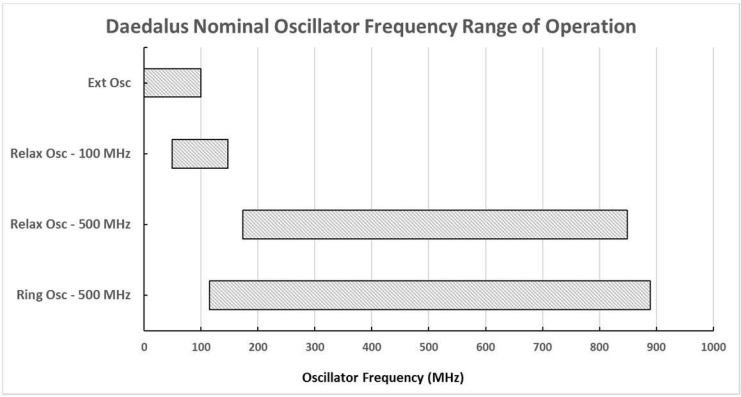

Figure 4. Plot of simulated oscillator frequency coverage.

2.1.3 Trigger Digital Delay Tuning Cell

The external asynchronous trigger that initiates image capture can now pass through a 40 bit, digitally programmable delay cell (Figure 5). The user can pre-program a specific number of delay elements to be inserted serially to the trigger signal. Each element is designed to provide a 145 ps nominal delay across a total tuning capacity of 5.8 nanoseconds. This block can be utilized to synchronize multiple ROICs, compensate for experimental facility timing error, or be bypassed completely to minimize insertion delay.

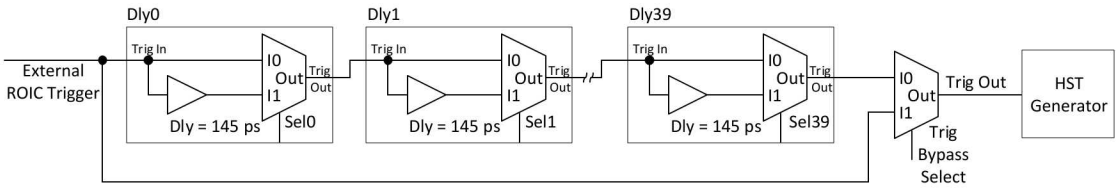

Figure 5. Trigger delay cell.

2.1.2 Shutter Pattern Generator/Deserializer

Independent shutter pattern generators for each hemisphere have been maintained as on Icarus. Register bit depth has been maintained at 40-bits. Each bit represents a single discrete unit of time associated with the oscillator frequency. Frequency doubling techniques using dual edge flip flops for the high-speed shutter pattern generator are implemented as in past designs [3]. The user pre-configures this pattern generator with a desired number of bits representing the shutter time and inter-frame time. One bit high and one bit low represents the fastest timing increment achievable. This timing pattern can be programmed to any combination of forty bits defining shutter integration time and interframe time. Fine tuning is accomplished by selecting a specific oscillator frequency (Figure 4) which dictates the discrete unit of time. Rather than deserializing the shutter pattern and passing through a non-overlap generator in this

block as in past ROICs, shutter information is maintained as a serial bit stream. This greatly simplifies distribution to the pixel rows.

2.1.4 Hemisphere Tuning Cell

Icarus utilized current starved analog delay cells to allow sub-nanosecond tuning between the left and right hemispheres to tune out hemispheric timing offsets that have been observed in past ROICs [1]. Analog delay cells were prone to noise injection on the bias lines affecting repeatability and potentially corrupting the shutter pulse width quality. Daedalus utilizes the same basic delay element as described in section 2.1.3 to provide ten stages of digitally programmed delay in 145 picosecond increments across a total tuning capacity of 2.9 nanoseconds. This yields a theoretical worst case tuned offset of 72.5 picoseconds between hemispheres. Digital programming also eliminates the need for the camera system to provide stable analog tuning references for this cell, thereby simplifying system design.

2.2 High Speed Timing Distribution

Maintaining shutter information as a serially encoded bit stream for global shutter distribution greatly simplifies design and physical implementation. As on past imagers, a binary replication tree distributes shutter information from the global generation point in the high-speed timing generator to 1024 individual pixel rows. However, only a single replication tree is required to replicate serial information while past imagers required ($N_{shutters}$ + 1) binary trees implemented in parallel, complicating design and limiting scalability in the number of frames. Each binary fanout stage output is shorted across all 1024 rows (Figure 6) to rebalance any timing errors introduced by each replication stage buffer. These errors manifest as row wise timing striations observed on past ROICs [1] and were reduced on Icarus with shorted output stages.

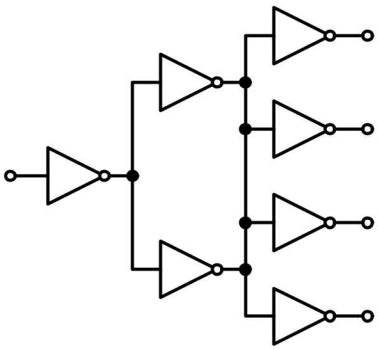

Figure 6. Binary replication tree with shorted output stages.

2.3 Row Shutter Logic

In its default mode, the (RSL) is clocked by HST Shutter Clock, output from the binary replication tree, to clock negative edge triggered D Flip Flops. This circuit deseriallizes the shutter clock information into individual shutters (SH0-SH2) and generates a non-overlapping complementary reset signal (RST) (Figure 7). RSL also provides shutter timing interlacing in a row wise manner as well as enabling additional timing modes: zero dead time (ZDT), and high full well (HFW).

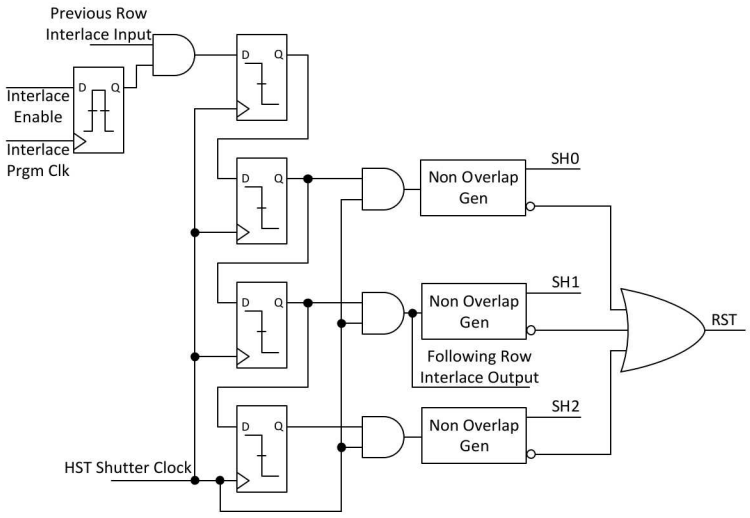

Figure 7. Row Shutter Logic (RSL) row-wise unit cell.

2.3.1 Interlacing

Interlacing allows the user to pre-program the sensor to be interlaced in N row banks, delivering 25 µm x (N x 25) µm spatial resolution and 3 x N frames (Figure 8). To implement interlacing, the user pre-programs each row interlacing register with an Interlace Enable bit using a slow speed Interlace Prgm Clk signal (Figure 7). This configures each row to hold off operation until the previous row has completed its shutter generation. The Following Row Interlace Output signal, derived by SH1 of the activated row will be passed to the subsequent row once the activated row has been triggered.

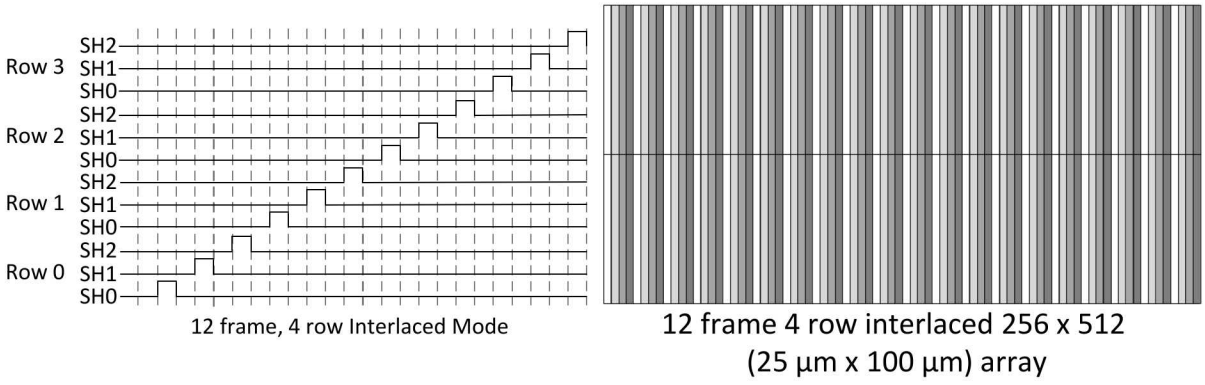

Figure 8. Row Shutter Logic (RSL).

2.3.2 Zero Dead Time (ZDT)

Zero dead time mode interlaces two rows spatially and offsets shutters temporally, allowing odd rows to be triggered during the reset of even rows. This function eliminates data loss during the inter-frame period while the pixel is being reset. Figure 9 is a representation of the 1024 rows and timing diagram describing this mode of operation.

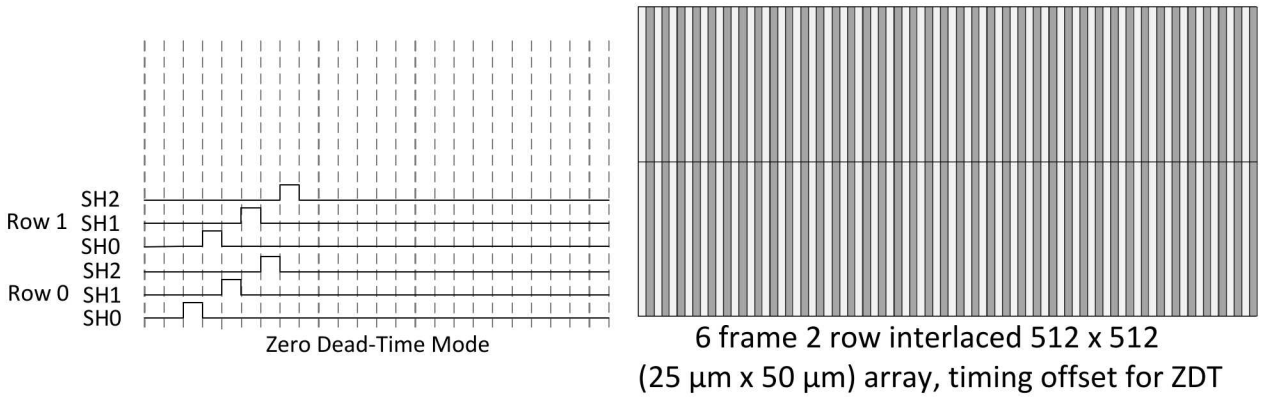

Figure 9. Zero Dead-Time (ZDT).

2.3.3 High Full Well (HFW)

High full well (HFW) mode triggers all shutter frames simultaneously. This mode exchanges additional frames of data for three times the storage capacitance of a single frame, theoretically allowing a single frame of data at up to 4.5 million e^- full well.

2.4 Multi-Frame Pixel

Architecturally, the Daedalus pixel (Figure 10) is identical to Icarus but has been reduced from four frames to three while the storage capacitor has been increased from 75 fF to 200 fF to accommodate the 1.5 million e^- full well requirement. Additionally, physical implementation has been optimized to reduce total shutter parasitic RC in each pixel while improving minimum shutter time to one nanosecond. The source follower transistor size was also increased to improve readout noise performance.

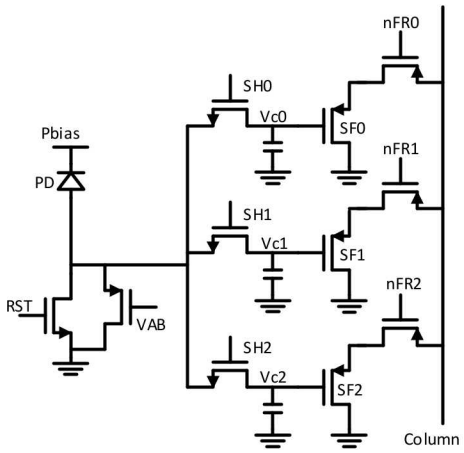

Figure 10. Daedalus unit pixel.

2.5 Analog Readout

Parallel analog readout has been maintained as on previous imagers. However, test data from the Icarus sensor demonstrated better than expected leakage performance [1] leading to the decision to reduce the number of parallel

readout channels from 32 to 16. On Daedalus, 512 pixel columns are multiplexed into 16 banks of 32:1 multiplexors (Figure 11). Additionally, a column-wise test input replicating a pixel source-follower has been incorporated to exercise all analog readout channels without requiring access the pixel array. Lastly, a bandgap voltage reference was included to provide stable analog biasing across temperature ranges as well as generate a current that is proportional to absolute temperature (I_{PTAT}) to provide on-chip temperature sensing. ROIC die temperature characterization will facilitate absolute calibration of the image sensor (Figure 12).

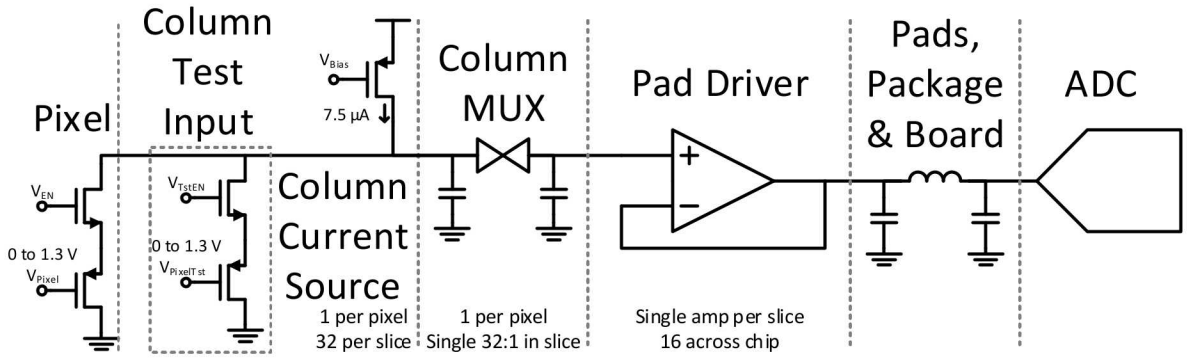

Figure 11. Analog readout chain with column test circuitry.

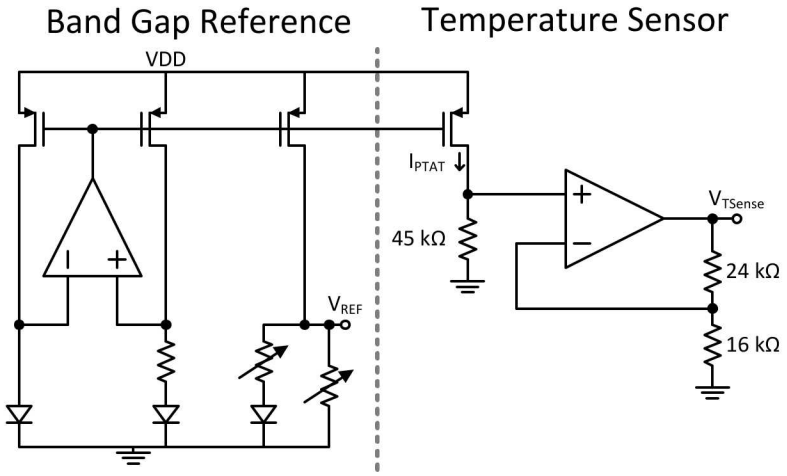

Figure 12. Bandgap reference and PTAT temperature sensor.

3. ROIC TEST RESULTS

Initial electrical testing and characterization has been conducted for the Daedalus un-hybridized ROIC. Full electrical functionality has been demonstrated and optical testing will be conducted as future work when a hybridized sensor is received. Below is a summary of electrical test and characterization of un-hybridized Daedalus ROICs.

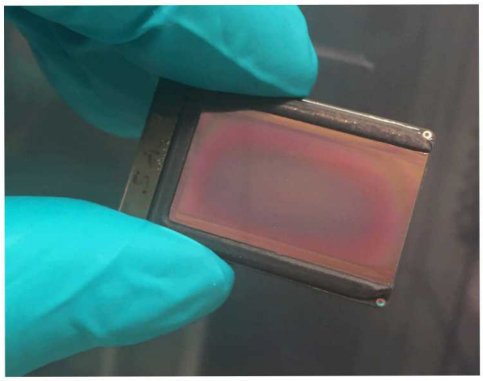

Figure 13. Image of un-hybridized, packaged Daedalus ROIC.

Table 2 is a comparison of insertion delay of Daedalus compared to past imagers.

Camera	Trigger-to-shutter latency	Timing propagation latency	Trigger-to-pixel latency
Furi	34 ns	48.13 ns	82.13 ns
Hippogriff	54 ns	26.6 ns	80.5 ns
Icarus	32 ns	4.7 ns	36.7 ns
Daedalus	**43.62 ns**	**7.66 ns**	**51.28 ns**

Table 2 is a summary of insertion delay for the successive generations of UXI cameras. Daedalus incurs additional propagation delay due to the digital hemisphere tuning delay circuitry. The dominant shutter generation delay is due to additional circuitry in the high-speed clock generation block. Shutter generation is disabled until the oscillator is operating in a stable, 50% duty cycle manner. This delay will scale with oscillator frequency.

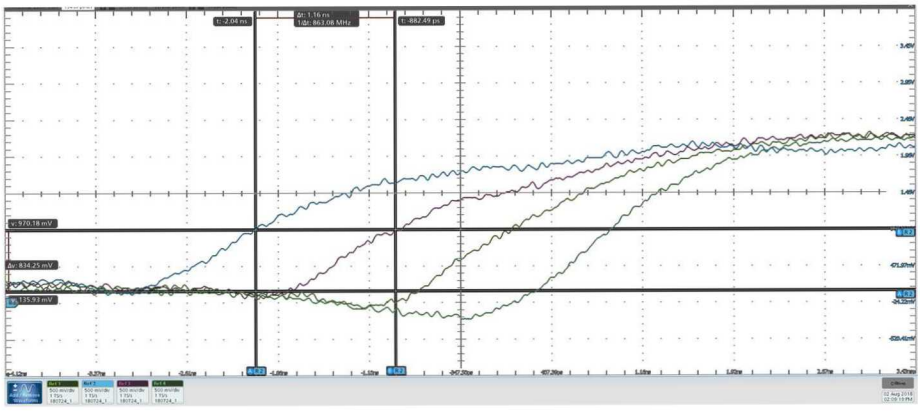

Figure 14. Oscilloscope screen capture of timing diagnostics showing shutter 0 pulse width, shutter 0 to shutter 1 interframe time, and shutter 1 pulse width with HSTGEN configured for 1 ns integration time. Shutter 0 was measured to be 1.16 ns shutter time with 0.95 ns interframe time between shutter 0 and 1 and 0.82 ns for shutter 1. Timing error from shutter-to-shutter may be due to routing mismatch on the system board. Optical testing will identify timing error with better fidelity than the electrical timing diagnostics used to obtain Figure 14.

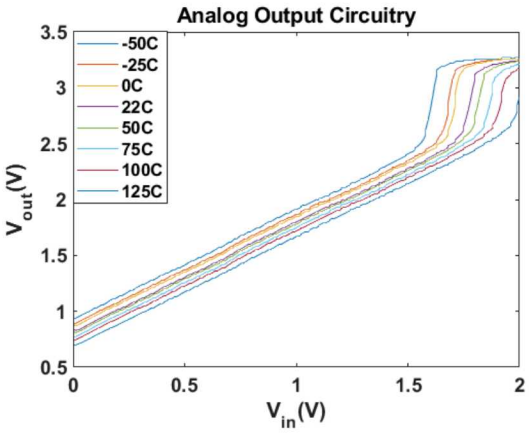

Figure 15. Analog output channel driven via column test circuitry demonstrating 1.4 V dynamic range across temperature for analog readout circuitry with analog gain of 0.975 at room temperature. Ultimately, sensor dynamic range is expected to be dominated by the shutter switch and will be determined under optical illumination.

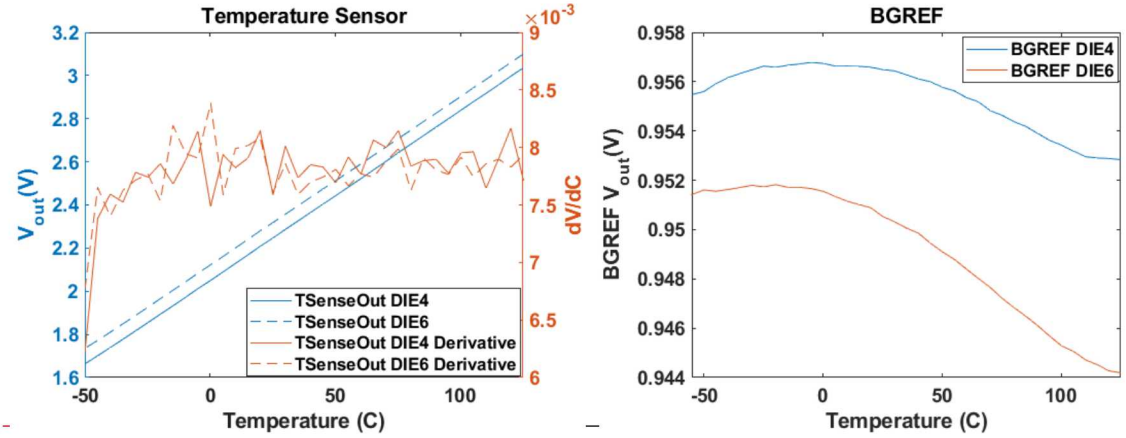

Figure 16. Temperature sensor output voltage (left) and bandgap voltage reference output (right) were measured across a temperature range of -55º C to 125º C for two separate die. Some die-to-die variation is present in the bandgap reference output as expected. The temperature sensor output circuitry has well matched gain from part-to-part, however part-to-part offsets are present so absolute temperature measurements will require calibration for each die.

Dark noise readouts were conducted. Figure 17 is comprised of data from 21 dark frame readout operations separated into each of the three separate frames. Standard deviation for each pixel was calculated across the 21 images. Figure 17 top are histograms of the standard deviations for all pixels in each frame, while the bottom of Figure 17 is a spatially resolved view of the standard deviations per pixel across the 21-image data set. Read noise per frame is 3.0, 2.2 and 2.2 LSBs for Frame 0, 1 and 2 respectively. However, one can observe outliers that manifest as horizontal, row wise striations in frame 0. These striations are tied to row-wise shutter lines, but the root cause of this error requires further investigation. Read noise of 2.2, 76 µV LSBs corresponds to 167 µV or 209 e^- rms noise floor.

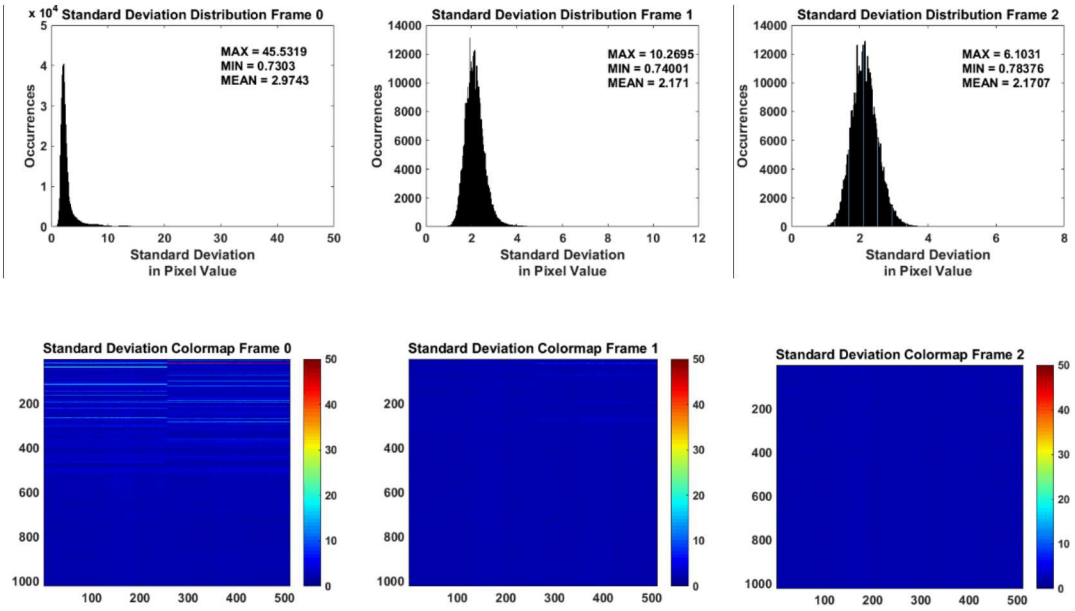

Figure 17. Dark frame read noise histograms and 2D maps for all three image frames.

4. CONCLUSION

A 1024 x 512 pixel, 25 μm spatial resolution, three frame-per-pixel imager has been built and electrically tested. Electrical testing indicates better than one nanosecond shutter times are achievable and readout circuitry can support 1.5 million e^- full well operation. On chip temperature sensing will allow for calibrating out timing generation and distribution error while dark noise has been reduced to 210 electrons. Optical testing will be initiated upon receipt of a hybridized sensor. The Daedalus image sensor represents a new capability demonstrating significant timing flexibility to improve existing diagnostics and drive future HEDP diagnostic development.

REFERENCES

[1] Claus, L., et. al., "Design and characterization of an improved, 2 ns, multi-frame imager for the Ultra-Fast X-ray Imager (UXI) program at Sandia National Laboratories," Proc. SPIE **10390**, 103900A (2017).

[2] Hurd, E., et al., "Performance characterization of a four-frame nanosecond gated hybrid CMOS image sensor," Proc. SPIE **10763**, 10763-20 (2018).

[3] Claus, L., et. al., "An overview of the Ultra-Fast X-ray Imager (UXI) program at Sandia Labs," Proc. SPIE **9591**, 95910 (2015).

[4] Chen, H., et. al., "A high-speed two-frame, 1-2 ns gated X-ray CMOS imager used as a hohlraum diagnostic on the National Ignition Facility," Rev. Sci. Instrum., 87, 11E203 (2016).

[5] Claus, L., et. al., "Initial characterization results of a 1024x448, 25-μm multi-frame camera with 2ns integration time for the Ultrafast X-ray Imager (UXI) program at Sandia National Laboratories," Proc. SPIE **9966**, 99660F (2016).

[6] Theobald, W., et. al., "The Single Line-of-Sight Time-Resolved X-ray Imager diagnostic on OMEGA," Rev. Sci. Instrum., (Accepted June, 2018).