Active Gate Current Control for Non-Insulating-Gate WBG Devices

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Abstract — This paper proposes an Active Gate Current Control (AGCC) strategy for non-insulating gate WBG devices, for example, gallium nitride gate-injection-transistor (GaN-GIT) and silicon carbide super junction transistor (SiC-SJT). It provides a tool for power converter designers to further improve the converter efficiency and to extend the life time of those higher cost power transistors. By continuously adjusting the device gate current, the proposed AGCC strategy can control the device switching speed, switching loss, conduction loss and gate loss together to achieve operation goals, including lower semiconductor loss, lower thermal stress, lower EMI spectrum, or smaller voltage overshoot across the full range.

Keywords — GaN GIT; SiC SJT; intelligent gate drive; dv/dt.

I. INTRODUCTION

New types of non-insulating gate (as known as current driven) WBG devices have demonstrated the normally off operation with low on-state resistance and high drain current. At least two types of them show superior device performance and became commercially available, including the GaN GIT from Panasonic [1], [2] and SiC SJT from GeneSiC [3], [4]. Compared to insulation gate (voltage driven) devices, current driven WBG devices have good EMI noise immunity and excellent electrical performance [5]-[8]. However, the gate drive design method is different from traditional voltage source power transistors. Additional gate drive power consumption may need to be considered in the gate drive design stage. A previous not considered tradeoff between the gate drive loss and device switching/conduction loss may exists in many power converter applications[9]-[13].

GaN GIT is a lateral structure 600 V power transistor. The device schematic of the latest hybrid-drain-embedded GIT (HD-GIT) is shown in Fig. 1. The recessed p-type gate of the GIT lifts the gate-to-source potential leading to the normally-off operation, at the same time, another p-GaN region is electrically connected to the drain electrode by the interconnection metal layer. While the device is on, continuous hole injection from the gate is required to produce electrons and increase the drain current. The gate current (I_{gs}) rating is up to 50 mA for a 26 A/600 V rated discrete GaN chip.

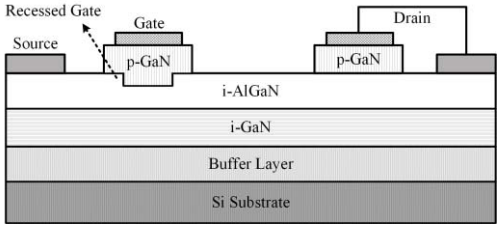


Fig. 1 Schemetic cross section of hybrid-drain-embeded GaN-GIT (adapted from [14]).

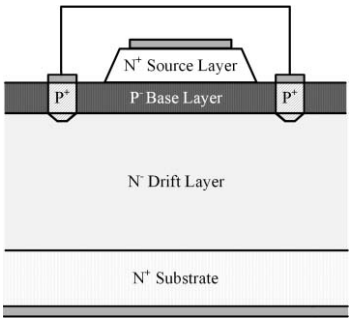


Fig. 2 Schemetic cross section of SiC -SJT(adapted from [4]).

SiC SJT is a vertical normally-off "Super-High" current gain SiC BJT. The typical structure of this transistor is shown in Fig. 2. Both GaN GIT and SiC SJT have similar driving principle, their on-state main channel conductivity is decided by the continuous I_{gs} amplitude. For a 160 A/1700 V rated single SIC-SJT, the rated maximum continuous I_{gs} is 7 A, which results close to 25 W gate drive loss. This means the device switching speed, switching loss, conduction loss and gate loss are linked to each other by the device gate current, and a proper gate current control strategy needs to be identified to optimize the transistor operation.

In past years, numerous intelligent gate drive circuits have been proposed for voltage source semiconductors to achieve switching transient/trajectory control. Circuit efficiency [15]-[17], device junction temperature[15], device voltage stress [18]-[20] and circuit conductive EMI [15], [18], [21] are the typical high-level control targets. To fulfill these targets, device dv/dt, di/dt and switching loss are always use as the direct control objects. Three classes of the trajectory control methods are summarized in Fig. 3, including basic open loop control [22]-[23], close loop

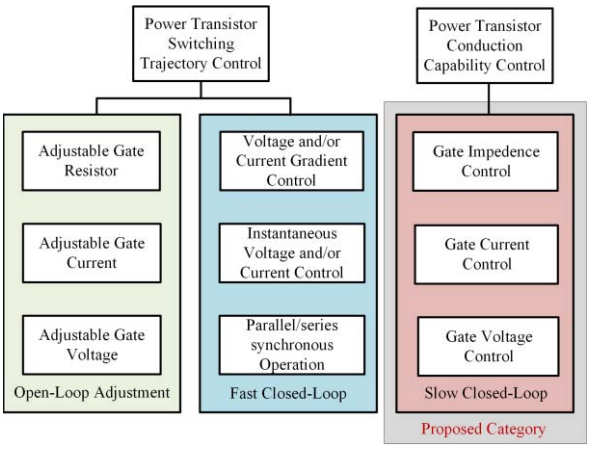


Fig. 3 Implementation methods and classification of power transistor gate drive control.

control [25]-[31], and synchronized feedback control [32]. However, very few gate drive circuits are designed for non-insulating gate devices. The device conduction capability and gate drive loss have never been considered as the control target.

In view of unique features of the current driven devices and existing intelligent gate drive technologies, a new gate current control strategy and circuits implementation is proposed in the paper. The gate drive circuits can control the device switching loss/speed, conduction loss, and gate loss separately by varying the gate driver pulse current and constant current. In this paper, section II reveals the influence of gate current on different control targets for GaN GIT and SiC SJT. Section III describes the proposed gate current control strategy and the hardware implementation. And section IV shows the experimental results to verify the concept.

II. Influence of Gate Current on Device Operation

For current driven WBG devices, gate current amplitude plays a key role in the device operation. In general, device switching on transient requires a large pulse gate current to charge up the gate-to-source (C_{gs}) capacitance. After that, continuous gate current (I_{gs}) needs to be provided to the device to remain the high conductivity of their main channel until another large current pulse to discharge the device C_{gs} and turn-off the device. To explain this three stages operation, this section will start from explaining the current driven device gate drive circuit, then analyze the device operation in each stage.

A. Non-Insulating-Gate Device Drive Circuit

Varies gate drive circuits have been proposed for current driven WBG devices, including RC-type circuit[7],[33]-[35], capacitor-less gate drive circuit [36] and multiple voltage level gate drive circuit [37], [38]. Among all of them, the RC-type circuit is the simplest circuit which can achieve reliable and efficient current drive. Typical MOSEFT/IGBT drive IC can be used

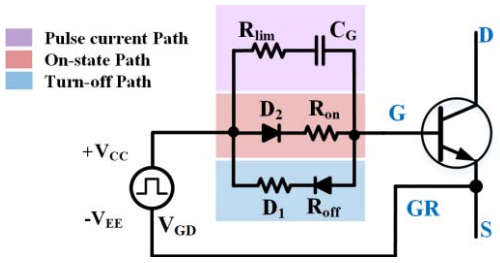


Fig. 4 RC-type gate drive schemetic for non-insulating gate device.

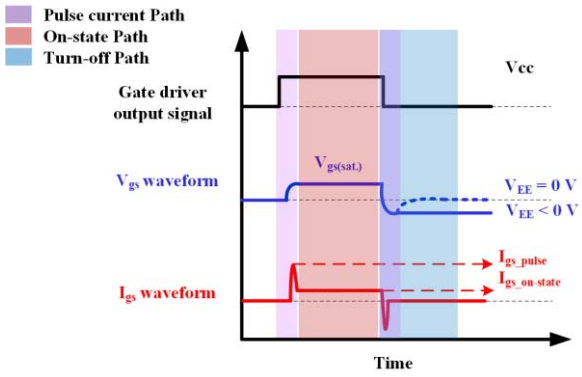


Fig. 5 Timing and stages of RC-type gate drive waveforms.

directly with several passive components, at the same time, it provides a negative turn-off voltage automatically, which is desired by high dv/dt and low threshold WBG devices. Therefor a RC-type circuit is used to explain the driving principle of current driven devices.

Fig. 4 shows the complete RC-type gate drive schematic. Fig. 5 shows the gate drive waveforms. The gate drive circuit has three separated impedance paths after the totem-pole driver. The 1st path provides the pulse current during device turn-on and turn-off transient to accelerate the device switching. The amount of charge provided by the C_G should match the device gate charge $Q_{g,\,which}$ can be formulated by equation 1.

$$C_G = \frac{Q_g}{V_{CC} - V_{gs(sat.)} + V_{EE}} \tag{1}$$

where $V_{gs(sat.)}$ is the device on-state saturation voltage, it is dependent on the device gate-to-source current I_{gs} and the drain current I_d. To simplify the calculation, this voltage can be set as 3.5 V for both GaN GIT and SiC SJT. A current limiting resistor R_{lim} is in series with the C_G to limits the maximum gate current during device switching transient. The calculation of R_{lim} can be formulated by equation 2.

$$R_{\lim} = \frac{V_{CC(\max.)} - V_{plateau}}{\left| I_{gs-pulse(\max.)} \right|} \tag{2}$$

The 2nd gate drive path provides the continuous on-state gate current. The value of R_{on} can be calculated from equation 3.

$$R_{on} = \frac{V_{CC} - V_{gs(\text{sat.})} - V_{f(\text{D2})@Igs}}{I_{gs-on-state}} - R_{g(\text{int.})} \quad (3)$$

where $R_{g(int.)}$ is the summation of power transistor internal gate resistance, the gate driver pull-up resistance and the gate driver upper switch on-state resistance. $V_{f(D2)}$ is the forward voltage drop of diode D_2 at rated I_{gs}. The value of I_{gs} is decided by the device characteristics and designed operation conditions, the method to set this value is discussed in section II-C.

The 3rd path provides the low impedance and negative voltage bias for the turn-off current, and with 1st path together to prevent possible device cross talk [39]. This path is optional if the required R_{off} is smaller than the R_{on}, and the diode D1 can be always removed to simplify the design. In practical cases, the value of R_{off} is around 1-2 Ω.

B. Device Switching Loss and Dv/dt

The switching loss of non-insulation gate WBG devices has no significant difference from insulation gate WBG devices. According to our previous work, the switching speed and loss trend of 600 V GaN-GIT is similar to 600 V cascode GaN HEMT [5] and the 1.7 kV SiC SJT is similar to 1.7 kV SiC MOSFET [7]. When device operation conditions are the same, gate pulse current amplitude dominate the device switching speed and loss. According to Eq. 2, adjusting V_{CC} is an effective way to control the device gate pulse current amplitude. The relationship between gate pulse current amplitude and the example GaN-GIT device switching performance (in half-bridge configuration) is shown in Fig. 6(a) and Fig. 6(b). Similar phenomenon can be observed on SiC-SJT as well.

Adjusting C_G to change the device switching speed is not recommended and difficult for implement. If the C_G is smaller than Q_g, the switching process will be stopped in the middle and the remaining gate current amplitude will be limited by the 2nd path R_{on} If C_G is larger than Q_g, the peak I_g is still the same and additional gate charge loss will happen. Adjusting R_{lim} is possible by paralleling additional resistor, however, it is still requiring significant effort for the implementation.

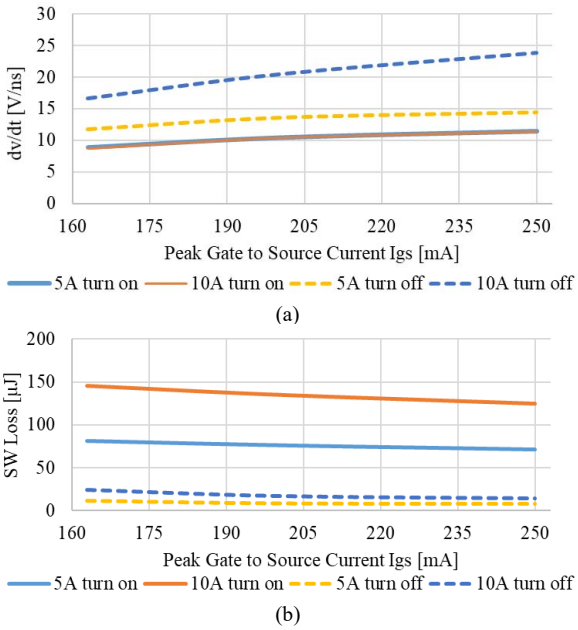


Fig. 6 GaN-GIT peak I_{gs} vs. (a) dv/dt and (b) switching energy.

C. Device Main Channel and Gate Channel Loss

The main channel conductivity of non-insulating devices is related to the device I_{gs} and junction temperature. For GaN-GIT, while the device is on, more holes injected from the gate leads to lower main channel on-state resistance. At 25 °C, increasing I_{gs} from 1 mA to 10 mA leads to 8% $R_{ds(on)}$ reduction. At 150 °C, these leads to 10% $R_{ds(on)}$ reduction. The resulting gate drive loss can be calculated by using equation 4.

$$P_{gate-loss} = (V_{CC} + V_{EE}) \times Q_g \times f_{sw} + V_{CC} \times I_{gs} \times D \quad (4)$$

where D is the equivalent device on-state duration and f_{sw} is the device switching frequency. Combine with Eq. 3, it concludes that higher V_{CC} leads to higher gate drive switching loss and device gate conduction loss. At the same time, amplitude of I_{gs} has a lower limitation. If the I_{gs} is too small to support the main channel conductivity, the device will run into saturation region immediately. For example, the minimum ratio between I_d and I_{gs} in SiC-SJT is defined as dc current gain (h_{EF}) [4]. In device datasheet [40], this h_{FE} is defined by equation 5.

$$h_{FE} = \frac{I_d}{I_{gs-on-state}@(V_{ds} = 8V)} \quad (5)$$

where the measured value of h_{EF} is 89 at 25 °C, which means 1 A I_{gs} can barely support 89 A drain current, but the V_{ds} is already 8 V. If the V_{ds} remains below 1.1 V, the required I_{gs} to support same I_{ds} (89 A) is around 1.7 A,

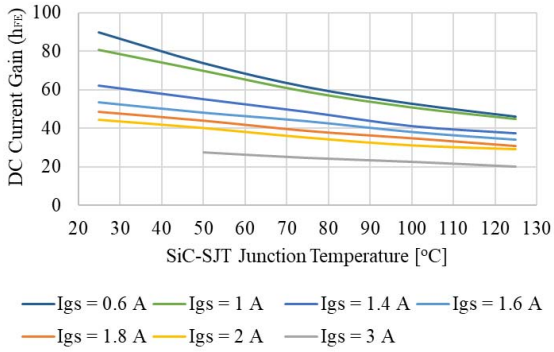


Fig. 7 SiC-SJT dc current gain h_{EF} vs. I_{gs}.

which means the h_{EF} drops to 52 with the new definition (V_{ds} = 1.1 V). At the same time, when device junction temperature increase, device h_{EF} also drops significantly, as shown in Fig. 7.

Another 20 to 30% decrease is expected when device junction temperature increased from 25ºC to 125 ºC. To maintaining the same V_{ds} drop, 1.7 A I_{gs} can only supports 63 A I_d when T_J is 125 ºC. Once the load current exceeds this value, device will quickly run into saturation and tripped the circuit de-sat protection.

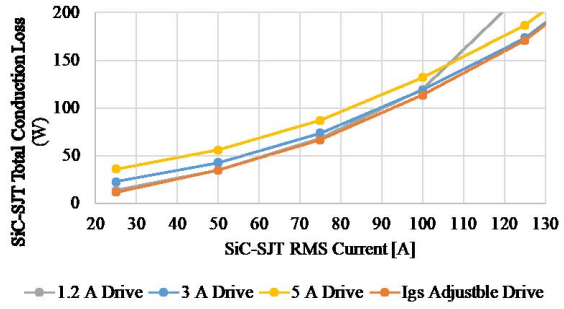
Beside the safe operation region consideration, the gate loss needs to be considered for current driven devices, especially when the circuit is operated in the light load condition. The loss function of the non-insulating-gate device can be formulated as equation 6.

$$P_{total-loss} = P_{gs-sw.} + P_{gs-con.} + P_{ds-sw.} + P_{ds-con.} \quad (6)$$

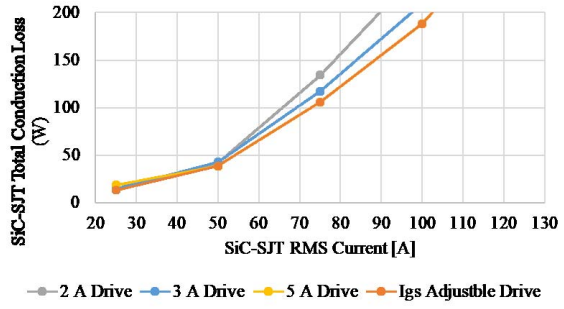
Since the switching loss ($P_{ds\text{-}sw.}$) of device is only controlled by pulse gate current. By substituting Eq. 4 and Eq. 5 into Eq. 6, the on-state I_{gs} related loss can be formulated by Equation 7.

$$P_{gs-con.} + P_{ds-con.} = ((V_{cc(@Igs)}) \times I_{gs\_on-state} + V_{ds(@Igs,Ids)}) \times D \quad (7)$$

where both V_{CC} and V_{ds} depend on the provided instantaneous gate current, load current, and device temperature. Using device manufacture data, a group of theoretical curves for SiC-SJT [40] total conduction losses (both $P_{gs\text{-}con.}$ and $P_{ds\text{-}con.}$) with different driving strategies are shown in Fig. 8(a) and (b). It can be concluded that accurately controlling the device gate current at different load current conditions and device temperatures will not only ensure the safe operation of non-insulating-gate power transistor but also save significant amount of power loss from both gate driver and device itself. The similar phenomenon has been observed on the GaN-GIT as well.



(a)



(b)

Fig. 8 SiC-SJT gate and main channel total conduction loss under different driving current(a) at 25 ºC and (b) at 150 ºC.

However, the equivalent dc current gain of GaN-GIT is much larger, which is close to 3,000 to 4,000. The high current gain means the saving on single device gate drive conduction loss is insignificant (milli-watt level), so providing fixed on-state gate current is more practical.

III. Control Strategy and Hardware Implementation

In general, the AGCC strategy is controlling the gate drive output voltage based on feedback information, then, device gate current can be indirectly controlled during the switching transient or on-state. As discussed in section II-C, for GaN-GIT, the AGCC method is mainly actively adjusting the device pulse gate current to control the device switching speed and switching loss. For SiC-SJT, the control target is device gate-to-source and drain-to-source total conduction loss.

Instead of choosing complex analog circuit to achieve high bandwidth control, digital control offers more flexibility and can significantly reduce the circuit complexity. However, it will be only suitable for micro-second level control. In this paper, two AGCC control is realized by designing gate drive hardware with digital control. Fig. 9. Shows the proposed control diagram for a single non-insulating-gate power transistor. The AGCC part includes the sensing circuit, a microcontroller (MCU) with pre-defined look-up table and one adjustable dc/dc. The adjustable dc/dc is used to control the gate drive power

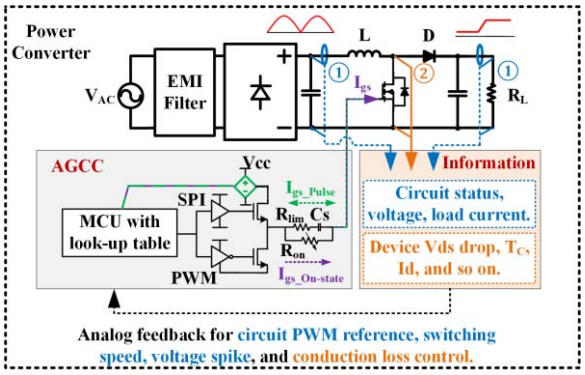


Fig. 9. The proposed AGCC Diagram in an example circuit (PFC).

supply voltage V_{CC}. Its output voltage is controlled by a digital voltage ladder and responds to the sensed information. For example, to adjust the circuit EMI and the device voltage overshoot, the converter load currant and, dc-bus voltage needs to be collected. Or, to minimize the device conduction loss, the load current information, device temperature or device V_{ds} drop needs to be measured.

The digital resistors to control the adjustable dc/dc are the only additional hardware circuitry required by the proposed AGCC gate drive. Generally, adjustable dc/dc converter requires a reference voltage created by the voltage ladder. By replacing one of the chip resistors to a digital resistor, the voltage reference created by the voltage

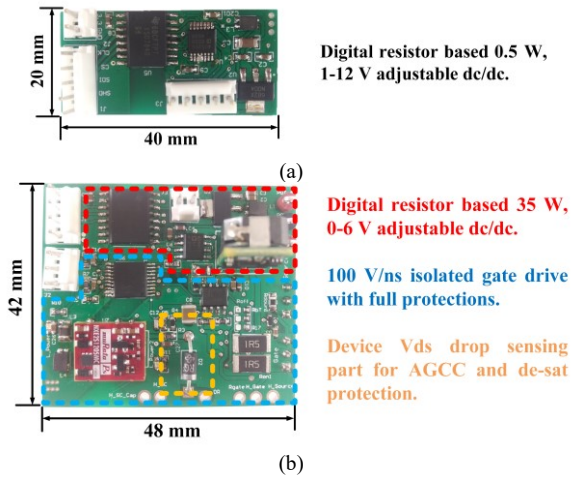


Fig. 10. The proposed AGCC (a) design I for GaN GIT switching speed control and (b) design II for SiC-SJT conduction loss control.

ladder can be adjusted through MCU SPI communication. The data loading rate of a typical digital resistor is 10 MHz.

To verify the proposed AGCC gate drive concept, two prototypes has been designed, built and tested with non-insulating-gate power transistors, their prototypes are shown in Fig. 10 (a) and (b). The design I is for GaN-GIT, the AGCC board is used to control the device switching speed. The maximum driving capability of the circuit is 0.6 W and 50 mA continuous current, which is sufficient for a typical GaN-GIT based MHz converter. The size of this board is 8 cm^2. The design II is for SiC-SJT, device on-state V_{ds} drop is used as the feedback signal to control the gate drive continuous gate current for loss reduction purpose. The maximum driving capability of the circuit is 36 W and 6 A continuous current, which is sufficient for a single 1.7 kV, 160 A rated SiC-SJT module. The V_{ds} drop detection circuit is combined with the device de-sat protection circuit, no additional sensing circuit is required. The size of the design II board is 20 cm^2, the larger size is due to feedback control and device higher gate current rating.

IV. Experiential Results

Two half-bridge test boards with the proposed active gate drive circuits are tested together to verify the proposed control targets. For GaN-GIT, the test is focusing on switching speed and switching loss control. Open loop control is used to pre-set the switching speed according to the controlled commend. For SiC-SJT, the test is focusing on total conduction loss control. TI 28027 is used as the controller to adjust the gate current according to device operation status.

A. Switching Speed and Switching Loss

By varying the adjustable dc/dc converter output V_{CC}, both turn-on and turn-off speed of the GaN-GIT can be controlled. The turn-on gate transient current ($I_{gs\text{-}pulse\text{-}on}$) and turn-off gate transient current ($I_{gs\text{-}pulse\text{-}off}$) has different amplitude when V_{EE} is not zero. Their values can be calculated by using equation. 8 and 9.

$$I_{gs-pulse-on} = \left| \frac{V_{CC(\max.)} - V_{plateau}}{R_{\lim}} \right| \tag{8}$$

$$I_{gs-pulse-off} = \left| \frac{V_{CC(\max.)} - V_{plateau} + V_{EE}}{R_{\lim}} \right| \tag{9}$$

where $V_{plateau}$ is 2.2 V for GaN-GIT and R_{lim} is 33 Ω in the tested gate drive. The GaN-GIT half-bridge test board is shown in Fig. 11, a 600 V/6 A Schottky diode is used as

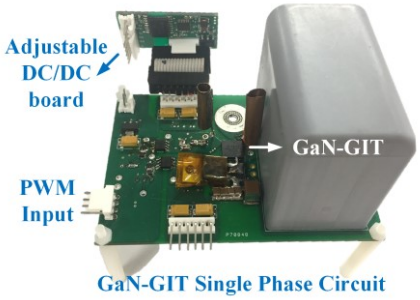


Fig. 11. GaN GIT single phase circuit with AGCC board I attached.

the upper switch. V_{CC} values are preset to be 5.5 V, 8.8 V and 12 V to drive the GaN-GIT with 100 mA, 200 mA and 300 mA pulse gate current, the V_{EE} is zero. The tested device load current is 5 A, the dv/dt and di/dt are plotted in Fig. 12 and Fig. 13, respectively. Device turn-on di/dt range is 1.3-4 A/ns, the average dv/dt range is 9-33 V/ns, the V_{CC} was adjusted from 5.5 V to 12 V. For turn-off

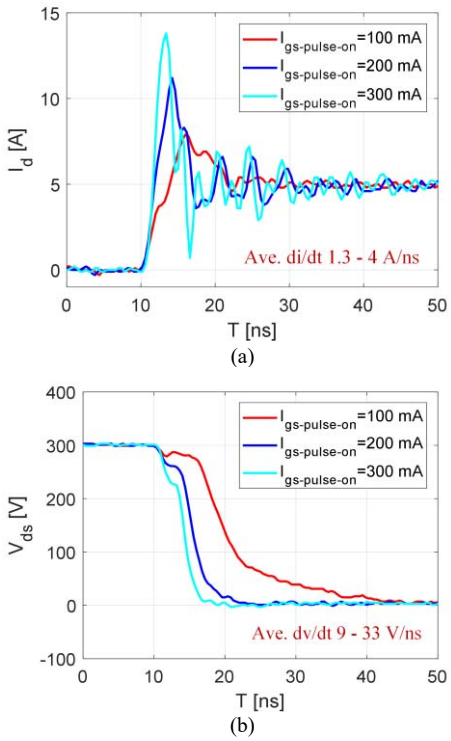
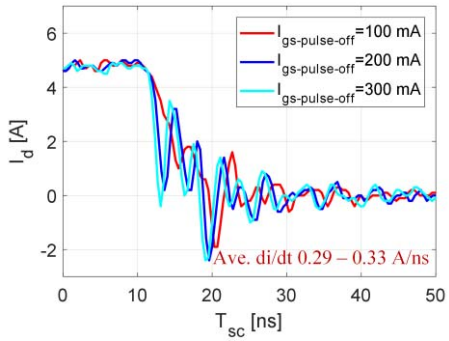
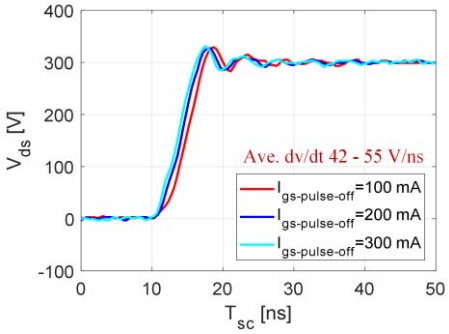


Fig. 12. The achieved GaN-GIT turn-on speed (a) Vds and (b) Id.



(a)



(b)

Fig. 13. The achieved GaN-GIT turn-off speed (a) Vds and (b) Id.

transient, the adjustable range of di/dt and dv/dt is much smaller. The average turn-on di/dt range is 0.29-0.33 A/ns, the average dv/dt range is 40-55 V/ns. Device drain-to-source voltage overshoot has negligible increase, which is due to the ultra-small stray inductance inside the device current commutation loop. Even though the controllable range of the turn-off speed is narrower than the turn-on, the turn-off loss difference can be amplified when circuit operated with higher frequency. To demonstrate the AGCC influence on the device loss, the GaN-GIT was operated in a critical conduction mode (CrM) boost converter circuit with different gate pulse current amplitudes. Device turn-on loss is negligible due to the circuit CrM operation. The only difference of device loss is caused by GaN-GIT turn-off speed. The tested circuit switching frequency is 540 kHz and the output power is 275 W. The thermal images of the boost converter are shown in Fig. 14. A 6.7 °C

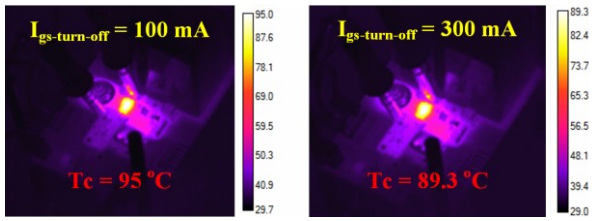


Fig. 14. GaN-GIT case temperature controlled by designed AGCC in CrM boot converter.

difference of device case temperature can be observed. Therefore, the proposed switching speed and switching loss control capability of the AGCC are verified.

B. Main Channel and Gate Conduction Loss

The conduction loss reduction with feedback control is designed in the AGCC board for SiC-SJT. The test circuit with AGCC board attached is shown in Fig. 15. To demonstrate the conduction loss control capability of the

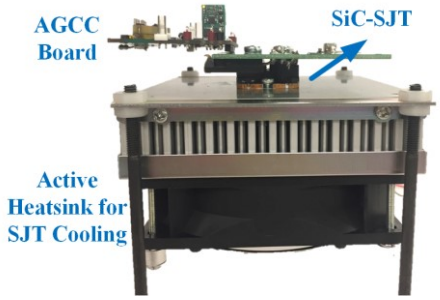


Fig. 15. SiC-SJT circuit with AGCC board II attached.

AGCC method, the SiC-SJT module is always conducting a 120 Hz AC load current after a diode bridge, and the device never turns off to avoid the influence of switching loss. Without the AGCC function enabled, the gate drive circuit is requested to supply constant drive voltage all the time, and the resulting device waveforms are shown in Fig.

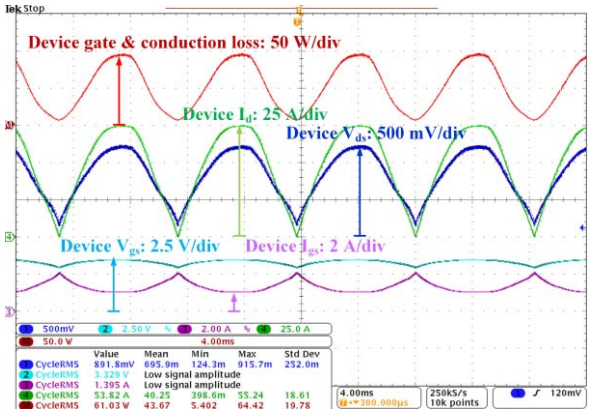


Fig. 16. SiC-SJT performance with traditional constant voltage gate drive.

16. The total loss occurs in the device is shown on the figure top (red curve), the cycle rms value of it is 61.03 W, and the device load current conduction loss dominates it. SiC-SJT V_{gs} is influenced by the load current, which causing a voltage ripple without any phase shift. Since the gate drive provides constant voltage, the resulting I_{gs} ripple is reversed from the V_{gs}, which can be calculated by equation 10.

$$I_{gs-on-state} = \frac{V_{CC} - V_{gs}}{R_{on}} \tag{10}$$

The resulting I_{gs} has the highest value (2.14 A) when device load current is low (0 A) and has the lowest (1 A) value when device load current is high (75 A). If the relationship between device $R_{ds(on)}$ and I_{gs} is considered, the resulting high device conduction loss is not desired.

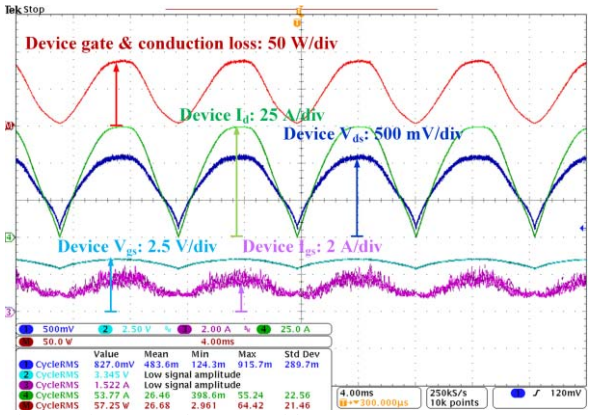


Fig. 17. SiC-SJT performance with AGCC.

After enabling the AGCC function, the gate drive current is changing with the sensed device voltage drop, which is reflecting the device load current and junction temperature at the same time. The test waveform is shown in Fig. 17. Same amount of load current is flowing into the device compared to previous test, but the resulting I_{gs} is in-phase with the device load current instead of 180° shifted. By enabling the AGCC function, SiC-SJT device loss is reduced to 57.25 W (6.5%) and almost same amount of gate drive current was used. The I_{gs} has highest value (2.6 A) when device load current is high (75 A) and has lowest (0.7 A) value when device load current is low (0 A). The function of AGCC is to redistribute the same amount of gate drive current based on the device load current to create a positive feedback on the device conductivity. The benefit of the AGCC drive method can be even larger when device load current is higher or device junction temperature is higher.

V Conclusion

The proposed active gate current control method provides a unique tool for non-insulating power transistor users. By controling the device gate current during switching transient or when the device is on, the switching loss, the conduction loss, and the gate drive loss can be controlled separately. This introduces new control freedoms to non-insulating power transistor users to control their power electronics circuit loss, EMI, voltage spike, and thermal profile without influence primary functions of the converter.

At the same time, this work is using the latest WBG devices as examples to demonstrate the proposed AGCC method. This gate drive method shows interesting benefits when applied to both the high frequency GaN converter and the high power SiC circuit.

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