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Diagnosis of factors impacting yield in multilayer devices for superconducting electronics

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Increasing SCE circuit complexity necessitates adaptation of failure analysis techniques developed for CMOS

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- The ability to diagnose failure mechanisms for complex SCE circuits is critical for future scaling
- Circuit failures can occur due to issues in design and/or fabrication
- Locating isolated defects in complex SCE circuits during operation at 4K is not yet possible
- Can techniques developed to find defects in complex CMOS circuits locate isolated defects in SCE circuits biased at ambient temperature?

This talk: explore Thermally-Induced Voltage Alteration (TIVA) analysis of HYPRES-designed circuits fabricated at MIT-LL

Thermally induced voltage alteration (TIVA) localizes defects on CMOS wafers sensitive to heat

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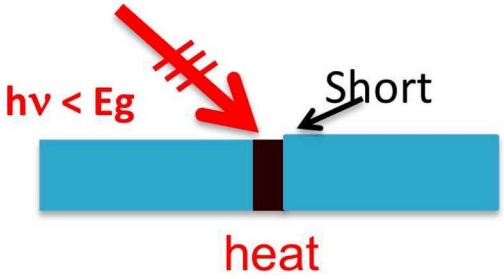
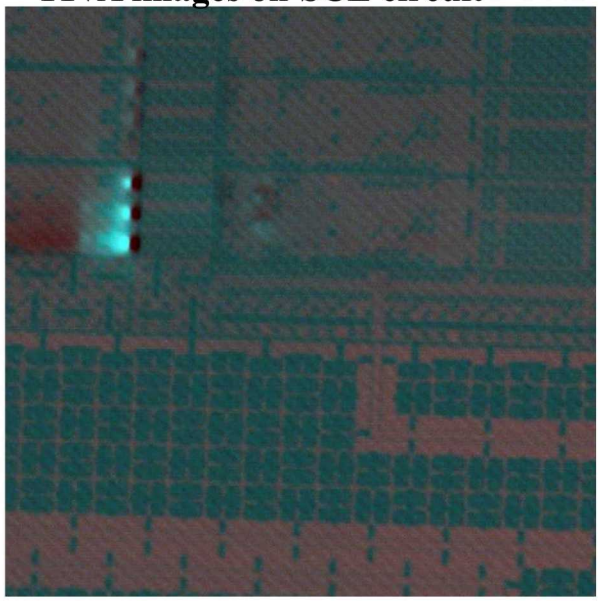
Scanning Laser Microscope

Checkpoint InfraScan 300TDE



Initial work on known defective SCE circuits: Overlay of reflected light and TIVA images on SCE circuit



Scan laser across wafer to induce heat, activate defect, generates EMF
Pulsed stimulus, lock-in detection eliminates spreading, 0.5 µm resolution
TIVA has been used to find shorts due to particles, design flaws, and resistive connections in CMOS circuits

Proof of concept: TIVA analysis of RF/decoder circuit with known fab issues– did not pass MIT-LL in house resistance tests

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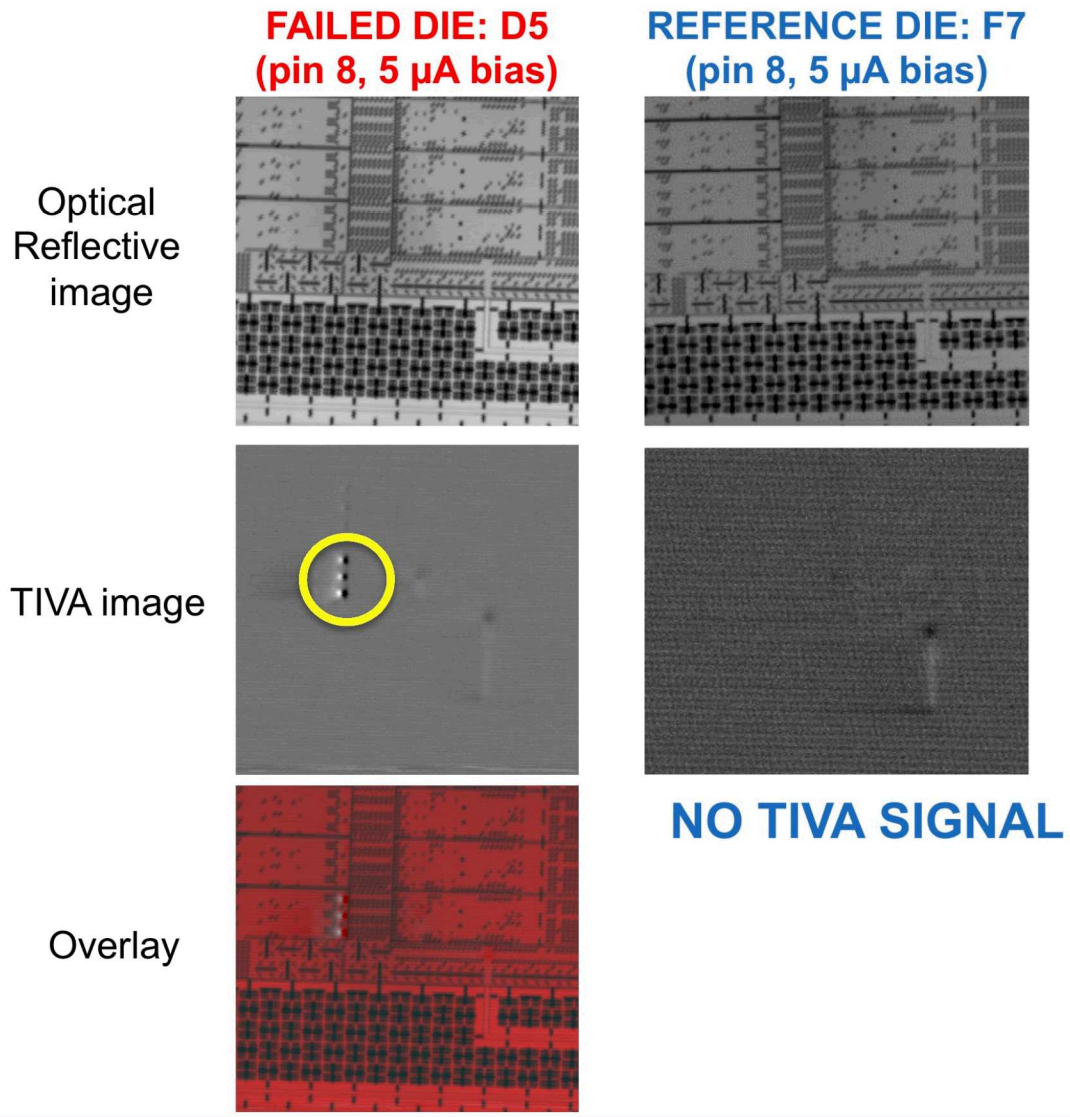

- Apply dc current bias to individual circuit bias points
- Measure change in voltage as laser scans across surface
- Correlate location of voltage change with reflected light image
- Use focused ion beam (FIB) cross-sectioning and scanning electron microscope (SEM) imaging to look for defects in vicinity of TIVA signals

Locate relevant areas for FIB/SEM based on TIVA signal/mask layout

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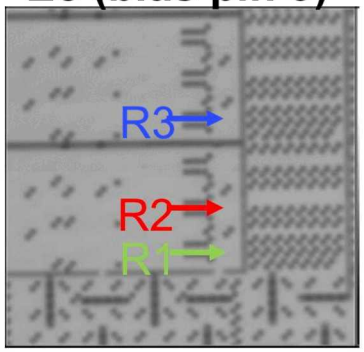
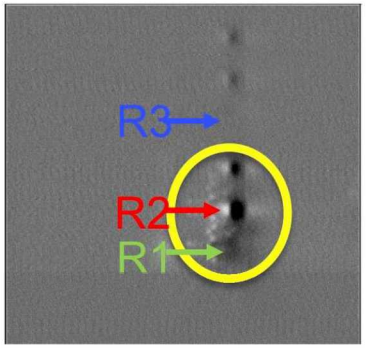
E5 (bias pin 9)

Optical Reflective image



TIVA image

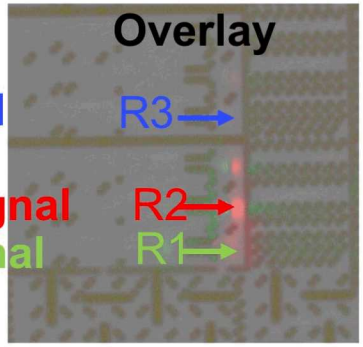


Overlay

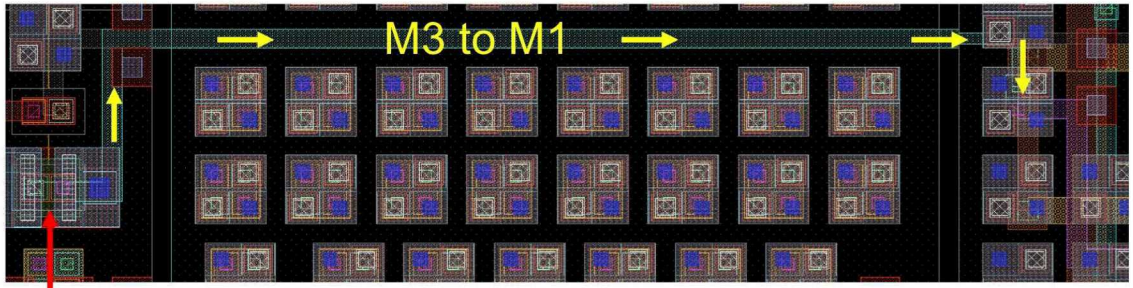
NO TIVA signal

Strong TIVA signal

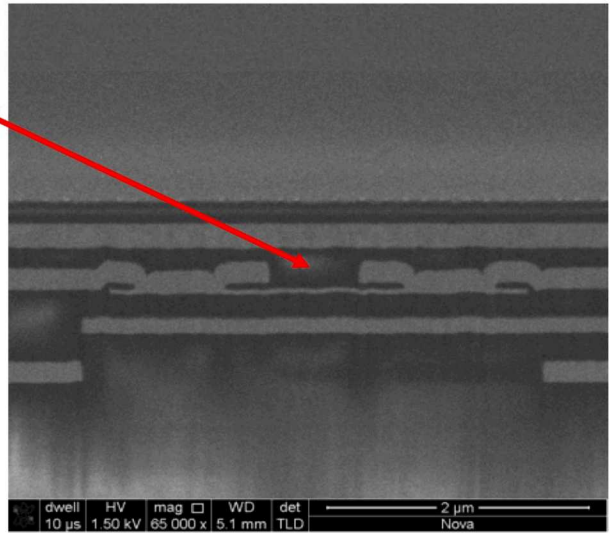
Weak TIVA signal



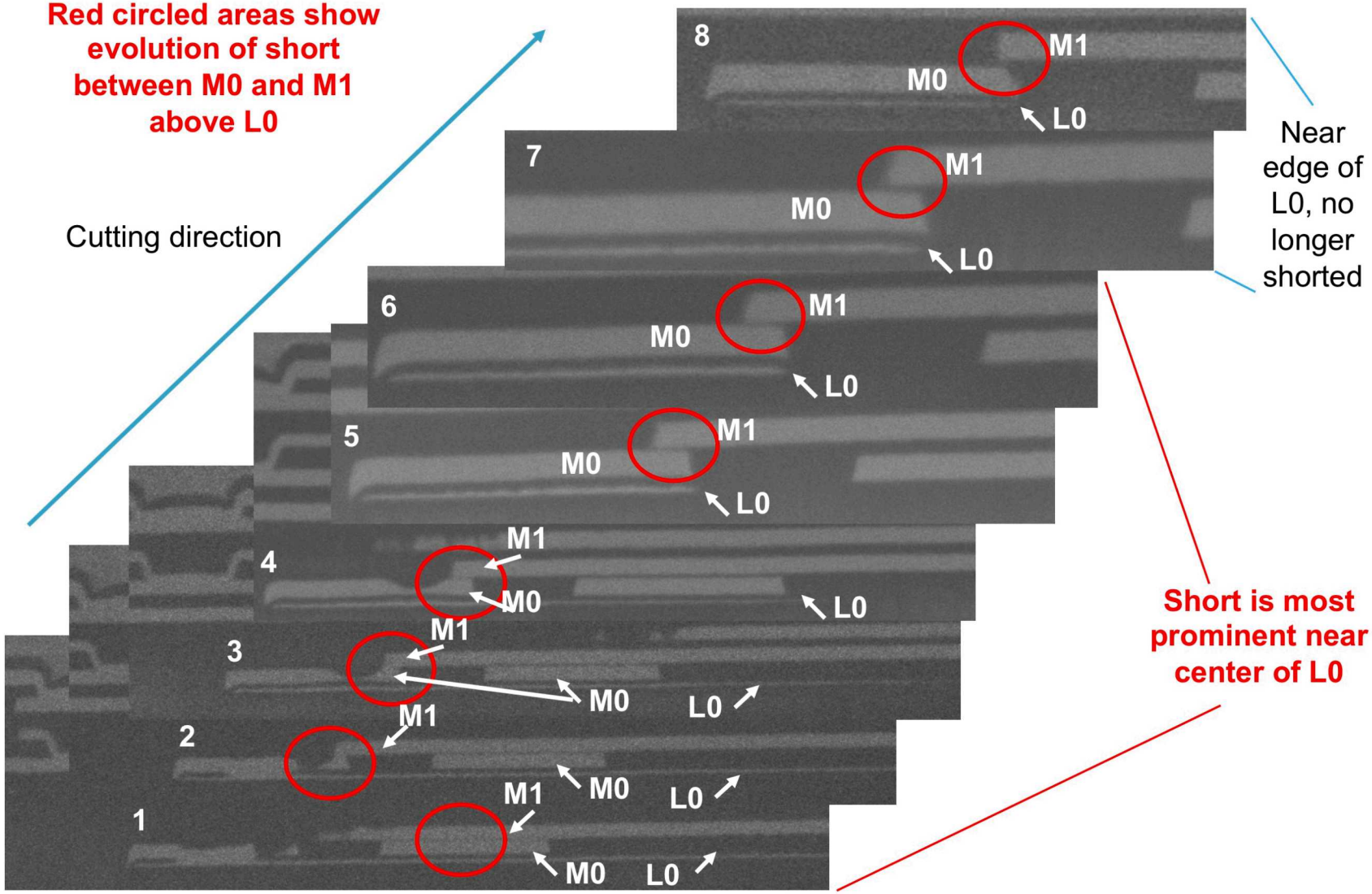
These decoder resistors ***should not*** be biased when RF pins 8,9 are biased – implies short to ground (M0): follow resistor wiring to find possible short



Resistor
R1,R2,R3 all identical
No defects observed



R2- strong TIVA signal, resistor wiring: M1 shorted to M0 only above L0



HYPRES-designed ALU in high frequency testbed fabricated at MIT-LL using SFQ5ee 8 layer Nb + HKL Mo-N process

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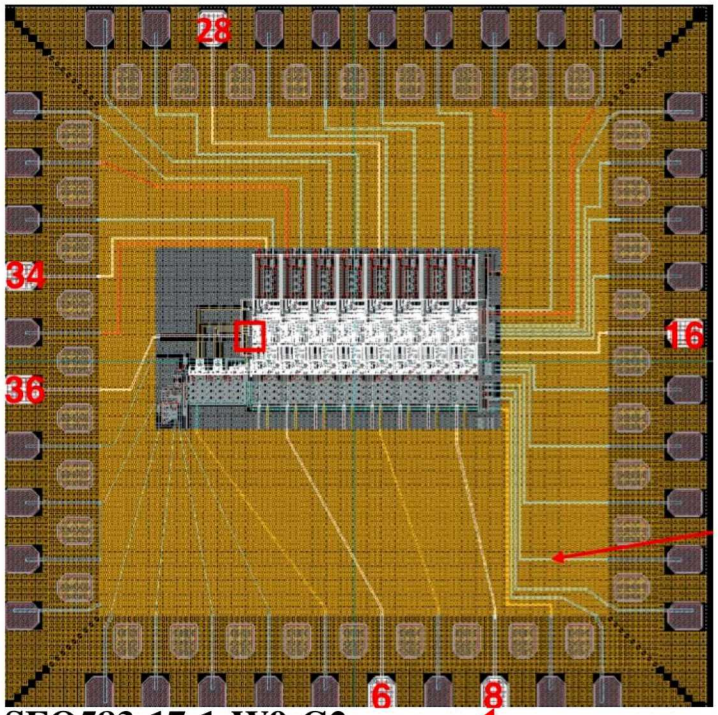
C2 is non-operational (no clock propagation) although other die from same wafer did work

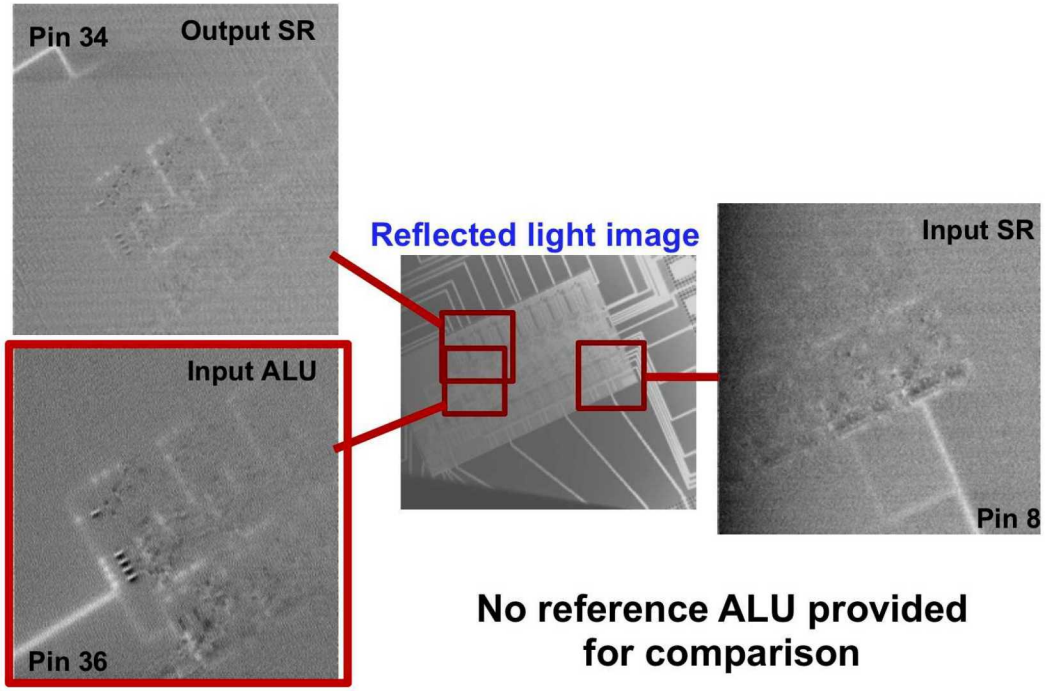


SFQ583-17-1-W9-C2

Apply 10μA dc current to individual circuit bias points

Ambient temperature

TIVA images obtained using different bias points



No reference ALU provided for comparison

TIVA: 532nm laser excitation, 10 µA bias pin 36

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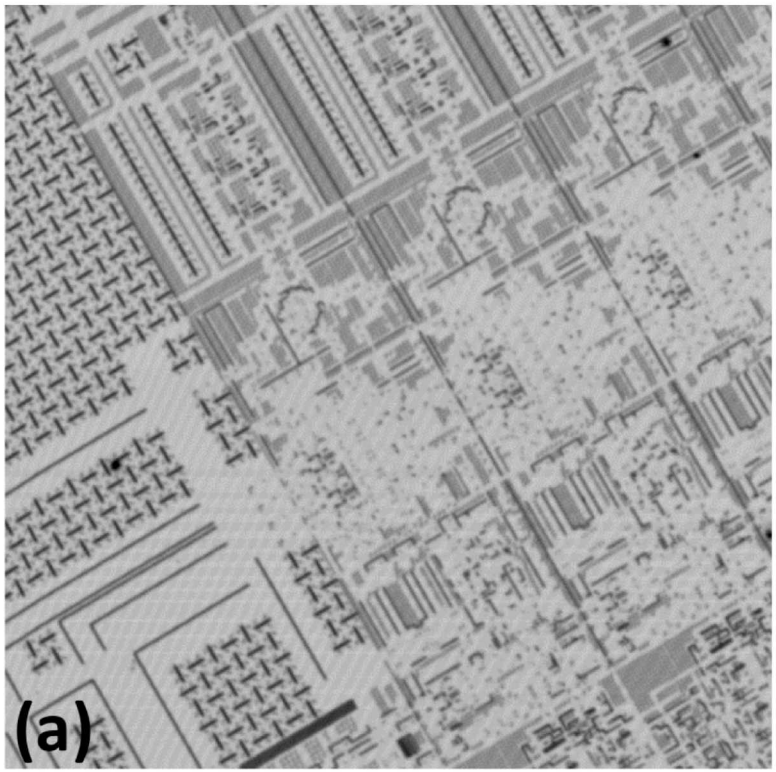
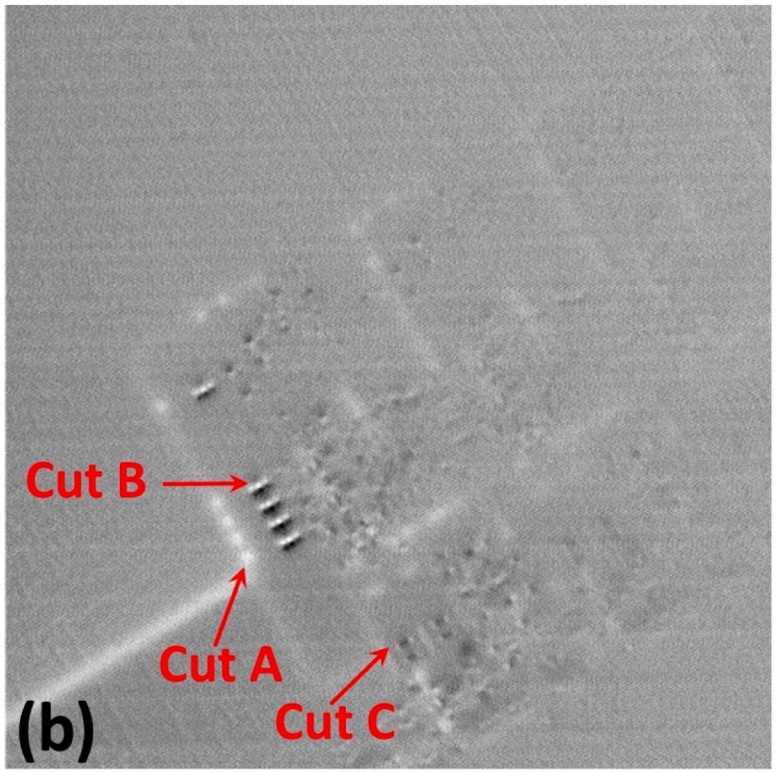
Reflected light

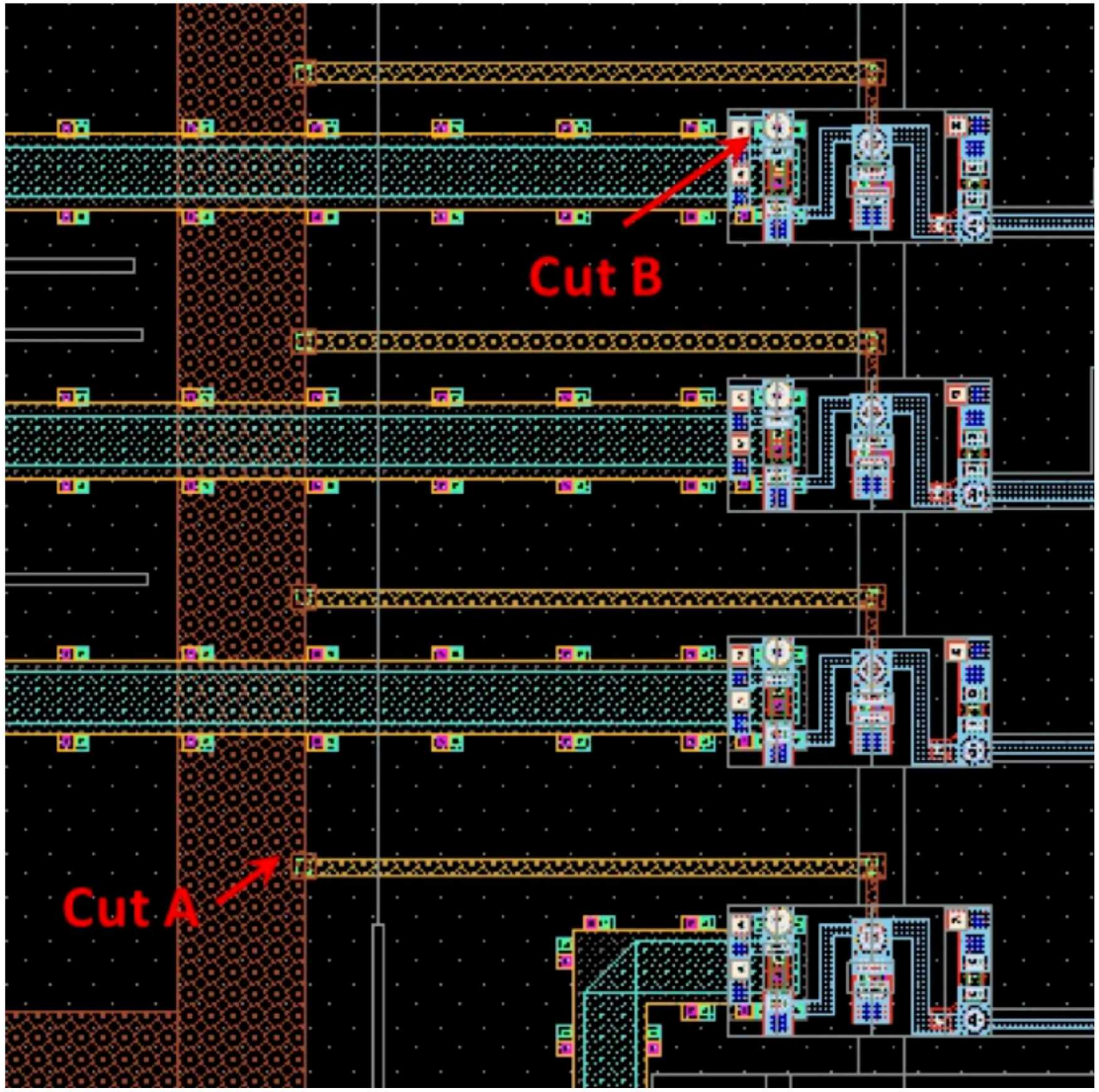


TIVA imaging



- Several sites show change in resistance as laser scans across biased circuit
- Use circuit layout to identify prominent sites for FIB cross-sections
- SEM imaging during FIB cross-sectioning to look for defects

Circuit layout in TIVA signal areas A, B



Cut A: L0 Mo-N HKL connection to M0 Nb

Cut B: Vias, JJs

SEM image of FIB cross-section at TIVA signal Area A

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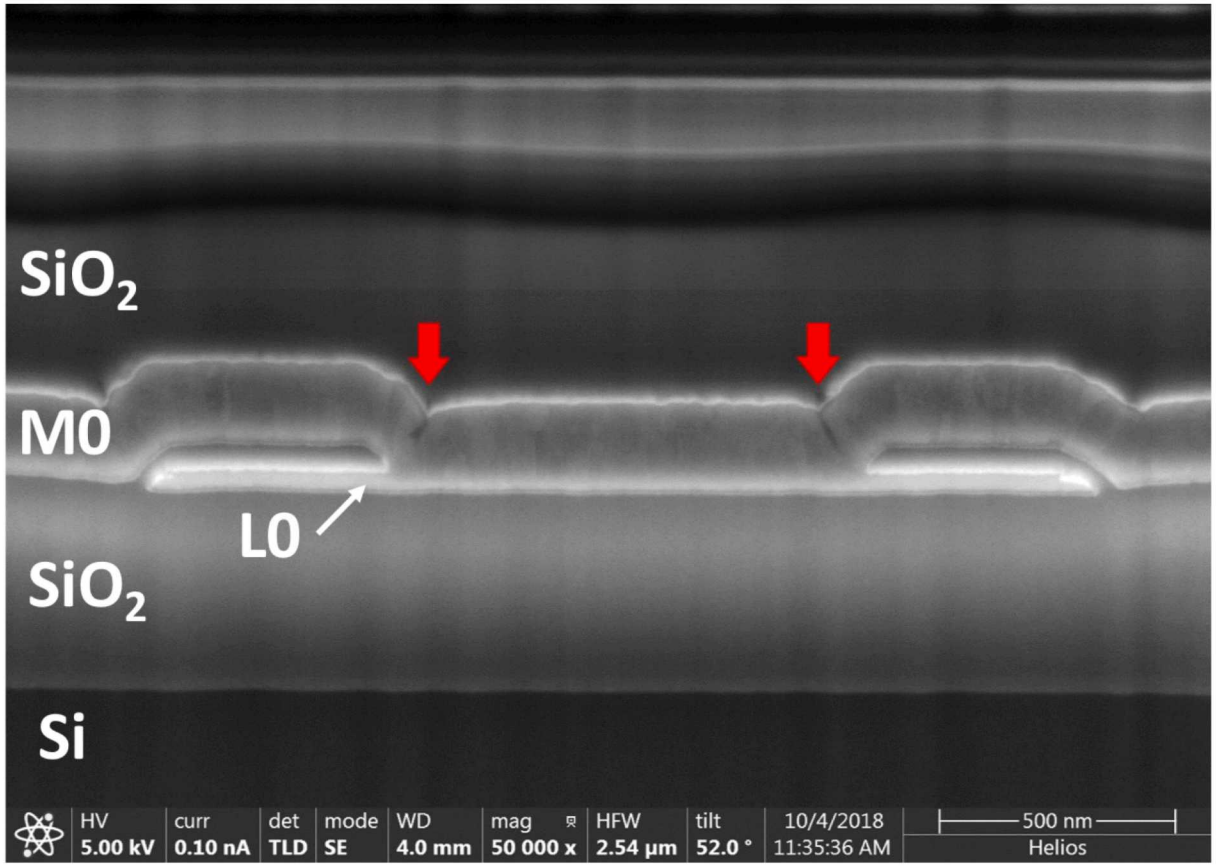
L0 to M0 contact area



Away from M0 contact: L0 is 56 nm thick

At contact to M0: L0 is 10 nm thick

All L0 to M0 contacts in areas with TIVA signals show similar etching into L0

Thin L0 is not likely to cause problems unless L0 is completely etched under the M0 contact – not the case on this die

Seam in M0 contact layer at edges of via to L0 (red arrows) reduces expected critical current through this area – needs to carry 1 mA – Nb without seam can carry > 30 mA unlikely seam is responsible for ALU failure

SEM image of FIB cross-section at TIVA signal Area B

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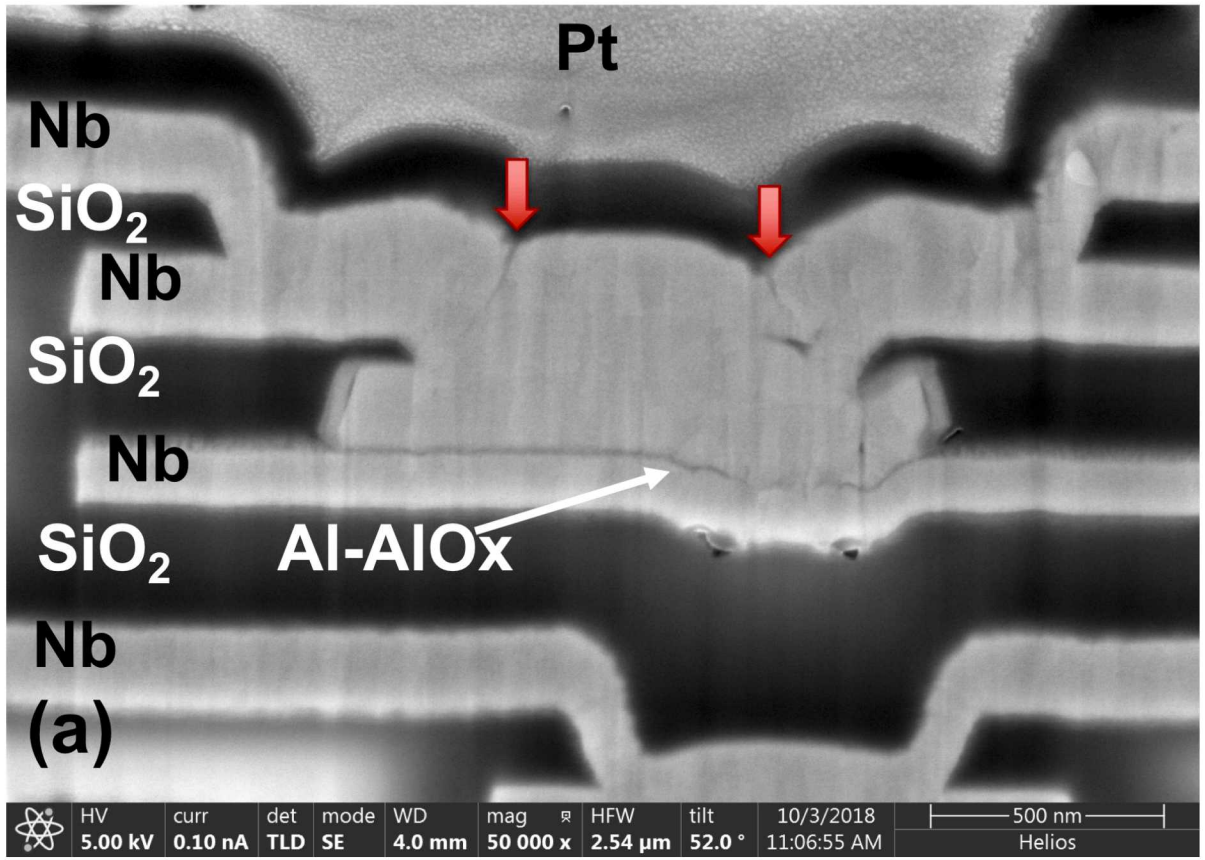
JJ above via



Again, seam in Nb wiring layers above JJ reduces expected critical current through this area – needs to carry 1 mA – Nb without seam can carry > 30 mA unlikely seam is responsible for ALU failure

CMP leaves depression in SiO_2 above via

Junction morphology is disrupted above via

Similar morphology observed at all JJs directly above vias at TIVA signal locations containing JJs

Expect this defect would result in compromised JJ properties – likely fatal flaw

SEM image of FIB cross-section at TIVA signal Area C

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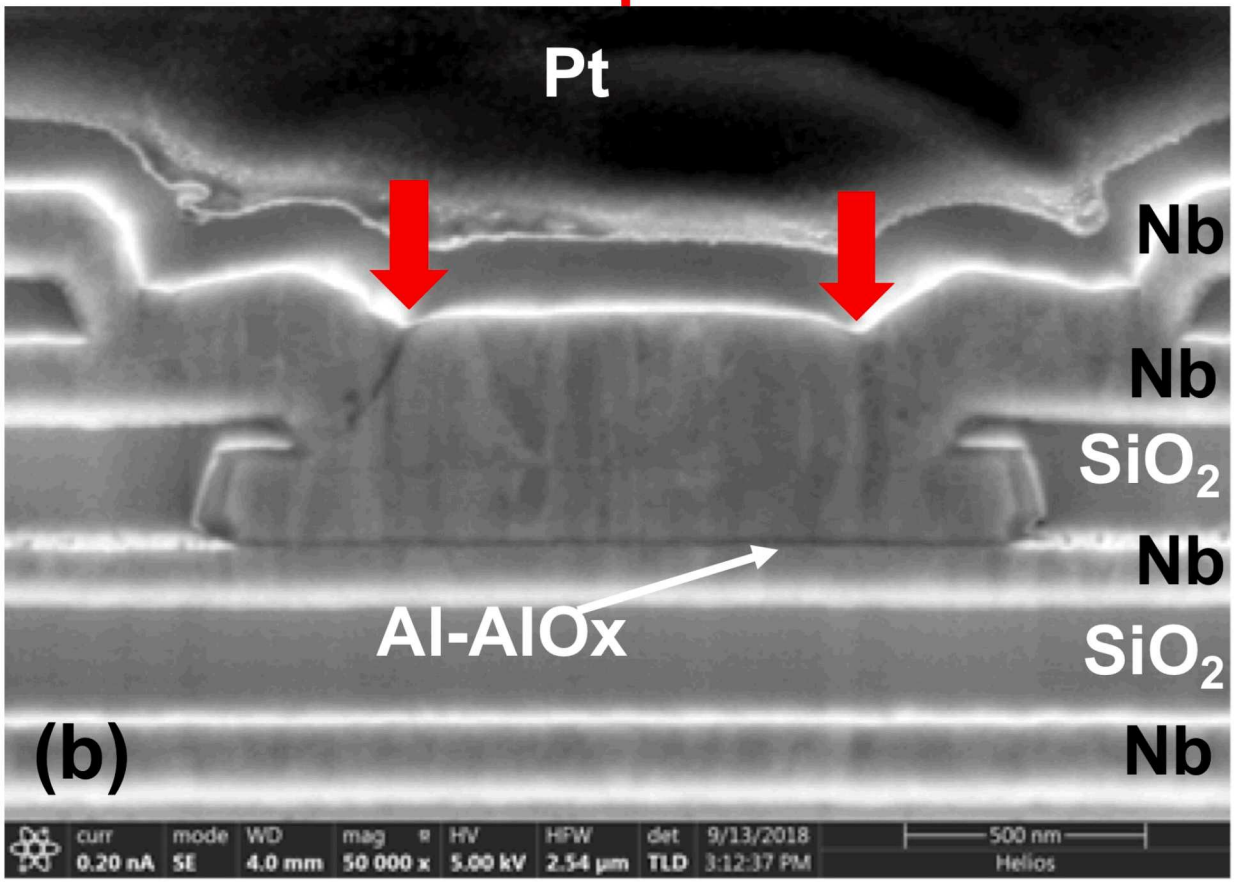
JJ above planar M4



JJs above planar M4 have no morphology issues in junction area

Voids leading to seam in Nb wiring are likely responsible for observed TIVA signal

Again, seam in Nb wiring layers above JJ reduces expected critical current through this area – needs to carry 1 mA – Nb without seam can carry > 30 mA unlikely seam is responsible for ALU failure

Conclusions

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- CMOS failure analysis techniques can be used to locate isolated defects in complex SCE circuits biased at ambient temperature
- Ambient temperature TIVA was successful in locating localized shorts between Nb layers in an RF/decoder circuit with known fabrication issues
- Ambient temperature TIVA was successful in locating morphologically disrupted JJs above faulty CMP and seams in Nb wiring layers
- Morphologically disrupted JJs are the likely cause of ALU failure
- Future studies include investigation of a HYPRES-designed register file matrix with a symmetric design but only one working output (the other output failed)