# Architectural Simulation

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## Challenge

Exascale architectures will be of unprecedented scale and complexity due to increased parallelism and heterogeneity of the processing and memory systems. Architectural simulation must provide actionable analysis of performance. Our challenge is to provide an insightful collaboration tool for the exchange of ideas, requirements, and issues between the key ECP stakeholders and vendors.

- **Multiple Scales**: Network architectures on O(1M) endpoint systems vs. core level instruction set changes
- **Applications**: Simultaneously inform application development based on emerging architectures and architectural choices based on emerging applications
- **Design Space**: Exploration of a vast design space requires efficient mechanisms to find optimal solutions
- **Performance/Fidelity**: Finding the "right" tradeoff between simulation performance, accuracy, and precision

## Approach

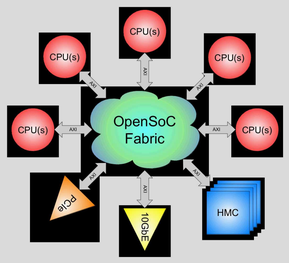
Evaluating Exascale architectures in the context of DOE applications requires a range of tools, techniques, and approaches.

- **Scalablity**: Large machines with high node counts, core counts, threads, and accelerators will need to be simulated using fast, efficient models
- **Multi-Resolution**: The set of DSE simulation tools must be able to examine performance impacts at both large (O(1M) nodes) scale with abstraction and small scale (single core) with precision.
- **Interoperable**: The diversity in tools and techniques but also allow close collaboration and cooperation both between labs and with industry partners
- **Open**: To facilitate broader engagement, tools will have to be open while still protecting proprietary design information.

## Tools

### OpenSoC Fabric

- Network on chip generation tool
- Enables simulation and FPGA emulation of on-chip networks
- When combined with processor models, enables modeling of complex SoCs with mixed cores




### Processor Models

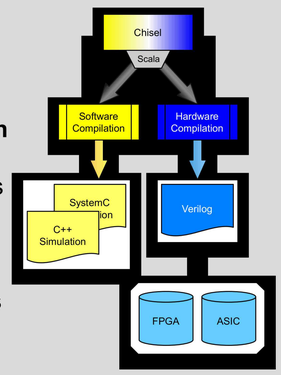
- Open source processor models based on RISC-V ISA
- Written in Chisel, highly customizable
- In-order and out-of-order variants
- Can be stitched together using future exascale processor designs

### Multi-scale/fidelity HW Simulation

- Structural Simulation Toolkit is the premier open-source tool for cycle accurate simulation of HPC architectures.
- Contributions and utilization by labs, vendors and academia
- Models ranging from existing to 'Beyond Moore' components.

### Rapid Hardware Module Generation

- The Chisel Hardware DSL allows rapid creation of hardware designs
- SW simulation and HW emulation produced from a single module
- Customize existing processor models or code mock-up IP blocks from vendors



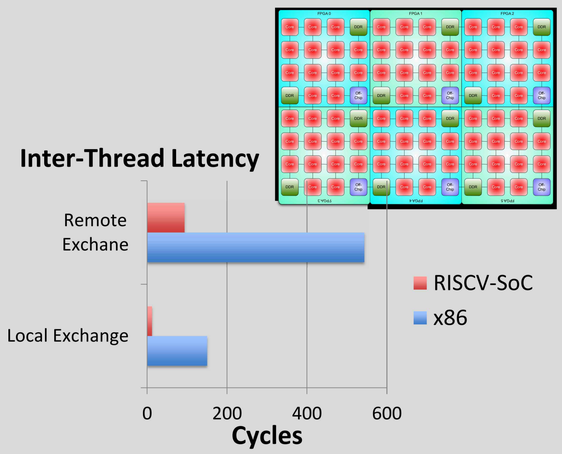

### Custom Processor Designs

- Utilizing the GEM5 open source processor model
- Acceleration strategies utilizing 'micro-engines'
- Optimize performance and energy

## Previous Work

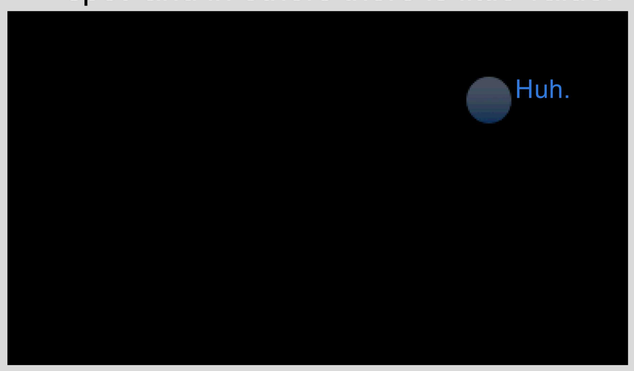
### 96 Core SoC Emulation

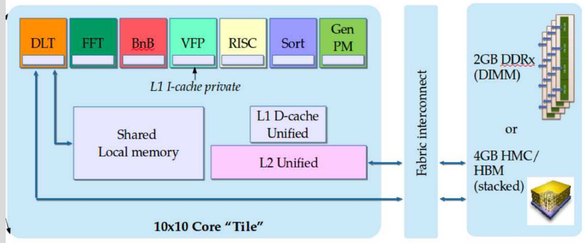
- 96 cores connected using a mesh network generated with OpenSoC
- Compared conventional cache coherence protocol to direct hardware support for global address space for halo exch.




### Impact of High Bandwidth Memory

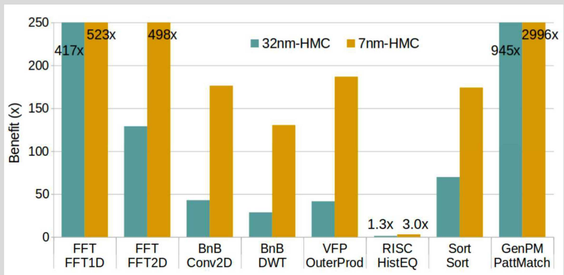
- For hybrid memory system (HBM & DDR4) how much HBM do you need?
- We explored and number of lab proxy apps and found that it depends.
- In some cases there is a clear 'sweet spot' and in others there is little value.



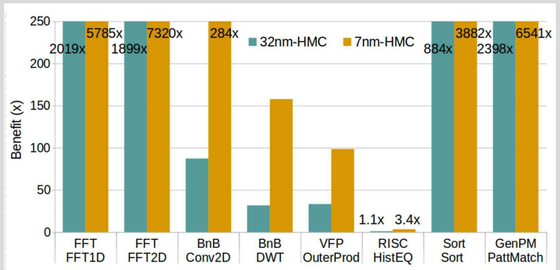




### Impact of HMC on Performance and Energy for Novel Architectures

- Model a novel processor architecture with specialized 'micro-engines'
- What are the gains realized utilizing different generations of HMC?
- Significant impact for memory bandwidth limited algorithms



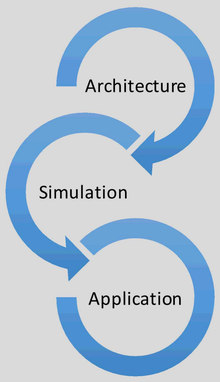

(b) 10x10 Energy benefit (32nm & 7nm, HMC).




(b) 10x10 Relative Performance (32nm & 7nm, HMC).

## Impact

Exploring the emerging design space of future architectures will require a robust set of tools and techniques. With this toolkit the DSE project will be able to examine future memory architectures, heterogeneous processor designs, network organizations, and I/O systems in the context of rapidly evolving applications. We will be able to analyze system changes to machines consisting of millions of nodes and smaller changes to individual system components. This analysis can inform both vendor and application design choices and can lead to better decisions for ECP's optimal choice of architectures to reach usable Exascale capability and beyond.

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