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Book Title: Design for Manufacturability: New Materials, Technologies and Processes

Book Chapter: Designing for Chemical-Mechanical-Polishing

Jeffry J. Sniegowski

Microsystems Assessments Department
Sandia National Laboratories, Albuquerque, NM 87185
sniegojj@sandia.gov

THE PROCESS

Chemical-Mechanical-Polishing (CMP), a planarization process first developed and used for the manufacturing of multi-level metal interconnects for high-density Integrated Circuits (IC), has been adapted as an enabling technology in the fabrication of microelectromechanical systems (MEMS) or more generally, microsystems technology (MST). The CMP planarization technique alleviates many manufacturing issues introduced by topography generated during the fabrication of multi-layer MST structures. Historically, this was specifically true with polysilicon surface micromachining, an additive manufacturing technology, which was comprised of as many as six added levels of polysilicon. Such a technology would not have been possible without the incorporation of CMP planarization between layers. For the designer, CMP not only eliminates design constraints introduced by non-planar topography generated at intermediate fabrication steps, but also improves the overall quality of surfaces and potentially provides an avenue for integrating disparate process technologies. In general, CMP is applied to substrates onto or into which MST devices are constructed in a batch fabrication process similar to how integrated circuits (ICs) are manufactured. These substrates, commonly referred to as wafers, are most often round, thin, and comprised of single crystal silicon having diameters from 100mm to 300mm with thicknesses of few hundred micrometers to maybe a few mm. Commercial CMP tools are normally setup to handle such substrates. Non-standard substrates can be CMP'd, but this may require specialized tooling at MEMS boutique foundries.

Most simply, CMP is a process to smooth and plane surfaces with the combination of chemical and mechanical forces. The CMP process produces both global and local planarization, as well as smoothing through relatively simple and quick processing. It can, in a way, be thought of as a hybrid of chemical etching and free abrasive polishing. Whereas mechanical grinding alone may theoretically achieve planarization, the surface damage is high as compared to CMP, and generally has no selectivity to materials. On the other hand, chemistry alone cannot attain planarization because most chemical etch reactions are isotropic.

CMP not only simply eases the design and manufacturability of MEMS devices by eliminating photolithographic and film deposition/etch issues generated by severe topography, but also enables far greater flexibility with associated designs and process complexity. First, CMP planarization includes topographic reduction on a local scale with the conversion of abrupt, vertical steps to much smaller steps that removes interferences and fabrication issues, while on a more global scale, it flattens transitions from large high areas to a large low areas. Second, CMP can provide microscopic surface smoothing that produces a mirror-like surface at the nanometer scale.

Figure 1 exemplifies the basic function of the CMP process wherein an oxide surface having topographic bumps generated from an underlying polysilicon layer is planarized, removing the bumps in the oxide film and making it more appropriate for subsequent processing. This is accomplished by rotating a wafer under pressure against a polishing pad in the presence of silica-based, alkaline slurry. The mechanical energy imparted to the abrasive slurry particle through pressure and rotation, in combination with materials-specific chemistry, causes high features to erode at a faster rate than low features, thereby planarizing the surface over time.

The motion and force of the MST substrate against the pad with slurry containing microscopic particles causes mechanical abrasion, while the added chemistry to the slurry alters the material being polished on the surface of the wafer illustrated in Figure 2. The combined mechanical abrasion with chemical alteration is called Chemical Mechanical Planarization or Polishing (CMP). The removal rate of the material can be easily an order of magnitude higher with the simultaneous chemical and mechanical effects as compared to either one taken alone. Selectivity and polishing stoppage can be gained with the proper selection of chemistry and particles. Finally, the smoothness of the surface after polishing can also be optimized by using chemical and mechanical effects together.

Before proceeding further, it is emphasized and highly recommended that the designer ask questions of the chosen manufacturing facility regarding specific data on the fabrication output of their CMP processes that may impact the designer's MST product. These data may include step reduction (or print-through reduction), global flattening, and surface smoothness, in addition to which material systems they apply CMP. These items are more evident following the examples below. The goal is to provide a basic understanding of CMP and a quick guide to formulate appropriate questions by which to evaluate or compare multiple fabrication facilities. Details of the CMP process are beyond the scope of this chapter, as entire treatises are dedicated to the CMP process and its integration into a MST fabrication technology. One CMP reference is provided if the designer is inclined to further understand CMP [1].

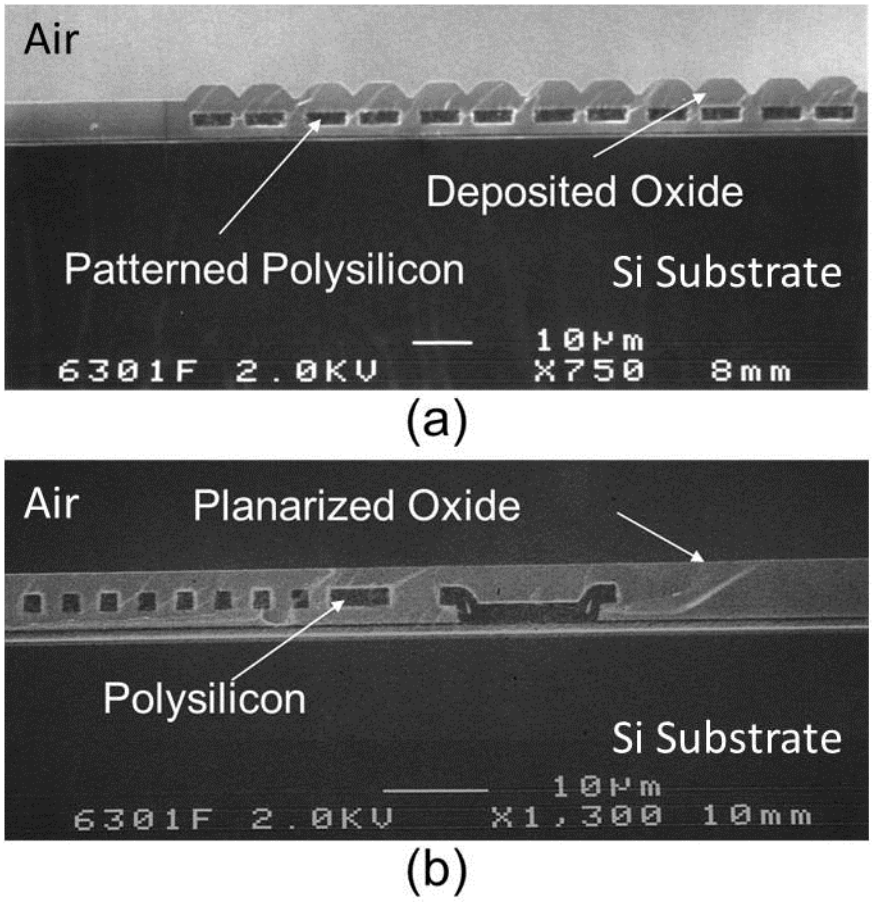


Figure 1. (a) Scanning electron microscope (SEM) cross-section image of a partially-fabricated MST silicon substrate illustrating the uneven, severe topography before CMP planarization. Such topography is generated by the addition of another uniform, conformal layer of material unto a surface previously patterned with a design layer (such as the polysilicon layer shown here). (b) SEM cross-section of a partially-fabricated MST substrate post CMP planarization. Subsequent patterning of the oxide and addition of more layers can be accomplished without the interference from topography.

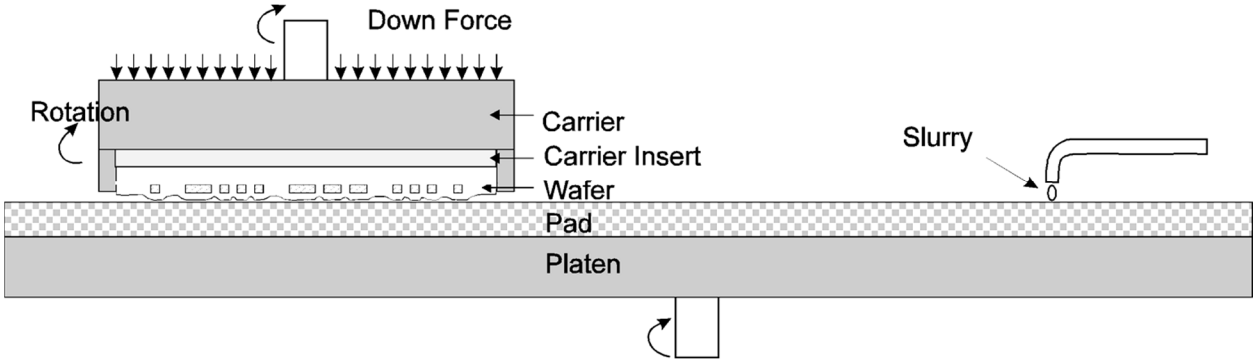


Figure 2. A schematic representation of a CMP process where an oxide surface with severe topography is planarized by rotating the inverted MST substrate under pressure against a polishing pad in the presence of silica-based alkaline slurry.

APPLICATION OF THE PROCESS

As a MST device is fabricated, layers of materials are added or removed, then patterned and etched with the device design. This cycle is potentially repeated numerous times, depending on how many levels are included in the design. Each cycle adds topography to the surface. The first layer on a pristine, flat substrate presents no problems, but as the subsequent layers are added, this topography introduces issues for manufacturing and eventually issues for the design function. The CMP process can be used to essentially re-flatten the surface topography, ameliorating both fabrication and design issues. This is the essential basic function of CMP. However, it can also provide more sophisticated functions that are described below.

In more general terms, there are three broad applications of the CMP process to MST fabrication. First, to planarize, or make flat, the layers enhances manufacturability and design. These can be layers that will later form structural or functional materials in the final design, or can be the layers that are temporary support layers that are removed in the final steps of fabrication, exposing functional layers or producing free-standing mechanical structures. These temporary support layers are often referred to as sacrificial layers, and can be removed by various chemical means as a final step. Second, to touch polish a surface, producing a high quality finish: this is important for applications such as optical devices. Third, to produce the design pattern in a layer (such as copper or tungsten) that cannot be patterned by the normal means of photolithography masking and etch. Such process is referred to as CMP damascene or dual-damascene. Damascene is basically the process of depositing the desired material into trenches having the desired design pattern and using CMP to polish away excess overlaying material.

As a starting point, from the designer's perspective three questions are proposed: (1) do I need planarization at all?; (2) if yes, does it only need to remove gross non-planar structure?; and (3) do I need a high degree of flatness and smoothness at either or both global and local scales? If the answer to (1) is no, then go design! If the answer to (2) is only the need for gross planarization, then most CMP processes

offered will very adequately accomplish this. If the answer to (3) is yes, I need an optically flat and smooth surface, for example, it becomes imperative that the designer work very closely with the fabrication personnel to clearly understand what degree of flatness and smoothness is produced in the particular fabrication facility. If the facility has a well-developed CMP capability for MEMS, they may offer several CMP processes optimized to produce specific results on specific materials. It is hoped that the following further description of CMP planarization will readily guide the designer through these three questions. With CMP planarization, a change in design perspective occurs since the need to circumvent mechanical interference in a non-planarized process is alleviated. Thus, more complex designs with greater functionality created from multiple levels are feasible.

The designer should inquire as to which layers in the fabrication technology are CMP'd and the relative thicknesses of those layers. Also, it is useful to inquire as to the purpose of each application of the CMP process. Whether it is for the purpose of: planarization (impacts manufacturing and design), touch polish (impacts surface quality for design), and damascene (layer patterning, primarily only of interest to the fabricator). Although each specific application of CMP is optimized to a single purpose, there may or may not be cross-over benefit to the other impact areas (e.g., planarization CMP can provide high quality surfaces, whereas a touch polish will not normally provide significant planarization). To first order, removal of mechanical interferences/obstructions and manufacturing issues is readily accomplished by a basic CMP process. However, where a high degree of flatness or ultra-smoothness is desired, the results are dependent on the specific material and CMP process. These can vary significantly foundry to foundry.

ENHANCED MANUFACTURABLILITY OF MST

The CMP process was first applied to a MEMS technology known as polysilicon surface micromachining, but can be applied to any MST wherein topography is introduced by the repetitive deposition and patterned etching of multiple films. Typically, at the completion of the MST fabrication,

sacrificial layers (as their name suggests) are selectively removed, leaving the free-standing device structures in the form of channels, gears and linkages, or mirrors. Figure s 3(a-c) illustrate both the essence of polysilicon surface micromachining and displays the vertical topography which arises during a non-planarized process. This topography can produce mechanical interference between moving parts and complicates subsequent process steps. Figure 3(a) schematically illustrates this interference, where a completed linkage element is intended to move a lateral distance, ΔD, but is stopped at a travel of $\delta t < \Delta D$ due to the obstruction from a non-planarized upper layer in the process.

The mechanical interference or physical obstruction arises when an upper layer of polysilicon must pass over the edge of a previously etched lower layer. An example of this interference is shown for a micro-actuator in Figure 3(b), where the upper link runs over the edge of a gear producing an overhang feature that can interfere with the desired range of motion. This feature is due to the conformal deposition of the upper polysilicon film. Such link/gear interference can be alleviated by appropriate design of the microactuator, as pointed out in Figure 4(a), or by planarization of the surfaces before subsequent deposition of additional films, as illustrated in the CMP-planarized joint in Figure 3(c), or the uncompensated design in Figure 4(b). Note such undesired obstruction also occurs if one is attempting to produce a fluid channel with a capping layer, wherein the intermediate layer is not planarized.

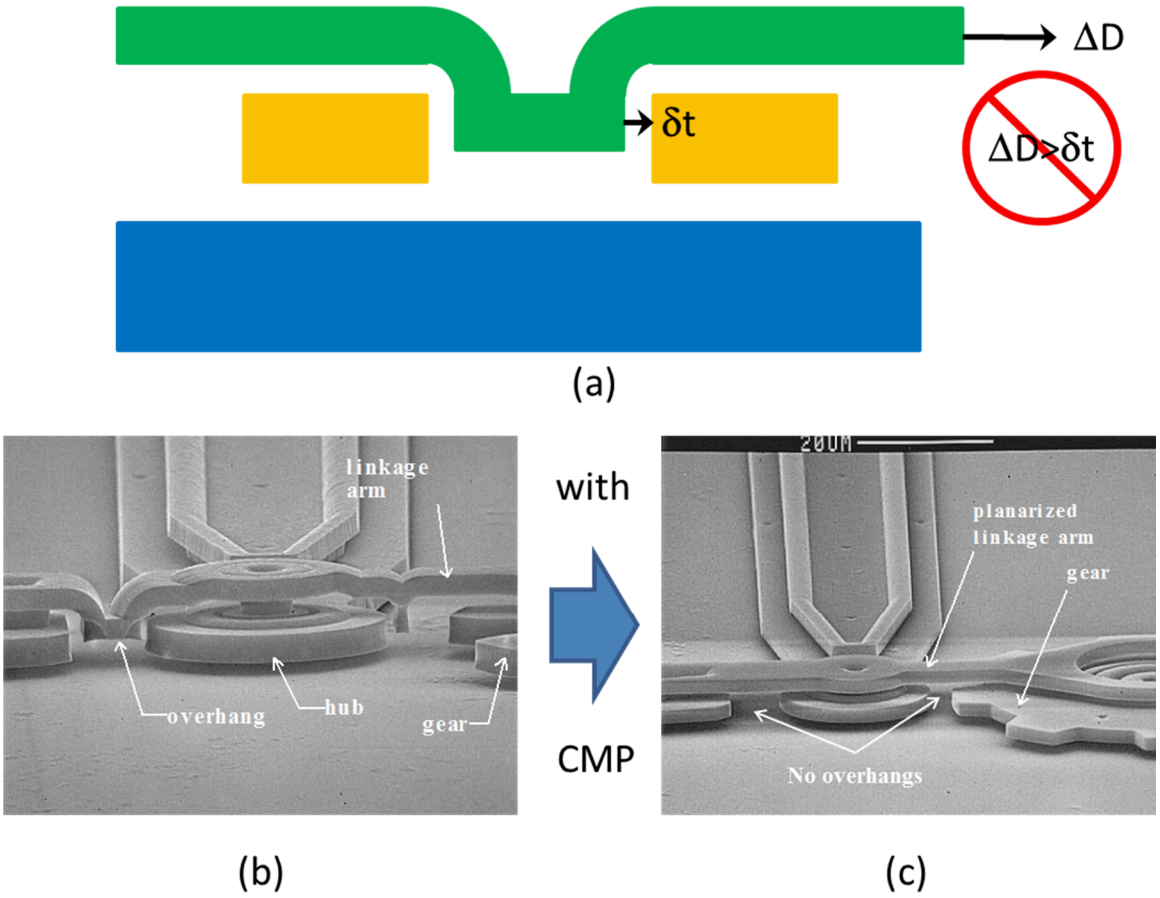


Figure 3 (a) Schematic illustrates an interfering protrusion generated in the green layer with a non-CMP process. In the final released device, under a displacement ΔD, the active MST linkage will stop in a collision with the underlying yellow layer. SEM image (b) is of a non-CMP fabricated linkage while (c) is the same linkage fabricated with CMP. The protrusion interference is removed allowing a movement ΔD>δt and no longer needs to be considered during design.

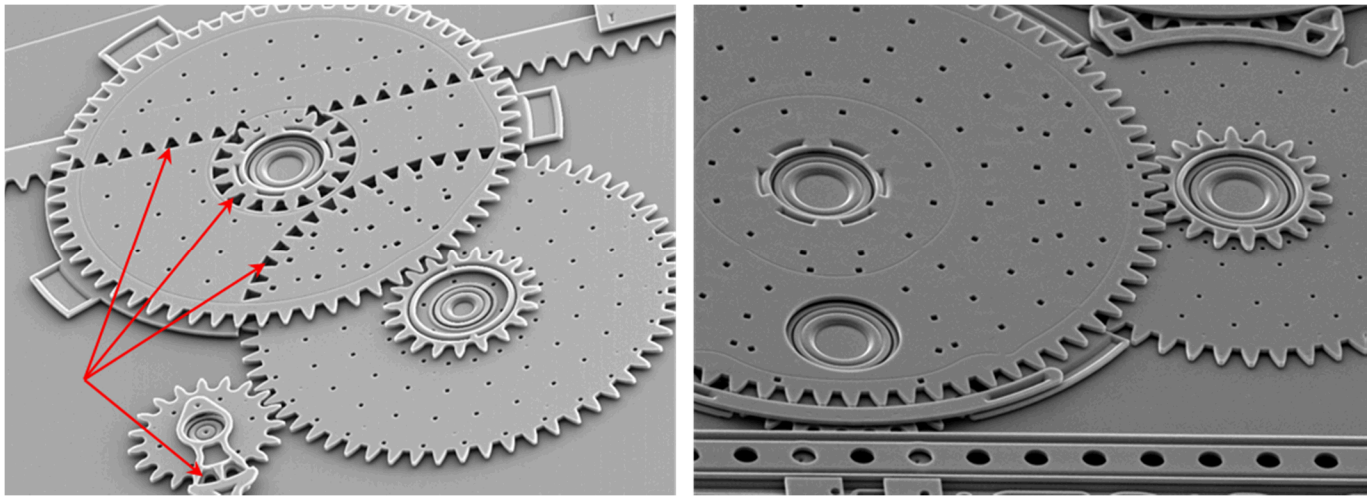
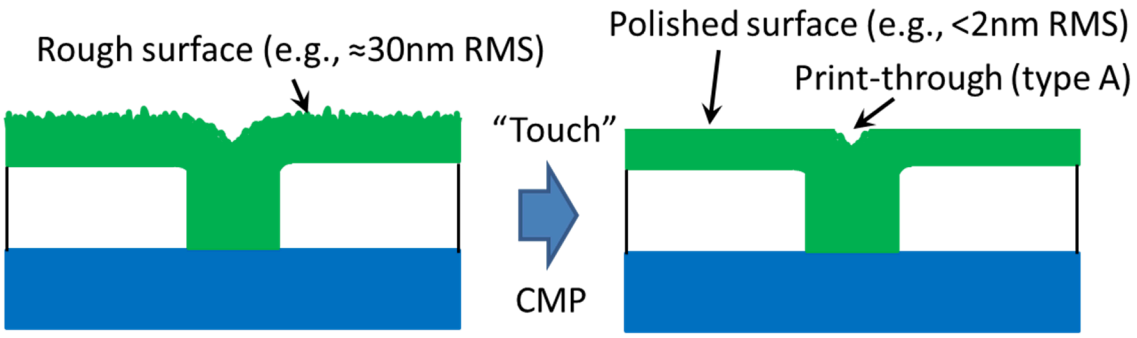


Figure 4 SEM images of (a) rack and pinion design with accommodation cuts (indicated by red arrows) in the gear design for a non-CMP'd early process, while (b) shows a similar design accomplished with CMP planarized processing having no accommodation cuts. Note: the small regular holes seen are to expedite the final release etch for the device.

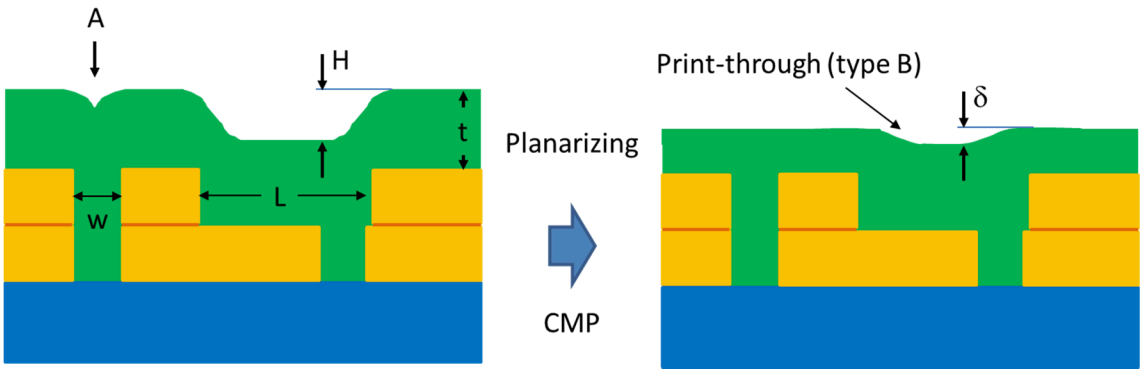
HIGHER ORDER CMP EFFECTS

CMP can optimize the top surface of a particular layer (e.g., a reflective metal surface). This includes smoothing the surface, eliminating or reducing print-through from the underlying layer topography, or improving the overall flatness on a larger scale. Print-through is defined as residual steps seen in the upper polysilicon surface from underlying layers following CMP. Regarding smoothing, CMP can produce surfaces with root-mean-square (RMS) roughness on the order of a few nanometers or less, where a specific example is CMP reducing the RMS roughness of as-deposited polysilicon from 46 nm to 2.2 nm. To illustrate the most relevant higher order CMP effects, schematic depictions with exaggerated dimension are shown in Figure 5. These include surface polish and print-through (type A), dishing (type B), and bowing (type C) that may impact a design if not known or accommodated. Following these schematic illustrations, actual fabricated examples of these effects are provided in Figure s 6, 7, and 8. Surface depressions, shown in Figure 5a and 5b, can produce type A and type B print-throughs as a byproduct of areas where the overlying film fills a patterned depression. Type A results when the width is less than about the thickness ($w<t$) of the deposited film, whereas type B occur as shallow dishing when L>>t. Normally, the touch polish is shallow and does not necessarily remove type A print-through if present in a design. This may

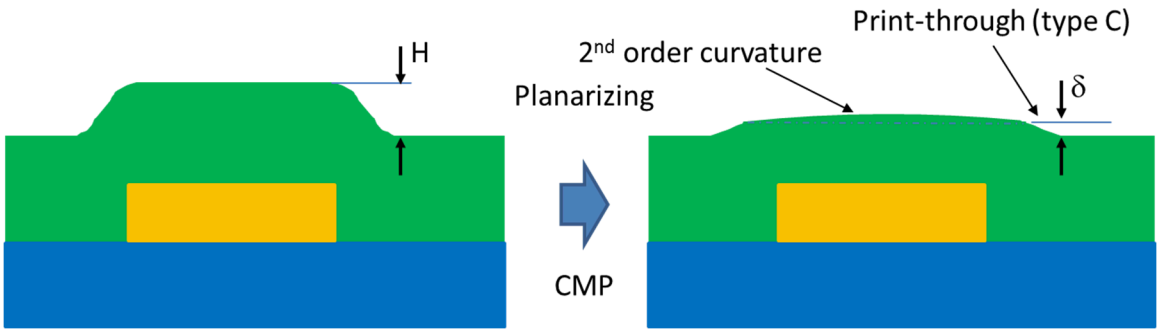
adversely impact an optical mirror-type surface by introducing light scattering artifacts. On the other hand, planarizing polishing that removes significant thickness of material usually greater than or equal to *H*, type A features are simply polished out. However, this is not necessarily true of type B print-through where residual small steps at the edges of large depressions (or bumps) where the characteristic width of the depression (or bump) is much greater than the deposited film thickness (*L*>>*t*). Another even smaller effect can be a very slight bow (small convex curvature) of the surface over a planarized large bump a shown in Figure 5c. There can also be a similar very slight dishing (small concave curvature) of the surface over a large planarized depression. (Note: this was not shown in Figure 5b to avoid clutter.) In either case, if an ultra-flat surface is required, these effects need to be known to exist and inquired of the fabrication facility. However, if the planarized surface becomes part of a free-standing structure in the final device, other effects such as curvature due to residual mechanical stress can dominate the final surface curvature.



a) CMP "touch" polish



b) CMP Planarization of depressions



c) CMP Planarization of bumps

Figure 5 illustrates schematically various second-order effects of CMP. Smoothing in the case of touch polishing in 5a), while 5b) and 5c) illustrate effects that occur while CMP planarizing large areas of depressions or bumps. These may help clarify the actual fabrication results shown in Figs. 6, 7, and 8.

Print-through effects on the order of a couple hundred nanometers do not necessarily cause mechanical or manufacturing interference but may adversely affect optical elements, causing scattering or phase shifts. For a real example, Figure 6 illustrates a typical surface profile of an overlying oxide pre- and post-CMP planarization. This oxide layer covers structures onto which additional structures may be built. One sees that the severe pre-CMP topography of 2.5 um, which can lead to mechanical and manufacturing interferences, is eliminated. However, a relatively small (< 200nm) global, residual bow remains, and even smaller (<100nm) localized print-through step (type C) still exists at structural edges. Specifically in the case of the global scale bow, it is good design practice to use CMP dummy structures to further reduce this residual. CMP dummies are simply extra, non-used structures consisting of all underlying layers that surround the active device areas. Dummies are used in all modern IC CMP processes to maintain a high degree of flatness, in that case to prevent manufacturing issues. IC foundries normally include these in the final design mask layouts through automated design tools. However, in the case of MST structures, it is critical that they are located well outside the range of motion of movable MST structures or the interior of channels or desired cavities. If the designer is not responsible for including CMP dummies in their MST

design, it is imperative that the designer work with the fabrication facility/mask house to ensure there are no inadvertent design interferences introduced if they are automatically generated.

A final example is provided to illustrate how variations in CMP can highly impact demanding optical designs, where flatness and smoothness can be extremely critical. Figure 7 shows three differential interference contrast (DIC), or Normarski mode, optical microscope photographs imaged after deposition of a final polysilicon micromirror layer for: (a) the baseline process, (b) modified oxide CMP step after an underlying polysilicon layer thermal anneal, and (c) modified process using baseline process up to the final micromirror polysilicon followed by a polysilicon CMP planarization/smoothing step. As shown in Figure 7, the baseline process produces a high degree of contrast and clearly shows the effect of the underlying pattern which has printed through to the front mirror surface resulting in increased topography. Such a result is unacceptable for micromirror applications. The second and third photographs correspond to the revised process flows described above. The Normarski mode photographs given in Figure 7(b) and Figure 7(c) show very significant topography reduction when compared to the baseline surface in Figure 7(a). Profilometer measurements for each of the process options and the baseline reference are given in Figure 8. Both process alternatives provide acceptable $< \lambda/10$ wavelength flatness. The profilometer measurement that indicates the best result is with the polysilicon CMP process option (c) (Δ step $_{max} = 20$ nm).

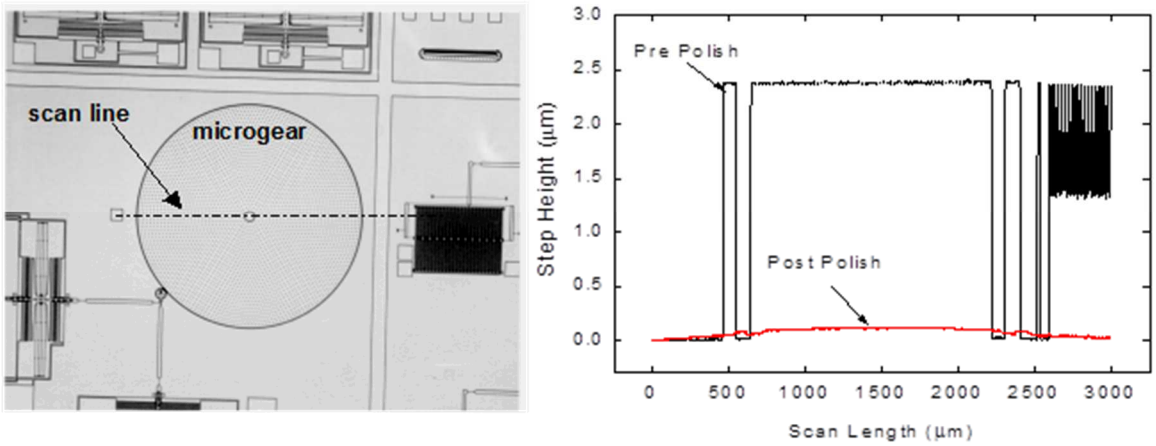
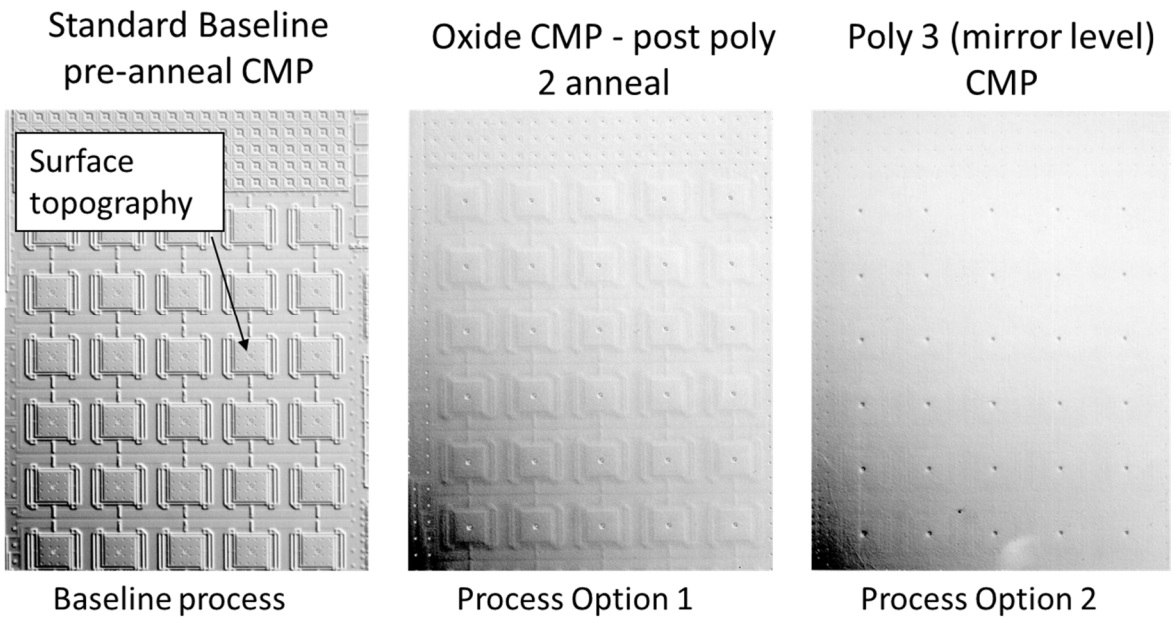


Figure 6. The profilometer scan on the right is across the gear in the optical micrograph on the left. Both the pre- and post- CMP topography heights of the oxide covering the gear are shown. The small < 200nm topography variation remaining over the microgear is acceptable for micro-mechanical applications.



(a) (b) (c)

Figure 7. Nomarski mode microscope photographs of the polysilicon 3 layer for (a) baseline process, (b) oxide CMP after the anneal step, and (c) baseline process with additional poly CMP step on poly 3 layer. The photographs give a good indication of the existing surface topography when viewed in the reflected light Nomarski interference contrast mode.

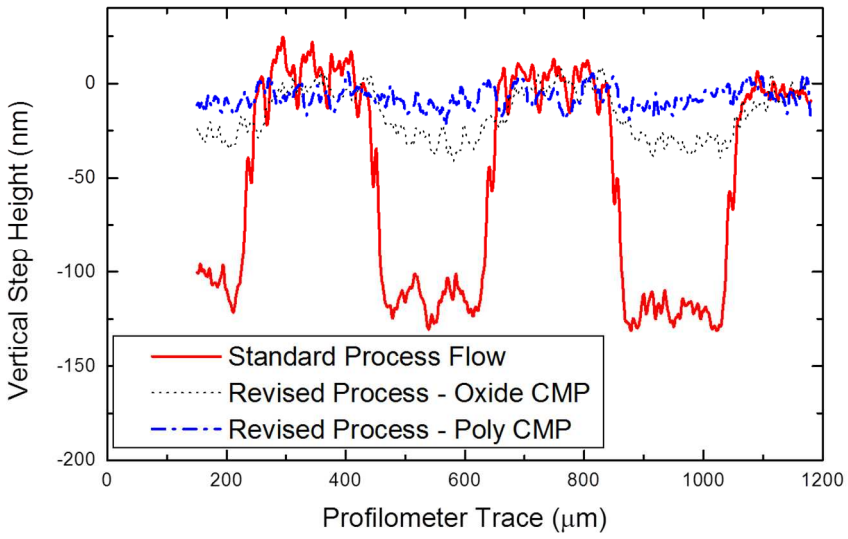


Figure 8. Profilometer measurement for the standard and revised process flows shown. Both of the revised process flows show an improvement in planarity and produce acceptable flatness for optical micromirror applications. The location of the profilometer scan is given in Figure 7a.

From this example, it is imperative to request representative examples of the print-through reduction, global flatness, and surface smoothness from your specific foundry to determine whether or not they meet your design criteria.

CMP LIMITATIONS

The principle limitation of CMP is total material removal, (i.e., height of topography removed). CMP provides a high quality finish with little substrate damage, but it is relatively slow at material removal and, therefore, becomes an expensive process as film thickness increases. Typical film removal can be in the sub-micron to several microns thickness. If significantly greater material must be removed, an initial removal using mechanical grinding or lapping followed by CMP to remove the damaged material and provide a high quality finish is an alternative process. For example, mechanical grinding can have removal rates of approximately 100 microns of Si in 6 minutes versus 0.65 micron SiO_2 in 2.5 minutes with CMP. Mechanical polishing alone is unacceptable in many cases and, most specifically, for semiconductor IC processing due to excessive mechanical damage to the wafer surface. Although one may think that this is not essential to micromechanical devices and structures, the damage can lead to mechanical stress gradients in layers that, upon release to form free-standing structures, generate undesired structural deformation (i.e., curvature of plates and beams). Again, strain gradients in layers and the resulting deformation are process parameters of which a designer must inquire at the foundry of choice.

MATERIALS

CMP is typically used on silicon dioxide, poly silicon and metal surfaces, which are all common materials in the IC industry. However, the basic technique is applicable to a wide variety of materials including polymers, semiconductors and their oxides, metals and metal alloys, composites, piezoelectrics, and many more. When used as a damascene process, it permits the use of difficult to etch metals such as copper, tungsten, or other materials of this character. The available materials are determined by the CMP

capabilities developed at the specific foundry and, ultimately, the chemistries and pads provided by CMP vendors. If the particular foundry does not offer the specific material/CMP process of interest, it is recommended that another foundry be sought. Development of new material processes is expensive and time consuming!

CRITICAL PROCESS PARAMETERS FOR THE DESIGNER

The designer can approach fabrication of their design from two directions. First, if the designer is already working with a specific foundry, identify what materials that foundry is capable of handling in their CMP process. If the materials are consistent with the requirements of the design, proceed to further understand the specific CMP process attributes, such as overall flatness dependency on design layout and final surface finish to see whether they also meet the design requirements. Second, if the existing material basis is not consistent with design requirements, determine whether the foundry is willing to develop the necessary material base. If not, proceed to locating alternate microfabrication facilities that offer the necessary materials, and then vet their CMP process attributes. It cannot be overstressed that close interaction with the manufacturing personnel at the early stage of design is critical for favorable CMP outcome. In any case, knowing the detailed specifications regarding CMP performance at the specific facility chosen is critical. With the multitude of CMP tools, pads, chemistries available to a given foundry, and subsequent idiosyncrasies during process development and integration, it is important to discuss the detailed specifications of their CMP results. It is important to ask for process data that indicates both global and local planarization Figure s of merit, dependencies on layout density, and final surface quality, if it is an important design parameter.

5. ACKNOWLEDGMENTS

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6. REFERENCES

[1] Chemical-Mechanical planarization of Semiconductor Materials, M. R. Oliver (Ed.), Springer Series in Materials Science, 2004, ISBN 3-540-43181-0.