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Deep level characterization: Electrical and optical methods

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Introduction

The most direct method for measuring the influence of defects on HEMTs is to examine how the I_{ds} changes under a given bias condition due to thermally- or optically-stimulated transitions of electrons and holes into or out of deep levels. The primary effect of changing the occupancy of a deep level defect on HEMT operation is the formation of a local space-charge that acts like a floating gate. Filling a defect with excess electrons creates a local negative potential that acts to partially pinch-off the channel and reduce I_{ds}. Conversely, electron emission from a defect state makes the local potential more positive and increases I_{ds}. Thus, defect states act to self-bias the HEMT and lead to instability in device operation as the occupancy of deep levels changes under dynamic operating conditions, such as switching or self-heating.

Analyzing the magnitude of variation in I_{ds} provides a straightforward means to assess the degree to which defects affect device performance, but mitigating defects requires understanding how they influence HEMT behavior. Explaining device behavior in the context of defects requires determining the electronic deep level energy (E_t), deep level concentration (N_t), and physical location of the corresponding defect in the HEMT. The energetic location of the defect in the band gap impacts the temporal response of the device, e.g. shallow defects cause dynamic instabilities during switching, while deep defects influence the DC operating points of the device. The deep level concentration determines the magnitude of variation imposed on I_{ds}. The physical location of a defect determines which aspects of device operation it impacts, e.g. defects under the gate impact V_{th}, while defects between the gate and drain impact R_{on}.

The major phenomena of degraded performance in high voltage GaN HEMTs that are associated with deep levels are dispersion[1] and current collapse.[2] The term dispersion refers to depressed HEMT *I-V* characteristics with fast pulsing compared to DC conditions. This is often ascribed to the role of AlGaN surface states in creating a so-called "virtual gate" effect illustrated in Fig. 1. The virtual gate model posits that during device pinch-off, the large potential difference between the gate and drain electrodes allows electrons from the gate to tunnel into the AlGaN barrier. There, the electrons can be captured by the ionized surface donors that supplied the free carriers constituting the 2DEG. By charge conservation, a reduction of ionized donors at the bare AlGaN surface must be met with a local reduction in 2DEG density (n_s) resulting in reduced channel conductivity. If the emission rate of the surface donors is much slower than the switching frequency driving the device, I_{ds} lags the gate voltage, an effect known as gate lag. Key aspects of dispersion are that the phenomenon becomes apparent with fast pulsing of the gate and is ascribed to trapping at surface donors.

Current collapse (also termed dynamic on-resistance) describes a degradation of *I-V* characteristics after a large bias is applied between the source and drain electrodes. This effect is attributed to the charging of deep levels within the AlGaN barrier or GaN buffer by electrons that are impact-ionized from the 2DEG

channel. The loss of carriers in the channel reduces the conductivity and thus the maximum achievable drain current. The drain current will not fully recover until the deep levels surrounding the channel emit their trapped electrons. Thus, the drain current lags the drain voltage, an effect known as drain lag. Note that current collapse manifests itself with large drain-source V_{ds} bias and is thought to involve deep levels in the GaN buffer. Current collapse is no longer an issue in RF GaN HEMTs, but it still persists in high voltage GaN power HEMTs. Standing off several hundred or even several thousand volts between the source and drain often requires the intentional inclusion of deep level defects in the GaN buffer region to suppress source-to-drain leakage. These buffer defects can also trap charge generated due to hot carriers scattering from the channel[3] or due to gate leakage.[4]

Further, very deep traps in III-N materials may have very long time constants, and the filling of such traps may shift the parametric characteristics of the device, since the emission time is so long compared to the switching time that the shift is effectively DC.[4,5] Such parametric shifts are reliability concerns analogous to the bias-temperature effects observed in silicon CMOS, since they may cause the device to drift away from the DC bias point for which the circuit that they are a part of was designed.[6]

Characterizing all of these aspects of defect activity in GaN HEMTs requires a panoply of spectroscopy techniques. Measuring I_{ds} transients under different gate and drain bias conditions provides information on the lateral positon of a defect, i.e. under the gate or in the access region. Lateral spatial resolution can also be achieved by measuring variation in V_{gs} or V_{ds} at fixed I_{ds}. Measuring gate-to-drain capacitance (C_{gd}) transients as a function of gate bias determines the vertical location of defects, i.e. barrier, channel, or buffer layer. The spectroscopy methods of DLTS and DLOS can be applied to either I_{ds} or C_{gd} to quantify E_t and N_t of the observed deep levels.

The remainder of this chapter describes the application of all of these techniques to GaN HEMTs. The fundamentals of Deep Level Transient Spectroscopy (DLTS) and Deep Level Optical Spectroscopy (DLOS) are reviewed, as they are the most often used methods to characterize defects in GaN HEMTs. The applications of DLTS and DLOS to I_{ds} and C_{gd} for GaN HEMTs are then described to assess the location of defects and their impact on devices.

Fundamentals of DLTS and DLOS

This section describes the use of DLTS and DLOS to characterize the electrical and optical properties of deep level defects. Capacitance-mode DLTS (C-DLTS) and capacitance-mode DLOS (C-DLOS) are reviewed first followed, by current-mode DLTS (I-DLTS) and current-mode DLOS (I-DLOS).

C-DLTS

C-DLTS is a well-known technique that is sensitive to thermally stimulated capacitance transients from deep levels as deep as ~ 1 eV from the conduction band edge. Thermally-stimulated transitions of electrons and holes into or out of deep levels located in the depletion region of a semiconductor junction produce capacitance transients. For the simple case of an *n*-type Schottky diode, majority carrier electron emission to the conduction band from a deep level is followed by removal of the free electron from the depletion region by the built-in electric field, as shown in Fig. 2. This process leaves behind a defect that now has a more positive electric charge. The net increase in space-charge in the depletion region is compensated by the incursion of the free electron tail at the edge of the junction. The resultant reduction in the depletion width (d) can be measured as an increase in depletion capacitance. It is important to note that C-DLTS is also applicable to *p-n* junctions and minority-carrier processes; however, only majority-carrier processes in an *n*-type semiconductor will be considered here. It is further noted that from the point of view of the net charge within a region of a semiconductor device and the resulting electrical transients, it can in some cases be difficult to distinguish between emission of one carrier type and capture of the other carrier type (e.g. electron emission vs. hole capture) unless simplifying assumptions are made (e.g. assuming that processes involving holes are negligible); the device structure under consideration and the bias conditions used usually provide reasonable confidence in such assumptions. Additionally, high electric fields such as those that occur in high-voltage HEMTs may influence the relative dominance of emission vs. capture.[6,7]

The electron emission rate from a deep level will influence the characteristic time constant associated with a capacitance transient. Such capacitance transients are readily measurable, so the emission rates of deep levels within a depletion region can be experimentally determined. Relating emission rates to the physical properties of a deep level allows one to characterize deep levels using depletion capacitance methods. From detailed balance considerations and neglecting degeneracy, the thermal electron emission rate of a deep level (e_{th}) can be expressed as

$$e_{th}(T) = \sigma_{th} v_{th} N_C \exp\left(\frac{E_t - E_C}{kT}\right) \qquad (1)$$

where T is the temperature, σ_{th} is the thermal carrier capture cross-section, N_C is the conduction band density of states, E_C is the conduction band energy minimum, and k is the Boltzmann constant.

For the case of a fully occupied acceptor-like deep level in a depletion region at large reverse bias, the space-charge in the depletion region will evolve in time as $q[N_d - n_t(t)]$, where $n_t(t) = N_t \exp(-e_{th}t)$ is the concentration of occupied traps, N_t is the total trap concentration, and N_d is the net concentration of ionized dopants. For $N_t << N_d$ the capacitance can be expressed as

$$\frac{\Delta C(t)}{C_0} = \frac{N_t}{2N_d}\exp(-e_{th}t) \qquad (2)$$

where C_0 is the final (steady-state) value of the capacitance and ΔC is the amplitude of the capacitance transient. This is the basis of depletion capacitance methods for deep level spectroscopy.

Determining the time constant and amplitude of a capacitance transient yields information about E_t and N_t. The DLTS measurement begins with the depletion region under a quiescent reverse bias V_r, and the traps residing therein are assumed to be empty. A fill pulse bias V_f is applied for a time t_f to collapse the depletion region and bring free electrons in proximity of the empty traps; capture ensues. When the fill pulse is removed and the free carriers retract, thermal emission of the trapped electrons produces an exponential capacitance transient with time constant $\tau_{th} = e_{th}^{-1}$, which from Eq. (1) depends on the temperature T and both E_t and σ_t. As T increases, τ_{th} decreases and the DLTS apparatus processes the transient into a signal that peaks at temperature T_{max} when τ_{th} equals a preset value τ_{ref}. Traps with different E_{th} or σ_{th} exhibit different T_{max} for a given τ_{ref}. By using several associated values of τ_{ref} and T_{max}, one constructs an Arrhenius plot of $\ln(\tau_{ref}T_{max}^2)$ *vs*. T_{max}^{-1}, from which E_{th} and σ_{th} are extracted via the slope and y-intercept, respectively. The deep level concentration is calculated by evaluating Eq. (2) at large t. More details regarding the DLTS measurement process and instrumentation can be found elsewhere.[8]

Practical limits on sample temperature as well as transient observation time typically limit DLTS sensitivity to deep levels within ~ 1 eV of a band edge. DLOS must be used to examine deep levels lying deep in the GaN band gap, as discussed next.

C-DLOS

DLOS measures the optical characteristics of a deep level such as the optical ionization energy E_o and Franck-Condon energy d_{FC} from the spectral dependence of the optical cross-section (σ^o), while N_t can be found from Eq. (2) similar to DLTS. The energy E_o is the energy required for an absorbed photon to promote an electron from a deep level to the conduction band for the case when the photoemission process is not assisted by phonons. Since the excitation is now optical rather than thermal, deep level defects as deep as ~ 6 eV below E_c can be observed using a xenon lamp. Again, we restrict discussion of DLOS to the case of an n-type semiconductor.

DLOS is similar to DLTS except now thermal emission rates are assumed to be negligible compared to optical emission rates. Monochromatic illumination is used to excite deep level emission. Rather than scanning T as in DLTS, for DLOS one scans the incident photon energy (hv) by using a monochromator coupled to a broadband light source. The capacitance transient for each value of hv can then be

recorded and analyzed to determine the optical emission rate (e^o) that is defined as σ_o multiplied by the incident photon flux (Φ).

To extract $\sigma_o(h\nu)$, one takes the time derivative of the photocapacitance transients $C(t)$ near $t = 0$, i.e. just at the beginning of the illumination period. Assuming that the sample temperature is low enough or that the occupied deep levels are sufficiently far (> 1 eV) from the band edges, thermal processes can be neglected. It then follows that the deep levels with E_o > 1 eV are fully occupied. In this case, the spectral dependence of σ^o is given by

$$\sigma^o \propto \frac{1}{\Phi}\frac{dC}{dt}\Big|_{t=0}. \quad (3)$$

The σ^o data are then fit to a theoretical model to determine the value of E_o. Many models exist that treat the general case of strong defect-lattice coupling in various ways. One model that is often used is that of Pässler,[9] and this is the model that is used in all of the studies recounted here. More details regarding the DLOS measurement process and associated instrumentation can be found elsewhere.[10]

Applicability of C-DLTS and C-DLOS to HEMTs

C-DLTS can be readily applied to HEMTs using the gate-to-drain Schottky diode. The only caveat is the signal-to-noise ratio of the C-DLTS apparatus. C-DLTS transients are typically less than 10% of the total depletion capacitance. Thus, the gate electrode must have sufficiently large area to produce a ΔC that can be resolved experimentally. This is not typically a problem for power GaN HEMTs due to their large area compared to RF GaN HEMTs.

The applicability of optical spectroscopies to GaN HEMTs should be considered in terms of metal coverage on the surface of the device and the optical transmission of the substrate. Back-side illumination is not ideal because the SiC substrates typical of RF HEMTs absorb in the UV and block any light from exciting defects in the AlGaN; the case is worse for Si substrates typical of power HEMTs, which absorb both visible and UV light, making both GaN and AlGaN inaccessible to back-side illumination. Thus, C-DLOS application to HEMTs typically requires measurements to be performed using front-side illumination. This can be done in one of two ways. Conventional GaN HEMTs use opaque metal gates that will block the incident illumination. Nonetheless, C-DLOS is possible because the gate electrode is typically very thin. Incident light can be scattered at the surface and internally reflected several times in the AlGaN/GaN heterostructure, which affords multiple optical passes below the gate electrode. Additionally, AlGaN/GaN Schottky diodes can be fashioned from the HEMT epitaxy with semi-transparent Schottky contacts on the surface. Semi-transparent Ni contacts can readily be formed on AlGaN, which is very similar to the typical Ni/Au Schottky

contacts used in GaN HEMTs. Thus, C-DLOS measurements performed on AlGaN/GaN heterostructures are directly applicable to HEMTs because they have identical semiconductor structure and similar metal/semiconductor interfacial electronic properties.

An important aspect of both C-DLTS and C-DLOS is that they have innate depth resolution. C-DLTS and C-DLOS only observe defects within the depletion region under the Schottky electrode. For the case of HEMTs, the extent of this depletion region under the gate is given by the usual parallel-plate capacitor approximation $C = A\varepsilon/d$, where A is the junction area and ε is the semiconductor dielectric constant (note that this neglects the quantum capacitance of the 2DEG). The depletion depth increases with more negative gate bias. Thus, the applied bias controls which region of the device under the gate will be probed by C-DLTS or C-DLOS. For example, if the bias applied to the gate is larger (more positive) than V_{th}, the 2DEG is accumulated, and the depletion region is primarily confined to the AlGaN barrier. When the gate bias is much smaller (more negative) than V_{th}, the 2DEG is pinched-off. In this case, the depletion depth is much larger than the AlGaN barrier thickness, so d is primarily constituted by the GaN spacer and buffer layers.

These arguments can be quantified. The relative contribution to the total depletion capacitance from a particular portion of the depletion region is

$$\frac{x_2^2 - x_1^2}{d^2}, \tag{4}$$

where $x = 0$ at the surface and the region of interest is bounded by depths $0 < x_1 < x_2 < d$.[11] When the 2DEG is accumulated, the depletion depth is coincident with the AlGaN/GaN heterointerface where the channel resides, typically ~ 20 nm below the surface. Thus, the AlGaN barrier and GaN channel dominate the depletion capacitance, and C-DLTS and C-DLOS will be primarily sensitive to any defects residing in these regions. Under pinch-off, the depletion depth typically extends several microns below the 2DEG channel. The AlGaN barrier contributes less than 0.01% to the total depletion capacitance, while the GaN spacer and buffer regions contribute the remaining 99.99%. This means that C-DLTS and C-DLOS sensitivity to AlGaN barrier defects is reduced by 10,000× when in pinch-off compared to accumulation. This strong bias dependence of C-DLOS sensitivity can be exploited to discriminate among deep level defects within the AlGaN barrier and GaN channel versus the GaN spacer and GaN buffer.[12]

I-DLTS and I-DLOS

I-DLTS and I-DLOS measurements typically proceed by measuring the emission rate associated with the recovery of I_{ds} with the transistor in the on-state after application of a large positive V_{ds} bias, a large negative V_{gs} bias, or both. Spectro-

scopic analysis of I-DLTS is largely the same as for C-DLTS,[13] and likewise spectroscopic I-DLOS analysis is similar to C-DLOS.[14] The respective deep level defect emission rates can be attained by substituting I_{ds} for C. Deep level parameters E_{th} and σ_{th} or E_o and d_{FC} can then be determined in the same way as described above.

Determining the spatial location of the defects that cause I_{ds} transients is important. Knowing where defects reside in the device helps to understand how they will influence device behavior for a given operating condition. Knowledge of which layer a particular defect resides in enables rational strategies to mitigate or eliminate their influence through optimized crystal growth, device design, and device processing. However, unlike C-DLTS and C-DLOS, neither I-DLTS nor I-DLOS provide inherent spatial sensitivity because I_{ds} is the same everywhere throughout the device.

Nonetheless, the physical location of defects can be ascertained. One method is to use different combinations of V_{gs} and V_{ds} stress conditions to fill defects in different regions of the device, i.e. to use different fill pulse conditions.[14,15,16] Another method is to use different operating bias conditions that are sensitive only to defects in certain regions of the device, i.e. to use different on-state conditions.[17]

Varying the HEMT fill pulse causes electron trapping in different regions of the HEMT. Application of a strongly negative $V_{gs} < V_{th}$ fill pulse can cause electrons to tunnel from the gate electrode and fill defects located under the gate region, in the surface access region between the gate and the drain, or both.[15,16] Application of a strongly positive V_{ds} bias along with a strongly negative V_{gs} bias emphasizes access region trapping due to enhanced electron tunneling in the direction of the drain. On the other hand, application of strongly positive V_{ds} with $V_{gs} > V_{th}$ causes hot electrons to scatter out of the channel and become trapped primarily in the AlGaN barrier or GaN buffer layers between the gate and the drain.[2,14,16] Therefore, defect states that are evident only for application of fill pulses with the channel pinched off (strongly negative V_{gs}) are likely to be related to the surface in the access region, while defect states that are evident only for application of fill pulses with the channel open ($V_{gs} \sim 0$ V) are likely to be related to the AlGaN barrier or GaN buffer. These concepts are summarized in Fig. 3.

Recently, I-DLTS and I-DLOS with lateral spatial resolution have been developed to differentiate deep levels under the gate from those located in the access region of HEMTs.[17] I-DLTS and I-DLOS are primarily sensitive to defects located in the access region when the device is biased to produce low mutual transconductance (g_m) and high output conductance (g_o), such as when operating in the triode regime with V_{gs} that is large relative to V_{th} and V_{ds}. In this case, I-DLTS and I-DLOS analyses are greatly simplified by operating under the condition of constant I_{ds}. If I_{ds} and V_{gs} are held fixed, the drain voltage of the intrinsic HEMT is constant. The change in gate-to-drain resistance $\Delta R_{gd}(t)$ due to defect emission in the access region is then measured as the change $\Delta V_{ds}(t)$ required to maintain constant I_{ds}. Then, R_{gd} (or V_{ds}) takes the place of I_{ds} when determining deep level emission rates, and the areal defect density (D_t) in the access region is calculated as[17]

$$D_t = \left(\frac{n_s^2}{n_s - \frac{L'}{qW\mu(-\Delta R_{gd})}} \right) \quad (5)$$

where n_s is the 2DEG sheet density, W is the gate width, μ is the channel mobility, and L' is the physical length of the virtual gate extension.

Conversely, I-DLTS and I-DLOS are primarily sensitive to deep levels located under the gate when bias conditions produce a large g_m and a small g_o, such as in saturation mode.[17] In saturation, the influence of defects in the active region on I_{ds} is negligible. Changes in R_{dg} do not impact I_{ds} because the output resistance is already very large. If I_{ds} and V_{ds} are held fixed, the shift in threshold voltage $\Delta V_{th}(t)$ due to deep level defect emission under the gate is equal to the change in gate voltage $\Delta V_{gs}(t)$ required to maintain constant drain current. Now, V_{th} (or V_{gs}) takes the place of I_{ds} when determining deep level emission rates, and D_t under the gate is calculated as

$$D_t = \frac{2\varepsilon \Delta V_{th}}{qd} \quad (6)$$

where the defects are assumed to be located in the AlGaN barrier.

Maintaining constant I_{ds} by dynamic feedback control of V_{ds} or V_{gs} can require sophisticated circuitry. For this reason, it may prove more convenient to investigate defects under the gate using C-DLOS and C-DLTS rather than establishing feedback control of V_{ds} or V_{gs} for I-DLTS and I-DLOS under constant-I_{ds} conditions.

Application of DLTS and DLOS to GaN HEMTs

This section reviews multiple studies applying C-DLTS, C-DLOS, I-DLTS, and I-DLOS to GaN HEMTs. Confident assignment of deep level defects to various regions of the device using DLTS and DLOS is demonstrated. DLTS and DLOS measurements of GaN HEMTs with different gate metals and surface passivation processes confirm that defects in different locations can be selectively probed as a function of fill pulse conditions.[15,16] Comparison of DLOS measurements of GaN HEMTs and GaN thin films demonstrates the ability of C-DLOS to differentiate between AlGaN barrier- and GaN buffer-related defects.[12,18] C-DLOS and I-DLOS measurements of the same GaN HEMTs also show that defects in the GaN buffer can influence V_{th} and R_{on} by trapping under the gate and trapping in the access region.[18] The lateral spatial selectivity of constant-I_{ds} mode I-DLTS and I-DLOS is also substantiated.[17]

Using fill pulses to spatially locate traps

A direct way to establish that different filling pulses can selectively prime defects either under the gate or in the access region of GaN HEMTs is to compare the C-DLTS of HEMTs with different gate electrodes and surface passivation layers. Such a study was conducted for GaN HEMTs and indeed validated the utility of fill pulses to distinguish defects in different regions of the device.[15]

In the study, three sets of HEMTs were fabricated.[15] Set A had devices with ITO gates and silicon nitride passivation, with V_{th} ~ -1.5 V. Set B had devices with Ni/Au gates and silicon nitride passivation, with V_{th} ~ 0 V. Set C had Ni/Au gates and no surface passivation, with V_{th} ~ -0.5 V.

C-DLTS analysis of devices from Set A using a (V_{gs} = -4 V < V_{th}, V_{ds} = 10 V) fill pulse revealed a defect state with activation energy of 0.63 eV. Based on the discussion above, a deep level observed with such a fill pulse is likely to exist either under the gate or at the passivation/surface interface in the access region. Fig. 4 shows pulsed I_{ds}-V_{gs} data for Set A using three different fill pulses. The (V_{gs} = 0 V, V_{ds} = 0 V) quiescent pulse was used as a control to produce minimal defect trapping. The (V_{gs} = -4 V, V_{ds} = 0 V) fill pulse was used to emphasize defect filling under the gate, and the (V_{gs} = -4 V, V_{ds} = 10 V) pulse was used to emphasize defect filling in the access region. The large shift in V_{th} indicates definitive trapping under the gate. However, increasing V_{ds} during the fill pulse did not change R_{gd} (i.e. dI_{ds}/dV_{gs}), suggesting that the 0.63 eV deep level is not related to access region traps. This conclusion was validated by analysis of Set B, where only the gate contact was different from the devices in Set A. Set B exhibited no significant trapping, providing conclusive evidence that the 0.63 eV deep level is due to trapping under the gate and is not related to surface states in the access region.

C-DLTS measurements of devices from Set C found a trap state with an activation energy of 0.099 eV using a (V_{gs} = -4 V < V_{th}, V_{ds} = 10 V) fill pulse. Again, the corresponding defect could be attributed to either a surface state or a defect under the gate based on the fill pulse used. Fig. 5 shows pulsed I_{ds}-V_{gs} data for Set C using the same three fill pulses as used for Set A listed above. No shift in V_{th} was observed for Set C, which suggests that the 0.099 eV trap is not located under the gate. However, a large change in R_{gd} was evident that increased with increasing V_{ds} bias. This behavior points to a surface-state-related defect in the active region. To corroborate this ascription, comparison was again made with Set B, which shared the same gate processing but included surface passivation compared to the bare surface in Set C. As noted above, Set B did not suffer any significant trapping effects, which validates the conclusion that the defect giving rise to the 0.099 eV trap state is located at the surface in the access region. Analysis of the thermal dependence of I_{ds} transients resulting from the (V_{gs} = -4 V, V_{ds} = 10 V) fill pulse revealed a defect state with a small activation energy of 0.099 eV but with unusually long time constants of ~ 100 ms. It was found that e_{th} for the 0.099 eV defect had an exponential dependence of $1/T^3$ typical of conduction hopping along a surface rather than a $1/T$ dependence that is expected for defects in a homogene-

ous crystal matrix. This finding further supports the attribution of deep levels to surface defects when using a fill pulse with $V_{gs} < V_{th}$ and strongly positive V_{ds}.

Prior studies have established that the spatial location of defects can also be determined using on-state fill pulses.[2,3,14,16] Early work in GaN HEMTs[2,19] reported a severe increase in R_{on} when applying a large V_{ds} bias with $V_{gs} > V_{th}$ and the channel accumulated. The lack of significant gate stress using on-state fill pulses discounts the role of gate leakage in filling defects located under the gate or surface states in the access region. In these studies, the channel was presumed to be the source of trapped electrons. The lateral location of the responsible defects was therefore likely between the gate and the drain because this is the lateral region where carriers are sufficiently accelerated to escape the channel. The vertical location of the defects was considered to be the adjacent AlGaN barrier or GaN buffer.

Comparison of DLOS of GaN HEMTs[2] and GaN MESFETs confirmed that carbon doping in the GaN buffer was indeed responsible for the large increase in R_{on}. The current collapse was characteristic of phenomena reported for GaN MESFETs that required hours for I_{ds} recovery at room temp,[20] indicating the need for optical spectroscopy to fully characterize the responsible defect states. Fig. 6 shows the I-DLOS spectra of GaN HEMT and MESFET devices subject to current collapse.[14] I-DLOS spectra of the HEMT devices are qualitatively similar to that of the MESFET, providing strong evidence that the two primary deep levels indeed exist in the GaN layer. Carbon-related defects were suspected as the microscopic origin of the 2.85 eV level because the I-DLOS spectra were similar to previous photoluminescence excitation results reported for GaN:C[21] and calculated defect density was found to track linearly with carbon impurity concentration.

It should be noted that defects located under the gate region can also exist under the access region. Thus, the same defects can appear in both off-state and on-state fill pulse stress and can impact both V_{th} and R_{gd}. Such defect activity has been reported using a combination of C-DLOS and I-DLOS applied to an AlGaN/GaN HEMT with a GaN:C buffer that exhibited both V_{th} and R_{gd} variations due to defect trapping.[18] Fig. 7 shows C-DLOS spectra taken on HEMTs using the gate electrode,[18] which found the same 1.8 eV and 2.85 eV deep levels reported by Klein *et al*. previously.[2,3,14] Shifts in V_{th} due to these defect levels were measured by capacitance-voltage sweeps while sub-bandgap illumination was used to excite the deep levels optically, as shown in Fig. 8. This confirmed that carbon-related defects in the GaN buffer impact V_{th} as well as R_{on}. Fig. 7 also shows I-DLOS measurements of the same device biased in the triode region to be sensitive only to trapping in the access region. Both gate stress ($V_{gs} < V_{th}$, $V_{ds} = 20$ V) and drain stress ($V_{gs} > V_{th}$, $V_{ds} = 20$ V) produced identical I-DLOS spectra that were also very similar to the C-DLOS spectrum. The conclusions from these data are that defects under the gate can also exist between the gate and the drain (in the GaN buffer in this case) and can impact R_{on}.

Using measurement bias to spatially locate traps

The electrical bias used to facilitate C-DLOS or I-DLOS measurements can also determine the vertical location of defects in HEMTs. Fig. 9 shows an example of bias-dependent C-DLOS performed on an AlGaN/GaN heterostructure that was formed from the same epitaxial structure as a fully-processed HEMT. The heterostructure and HEMT contained a semi-insulating Fe-doped GaN buffer.[12] The spectral features of the C-DLOS measurements show a strong bias dependence. This is expected based on the discussion above. At 0 V, the 2DEG is accumulated, so C-DLOS is primarily sensitive to both the AlGaN barrier and the GaN channel. At -3.6 V bias the 2DEG is depleted, so C-DLOS is primarily sensitive to the underlying GaN:Fe buffer layer. Therefore, defects that appear only in the 0 V C-DLOS spectrum can be ascribed to the AlGaN barrier, while defects only appearing at -3.6 V spectrum can be attributed to the GaN:Fe layer, and defects appearing in both C-DLOS spectra are common to the GaN buffer and GaN channel regions.

C-DLOS sensitivity to the AlGaN barrier at 0 V is confirmed by spectral features above the band gap energy of GaN. The C-DLOS spectrum at 0 V evidences saturation at 4 eV due to AlGaN band-edge absorption, and the 3.85 eV defect level is also necessarily related to the AlGaN barrier. This is definitive evidence that C-DLOS has requisite depth resolution to probe nanoscopic layers embedded in heterostructures and to distinguish nanoscopic layers from microns of surrounding material. The 2.00 eV defect level is also AlGaN-related due to its singular appearance at 0 V. Conversely, the 2.42 eV deep level only appears at -3.6 V, so it can be confidently ascribed to the GaN:Fe buffer layer in the HEMT. The 2.64 eV and 3.30 eV levels are common to both C-DLOS spectra, so the corresponding defects are located in the GaN channel and the GaN buffer layers. It is worth noting that defect levels appear at an energy near 3.3 eV in Figs. 6, 7, and 9. Given that these DLOS spectra were taken on samples grown independently, these data indicate that the ~ 3.3 eV defect level is quite common in GaN. Based on extensive study, the 3.3 eV defect level is most likely related to a carbon impurity.[18,22]

Layer spatial resolution has also been demonstrated using I-DLTS and I-DLOS.[17,23,24] Fig. 10 shows I-DLOS measurements of an AlGaN/GaN HEMT. The measurements were performed under a saturated bias condition, and the V_{gs}, (equivalently V_{th}) variation was measured in the constant-I_{ds} regime to be exclusively sensitive to defects below the gate electrode.[23] To validate exclusive gate-region sensitivity, measurements were performed on an AlGaN/GaN HEMT that was not passivated. Significant trapping by surface states in the access region is expected due to the lack of passivation. Fill pulse conditions of (V_{gs} = -8 V, V_{ds} = 5 V) or (V_{gs} = -8 V, V_{ds} = 10 V) were used to fill surface states. Only the deep level occupancy in the access region is expected to vary for these fill pules because only V_{ds} was changed. Any I-DLOS sensitivity to deep levels arising from surface states could then be recognized because their magnitude in the I-DLOS spectra should be enhanced by the fill pulse with the larger V_{ds}. As expected, the

I-DLOS spectra do not show significant increase in magnitude for the two fill pulses. Indeed, the fill pulse with the larger V_{ds} indicated a slightly reduced density of defects. The small differences in the I-DLOS spectra were attributed to variations in the source-to-drain resistance. This finding validates the exclusive sensitivity of I-DLOS to defects located under the gate when the measurement is performed in saturation mode.

I-DLOS measurements of the same AlGaN/GaN HEMT were also performed in the triode operating condition to probe surface states in the access region, as shown in Fig. 11. In this implementation of constant-I_{ds} I-DLOS, V_{gs} was fixed and ΔV_{ds} was measured to monitor changes in R_{gd} due to defect emission. A fill pulse of (V_{gs} = -8 V, V_{ds} = 10 V) was again used to fill surface defects. Significant ΔV_{ds} was measured, indicating the existence of surface states. Comparison of Figs. 10 and 11 substantiates the sensitivity of I-DLOS to access region defects when performed in the triode regime. The typical 3.3 eV defect level evident in the I-DLOS spectra in Fig. 10 (which measures defects only under the gate) is absent from the I-DLOS spectrum in Fig. 11(which focuses on the AlGaN surface in the access region). As discussed above, the 3.3 eV defect level is commonly observed in GaN, so its absence in Fig. 11 corroborates the measurement's primary sensitivity to the AlGaN barrier. Thus, I-DLOS measurements performed in the triode region are demonstrated to have primary sensitivity to defects located in the access region.

Additional methods to measure spatially localized traps

Drain current transient techniques may also be combined with physical characterization methods such as surface potential measurements to further refine the ability to determine where charge is trapped within the HEMT. One study of high-voltage HEMTs that correlated Kelvin force microscopy with slow drain current transients following electrical stress in the pinch-off state concluded that the thickness of the AlGaN barrier and the associated magnitude of the electric field near the gate edge largely determined where in the device charge was trapped; factors such as surface passivation and buffer doping were found to be of secondary importance in these devices.[25] Fig. 12 shows the correlated drain current transient and surface potential measurements for a device with a thick (50 nm) AlGaN barrier, a carbon-doped buffer, and Al_2O_3-based surface passivation (Device A). Despite the surface passivation and the carbon-associated deep levels in the bulk GaN, this device shows a large change in surface potential with time, indicative of significant charge trapping during stress. In contrast, a device with a thinner (20 nm) barrier, no buffer doping, and no surface passivation (Device B) showed much less change in surface potential. This unexpected result was explained by the thicker barrier in Device A, which resulted in a lower electric field near the gate edge and less tendency to inject electrons deep into the device.

Finally, it is noted that in order to achieve normally-off operation, many power HEMTs utilize a recessed gate to make V_{th} more positive; such devices often uti-

lize gate dielectrics to limit gate leakage current.[7] Thus, charge trapping may occur both within the dielectric and at the dielectric-semiconductor interface for such MIS structures, and variations of the techniques described herein are applicable to the characterization of such structures. For example, constant-capacitance (CC) DLTS and DLOS have been utilized to determine interface state density in Al_2O_3/GaN MIS capacitors.[26] In this technique, the voltage across the MIS structure is adjusted such that the capacitance remains constant during the emission transient,[27] analogous to constant-current DLTS/DLOS in HEMTs.

Conclusion

Optical and electrical characterization techniques such as DLTS and DLOS are powerful and effective methods that may be used to ascertain both the nature and spatial location of traps within AlGaN/GaN HEMTs for both RF and high-voltage power switching applications. Due to its reliance on thermal emission from deep level states, DLTS is most useful for shallow traps less than ~ 1 eV from the band edges. Conversely, owing to the optically-stimulated emission inherent to DLOS, it is most useful for deeper states and thus finds great utility in the (Al)GaN materials system. Further, differentiation between thermal and optical energies may be ascertained, and defect-related parameters such as the Franck-Condon energy associated with lattice relaxation may be determined. While originally developed to characterize capacitance transients for simple one-dimensional structures such as Schottky and *pn* diodes, DLTS/DLOS of HEMTs has spurred the development of a much broader range of measurement techniques owing to the ability to utilize both capacitance and current transients for time constant characterization. Further, the ability to sample various spatial regions within the device due to the availability of both the gate and the drain to set the bias condition affords yet more flexibility. Thus, both vertical and lateral spatial discrimination of deep levels may be achieved, allowing one to identify whether defects reside within the GaN buffer/channel region, the AlGaN barrier, or at the surface of the device. While of high interest from the fundamental physics point of view, characterization of deep levels is also of great practical importance given that such defects influence many aspects of the performance of RF and power switching HEMTs, such as dispersion, current collapse, and dynamic on-resistance; additionally, very deep levels with long time constants may impact the DC parametrics of the device. Thus, deep level characterization techniques such as DLTS and DLOS are likely to remain vital to the robustness of III-N HEMTs in the coming years, and further refinements and enhancements of these methods are sure to be developed.

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FIGURE 1

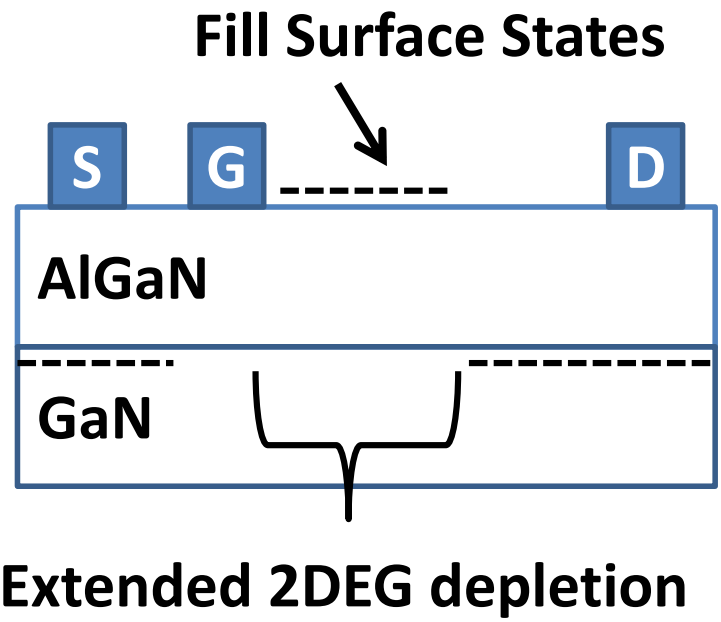

Fig. 1. Electron leakage from the gate electrode fills surface states. The excess negative charge on the AlGaN surface in between the gate and drain depletes the underlying 2DEG. The charged surface states are referred to as a "virtual gate."

FIGURE 2

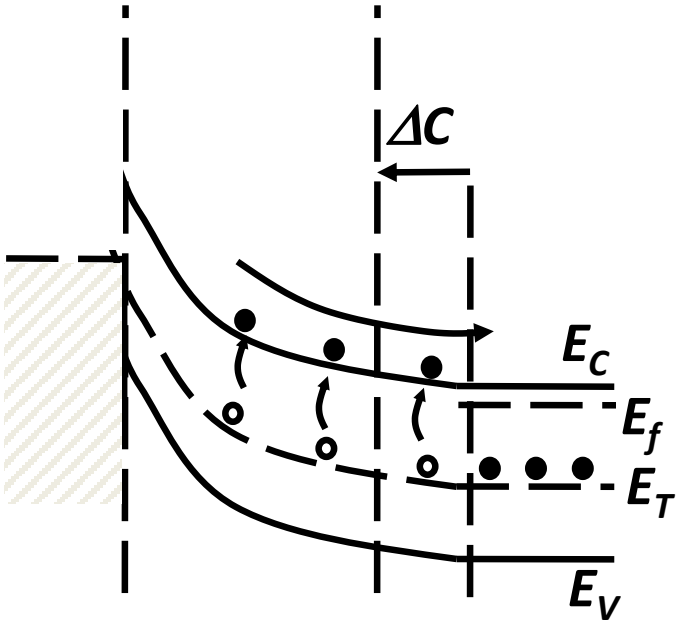

Fig. 2. Electron emission from defects in a depletion region. The electrons are swept out of the depletion region, leaving behind a fixed positive charge on the defects. This increase in space-charge causes the depletion region to contract, which is measured as an increase in the junction capacitance.

FIGURE 3

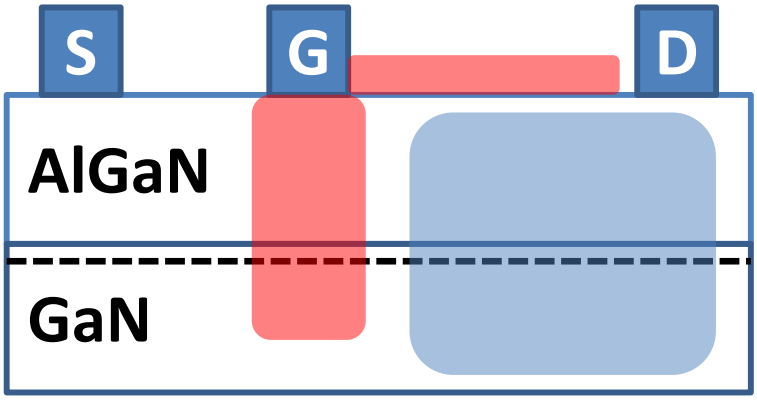

Fig. 3. Regions where defects are filled with electrons for various fill pulse conditions. The red boxes correlate to fill pulses with ($V_{gs} < V_{th}$, $V_{ds} \geq 0$ V), and the blue box correlates to fill pulses with ($V_{gs} > V_{th}$, large V_{ds}).

FIGURE 4

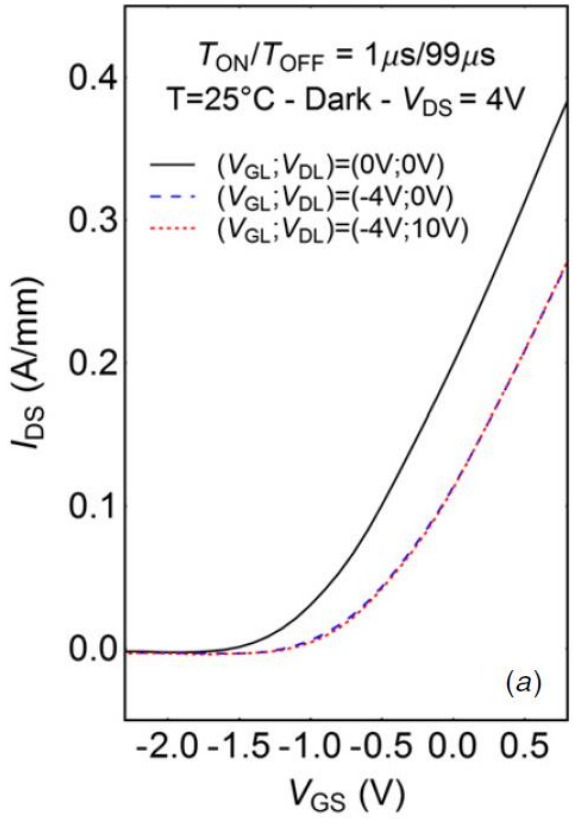

Fig. 4. Pulsed I_{ds}-V_{gs} data for an AlGaN/GaN HEMTs with an ITO gate and silicon nitride surface passivation (Set A from text). Note that the response to the V_{gs} = - 4 V fill pulse is invariant to V_{ds}, suggesting that the defects causing reduced I_{ds} are located under the gate and are not located in the access region. From Ref. 15.

FIGURE 5

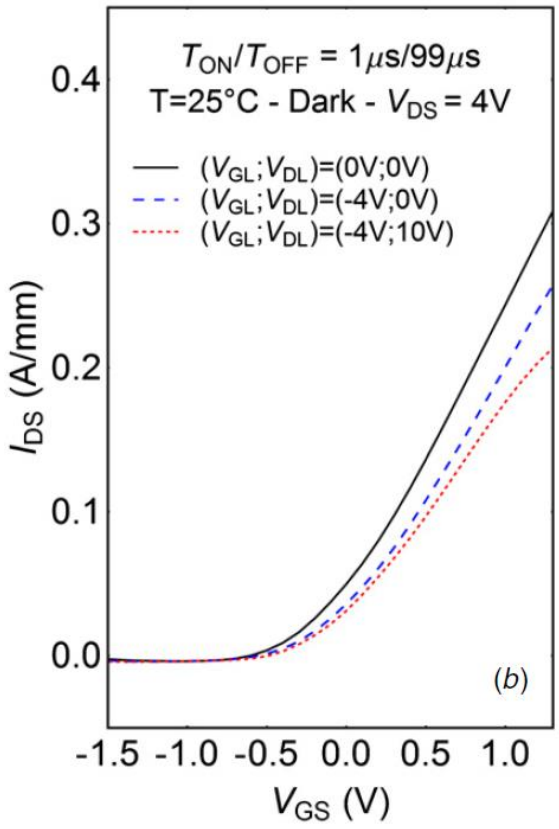

Fig. 5. Pulsed I_{ds}-V_{gs} data for an AlGaN/GaN HEMTs with a Ni/Au gate and without surface passivation (Set C from text). Note that the response to the V_{gs} = - 4 V fill pulse depends strongly on V_{ds}, suggesting that the defects causing reduced I_{ds} are located in the access region and not under the gate. From Ref. 15.

FIGURE 6

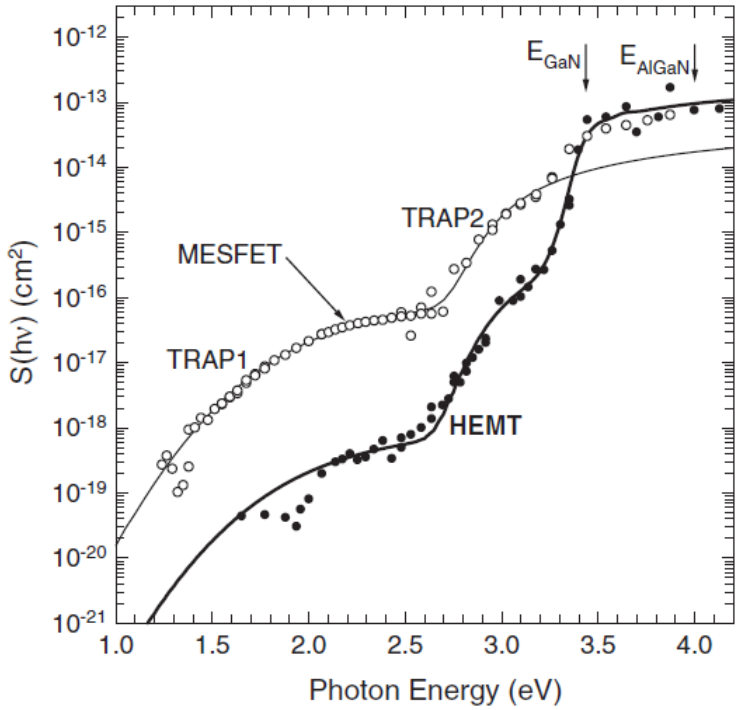

Fig. 6. I-DLOS spectra of a GaN HEMT and a GaN MESFET. The similar deep level spectra indicate similar defects in both devices; these were attributed to the carbon-doped GaN buffer in each. From Ref. 14.

FIGURE 7

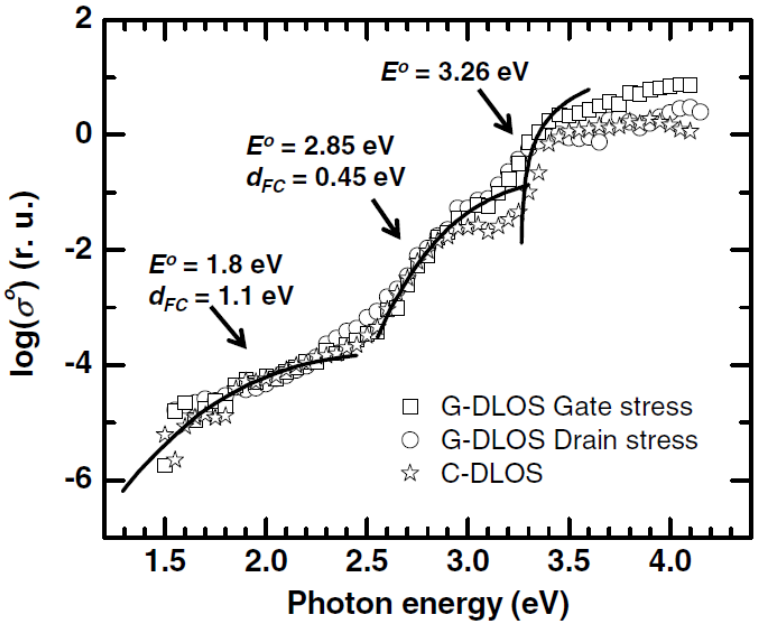

Fig. 7. C-DLOS and I-DLOS (marked as G-GLOS, where the G for conductivity is analogous to the I for current) spectra of a GaN HEMT. The C-DLOS spectrum is sensitive only to defects under the gate, while the I-DLOS spectra are sensitive only to defects in the access region. The similarity of the DLOS spectra show that defects under the gate can also exist in the access region. From Ref. 18.

FIGURE 8

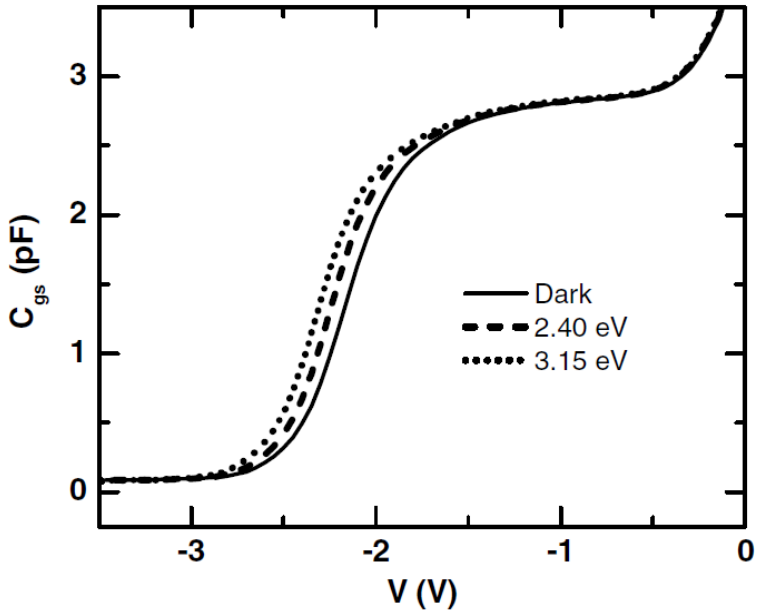

Fig. 8. Capacitance-voltage measurements of an AlGaN/GaN HEMT in the dark and under illumination. The lateral shifts in the curves with illumination indicate that the defects observed in Fig. 7 influence V_{th}. From Ref. 18.

FIGURE 9

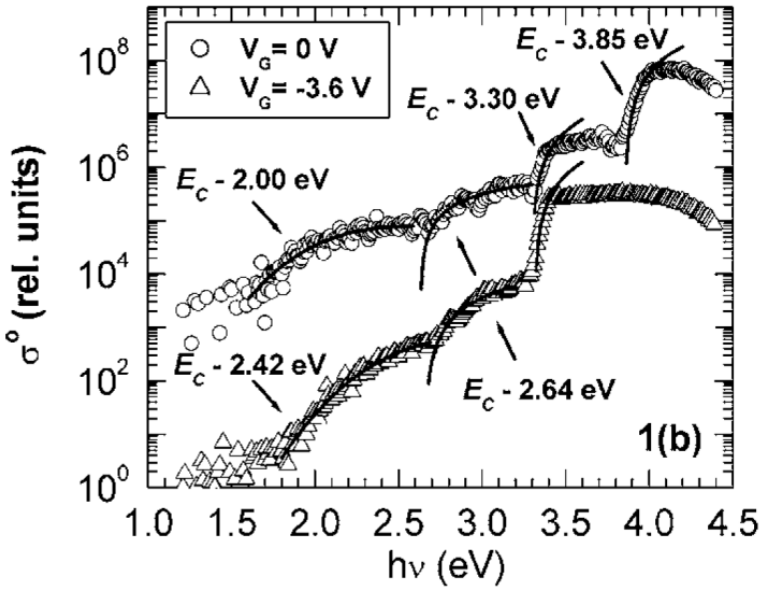

Fig. 9. C-DLOS spectra of an AlGaN/GaN heterostructure. The bias dependence of the spectra demonstrates the depth-sensitivity of C-DLOS. The 3.85 eV deep level and the 4.0 eV AlGaN band edge confirm C-DLOS sensitivity to the AlGaN barrier at zero gate bias. Conversely, the absence of AlGaN features at reverse bias confirms exclusive sensitivity to the GaN buffer. From Ref. 12.

FIGURE 10

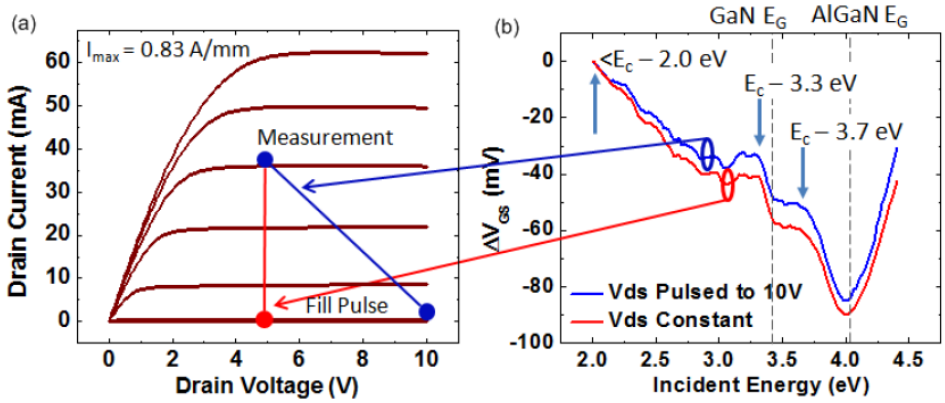

Fig. 10. I-DLOS of an AlGaN/GaN HEMT without surface passivation. I-DLOS was performed with the device in saturation to probe defects under the gate. The weak dependence of I-DLOS to V_{ds} for fill pulses with $V_{gs} < V_{th}$ indicates that defects in the access region do not contribute to the deep level spectra when the device is biased in saturation. From Ref. 23.

FIGURE 11

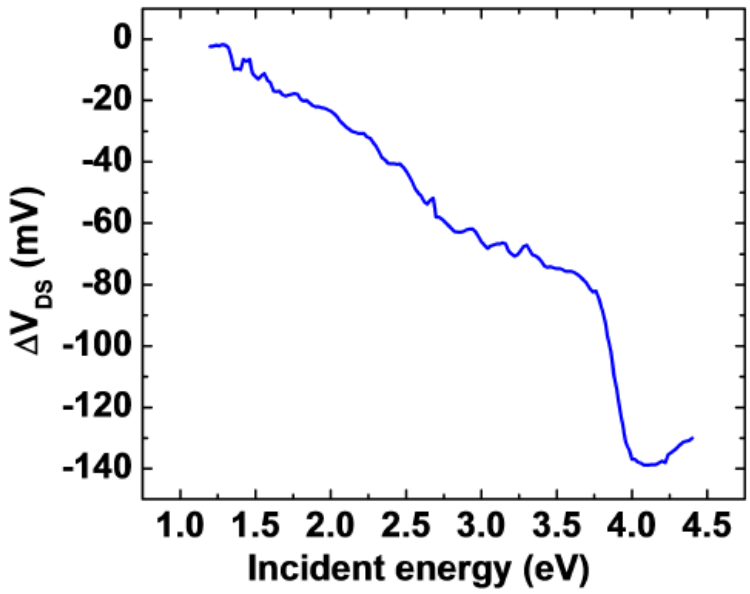

Fig. 11. I-DLOS measurement of an AlGaN/GaN HEMT without passivation. The I-DLOS was performed in the triode regime to enable sensitivity to defects in the access region. From Ref. 23.

FIGURE 12

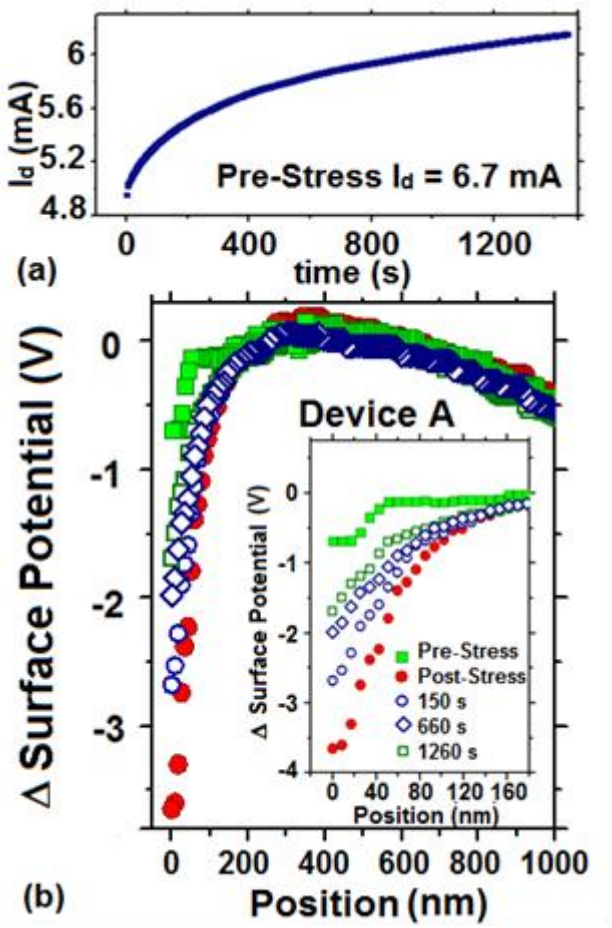

Fig. 12. I_{ds} **transient following (**V_{gs} **= -9 V,** V_{ds} **= 0 V) stress in an AlGaN/GaN HEMT with a 50 nm AlGaN barrier, a carbon-doped GaN buffer, and** Al_2O_3**-based surface passivation (this device was termed "Device A" in the study), and associated surface potential measurement. Position is measured from the drain side of the gate edge. The large change in surface potential near the gate edge is indicative of surface trapping. From Ref. 25.**

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