I Electric Drive Technologies

I.1 Electric Drive Technologies Research

I.1.1 Power Electronics: Vertical GaN Device Development (Sandia National Laboratories)

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Project Introduction

This project is part of a multi-lab consortium that leverages U.S. research expertise and facilities at national labs and universities to significantly advance electric drive power density and reliability, while simultaneously reducing cost. The final objective of the consortium is to develop a 100 kW traction drive system that achieves 33 kW/L, has an operational life of 300,000 miles, and a cost of less than $6/kW. One element of the system is a 100 kW inverter with a power density of 100 kW/L and a cost of $2.7/kW. New materials such as wide-bandgap semiconductors, soft magnetic materials, and ceramic dielectrics, integrated using multi-objective co-optimization design techniques, will be utilized to achieve these program goals. This project focuses on a subset of the power electronics work within the consortium, specifically the design, fabrication, and evaluation of vertical GaN power devices suitable for automotive applications.

Objectives

Gallium Nitride (GaN) is a promising wide-bandgap (WBG) semiconductor material that could enable higher-performance power electronic devices than traditional Silicon (Si) or even its WBG counterpart, Silicon Carbide (SiC). This is based on the increased critical electric field of GaN, which would enable lower-resistance devices with the same hold-off voltage as devices fabricated from the other materials. This is a key performance metric for power devices. While laterally-oriented, High Electron Mobility Transistors (HEMTs) based on AlGaN and GaN materials are common in high-frequency applications and are being established in lower-voltage power switching applications (approximately 600 V and below). However, with the emerging commercial maturation efforts for GaN substrates using various methods, traditional vertically-oriented device structures (such as are common in Si and SiC) can now be realized in GaN, with several promising demonstrations of high-voltage PN diodes and vertical transistors appearing in the literature[1], [2], [3]. While GaN PN diodes may be of interest, the ~3 V turn-on voltage, determined mainly by the bandgap of the material, discourages their use in some power-switching circuits due to the loss of power conversion efficiency resulting from this high turn-on voltage. Instead, more promising candidates for these power conversion systems, including automotive inverters, are GaN Schottky barrier diodes (SBDs) and Junction Barrier Schottky (JBS) diodes, shown in Figure I.1.1.1 (top), which have turn on voltages of ~1 V as determined by the Schottky barrier height of the metal to the semiconductor material, rather than the semiconductor bandgap.

Similarly, vertically-oriented GaN transistors promise high-performance power electronic devices if several key growth and fabrication challenges are overcome for the GaN material system. Interestingly, several different types of vertical GaN transistors have been demonstrated including Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) in the trench configuration (T-MOSFET, shown in the bottom portion of Figure I.1.1), the double-well (D-MOSFET) configuration, and the Current Aperture Vertical Electron Transistor (CAVET) configuration [4], [5], [6]. Each of these device topologies has benefits and challenges associated with fabrication and performance, but the MOSFET designs show the most promise for power switching applications and will be investigated during this effort. With the MOSFET device designs, challenges exist in making the semiconductor/insulator (or oxide) interface due to the lack of a good native oxide for GaN (Si and SiC both have native oxides). In addition, selective-area doping control, which is needed to form lateral PN junctions, cannot be easily achieved in GaN. Current state-of-the-art GaN devices use techniques such as ion implantation with special anneal processes (high-pressure and high-temperature) [7] or epitaxial regrowth [8] to realize selective-area doping control. Both techniques are relatively immature in GaN, and their behavior needs to be studied and techniques need to be developed to control these processes for eventual use in power systems for electric vehicles.

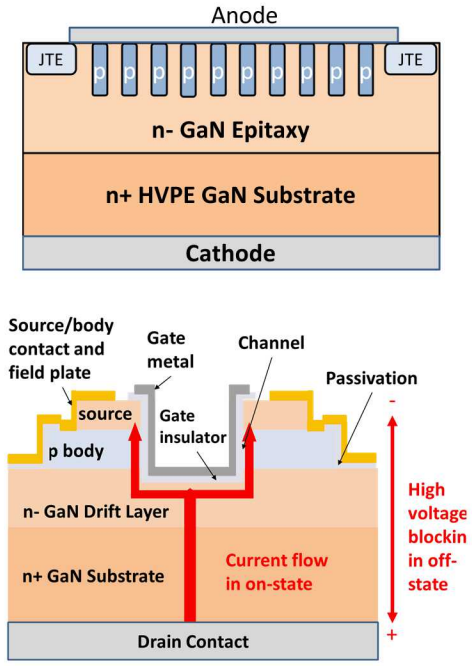

Figure I.1.1.1. (top) Schematic drawing of JBS diode. (bottom) Schematic drawing of Trench MOSFET.

The first year of this effort focused on the development of simulation and modeling capabilities to help drive the designs of future GaN diodes and transistors. In parallel, epitaxial growth and fabrication processes were initiated toward realizing and demonstrating these devices. Once devices of sufficient performance are achieved, these will be further characterized in a performance and reliability test-bed (created under a different project within the consortium) to evaluate their suitability for electric drive applications, especially regarding their ability to meet the DOE consortium targets. Also, with increasing maturity, the devices can be shared with the consortium partners, who will evaluate them in electric drive systems and provide feedback to us for further improvement in their performance for power electronics.

Approach

Vertical GaN Diodes

To understand the designs for development of the vertical GaN diodes, Technology Computer-Assisted Design (TCAD) models were co-developed at Sandia National Laboratories and Lehigh University (subcontract to Professor Jon Wierer) using the Silvaco software suite. The first efforts focused on simulations of the Schottky barrier diodes in forward and reverse bias operating modes while using various models for leakage currents available in Silvaco. Figure I.1.1.2 shows the simulated reverse-bias current-voltage behavior of a GaN SBD with different models being used in the TCAD simulation. These included the thermionic emission, thermionic emission with barrier lowering, universal Schottky tunneling, and phonon-assisted tunneling models. GaN material was grown using Sandia's Metal-Organic Chemical Vapor Deposition (MOCVD) facilities and SBDs were fabricated and tested using a simple shadow-mask process where metal is deposited onto the surface of the GaN through a perforated metal mask to form circular devices. With the fabrication and testing of these simple GaN SBDs during the first year, these models were evaluated based on their ability to match experimental results and were optimized to allow predictive behavior of the diodes. This iterative process will be continued in future

modeling and simulation efforts to drive realistic simulation capabilities to help with future, more complicated device designs.

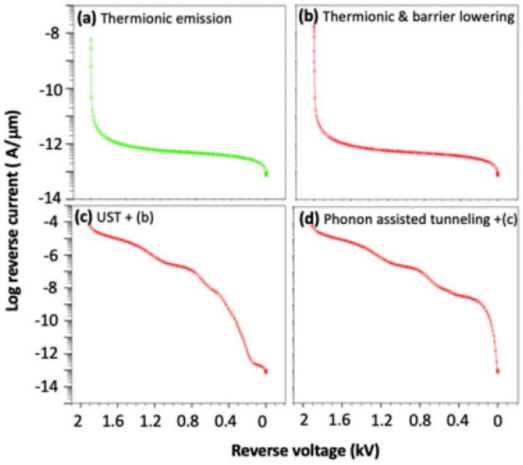

Figure I.1.1.2. Simulated reverse-bias curves of GaN Schottky diodes using various tranpsort models (courtesy of Lehigh University).

With the successful modeling of SBDs and previous work in GaN PN junctions, Junction Barrier Schottky (JBS) diode models were also developed during the first year. The JBS diode is a hybrid between a SBD and PN junction diode that combines the best of both, namely high breakdown voltage and low forward turn-on. To drive design optimization of the fabrication efforts for future JBS diodes, a systematic study of the JBS parameter space was conducted to evaluate different device designs. The parameters analyzed included the width of the n-GaN and p-GaN layers, the Mg-doping level of the p-GaN layer, and the thickness of the p-GaN layer. To optimize the design, simulated device performance parameters including the breakdown voltage, the forward specific on resistance, and the Baliga Figure of Merit (BFOM) which is equal to the breakdown voltage squared divided by the specific on-resistance, were used to evaluate the different designs and to gauge the parameter space best for future fabrication efforts.

To begin to develop the vertical GaN diodes, work was performed in material synthesis using Sandia MOCVD GaN growth capabilities, coupled with device fabrication process development to assemble the tools necessary to fabricate these devices. For the material synthesis portion, thick n-type GaN layers were grown on commercially available GaN substrates, and the net carrier concentration was measured using capacitance-voltage techniques to optimize the processes for the designed values. Using these grown structures, SBDs were fabricated using standard lithographic patterning, etching, and metallization processes, and were subsequently characterized to understand their performance. With the development of the JBS designs, photolithographic mask sets were designed and fabricated for the first generation of the JBS diode effort. Fabrication short loops were begun to develop the fabrication processes needed to realize the JBS devices. These included investigations of contact lithography and etch processes to form the small patterns in the JBS device area.

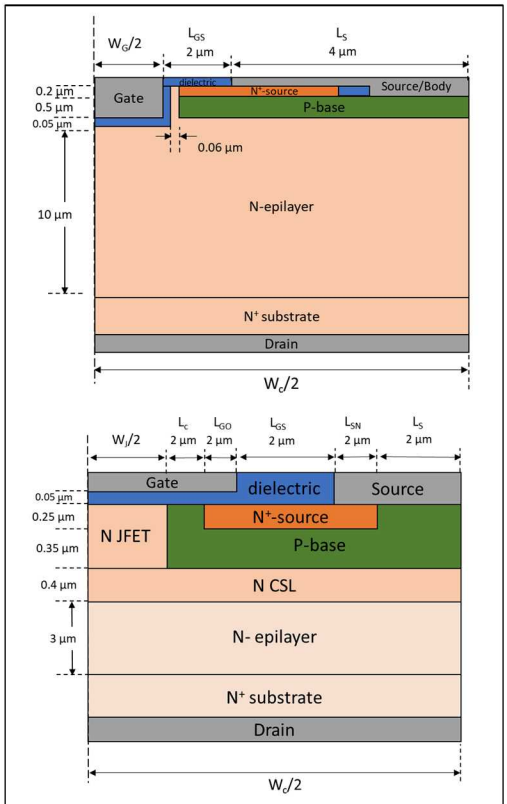

Figure I.1.1.3. Schematic drawings of (top) trench MOSFET and (bottom) double-well MOSFET.

Vertical GaN Transistors

Due to the increased complexity of the vertical GaN transistors, the work in the first year was primarily focused on the simulation of two candidate device structures, and work was also started to develop and understand the dielectric/semiconductor interface that is critical to the gate control of the devices. Cross-sectional diagrams of the two types of MOSFETS are shown with the T-MOSFET at the top and the D-MOSFET at the bottom of Figure

I.1.1.3. Using TCAD simulations, the sensitivity of the device performance to various parameters was investigated to understand the performance trade-offs of the different devices and to look for possible limitations in the theoretical device performance imposed by material growth and device fabrication challenges. Based on the results of the simulations, it was clear that both device architectures are viable for automotive drivetrain applications, and we continue to investigate both during the fabrication process development. This is not surprising since both device architectures are commercially produced using SiC, with no obvious advantage to either choice at this time.

To begin the development of the transistors, investigation of the dielectric/semiconductor interface was studied to develop and optimize this process using Atomic Layer Deposition (ALD) of Silicon Dioxide (SiO_2) as a starting point. GaN wafers were grown, similar to those used for GaN SBDs, and various surface treatments were investigated before deposition of the ALD SiO_2 film. Next circular metal contacts were deposited on the ALD films to form MOS capacitor structures. These MOS capacitors were characterized using current-voltage, and variable frequency capacitance-voltage techniques to evaluate and understand the interface trap density between the dielectric and semiconductor layer, which will eventually limit the performance of the transistors.

Results

Vertical GaN Diodes

To evaluate the GaN SBD simulations that were developed, actual devices were fabricated to compare their performance to predicted results. Initially, simple shadow-masked devices were made by depositing a Pd Schottky contact through a perforated metal screen to form circular devices. While this method can help to give understanding of device performance, it will not allow for more complicated device structures to be made that would eventually be needed to yield devices for electric drive systems. More complicated devices would include thick wire-bond pads, surface passivation, device identifier numbers, and other features to enable large-scale parallel processing, characterization, singulation, and packaging for insertion into circuits. To realize GaN SBDs using these more traditional methods was not straightforward due to the effects of GaN surfaces on device performance. Inherently, SBDs are sensitive to surfaces, and care must be maintained to develop a robust and stable process. Eventually, we were able to realize photolithographically-defined GaN SBDs using a blanket metal layer with a pattern-and-etch used to define the metal. Using this process, we were able to realize high-performance GaN SBDs with highly uniform results for devices of 250 µm diameter. The forward IV curves for representative devices are shown in Figure I.1.1.4 (top) along with the extracted ideality factors for these devices (bottom). These devices show ideality factors of 1.05 to 1.10, which is good for state of the art GaN SBDs (the ideality factor is a measure of the quality of the diode, with a value of 1.00 being ideal).

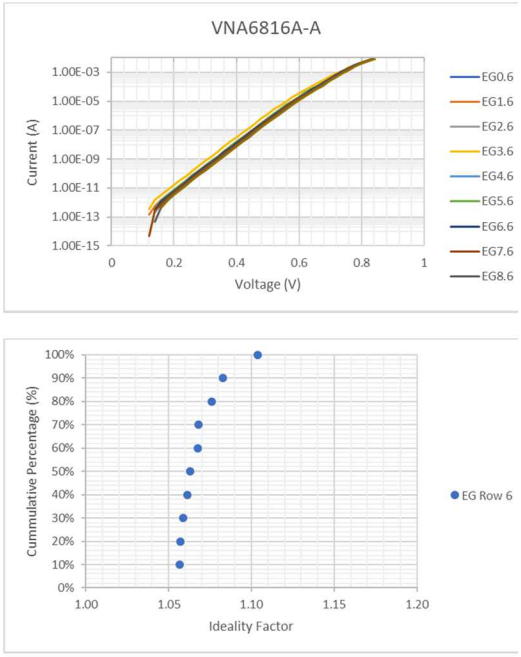

Figure I.1.1.1. (top) IV curves of GaN Schottby Barrier Diodes, and (bottom) extracted ideality factors of the same diodes.

Using the empirical results from the GaN SBD work, simulations for the JBS diodes were performed as described above. For the parameters swept in the simulation work, Table 1 defines the variables. The n-GaN drift layer for the device was kept constant at a thickness of 10 µm with a net carrier concentration of 2×10^{16} cm^{-3}. From these simulations, charts were constructed for analyzing various performance parameters by color-coding the performance metric on a 2-dimensional plot with two of the parameters swept in the simulations. For each colored dot, a forward and reverse IV curve have been simulated and the performance metric extracted to represent the color. The scale for the color is along the side of the plot as shown in Figure I.1.1.5. The analysis showed that the performance was highly sensitive to the widths of the p-GaN and n-GaN as expected. Other parameters such as the p-GaN doping level and p-GaN thickness also had effects. The BFOM was chosen as the operating parameter because it includes both forward and reverse performance metrics, and the desired outcome was to have as large a parameter space as possible for the p-GaN and n-GaN widths to allow for process variations in the growth and fabrication of the diodes. A Mg doping level for the p-GaN layers of 1×10^{18} cm^{-3} was chosen for several reasons, including empirical results with good device performance for GaN PN diodes.

Table I

Parameter	Variation in Simulation
p-GaN thickness (T_p) (µm)	0-2, spaced by 0.5 µm
p-GaN trench width (W_p) (µm)	0-5, spaced by 0.5 µm
p-GaN Mg doping concentration (cm^{-3})	10^{17} - 10^{19}
n-GaN trench width (W_n) (µm)	0-5, spaced by 0.5 µm

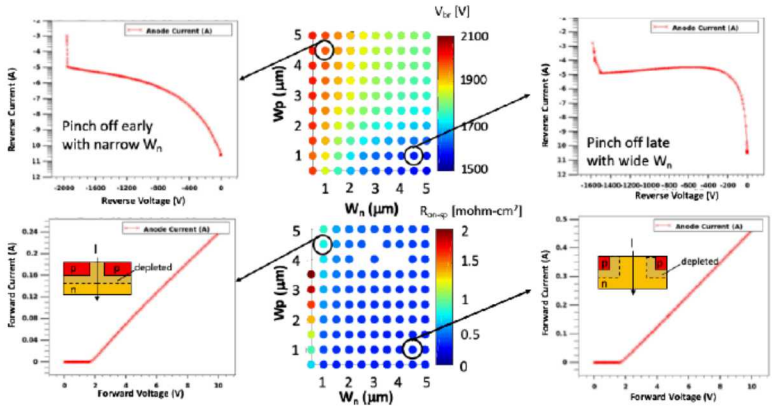

Figure I.1.1.2. (top row) Simlulated breakdown voltage and (bottom row) on-resistance of GaN JBS diodes. Left column is a design with a narrow current-carrying channel, while right colum is a design with a wide current-carrying channel. The middle column represents the device performance.

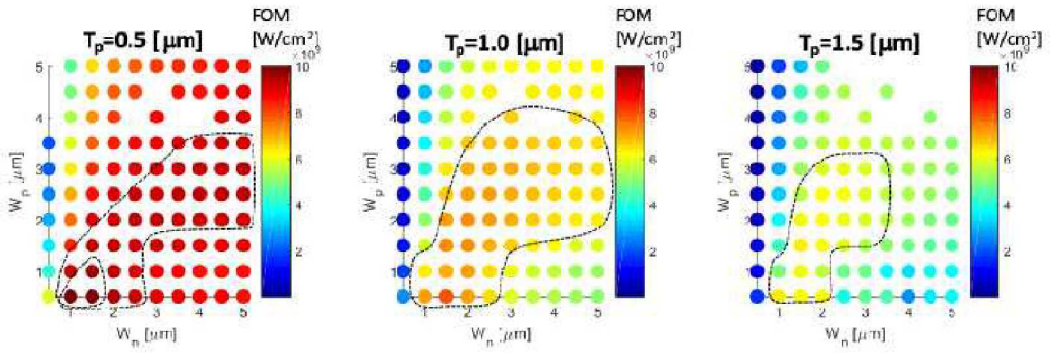

Figure I.1.1.6. Simulated Baliga Figure of Merit for JBS diodes with three different p-layer widths.

Doping levels higher than this reduce the parameter space over which good simulated results are obtained, and doping levels lower than this pose some risk for device operation. Figure I.1.1.6 shows the color plots for the BFOM plotted as a function of p-GaN and n-GaN trench width for three different p-GaN layer thicknesses at a Mg doping level of 1×10^{18} cm^{-3} The results indicate that there is potentially a wide set of p-GaN and n-GaN widths that can give good BFOM results, with a thickness of 0.5 µm giving the best BFOM values (these are encircled by the dashed lines). These data were used to bound the designs of the mask sets to fabricate the JBS diodes, and these masks have been made. Experiments are underway to develop the processes (growth and fabrication) needed to realize these designs. In addition, design methodologies and fabricated device results for SiC devices were obtained through the subcontract with Jim Cooper (Sonrisa) to allow us to further refine the design space for the GaN devices.

Vertical GaN Transistors

As mentioned previously, TCAD simulations were used to investigate the performance of the T-MOSFET and D-MOSFET devices. To limit the simulation space, a gate dielectric composed of Silicon Nitride (SiN_x) was chosen, and the forward and reverse bias performance of the transistors was simulated to examine changes in parameters such as layer thickness and doping. Performance metrics including breakdown voltage, forward specific on-resistance, and the BFOM were evaluated as they were in the diode simulations to find the optimal designs. Figure I.1.1.7 shows the optimization information for the D-MOSFET analyzing four parameters: JFET region width (area under the gate), epilayer (drift layer) doping, current spreading layer (CSL) doping, and JFET region doping. To bound the simulations, a p-GaN (source) layer doping of 1 x 10^{18} cm^{-3} and a source layer doping of 5 x 10^{18} cm^{-3} were chosen. The blue lines represent the simulated breakdown voltage as determined by either the breakdown of the GaN or the peak field in the gate dielectric reaching 4 MV/cm (a known limit to reliability for SiC devices). The black lines represent the forward specific on resistance, and the red lines represent the BFOM for the devices. Using the BFOM as the design optimization parameter, the ideal GaN D-MOSFET would have a JFET width less than or equal to 1 µm, a JFET doping level of 5×10^{17} cm^{-3} (n-type), an epilayer (drift layer) doping level of ~1-1.5$\times10^{16}$ cm^{-3}, and a CSL doping levels of 1-2$\times10^{17}$ cm^{-3}, all of which are achievable using our GaN MOCVD capability. Based on these simulations, the D-MOSFET looks like a promising candidate for a vertical GaN transistor for an automotive drivetrain, and process development is underway to realize this device.

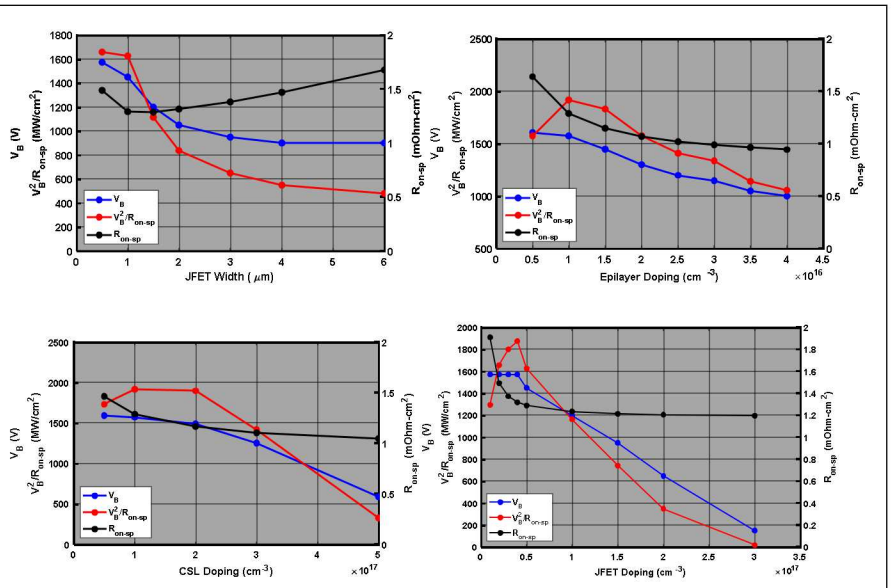

Figure I.1.1.7. TCAD simulations of D-MOSFETS, examine four design parameters: (top left) JFET region width, epilayer (drift layer) doping (top right), current spreading layer doping (bottom left), and JFET region doping (bottom right).

Additionally, T-MOSFETs were simulated and show promise for vertical GaN transistors. A set of similar simulations was performed to investigate the forward and reverse bias performance of the device as well as the internal electric fields within the device, which might limit performance. For a device with the cross-section as defined in the top portion of Figure I.1.1.8, the reverse-bias operation was simulated and the resulting internal electric field profile (middle) and IV performance (bottom) are shown. The inputs for the simulation are: source doping of 5×10^{18} cm^{-3}, base doping of 1×10^{19} cm^{-3}, epilayer doping of 1×10^{16} cm^{-3}, p^+ trench doping of 3×10^{19} cm^{-3}, buffer layer doping of 5×10^{18} cm^{-3}, and CSL doping of 3×10^{16} cm^{-3}. The peak electric field occurs near the corner of the trench area and has a value of 7 MV/cm, resulting in a breakdown voltage for the device of over 1.7 kV. The peak electric field in the gate dielectric layer is 2.6 MV/cm which is below the threshold of concern for device reliability. The same device was simulated in forward-bias operation and showed good performance with a threshold voltage of 2.1 V, a specific on-resistance value < 1 mΩ-cm^2, and a maximum drain current of nearly 0.5 A/mm. These results are similar to the simulated D-MOSFET performance.

Because of the good performance of both types of MOSFETs, a down-select to one of the topologies does not make sense at this time. Instead, both structures are being considered for additional evaluation by looking at other constraints, including thermally-induced degradation in performance using additional thermo-electric simulations and growth and/or fabrication concerns that might limit the performance of a realistic device. To evaluate the growth and fabrication limitations to device realization, a series of short experiments is planned to demonstrate and evaluate the process capability needed. After further consideration, one of the structures will be selected on which to focus the resources of a single device development effort.

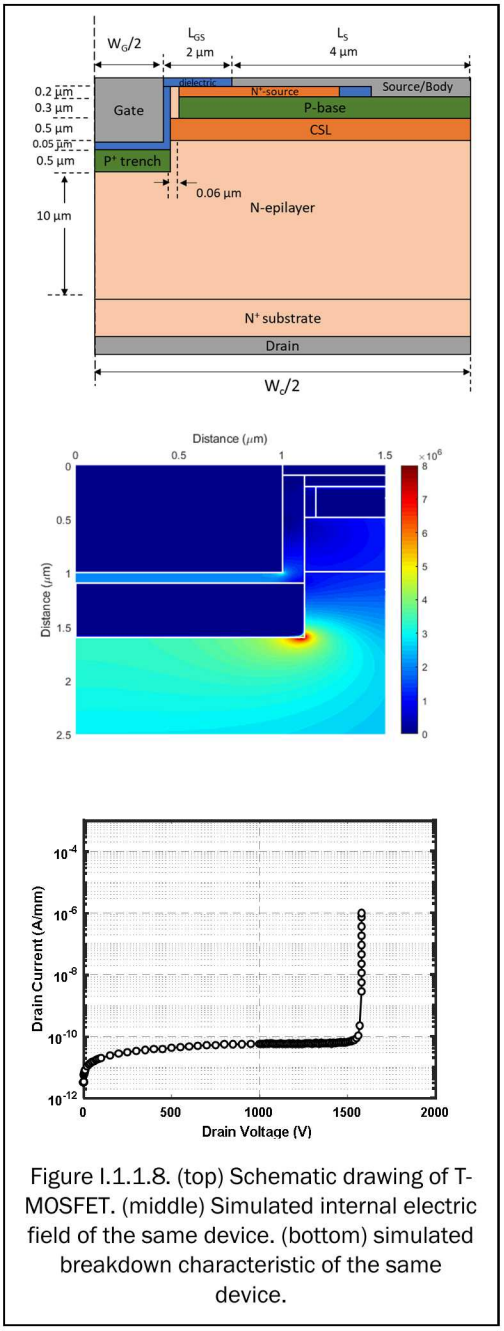

Figure I.1.1.8. (top) Schematic drawing of T-MOSFET. (middle) Simulated internal electric field of the same device. (bottom) simulated breakdown characteristic of the same device.

Conclusions

GaN offers the promise of power electronic devices with performance that exceeds conventional Si and even SiC-based devices. This is due to its advantageous material properties, chiefly its higher breakdown electric field. Due to the increased maturity of GaN substrates, vertical GaN devices showing promising performance are being demonstrated and are being considered for insertion into power conversion applications This project has focused on the design, simulation, and fabrication processes needed to build vertical GaN diodes and transistors for use in electric drive traction systems. GaN SBDs have been simulated, and simple devices have been fabricated to help improve predictive ability of the models. GaN SBDs with excellent ideality factors of 1.05 were characterized and are indicative of the high quality of the metal/semiconductor junction using with our fabrication processes. JBS diodes were then simulated using the SBD models and existing PN diode models as input to develop a design optimization for future fabrication of these devices. Using the outcome of the simulations, experiments have begun to further develop the growth and fabrication processes necessary for realization of these devices. For GaN transistors, a careful simulation study was done to understand the performance comparison between T-MOSFETs and D-MOSFETs. Based on these

results, both device topologies look promising for future automotive applications and are being considered as potential candidates for the traction drive system. Future work will focus on demonstrating and characterizing prototypes of GaN JBS diodes and demonstrating gate control on GaN MOSFETs. The characterization of the first prototypes will help provide feedback into the design efforts to continually improve the devices.

Key Publications

1. L. Yates, A. Binder, J. Dickerson, G. Pickrell, and R. Kaplar, “Electro-thermal Simulation and Performance Comparison of 1.2 kV, 10 A Vertical GaN MOSFETs,” Rio Grande Symposium on Advanced Materials, Albuquerque, NM (September 2019).

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II Electric Drive Technologies

II.1 Electric Drive Technologies Research

I.1.2 Power Electronics: Active Device and Passive Component Evaluation (Sandia National Laboratories)

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Project Introduction

This project is part of a multi-lab consortium that leverages U.S. research expertise and facilities at national labs and universities to significantly advance electric drive power density and reliability, while simultaneously reducing cost. The final objective of the consortium is to develop a 100 kW traction drive system that achieves 33 kW/L, has an operational life of 300,000 miles, and a cost of less than $6/kW. One element of the system is a 100 kW inverter with a power density of 100 kW/L and a cost of $2.7/kW. New materials such as wide-bandgap semiconductors, soft magnetic materials, and ceramic dielectrics, integrated using multi-objective co-optimization design techniques, will be utilized to achieve these program goals. This project focuses on a subset of the power electronics work within the consortium, specifically the evaluation of wide-bandgap power semiconductor devices (primarily SiC) as well as passive elements (primarily ceramic capacitors).

Objectives

Silicon Carbide (SiC) is a wide-bandgap (WBG) semiconductor that has matured to the point where power electronic devices are now commercially available. However, it remains to be seen whether such devices can be used to construct a power converter (inverter) that meets the consortium's goals for performance and reliability. As such, in collaboration with consortium partners (other national labs as well as universities), this project is focused on the performance and reliability evaluation of these devices. Additionally, the passive elements within power electronic converters must be concurrently developed and evaluated to ensure that the performance promised by SiC can be realized in a real converter, and this project addresses that need as well. Note that another WBG semiconductor, Gallium Nitride (GaN), is addressed under a different project under the consortium. Similarly, magnetic materials, which are likewise critical to the performance of WBG-based power converters as well as electric motors, are addressed under a different project. Details regarding SiC device and capacitor testing, as well as the test circuit developed to perform this work, are described below.

SiC Testing

WBG semiconductors will be necessary to achieve the performance targets of the inverter, and the most mature WBG semiconductor (SiC) will be used extensively the near future to achieve advances in electric drive technology. In conjunction with university partners, state-of-the-art SiC devices (switches and diodes) will be evaluated. Further, a strong focus will be placed on design for reliability, which to date has often been traded for high performance and low cost. While the latter two attributes are necessary for automotive applications, reliability is also of paramount importance. Thus, designs that meet all three criteria specific to the traction drive

inverter of interest will be created, and devices based on these designs will be fabricated. In conjunction with NREL and ORNL, these devices will then be incorporated into power modules featuring advanced thermal management and minimized electrical parasitics to meet the performance goals of the program.

Capacitor Testing

Passive components (inductors and capacitors) are also of high importance to the overall consortium metrics. Ceramic dielectric capacitors are preferred because of their high energy density and reliability. However, achieving high performance and long lifetime at elevated temperatures has proven elusive for ceramic dielectrics. Instead of addressing this deficiency through alterations in material composition (which have not yet proven fruitful), an innovative bipolar switching strategy to periodically clear a build-up of oxygen vacancies at electrode surfaces has been implemented. This allows for ceramic dielectrics to exhibit long lifetime at high temperature. The dynamics of this strategy will be explored and optimized through the design and fabrication of a large-scale testbed for capacitor degradation evaluation.

WBG Device Test Circuit

In order to evaluate fabricated devices within the consortium (including the SiC active devices and ceramic capacitors described herein, and also GaN devices and inductors), Sandia has designed an advanced component test-bed that reproduces the functionality of an end-use vehicle inverter that is consistent with the consortium's targets. This allows for analysis of device performance and reliability under realistic scenarios. Once fabricated devices ae available, the realistic evaluation of the operation of devices in the test-bed will be used by device designers to identify performance or reliability issues before incorporation into a high-power, high-density consortium exemplar inverter. Additionally, the test-bed provides validation opportunities for the development of realistic device models under varied usage scenarios for incorporation into system topology optimization.

Approach

SiC Testing

Sandia has been consulting with consortium university partners (primarily OSU and SUNY) and providing feedback on device designs and testing. Design criteria have focused on field-shaping within SiC devices through the design of the junction termination extension (JTE), as well as evaluating current commercial SiC devices for reliability. Pending the completion of the test circuit and receipt of devices from the university partners, evaluation of SiC devices will be carried out in the testbed.

Capacitor Testing

In order to reduce costs, ceramic capacitors are typically fabricated using base-metal electrodes such as Ni [1]. During the fabrication process, these require a reducing environment during sintering to avoid oxidation. An unintended side-effect of this reducing environment is that oxygen vacancies are created in the ceramic material [2]. As with any charged species, these vacancies will migrate under an applied voltage and preferentially collect at the electrode/dielectric interface (see Figure Figure I.1.1.). This gettering of defects results in a loss of insulation resistance and an increase in the DC leakage of the capacitor, which negatively affects the performance of the power electronics [3]. Furthermore, this leakage will increase operational temperature, resulting in quicker diffusion of vacancies. This process is a positive feedback loop that leads to an accelerating failure mechanism.

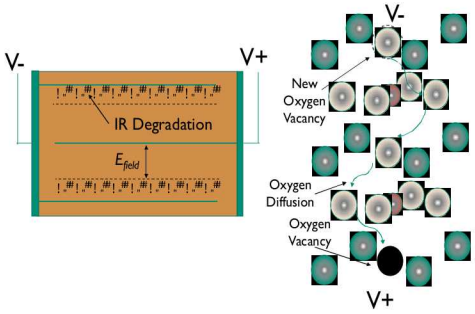

Figure I.1.2.3 Oxygen vacancy migration under applied bias can lead to degradation of ceramic capacitors.

The conventional wisdom for increasing capacitor reliability is to alter the fabrication process or materials properties of the capacitor. This is a long, complicated process that requires significant cost and effort to achieve. Instead of altering the capacitor properties, we are investigating the ability to heal capacitors periodically via

reverse biasing. This reverse biasing should allow for re-distribution of oxygen vacancies to lengthen the lifetime of the component. To evaluate this mechanism, we propose a method of altering the typical DC-field highly accelerated lifetime tests on the capacitor to an AC field variety. This reversing electric field can limit the transport of oxygen vacancies.

Test Circuit

Fabrication of new laboratory-scale devices can be beset with many reliability and performance challenges that are not present in commercialized devices. In order to move forward to a next generation of prototype device, it is necessary to understand its strengths and weaknesses in an appropriate end-use testbed. This testbed must deliver realistic stresses on the device that it will see in field use, but at a lower stress level than would be experienced in the field. By having realistic usage data available to device designers and fabricators, the process of developing a device can be accelerated and weaknesses of past devices can be addressed quickly in future generations (Figure Figure I.1.1.).

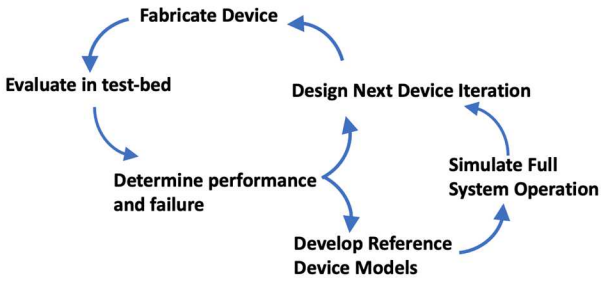

Figure I.1.2.4. The evaluation of prototype devices in a custom testbed can inform both device designers on the strengths/weaknesses of their prototypes, as well as validate device models for simulation.

In order to evaluate fabricated devices in the consortium, SNL is developing a scaled motor drive test-bed that can be tailored to prototype devices (both in voltage and current stress delivered) while still applying realistic end-use stress profiles that the device will see when mature. In order to carry this out, a 3-phase DC motor drive was designed (Figure Figure I.1.1.3). This design is split into two sections, a control section and a power stage section. The control section applies a realistic PWM profile to the device using an embedded microcontroller specifically for motor drive applications. The three-phase power stage contains a single stage that is daughter-carded. This daughter card can be quickly removed and replaced with a card containing new device types. By daughter-carding the entire stage, parasitic inductance is kept commensurate with the other two stages to minimize asymmetric operation and get a better view of the device performance.

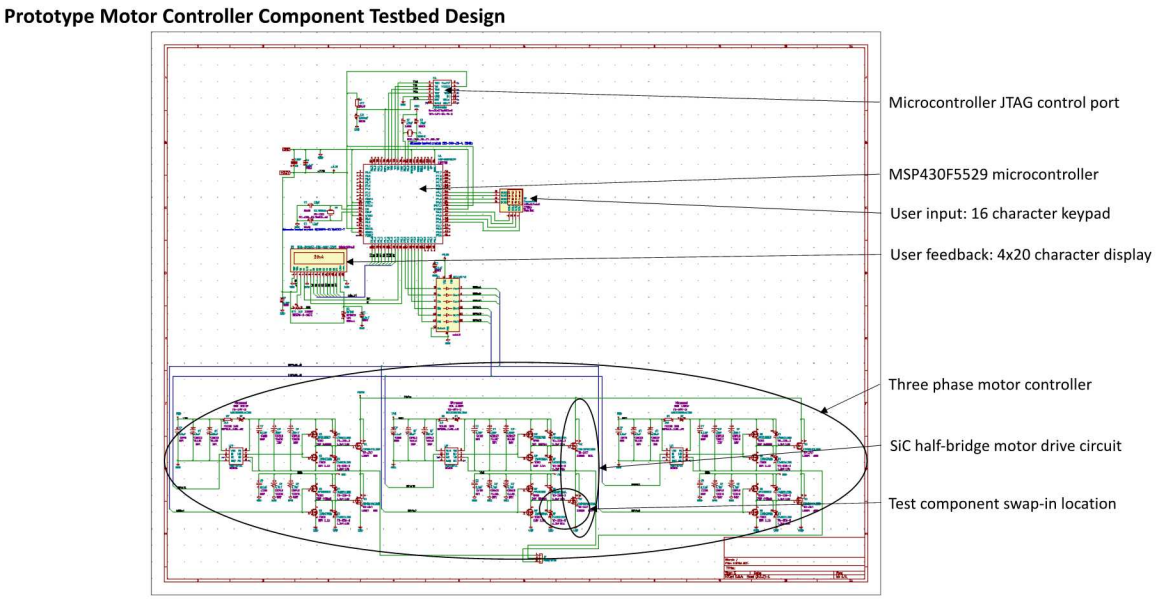

Figure I.1.2.5. Schematic for WBG device testbed with embedded motor control.

Results

SiC Testing

As discussed above, testing of SiC power devices is awaiting the receipt of consortium-fabricated devices as well as the completion of the motor-drive testbed.

Capacitor Testing

SNL carried out preliminary bipolar switching testing on commercially available X7R capacitors. A DC bias of 10x the rated voltage was applied at a temperature 125°C above the rated temperature. These voltage and temperature levels are characteristic of highly-accelerated DC life tests for capacitors. The leakage current of the devices was monitored at DC bias (no switching) and bipolar operation with switching frequencies of 0.1 and 2.5 Hz. These preliminary results (subset shown in Figure I.1.1.4) show that bipolar switching can result in significantly increased time-to-failure for ceramic capacitors. The 2.5 Hz bipolar switching scheme (blue trace) demonstrated a ~4x lifetime increase compared to the DC voltage stress (black trace).

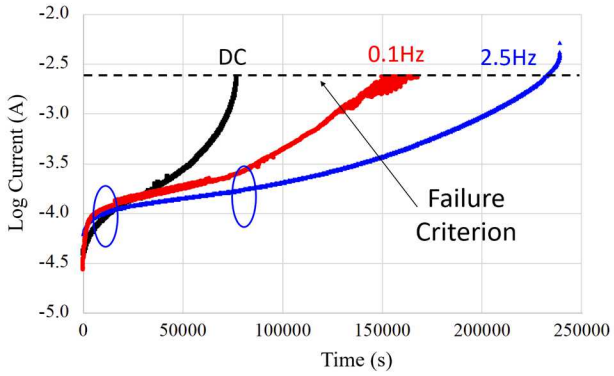

Figure I.1.2.6. The lifetime of DC capacitors can be increased through the implementation of a bipolar switching scheme.

While this initial testing shows promise, further work is needed both to elucidate the exact mechanisms for this bipolar switching and evaluate if the effect is large enough for real-world practical application. The necessary frequency of healing procedures should decrease significantly at less accelerated conditions. Larger sample sets are required to both obtain Weibull statistics and, simultaneously, explore changes in MTTF within a wide temp/field/frequency space. To accomplish this, a test setup with more flexibility for application of stress (both voltage and temperature) and large sample population is needed. SNL has been in the process of designing this second-generation test setup for bipolar capacitor switching (Figure Figure I.1.1.5).

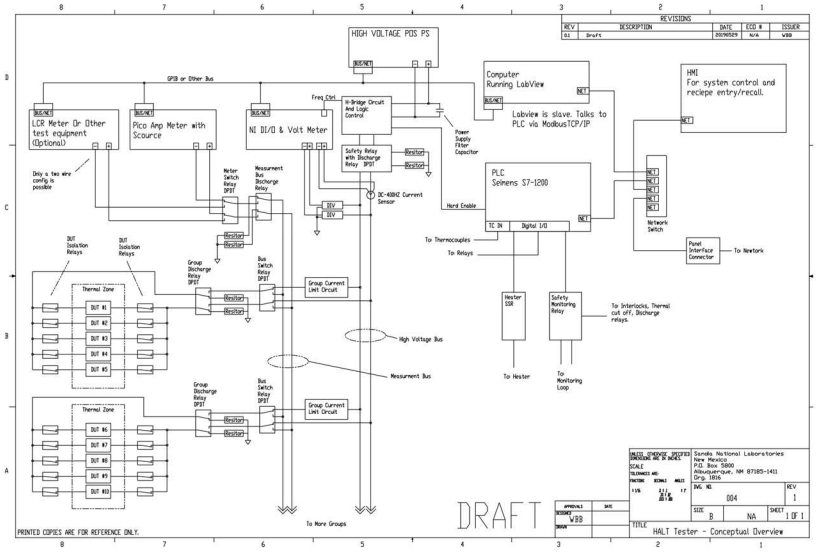

Figure I.1.2.7. Design layout for capacitor test setup which allows for stress and evaluation of a population of 40 capacitors under bipolar switching.

This test setup will be able to carry out a stress-and-measure protocol for a population of 40 capacitors. The system is divided into two buses, one for stressing and one for measurement. Each of the DUTs are divided into 5-10 groups and one group may be measured while the rest can be stressed. Failed DUTs will be detected by a combination of voltage/current monitoring and power supply compliance monitoring. Upon a DUT failure, the

DUT will be identified during the measurement sequence, then isolated. All cycle times between stress and measure are user-controllable with a maximum temperature of 300ºC (with 25ºC/min ramp rate) and a voltage stress of 600 V (2.6 A/1.5 kW).

The design review of this test setup has been completed and fabrication and procurement of the bill of materials is underway.

Test Circuit

The motor drive test circuit has been fabricated on a breadboard to ensure correct functionality before the PCB design files are sent to a fabrication house. Figure Figure I.1.1. shows the as-fabricated power stage board and daughter-card (left) as well as the embedded motor control with user input (right).

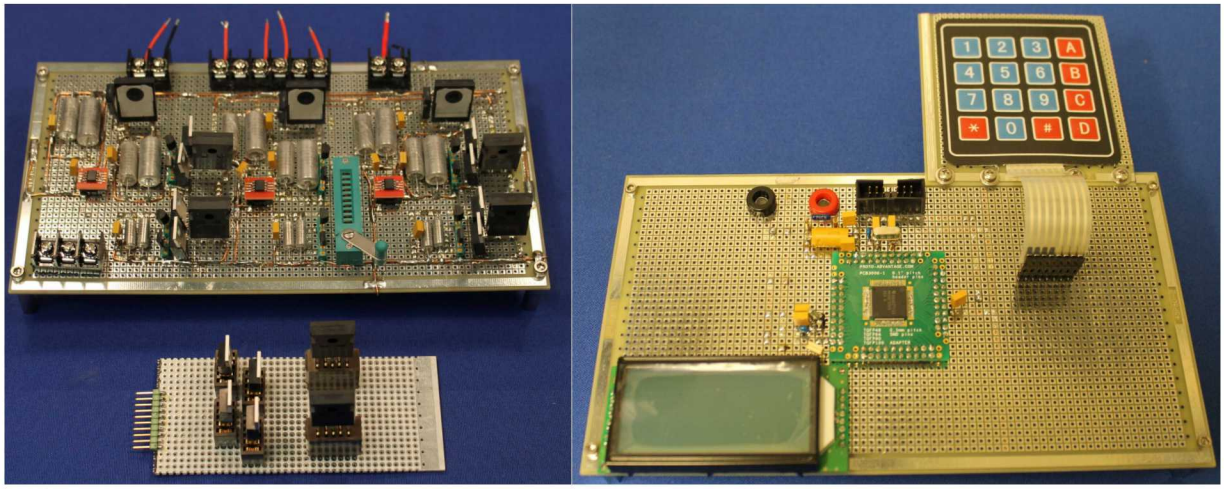

Figure I.1.2.8. Breadboard of 3-phase DC motor drive power stage (left) and embedded controller (right).

The motor drive power stage and controller were tested to ensure correct functionality. Power was supplied by a 1000 V, 10 A DC power supply and a three-phase controllable load was placed on the drive output. The board functioned correctly up to a level of 200 V (see Figure Figure I.1.1.7). At this level, the load consumed 7.5 A (1500 W or ~2 HP), the temperature of the discrete gate driver (without heat-sinking) rose to 105ºC, and the power switches (also without heat-sinking) rose to 80ºC. In a full PCB-fabricated setup with surface-mount parts and proper heat-sinking, there should be no issues achieving the ~1000 V DC bias level.

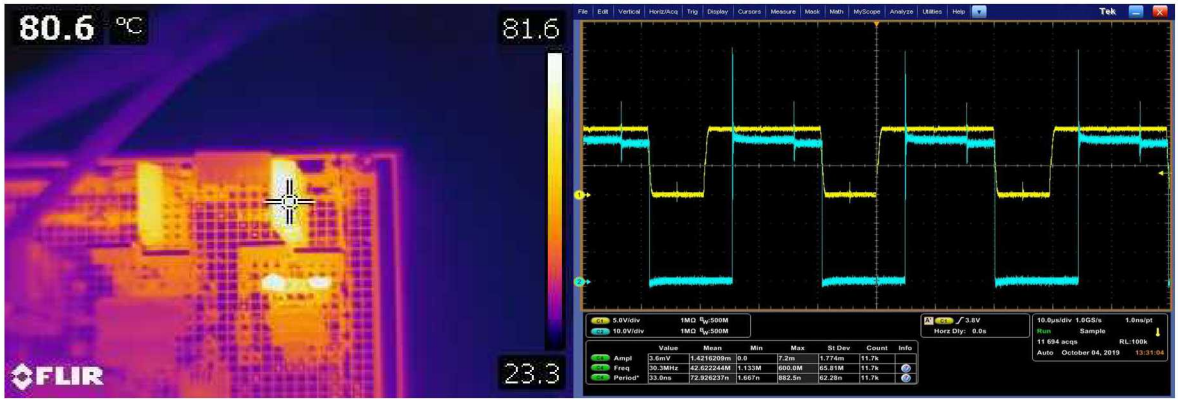

Figure I.1.2.9. (left) Thermal image of one leg of the power stage showing the temperature of power switches (centered at the crosshairs) and gate driver (just below the crosshairs) at 200 V and 7.5 A. (right) Gate drive signaling at 200V and 7.5 A.

Conclusions

During FY19, we have demonstrated the ability of a bipolar switching scheme to improve ceramic capacitor lifetime. This proof-of-concept result is being expanded through the fabrication of a test setup that will allow for testing of a large population of capacitors (40) under a variety of temperature and voltage stresses and bipolar switching profiles. This will allow for full characterization of the activation energy for oxygen vacancy migration as a function of voltage/temperature as well as the efficacy of different bipolar switching profiles. Such information will allow for incorporation of ceramic capacitors with bipolar switching into an electric traction drive.

Additionally, in FY19 a three-phase motor drive component test-bed was fabricated. This test-bed allows for the application of realistic operational stress to prototype devices fabricated within the consortium. A preliminary breadboard of the circuit has been fabricated and tested to ensure operation. A fully-integrated version is being constructed and will be used to test both SiC and GaN devices fabricated by Sandia as well as consortium partners.

Key Publications

No publications to date.

References

[1] D Donahoe and C Hillman. Failures in base metal electrode (bme) capacitors. In 23rd Capacitor and Resistor Technology Symposium, pages 129–138, 2003.

[2] T Nomura, Y Nakano, and A Satoh. Multilayer ceramic chip capacitor. US Patent 5,319,517, 1994.

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Acknowledgements

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III Electric Drive Technologies

III.1 Electric Drive Technologies Research

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Start Date October 1, 2018: End Date: September 30, 2023
Project Funding (FY19): $200,000 DOE share: $200,000 Non-DOE share: 0

Project Introduction

This project is intended to support the development of new traction drive systems that meet the targets of 100 kW/L for power electronics and 50 kW/L for electric machines with reliable operation to 300,000 miles. To meet these goals, new designs must be identified that make use of state-of-the-art and next-generation electronic materials and design methods. Designs must exploit synergies between components, for example converters designed for high-frequency switching using wide band gap devices and ceramic capacitors. This project includes: (1) a survey of available technologies, (2) the development of design tools that consider the converter volume and performance, and (3) exercising the design software to evaluate performance gaps and predict the impact of certain technologies and design approaches, i.e. GaN semiconductors, ceramic capacitors, and select topologies. Early instantiations of the design tools enable co-optimization of the power module and passive elements and provide some design guidance; later instantiations will enable the co-optimization of inverter and machine.

Objectives

- Identify performance measures corresponding to consortium design targets
- Develop metrics for performance/reliability of power electronics and electric motors
- Evaluate reliability/performance of state-of-the-art power devices and identify gaps
- Evaluate state-of-the-art/baseline traction drive system
- Utilize optimization tools to inform designs
    - Identify co-optimized designs
    - Evaluate parameter sensitivities and identify target specifications

Approach

The approach includes four strategies for generating design guidance and optimal designs, listed in order of increased fidelity and resources:

1. ***Empirical and First-Principles Analysis***: This uses first-principles knowledge, such as physical models, as well as comparative designs to inform the design.
2. ***High-Fidelity Modeling and Analysis***: This uses higher-order models that consider the component equivalent circuits, dimensions, reliability calculations, etc.

3. ***Global Co-Optimization***: With the definition of one or more performance metrics, components are simulated together and their performance is measured and compared.
4. ***Hardware Iteration***: Using optimal designs identified in software, hardware exemplars are built and evaluated; 3 and 4 are iterated to create the best results.

In FY19, the project focused on the first three strategies. Strategy 1 entailed an extensive literature search and the use of first principles to define metrics and down-select the design space. Models were then created for select components, and co-optimization software was developed to identify Pareto-optimal designs. Hardware iteration will begin in FY20.

For co-optimization, the team used the Genetic Optimization System Engineering Tool (GOSET) developed by Purdue University **Error! Reference source not found.**. This MATLAB®-based software package consists of several scripts for implementing and solving a genetic algorithm optimization problem. The genetic algorithm is a probabilistic method for optimizing multi-input systems with non-convex solution spaces using the principles of genetics and a user-defined fitness function. GOSET allows for multiple fitness functions to be co-optimized into a Pareto front. To set up the optimization, the circuit schematic and physical layout must be partially defined, and the dimensions of and between components, thicknesses of insulators, lengths of conductors, etc. must be formulated and linked to the schematic definition in order to compute a volume and evaluate the circuit/system performance using a dynamic simulation. In FY19, optimization efforts focused on the electric drive; future efforts will seek to merge the models with those of the machine currently being developed at Purdue, to enable co-optimization.

Results

Performance Measures/Targets

The targets indicate a 100 kW/L power density for the electric drive and 50 kW/L for the machine. Though this project will primarily rely on optimization to select the actual component dimensions, it is convenient to generate initial targets for component volumes for down-select. Using the US Drive 2017 Roadmap, component volumes were estimated for the BMW i3 and interpolated to these new targets. These include, for example, a volume target for the power module + DC link capacitor of < 175 cm^3.

To clarify the reliability metrics in terms of what can be measured and validated through laboratory measurements and lifetime models, the DOE Targets were mapped to performance criteria based on recent driving statistics as follows:

- Establish a range of 300,000 miles (DOE target); assuming 13,456 miles/year average [2] and 435 hours/year in vehicle [3], this becomes 22.3 years reliability (roadmap indicates 15 years), and 9702 hours of operation
- Process approximately 102 MWh [4] over 300,000-mile lifetime

Many reliability metrics were considered for integration into the co-optimization code. In general, reliability models can range from highly specific failure-based mechanisms that rely on models of physical process to reproduce lifetime, to more statistical measures. Failure-based mechanisms are the most realistic, but only apply for a specific failure mechanism in a specific component. Statistical-based methods, on the other hand, do not rely on a given failure mechanism, but on the aggregate behavior of many competing failure mechanisms in a large population of devices. These types of statistics typically give information on *mean time between failure* (MTBF). This, in itself, is a statistical measure of the reliability of an aggregation of devices and gives an idea of the "useful life" of a device, but does not predict end-of-life. For example, a statistical measurement may give an MTBF reliability of 100,000 hours for a system. This does not mean that any given system may have a lifetime of 100,000 hours, but that one expects an average failure rate of 1 per hour per 100,000 devices. In light of this, and in order to balance the tractability of the calculation needed for optimization and accuracy, we chose to incorporate MIL-HDBK-217F calculations [5]. This statistical measure of MTBF is simple, conservative, and specifically designed for high-reliability systems, but is not as accurate as other methods (physics-of-failure, telecordia, etc.) For every component, a 217F-style calculation takes the generic form of: $\lambda = n \cdot \lambda_b \pi_T \pi_A \pi_Q \pi_E$

where λ is the failure rate, n is the number of units in the system, λ_b is the base failure rate, π_T is the temperature factor, π_A is the electrical stress factor, π_Q is the quality factor, and π_E is the environmental factor. Each factor can be determined either through look-up tables in the handbook or via calculations based on physical phenomena.

Design Space

The inverter design space includes the selection of semiconductor material, the capacitor technology, circuit topology, and layout scheme. As part of this effort, the feasibility of using Gallium Nitride (GaN) devices for the drive train was investigated. In [6], an empirical analysis predicts that GaN-based converters can realize an improvement in power density over SiC-based converters by approximately 2x. GaN is already being considered for charging applications [7]. However, in [8], a genetic optimization of a converter + machine design showed only marginal gains in specific power with GaN compared to SiC. However, the circuit in [8] contained a passive rectifier with six GaN PiN diodes operating at low frequency, and the higher turn-on voltage (and hence loss) of these diodes drove up the circuit volume. Thus, to predict the impact of vertical GaN Junction Barrier Schottky (JBS) diodes (in development within the consortium), a comparative analysis presented in [9] was applied to compare optimally-designed GaN PiN, GaN JBS and SiC Merged PiN Schottky (MPS) diodes under operating conditions for the vehicle environment. Figure illustrates the difference in predicted power loss in vertical GaN JBS diodes compared to SiC MPS diodes for a 50% duty cycle. In fact, at relevant voltages and frequencies, GaN JBS diodes show a considerable advantage over SiC MPS diodes, with about 1/3 the electrical loss. Likewise, for a vertical FET device, assuming a fixed device structure (for comparison), the predicted R_{on} was computed as a function of breakdown voltage for devices based on Silicon, SiC, and GaN (see Figure I.1.1.1). Therein, R_{on} for the GaN device is approximately ½ that of the SiC device. Based on these results, vertical GaN technology may provide significant gains over SiC at higher voltage and frequency. Further work is ongoing for a full switching-based device loss analysis.

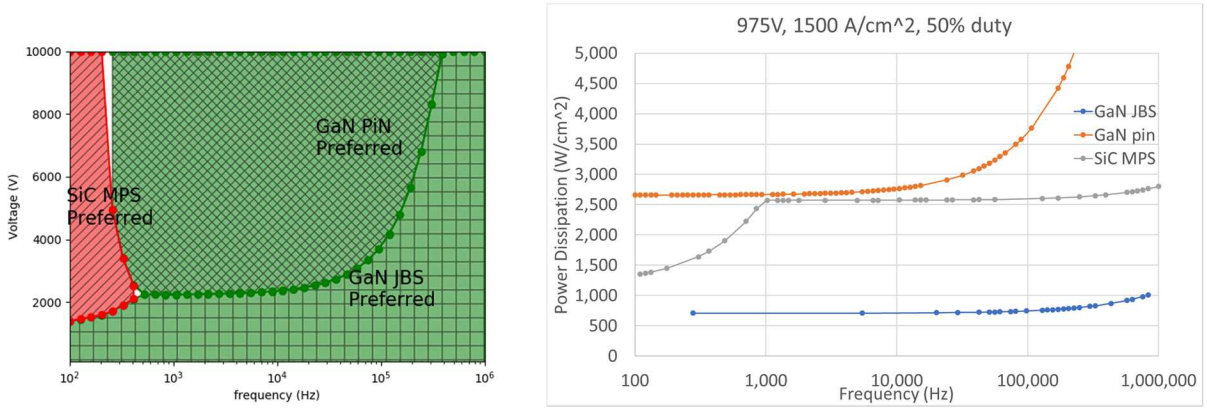

Figure I.1.1.1. Comparison of power loss in SiC MPS, GaN PiN, and GaN JBS diodes showing (left) preferred device as a function of voltage and frequency at 50% duty cycle, and (right) the comparison of loss at 650 V, 50% duty cycle

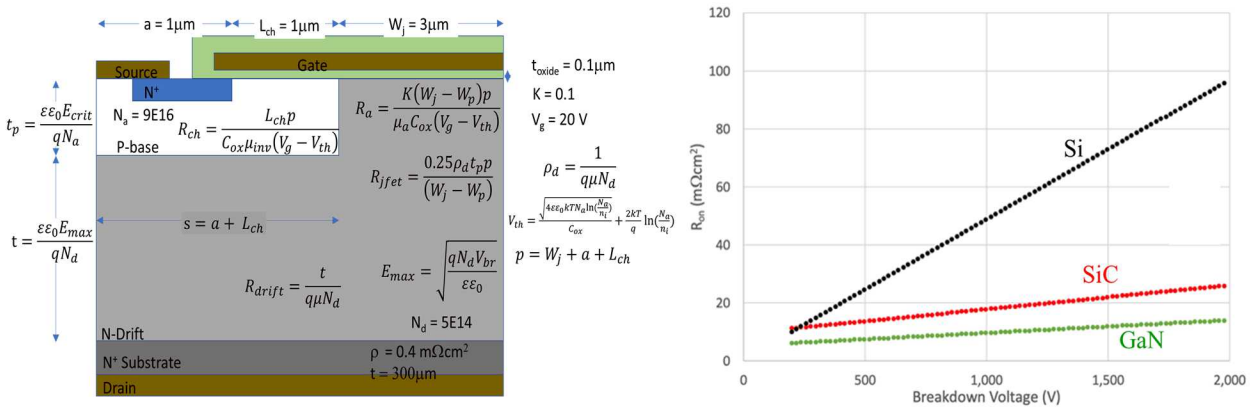

Figure I.1.1.1: Comparison of R_{on} in MOSFETs made in Silicon, SiC, and GaN showing (left) the device structure and (right) the predicted results.

Topologies and Capacitor Technologies

Several converter topologies were considered including the combined DC-DC⇔DC-AC architecture identified in [10] as well as multi-phase topologies [11], and more exotic configurations [12]. Given the higher projected available battery voltage, the team focused on direct-connect DC-AC (no DC-DC boost). Due to the beneficial effect of additional phases on required dc-link capacitance and dc-link capacitor current ripple [11], the team focused our design on the multi-phase topology. Figure I.1.1.2 shows the selected circuit topology used in the co-optimization problem consisting of a multi-phase inverter, DC-link capacitor, input inductor, and multiple parasitic terms which vary with component selection and layout. The design parameters included in the optimization are the battery open-circuit voltage V_{in}, the input inductance L_{in}, the link capacitance C_{link}, the number of phases N_ϕ, the switching frequency f_{sw}, the fundamental frequency of the output voltage ω_r, and the AC filter inductance L_f, resistance R_f, and capacitance C_f. A MATLAB® script was developed that took these parameters, solved a set of differential equations for the circuit, and then post-processed the behavior of the voltages and currents in the circuit to determine the volume and losses of the design as well as the voltage and power loss in specified components. The form factor selected for the principal converter elements is shown in Figure I.1.1.3. Therein, the module with the devices, conductors, and flat capacitor assembly are packaged together. This form factor was used as a basis for the dimensional analysis. This approach has several advantages discussed in [13].

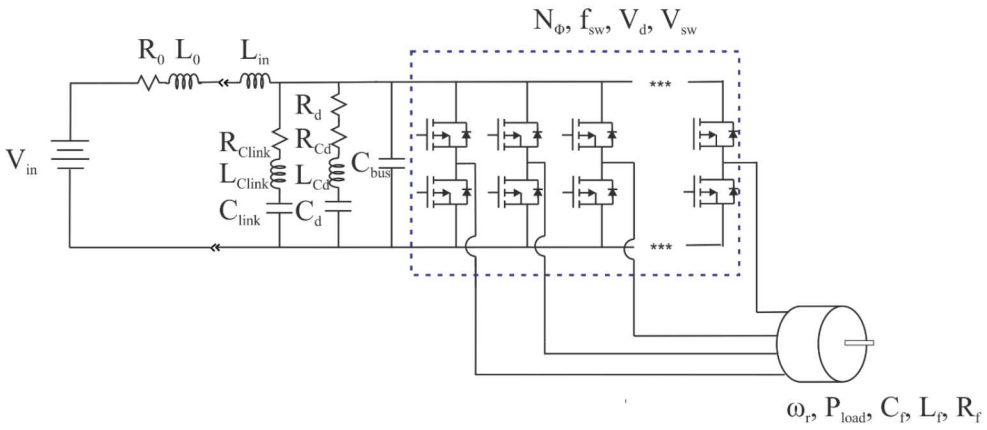

Figure I.1.1.2: Circuit topology for co-optimization.

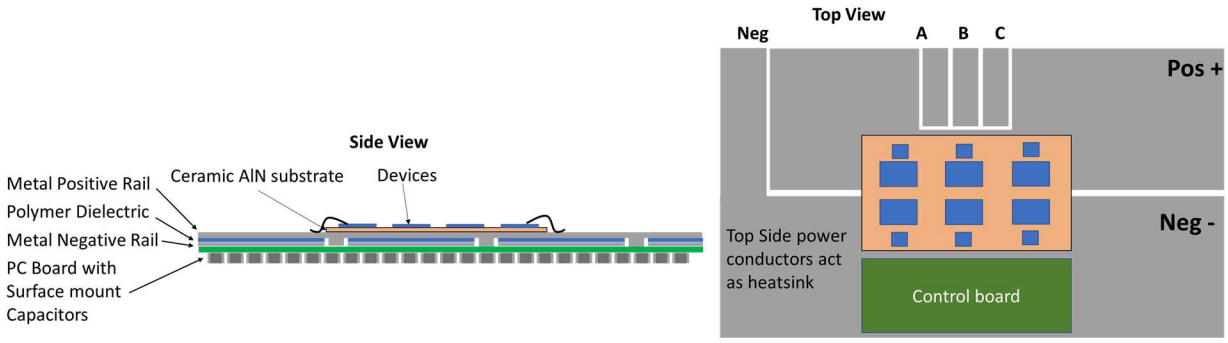

Figure I.1.1.3: Candidate design considers a flat integrated form factor that includes module and DC link capacitor.

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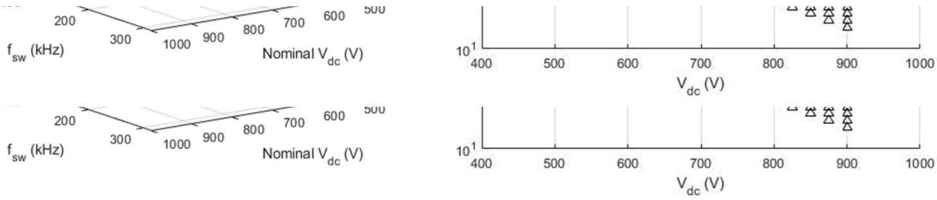

Figure I.1.1.4, right panel for designs complying with 175 mL volume. Additional factors must be considered, however. For example, the Ceralink capacitors indicate a high energy density and a favorable C-V characteristic, but this is achieved at very high field strengths which may impact their reliability. Reliability considerations are factored into the design within the optimization.

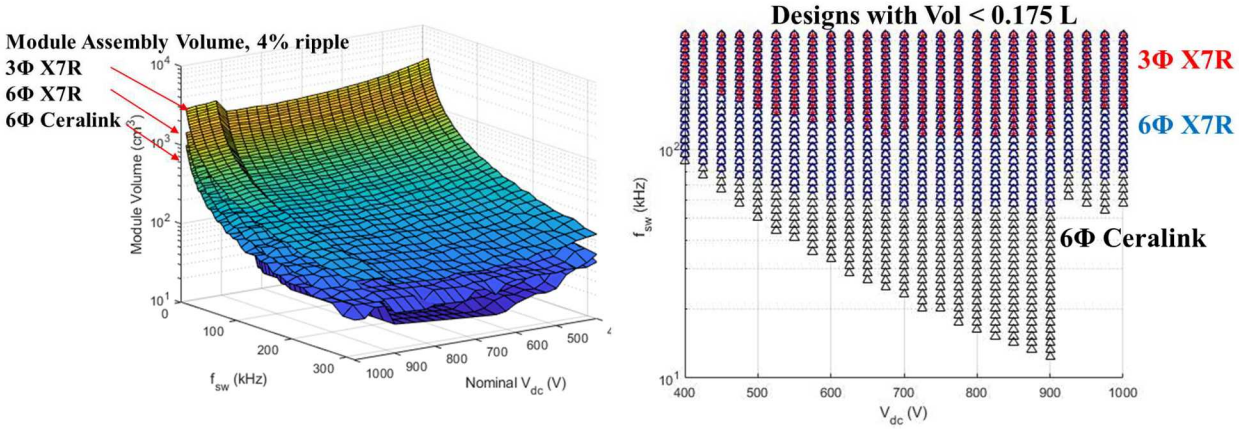

Figure I.1.1.4: Module volume estimate as a function of voltage and frequency for Ceramic X7R and Ceralink Capacitors.

Machine Design

Highly desirable features of electric vehicle drive motors are high starting torque, high power density, and high efficiency over the full operating range. These requirements place significant limits on motor type as well as the materials used in their construction. Using hard permanent magnet materials in the motor construction is the current preferred approach to addressing volume and weight requirements. NdFeB magnets offer the highest residual induction, coercive force, and energy product compared to Ferrites, AlNiCo, and SmCo. NdFeB magnets, however, do pose potential supply-chain issues necessitating new magnetic materials and motor designs. Recently, motors based on different magnetic materials have been compared based on machine constant of mechanical power [14] (MCMP is defined as P_{mech}/[motor volume] × [rotor frequency in Hz]) which gives a measure of potential output mechanical power. The comparison includes both prototypes and simulation data. While NdFeB-based IPMSM demonstrate ~0.9 kWs/L of MCMP with 96% efficiency, various ferrite-based

PMSMs also show performance approaching this limit with MCMP ranging from 0.7-0.8 kWs/L with an efficiency range of 93-97% with rotor speeds ranging from 1500-2800 rpm. Taking rotor speed into account, these motors provide 20-40 kW/L. For comparison, the BMW i3 was evaluated to be 9.2 kW/L with a top speed of 11.5 krpm. To meet DOE targets (50 kW/L) while eliminating permanent magnets, the team plans to consider new homopolar motor designs, which establish a rotor field using a static field winding and may achieve speeds > 20 krpm. Next year's work will include a collaborative effort with Purdue University; Purdue is developing design codes for the homopolar machine and is investigating the feasibility of meeting the DOE targets using this approach.

Co-Optimization

Two co-optimization examples are presented here. The first considers a simple bi-directional 10 kW boost converter, like one that might connect a battery to an inverter. Therein, the converter was optimized for DC link capacitor MTBF versus converter volume. Results are shown in Figure I.1.1.5. The optimization pulls the solutions to the upper left of the trade-space, showing a clear trade-off between reliability and size. The second optimization was performed on a 100 kW inverter (Figure I.1.1.2 and Figure I.1.1.3) module and DC link capacitor (no thermal management) with the parameters noted above. The genetic optimization algorithm was run on a population of 50 individuals in this parameter space over 100 generations with fitness functions to maximize the power density of the module + link capacitor size and minimize loss. There was also a constraint placed on the maximum RMS of the DC bus voltage ripple. The resulting Pareto front is shown to the right in Figure I.1.1.5. The genetic optimization pulls all the individuals towards the lower right. Examining the parameter values for the individuals on the Pareto front shows a tendency of the individuals to have a 450 V input, 9 phases, and over 250 kHz switching. Since only the volumes of the capacitor and module were considered in the optimization, voltage was minimized to minimize the number of capacitors needed to stand off the voltage. After adding the magnetics and thermal management components to the model, solutions with higher DC-link voltage are expected.

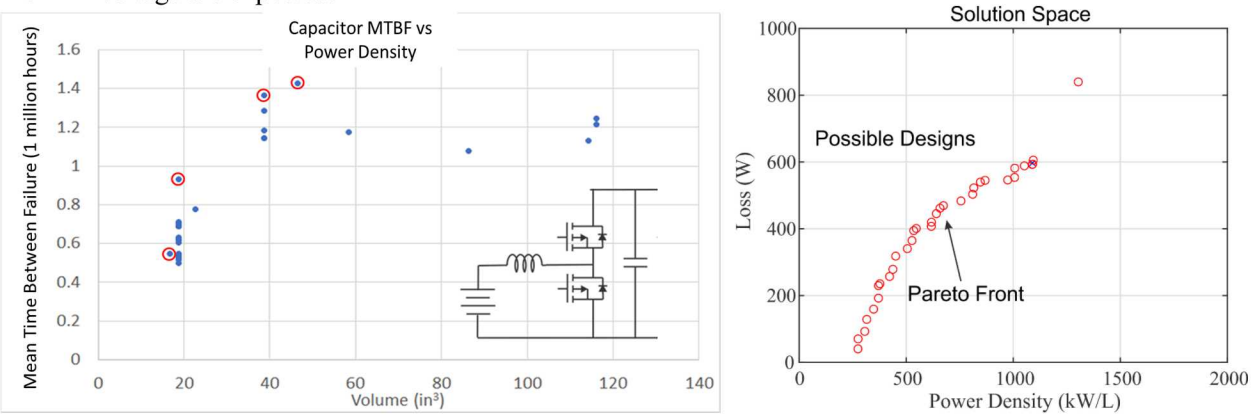

Figure I.1.1.5: Co-optimization results for (left) 10 kW boost converter and (right) 100 kW inverter module + capacitor.

Conclusions

This project first focused on down-selecting the design space for future traction drive systems; combined, the use of GaN devices, ceramic capacitors, high-frequency switching, and multi-phase designs may enable considerable improvements in power density. This work also developed tools to perform multi-objective optimizations on electric drive designs. Unlike previous work, these include optimizations that consider component reliability. Future work will refine these tools and extend their use to co-optimize the inverter and machine designs.

Key Publications

No publications to date.

References

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IV Electric Drive Technologies

IV.1 Electric Drive Technologies Research

I.1.4 Bottom-Up Soft Magnetic Composites (Sandia National Laboratories)

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Project Funding (FY19): $125,000 DOE share: $200,000 Non-DOE share: $0

Project Introduction

In order to meet 2025 goals for enhanced peak power (100 kW), specific power (50kW/L), and reduced cost (3.3 $/kW) in a motor that operates at >20,000 rpm, improved soft magnetic materials must be developed.

Additionally, improved soft magnetic materials will enable high performance motors that do not rely on rare earth materials. In fact, replacement of permanent magnets with soft magnet materials was highlighted in the Electrical and Electronics Technical Team (EETT) Roadmap [1] as a potential R&D pathway for meeting 2025 targets. At the higher targeted rotational speeds, eddy current losses in conventional soft magnetic materials, such as silicon steel, will begin to significantly decrease motor efficiency. One possible solution is to use soft magnetic composites (SMCs), which combine magnetic particles with an insulating matrix to increase electrical resistivity (ρ) and decrease eddy current losses, even at higher operating frequencies (or rotational speeds). Currently, SMCs are being fabricated with values of ρ ranging between 10^{-3} to 10^{-1} μohm·m [2], which is significantly higher than 3% silicon steel (~ 0.5 μohm·m) [3]. Additionally, the isotropic nature of SMCs is ideally suited for motors with 3D flux paths. Furthermore, the manufacturing cost of SMCs is low and they are highly amenable to advanced manufacturing and net-shaping into complex geometries, which would significantly reduce or eliminate manufacturing costs. However, there is still significant room for advancement in SMCs, which will allow for improved performance in electrical machines. For example, despite the inclusion of non-magnetic insulating material, their electrical resistivities are still far below that of ferrites ($10 - 10^{8}$ μohm·m).

In this project, we are developing SMCs from the bottom up, with a final objective of creating composites with high volume loading (and therefore high saturation magnetization) while increasing the value of ρ several orders of magnitude over the current state-of-the-art in SMCs. We are accomplishing our goals by starting with particles of the γ'-Fe_4N phase of iron nitride, which has a saturation magnetic polarization (J_s) slightly greater than Si steel (1.89 T) [4] and a ρ of ~ 2 μohm·m [5]. In our bottom-up approach we begin by coating the magnetic particles with a diamine, which can chemically react directly with epoxide terminated monomers and form a cross-linked epoxy composite. This "matrix-free" approach to composite formation will not suffer from the same nanoparticle aggregation and phase separation effects commonly observed in conventional nanocomposites [6]. Furthermore, it should ensure better separation between magnetic particles and significantly reduce or eliminate inter-particle eddy currents. There is already an established precedent for the use of epoxies in electrical machine construction [7, 8]. Also, it is possible to design epoxy systems with glass transition temperatures (T_g) well in excess of the target motor operating temperature of 150°C [9]. Furthermore, composites have been successfully demonstrated in high-speed motors [10] and even flywheels rotating at speeds up to 60,000 rpm [11].

Objectives

The project objective is to develop high-magnetization, low-loss iron-nitride-based soft magnetic composites for electrical machines. These new SMCs will enable low eddy current losses and therefore efficient motor operation at rotational speeds up to 20,000 rpm. Additionally, our iron nitride and epoxy composites will be capable of operating at temperatures of 150°C or higher over a lifetime of 300,000 miles or 15 years.

Approach

A high-level overview of our approach is:

1. Convert commercially available mixed-phase iron nitride powder to nearly phase-pure γ'-Fe_4N
2. Coat iron nitride particles with diamine molecules (part A of epoxy chemistry)
3. Combine surface functionalized particles with epoxide terminated monomers (part B of epoxy chemistry)
4. Fabricate SMC part by pouring mixture from #3 into a mold. In future years of the project, hot pressing can be used to increase the volume loading of the magnetic particles.
5. Evaluate and test the fabricated SMC part

Each of these steps involves many possible optimization steps such as processing conditions, epoxy monomer selection and curing conditions, and hot-pressing conditions.

Results

Production of phase-pure γ'-Fe_4N

We demonstrated the conversion of mixed-phase commercially available iron nitride powder to nearly phase-pure γ'-Fe_4N. Our starting material was commercially available iron nitride powder, acquired from Alfa Aesar. This commercial iron nitride powder is a mixture of both Fe_3N and Fe_4N. We developed a straightforward heat treatment to convert almost all of the Fe_3N phase to the higher J_s Fe_4N at a temperature slightly above 550°C, conducted in an inert atmosphere. Temperature-dependent X-ray diffraction (XRD) data of this process, collected under flowing nitrogen, is displayed in Figure I.1.1.1. This data shows that at a temperature slightly above 550°C the diffraction peaks associated with the F_3N disappear, leaving nearly phase-pure Fe_4N.

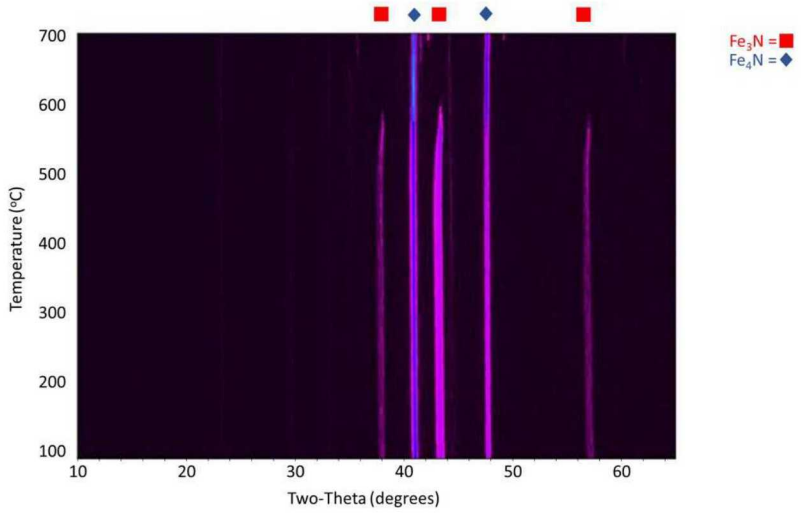

Figure I.1.1.1. Temperature-dependent XRD data of commercially available mixed phase iron nitride powder and its conversion to nearly phase pure Fe_4N.

Coating of Iron Nitride Particles and Composite Formation

To fabricate iron-nitride-based magnetic composites, iron nitride powder and 1,6-hexanediamine (see Figure I.1.1.2) were added to a SPEX high-energy ball mill and were milled until the particles were coated by the diamine, as confirmed by infrared (IR) spectroscopy. Next, the diamine coated particles were mixed with one of a number of different epoxides: neopentyl glycol diglycidyl ether (which has two epoxide groups); trimethylpropane triglycidyl ether (three epoxide groups); or *N,N*-diglycidyl-4-glycidyloxyaniline (3 epoxide groups). For the sake of brevity, only an image of *N,N*-diglycidyl-4-glycidyloxyaniline is displayed (see Figure I.1.1.3). After mixing the amine functionalized particles with one of the three epoxide-terminated monomers listed above, the mixture was poured into a mold and cured. We fabricated a 3D-printed toroidal mold (9 mm O.D.) for this project. The toroidal geometry is ideal for characterization on our Iwatsu B-H analyzer.

All three epoxide-terminated monomers formed suitable epoxy-based composites. The collection of additional data in the upcoming fiscal year (T_g, mechanical strength, thermal conductivity, and ρ) will allow us to down-select to the epoxide-terminated monomer that yields the best properties for electric motor implementation. An image of three cured magnetic composite cores wound for B-H analysis is shown in Figure I.1.1.4. A B-H loop collected at 10 kHz for a magnetic composite toroid is displayed in Figure I.1.1.5. We fully expect that magnetic properties will be significantly enhanced in the future as we optimize processing conditions and volume loading of the magnetic particles.

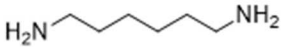

Figure I.1.1.2. 1,6-hexanediamine.

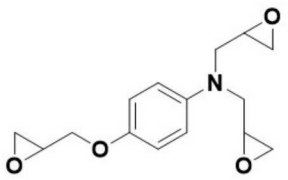

Figure I.1.1.3. *N,N*-diglycidyl-4-glycidyloxyaniline.

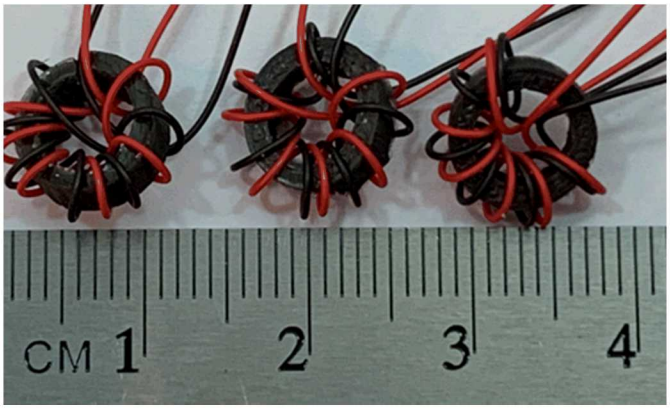

Fig I.1.1.4. Magnetic composite toroidal cores wound for B-H analysis.

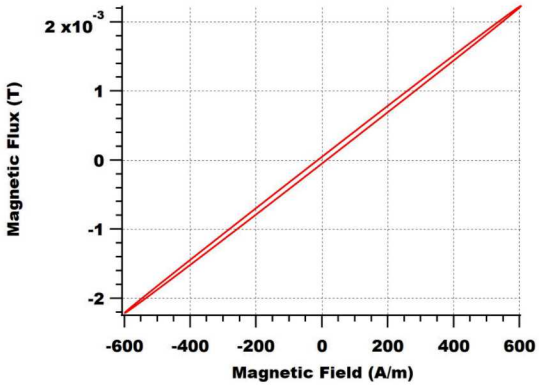

Figure I.1.1.5. B-H hysteresis loop for a magnetic composite toroid. This hysteresis loop was collected at a frequency of 10 kHz.

Magnetic Composite Rotor Fabrication

We fabricated portions of a rotor design from Oak Ridge National Lab (ORNL) via two different methods. First, a commercially available magnetic composite filament (purchased from Proto-pasta) was used to 3D print a portion of Oak Ridge's rotor design (see Figure I.1.1.6). Manufacturing this part serves as a demonstration of our capability to 3D-print magnetic parts for both electric drive power electronics and motors. Although this first 3D-printed rotor part used a commercially available magnetic filament, we are developing our own high magnetization magnetic composite filament. To this end we have purchased, assembled, and tested a Filastruder and Filawinder, which will allow us to create printable magnetic composite filaments using iron nitride particles and any suitable polymer of our choice. This will be an important capability both for the fabrication of inductors for power electronics and soft magnetic motor components.

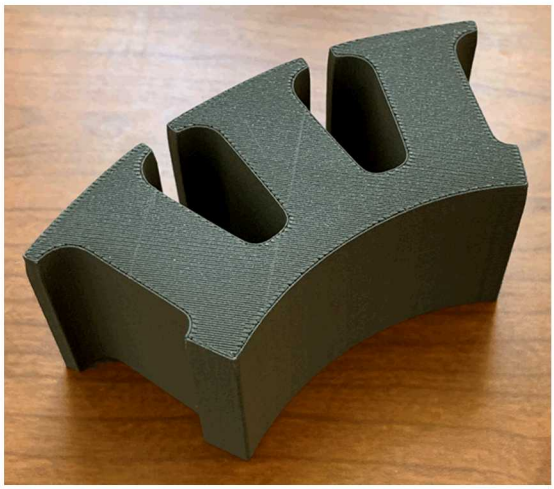

Figure I.1.1.6. 3D printed magnetic composite rotor (1/6 of total rotor design).

Second, an iron nitride and epoxy composite was prepared, mixed (as described above), and poured into a silicone mold for curing. In curing these larger epoxy-based composites, it was discovered that 1,6-hexanediamine reacted too vigorously with the epoxide monomers and led to an exothermic cure. This resulted in excessive heating of the curing epoxy. We switched from using 1,6-hexanediamine to 4-aminophenyl sulfone (see Figure I.1.1.7) which cures more slowly and does not result in an overly aggressive exothermic cure. In fact, when 4-aminophenyl sulfone is used as the diamine, the uncured epoxy mixture must be heated to a temperature of 130°C to initiate the curing process. We incrementally increased the size of the parts we were fabricating in order to ensure we were controlling the curing process adequately, gradually approaching a full-sized rotor tooth. An image of three different sized magnetic composite rotor teeth, along with a composite toroid, is displayed in Figure I.1.1.8.

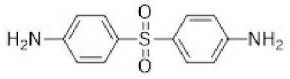

Figure I.1.1.7. 4-aminophenyl sulfone.

Figure I.1.1.8. Three differently-sized magnetic composite rotor teeth and a magnetic composite toroid.

Conclusions

During FY19, we successfully demonstrated the fabrication of iron nitride (γ'-Fe_4N) based magnetic composite parts for electric motors. These parts will also be suitable as inductor cores for electric drive power electronics. Custom epoxy chemistries were selected, evaluated, and used to fabricate magnetic composite toroids and rotors. Additionally, we demonstrated the capability of not only fabricating complex shapes using molds but also via 3D printing. We expect this capability to be particularly fruitful in the fabrication of inductor cores for power electronics. Future work will focus on improving processing conditions and magnetic material volume loading in the fabrication of magnetic composites to enhance magnetic performance for motor and power electronic applications.

Key Publications

1. T. C. Monson *et al.*, Soft Magnetic Multilayered FeSiCrB–Fe_4N Metallic Glass Composites Fabricated by Spark Plasma Sintering. *IEEE Magnetics Letters* **10**, 1-5 (2019).

2. J. M. Silveyra, E. Ferrara, D. L. Huber, T. C. Monson, Soft magnetic materials for a sustainable and electrified world. Science **362**, eaao0195 (2018).

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